Power Loss Protection System Guide

Abstract

This application note outlines power loss protection features of Qorvo enterprise solid-state drive and server application solutions. It offers a general overview of Qorvo's PLP and PLP+PMIC product families, explaining their fundamental operating principles and key function blocks. The focus is on power loss protection functionality. Further implementation details are contained in corresponding product datasheets, application notes, and evaluation kits.

1. Introduction

Qorvo power loss protection (PLP) controllers integrate several functions including hot swap (also known as hot plug), protection, and power hold-up to prolong operating time in the event of sudden power loss. A common application of PLP is in an enterprise solid-state drive (SSD). Upon sudden power loss, PLP supplies power to the SSD long enough for the SSD to transfer data from volatile memory to non-volatile FLASH memory and update mapping tables. The SSD power hold-up time enables a controlled shutdown. Some products also include flexible power management features, designated as PLP+PMIC. This application note focuses on common power loss protection functionality of these devices. Power management features differ for each PLP+PMIC and are comprehensively explained in corresponding datasheets.

2. PLP Controller Overview

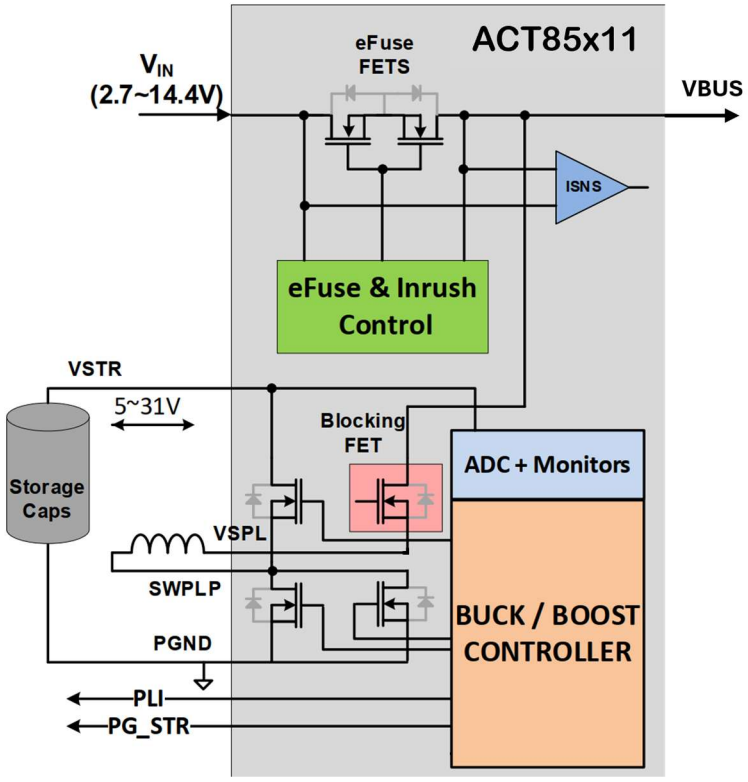

Fig. 2-1. Partial block diagram of a Qorvo PLP & Power Management IC

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The partial block diagram of Fig. 2-1 shows the connection between PLP-related components. Qorvo PLP products contain an e-fuse and a boost converter that shares an inductor with a buck converter. Most devices also include a blocking FET. External storage capacitors provide the SSD with enough energy to shut down without data loss. In normal operation when power is stable, the e-fuse connects the input V_{IN} to the load at V_{BUS} with minimal power loss. If an input voltage fault occurs, the e-fuse switches off and operation transitions to supplement mode. The PLP buck converter then draws energy from the storage capacitors and delivers it to the voltage-regulated output V_{BUS}. During startup or restart, the boost converter stores energy in the storage capacitors and subsequently maintains the storage voltage. High storage voltage reduces the storage capacitor bank volume by reducing the parallel capacitor count. Interface signals indicate to the SSD controller the status of input and storage voltages. Periodic telemetry checks during a slight discharge indicate capacitor fitness for use. An analog-to-digital converter (ADC) provides measurements of input, output, and storage capacitor voltages, e-fuse current, and chip temperature.

3. Normal Startup Sequence

The startup sequence has multiple states to ensure that all loads power up smoothly. This applies to both PLP and PMIC (if included), but the focus here is only on PLP.

Table 3-1. PLP normal startup sequence

State	E-Fuse	Blocking FET	Notes
1	Off	Off	UV/POR, waiting for V_{IN} > UVLO
2	Partially on	Off	E-fuse soft start
3	On	Default off	E-fuse fully on, blocking FET (if present) soft starts storage capacitors when enabled
4	On	On	Health checking, PLP boost active, normal operation

Table 3-1 lists the PLP states during a normal, fault-free startup. Note that actual IC states may differ.

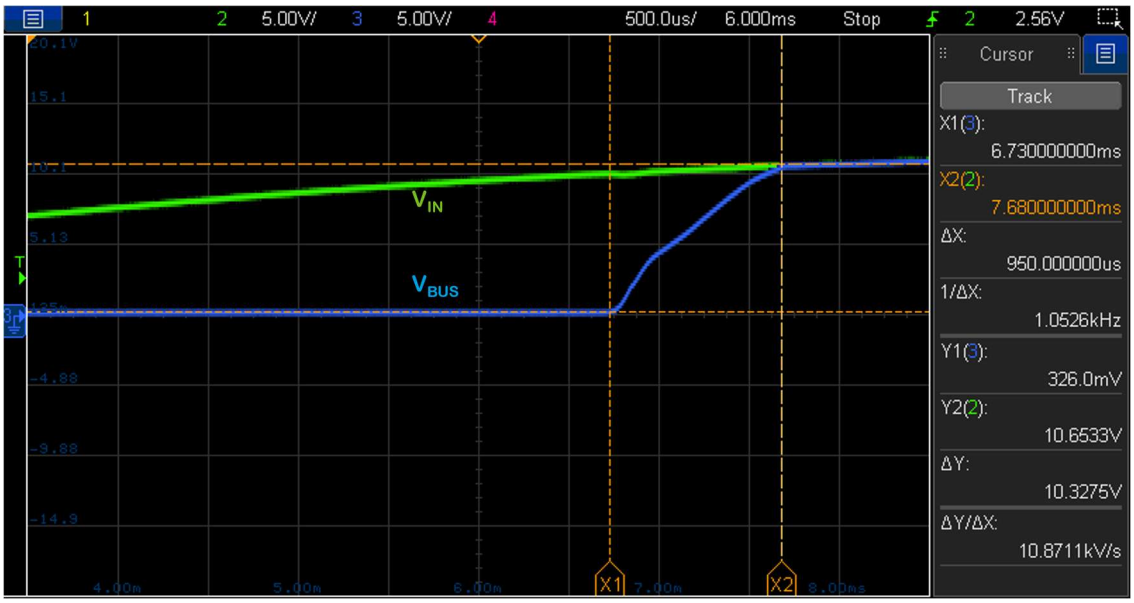

Fig. 3-1. ACT85411 V_{IN} and V_{BUS} during startup with C_{SS} = 6.8 nF

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3.1. UV/POR State

In state 1, the undervoltage (UV)/power on reset (POR) state, the input supply voltage rises but is below the UVLO threshold. The PLP or PLP+PMIC IC is in a safe state for the system. The e-fuse, blocking FET, and PLP buck are off, preventing current flow between V_{IN} and loads or between the storage capacitors and V_{BUS}. The e-fuse has two common-source (back-to-back) MOSFETs that block current in either direction when off. It therefore functions as a disconnect between the input and the load. The blocking FET is a single MOSFET that can be manually switched on or off by a register bit accessible by I^2C. When the blocking FET is off, the PLP boost is disabled. Some ICs have an enable/disable pin for keeping the blocking FET, PLP boost, and PLP buck off. The blocking FET blocks current into the storage capacitors. The high-side MOSFET that is part of the PLP boost and buck blocks or allows current to flow from the storage capacitors.

3.2. E-Fuse Soft Start

When V_{IN} exceeds the UVLO threshold, the operating state transitions to e-fuse soft start, state 2 in Table 3-1. The IC includes either a configurable delay or configurable UVLO and overvoltage lockout (OVLO). Taking the ACT85411 as an example, its factory default, configurable UVLO is 9.6 V. With the ACT85411 soft start capacitor value equal to 6.8 nF, V_{BUS} rise time is about 1 ms, as seen in Fig. 3-1. This is accomplished by partially turning on the e-fuse MOSFETs that are inside the IC. E-fuse soft start prevents input voltage chatter or excessive inrush current from reaching loads. The overcurrent threshold during e-fuse soft start is low due to high power dissipation in the partially-on e-fuse MOSFETs. The load has smooth startup voltage even during hot swap, also called hot plugging. This allows an SSD, for example, to be inserted into a rack with other SSDs that are already powered. Soft start time is programmable by an external capacitor or by another voltage source to track another power supply voltage.

If the e-fuse current exceeds a configurable limit during e-fuse soft start, or if the IC temperature exceeds a safe level, the e-fuse switches completely off until fault conditions clear. Then after a certain delay time, the IC restarts the soft start process. When the difference between the input and load voltages falls below a threshold, the e-fuse soft start process completes, and the operating state proceeds to state 3 when the e-fuse is fully on for normal operation.

3.3. E-Fuse Fully On

The blocking FET (if included) is off by default, and the same is true of the PLP boost. This provides time for the controller to change configuration settings. Writing to a certain I^2C register enables the blocking FET and PLP boost. Then the blocking FET, if included, allows a constant current to charge the storage capacitors to the input voltage. This charge current is configurable for some ICs. Fig. 3-2 shows an ACT85411 charging 890 µF at 305 mA during storage soft start.

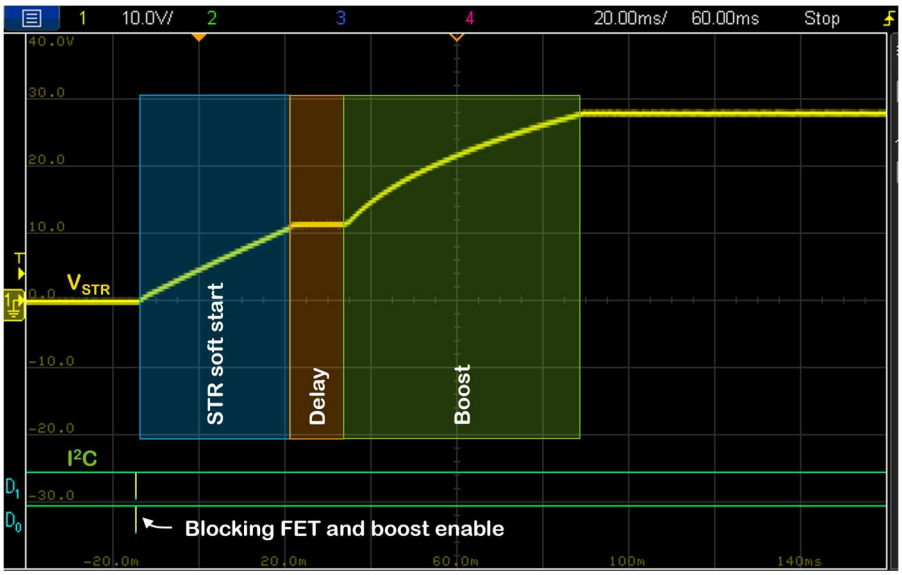

Fig. 3-2. Storage capacitor voltage during startup

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If the storage capacitors fail to charge within a certain time limit, the IC responds in one of two ways, depending on the IC design and its configuration. It either waits and tries again repeatedly, called “hiccup mode”, to accommodate very large storage capacitance, or it goes into a fault state. This prevents the blocking FET from overheating, even if the storage capacitors are shorted. After charging the storage capacitors to the voltage at V_{BUS}, the blocking FET turns fully on. After a delay, the PLP boost converter can charge and maintain a higher, preconfigured voltage on the storage capacitors.

3.4. Health Checking

With the PLP boost enabled and blocking FET fully on, operation moves to state 4 in Table 3-1, which is normal operation. The e-fuse connects the input V_{IN} to the output V_{BUS} with minimal power loss. The IC remains in this state unless the controller sends a shutdown command either by an input pin or by an I^2C command, or there is a fault condition.

Configurable health checking discharges the storage capacitors with a small, constant current. Discharge voltage versus time determines the status and capacity of the capacitors. For some ICs, storage capacitors health checking can be autonomous.

4. Supplement Mode

Fault conditions that put the IC in supplement mode from the health checking state include:

- Overcurrent (OC), with configurable threshold and deglitch delay, which is configurable for some ICs. During the OC deglitch delay, the e-fuse transitions from fully on to partially on to limit the current, enabling ride-through of short OC transients. If the OC condition persists after the deglitch time, or if V_{BUS} is shorted, then the e-fuse switches off, and the IC enters supplement mode.
- Input undervoltage or overvoltage, with configurable thresholds and deglitch
- $V_{IN} – V_{BUS}$ exceeds a threshold
- $V_{BUS} – V_{IN}$ exceeds a threshold, protecting from reverse current

In supplement mode, the e-fuse is off. This disconnects the input from the output and blocks current in either direction, so the load cannot back feed to the input. The PLP buck activates, taking energy from the storage capacitors and delivering it to the load at a preconfigured voltage.

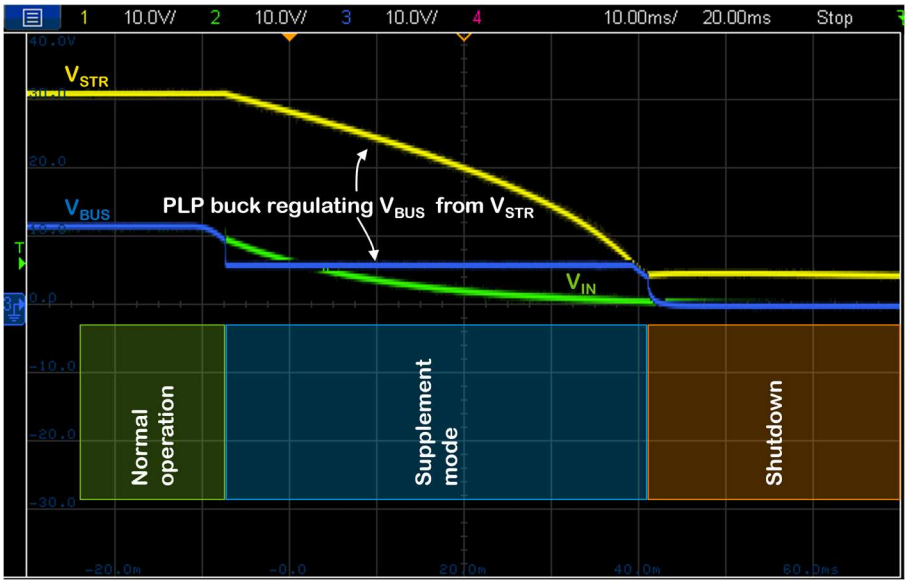

Fig. 4-1. Input, output, and storage voltages after sudden power loss

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Fig. 4-1 shows an ACT85411 responding to a sudden input power loss. During normal operation with the e-fuse fully on, the voltages at V_{BUS} and V_{IN} are equal at 12 V. V_{STR} is set at 30 V, the storage capacitance is 890 µF, and the load at V_{BUS} is 5 Ω. After the power loss, V_{IN} settles to zero. V_{BUS} tracks V_{IN} until it crosses the UVLO threshold, triggering a fault condition and the transition to supplement mode. The e-fuse then switches off and the PLP buck converter draws current from the storage capacitors to regulate V_{BUS} at 6 V, which is its preconfigured supplement mode voltage. Supplement mode duration is about 47 ms, after which V_{BUS} crosses the V_{STR} UVLO threshold and the IC shuts down. Theoretically, the hold time is:

$t_{hold} = \frac{C_{STR} \cdot \eta \cdot (V_{STR}^2 - V_{BUS}^2)}{2 \cdot P_{out}} = \frac{0.000890\ F \cdot 0.90 \cdot (30\ V^2 - 6\ V^2)}{2 \cdot 7.2\ W} = 48$ µs. (See PLP Capacitor Selection and Configuration) This matches closely with the measured hold time, so the efficiency estimate of 90% at the tested load power of 7.2 W is reasonable. The ACT85411 EVK User's Guide includes information about efficiency versus load current.

5. Supplement Disable

Fault conditions that put the IC in supplement disable mode from the health checking state include:

- Excessive IC temperature
- Insufficient IC supply voltage
- IC power supply fault
- Storage capacitors overvoltage

The e-fuse remains on in this state, but the PLP buck is disabled, so the IC will not provide power to V_{BUS} if input power fails.

For exit conditions from this state, please refer to the corresponding datasheet.

6. I²C Communication

All PLP and PLP+PMIC communicate by I²C as targets. The controller is typically an SSD controller. There are only two bus lines: serial data (SDA) and serial clock (SCL). Some ICs include configurable pullup resistors to minimize component count. Setup and hold time characteristics comply with I²C timings for 1MHz operation - Fast Mode Plus. I²C is serial, 8-bit oriented, and allows bidirectional data transfers. The details of I²C implementation are readily available in an I²C-bus specification and so are not repeated here except by way of examples relating to Qorvo PLP and PLP+PMIC ICs.

Some PLP+PMIC ICs implement a write passcode, which prevents accidental register changes by ignoring register writes. Corresponding datasheets explain how to enable I²C write functionality by writing a passcode to a certain register. The PLP and PMIC portions of a PLP+PMIC IC use different I²C target addresses, and the passcode must be independently written for each I²C address.

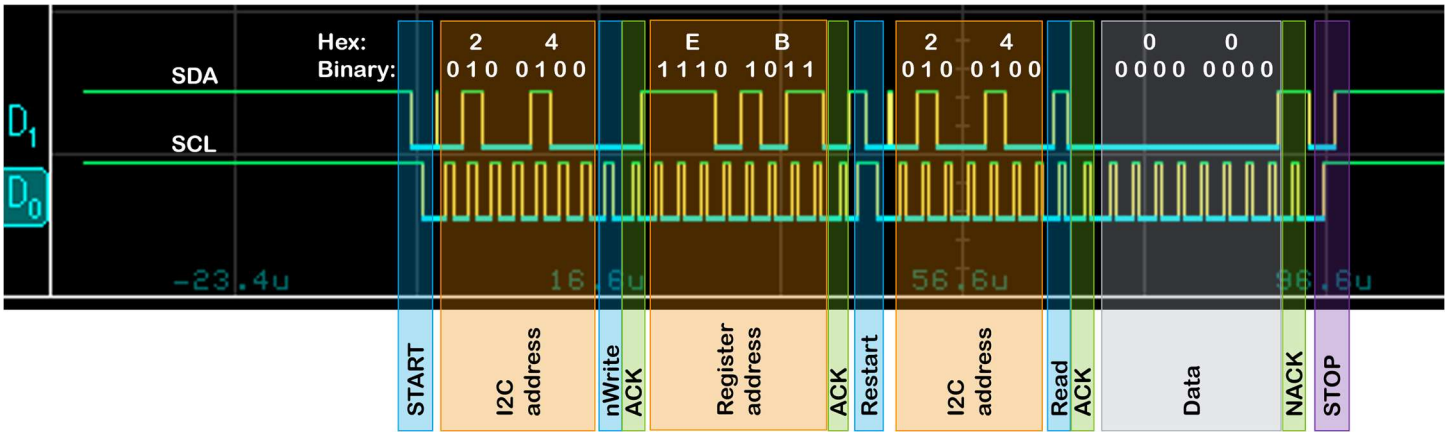

Fig. 6-1. I²C read example, ACT85411 PLP register at 0xEB

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Fig. 6-1 shows a typical I²C read transaction. In this example, the IC is ACT85411, a PLP+PMIC, installed in an ACT85411 evaluation kit. The I²C controller is inside a USB dongle that is included with the kit. The ACT85411 PLP I²C address is 0x24, and its PMIC address is 0x25. The controller first "claims the bus" with a START condition, then transmits the 7-bit I²C address 0x24, followed by writing the address of the PLP register to be read in the ACT85411, which in this case is 0xEB. After a restart (repeated START), the controller sends a read request at the I²C address (0x24), and the ACT85411 responds by sending the contents of its 8-bit internal register at 0xEB; it contains all zeros. The controller signals the end of the transfer to the ACT85411 (target transmitter) with a NACK (SDA is high on the 9th clock) followed by a STOP condition. The transfer speed in this example is 400 kbits/s, which is Fast-mode.

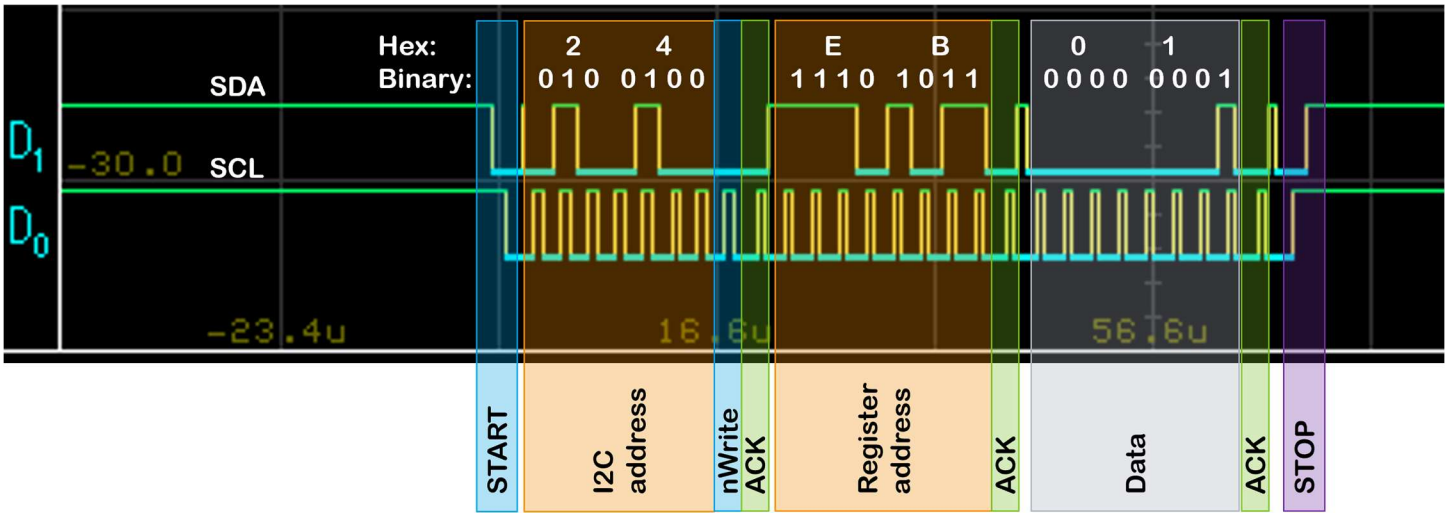

Fig. 6-2. I²C write example, writing 0x01 to ACT85411 PLP register 0xEB to set EN_BFET

Fig. 6-2 shows a typical I²C write transaction with the same ACT85411 PLP+PMIC. The controller first issues a START condition, then transmits the 7-bit I²C address 0x24, followed by writing the address of the PLP register to be written in the ACT85411, which in this case is 0xEB. The controller then immediately sends 8-bits of data (0x01) to internal register at 0xEB. This transaction results in register 0xEB, bit 0 (EN_BFET) being set to '1', which enables blocking FET and PLP boost functions. The controller signals the end of the transfer with a STOP condition.

Status and configuration transactions are the same as the above read and write examples but with corresponding addresses and data.

7. Summary

Qorvo PLP and PLP+PMIC ICs provide sophisticated solutions to common enterprise SSD challenges by incorporating many functions into a single, small package. The coordination of functions greatly simplifies designs that require power loss protection as well as power management. This application note provides a general overview of power loss protection, and PLP+PMIC ICs also include highly configurable power management (DC-DC converters, regulators, inputs/outputs). Features and implementation details vary between ICs. Qorvo datasheets contain detailed operating and application information, and evaluation kits are available.

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Revision History

Revision	Author	Date	Description
A	Jonathan Dodge, P.E.	1 Dec. 2025	Initial draft

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