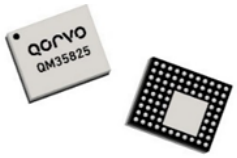
Production Data Sheet

QM35825

UWB Low-Power SoC

The QM35825 is a fully integrated Ultra-Wideband SoC compliant with IEEE 802.15.4™-2024.



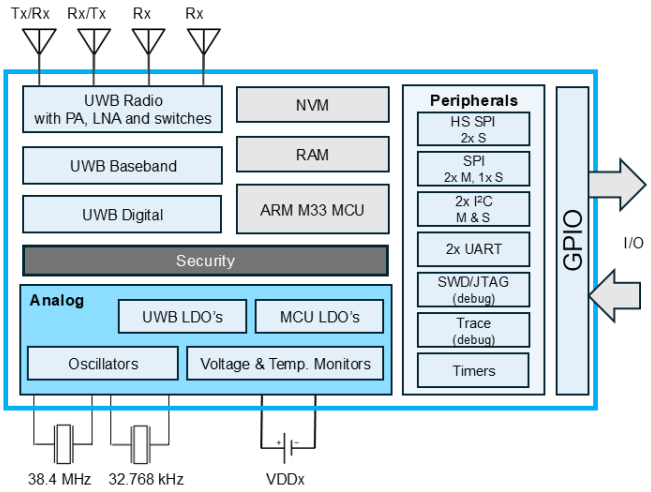
The SoC is optimized for all applications supporting FiRa™, Aliro and Omlox ranging schemes with an accuracy of +/- 5 cm and AoA at +/- 2°. And features on-chip computing for ranging, angle of arrival, radar and data transfer functions.

It integrates 4 flexible RF ports, LNAs, PA and RF switches, a Cortex-M33 with Secure Enclave and a wealth of security features and communication peripherals.

1 Key Features

- Full support for UWB HRP, BPRF & HPRF modes
- Supports channels 5 and 9 (6.5 GHz and 8 GHz)
- Supporting common data rates, incl. 31.2 Mbps and proprietary 62.4 Mbps
- Designed for worldwide UWB radio regulatory compliance, and FiRa 3.0 certified
- -98 dBm 1% RX sensitivity (BPRF-3)
- 104 dBm link budget
- 4-antenna flexible configuration solution
- Rx diversity with automatic switching
- Radar support
- Secure ranging/distance measurement using STS (Scrambled Time Stamp) and enhanced Time-of-Flight security options without external secure element
- ARM M33-Core with Secure Boot, Secure Debug, Secure Enclave
- HW support for RSA, ECC, SHA, AES, TRNG
- 2x Hi-Speed SPI slave, 2x SPI Master, 1x SPI Slave, 2x I^2C (master & slave) and 2x UART
- 25x GPIO, GPIO 1.2 V and 1.8 V support.

2 Functional Block Diagram



3 Applications

Enterprise and Industrial:

- Asset tracking and indoor navigation enabled by Precise Real Time Location Systems (RTLS) using TWR, TDoA or AoA schemes in a variety of mobile and IoT applications
- Secure Identification & logical access (payment console, barcode readers, laptops)
- Low latency wireless data comm
- Geofencing for safety
- Radar for Motion Detection, vital sign monitoring, people counting, gesture detection.

Consumer IoT:

- Enhanced user experience with location aware sensing based on FiRa 3.0 (TV and Air Mouse, Speakers and Smart Thermostats)
- Seamless Aliro Door Lock access.

4 Key Benefits

- High accuracy Secure Asset location: +/- 5 cm ranging, +/- 2° Angle-of-Arrival
- Flexible radar use cases, secure UWB positioning with radar sensing, 2D-AoA, 360°-AoA, 3D-AoA
- Best in class RF Performances with up to 104 dB of link budget, high multipath fading immunity
- Ease of design-in using only SPI interface and Qorvo drivers supporting multiple host processors & OS
- Low power consumption suitable for coin cell applications
  (2 µA DeepSleep, no retention)
- Supports high tag densities in RTLS
- On-chip and off-chip computing for secure ranging and radar applications.

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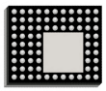
5 Description

The QM35825 is a fully integrated low-power CMOS RF 6.5 GHz - 8 GHz IR-UWB SoC (System-on-Chip), compliant with IEEE 802.15.4-2024.

It integrates UWB LNAs, PA and RF switches, 4 RF ports with highly flexible configuration, a Cortex-M33 with TrustZone and a wealth of security features and communication peripherals.



74-ball BGA
typical dimensions:
4.08 x 3.38 x 0.63 mm

The QM35825 embeds NVM (RRAM), RAM and on-chip One-Time Programmable (OTP) memory. RRAM can be used to store data such as antenna calibration data, Tx power level and crystal initial frequency error adjustment. These adjustment values can be automatically retrieved when needed.

The QM35825 consists of an analog front end (both RF and baseband) containing a receiver and transmitter and a digital back end. The latter interfaces to an external host processor, controls the analog front end, accepts data from the host processor for transmission and provides received data to the host processor over an industry standard SPI interface.

6 Key Features

6.1 Full Support for IEEE 802.15.4z BPRF and HPRF Modes

The QM35825 supports all mandatory and optional packet formats and modes (BPRF and HPRF) as first introduced in IEEE 802.15.4z.

6.2 High Accuracy AoA, TDoA and ToF

The Time-of-Flight (ToF) function enables +/- 5 cm ranging accuracy, supporting most indoor localization use-cases. The QM35825 supports Time Difference of Arrival (TDoA) and Angle of Arrival (AoA) with a +/- 2° accuracy over a single frame. Note: the ranging accuracy will also depend on the used firmware protocol.

See also section 8.9.

6.3 Security

Applications requiring High Security grade leverage an integrated secure link in the application processor to an external secure element, e.g., a standalone embedded secure element (eSE) or an integrated Secure Element (iSE), to reach compliance with the Common Criteria (CC) standard.

Using its integrated Secure Enclave with hardware cryptographic accelerators, the QM35825 can also manage non-CC-graded secure use cases standalone, without the support of an external secure element,

Access is enabled through additional interfaces such as a second high-speed SPI.

6.4 Performance and Power Consumption

Next to the standard data rates, the QM35825 also supports the higher proprietary data rate of 62.4 Mbps.

Power optimization gains come not only from the RF front end and channel impulse response data computing logic, but also on the whole system level by offloading the lower layers of the UWB stack directly in the chip itself.

6.5 Ease of Integration and Extensibility

The QM35825's software is built on a split protocol stack where the lower layer runs directly on the QM35825 itself, exposing a clean and highly abstracted interface (UCI API) to the upper layers running on an application processor. This two-tier split of work also allows a better power efficiency by offloading the most often used UWB MAC layers in the chip and allowing operations without any external application processor (AP) support.

The stack and firmware are extensible by means of plugins for adapting the software to the customer's needs and providing turn-key SW services such as advanced Tx power control, “Air Mouse” or advanced positioning “indoor GPS”.

7 Pin Configuration and Descriptions

The QM35825 is supplied in a BGA (74 balls) package. The pin assignments with descriptions are given in the figure and tables below.

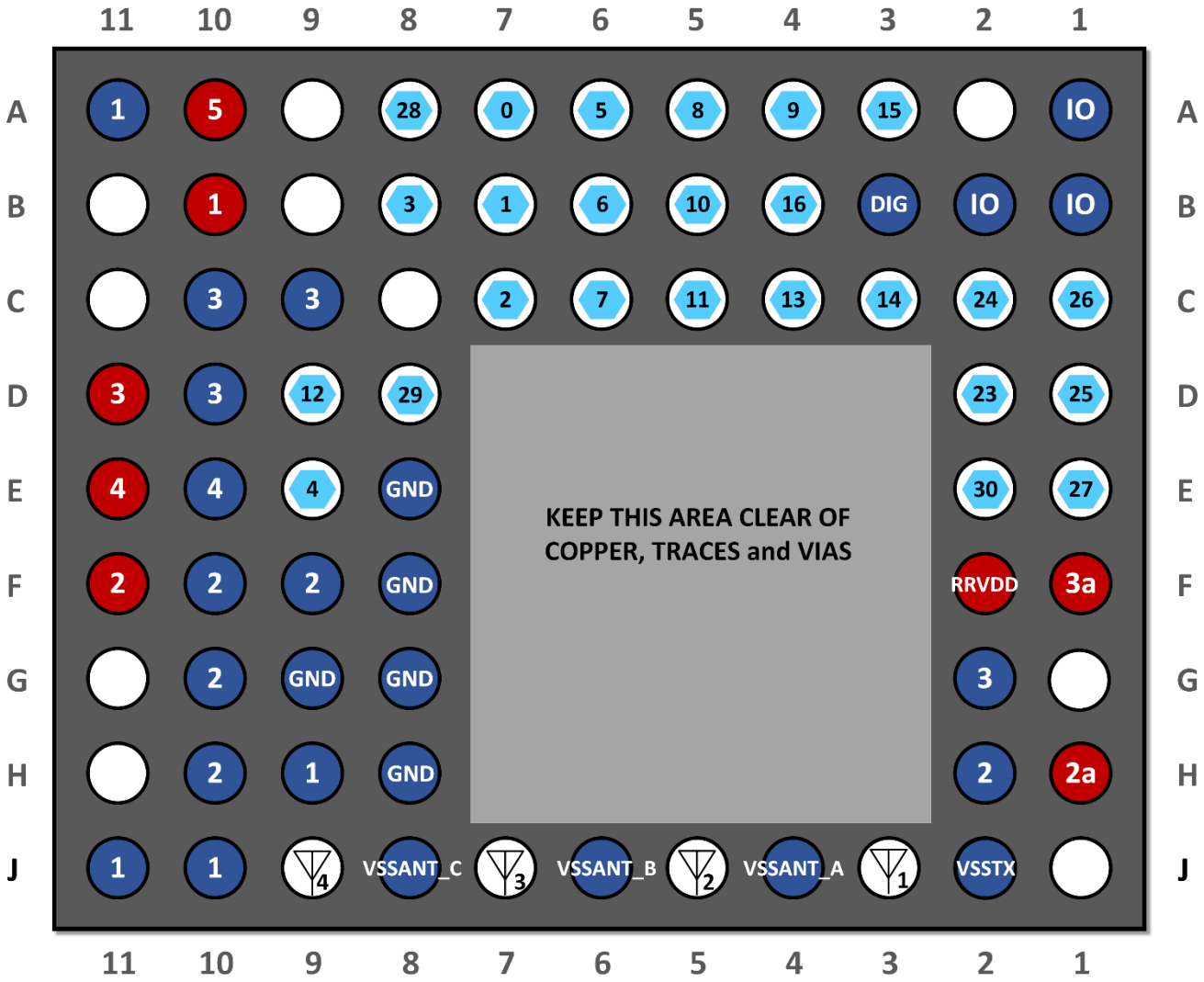


Figure 1: BGA-74 Ball Configuration – Bump Up / Bottom View

Symbol	Meaning
x	pin for GPIOx
x	pin is dedicated for power supply VDDx (VDD1-5, RRVDD)
x	VSSx (ground return) for VDDx, or VSSANT_X (ground return for antenna)
GND	general ground
	RF port for antenna x
	other

7.1 Pin Functions – GPIO

Table 1: Pin Functions – GPIO

Pin Name	Ball Nr	Supply	I/O Type (default)	Description
GPIO0	A7	VDDIO	Dig. I/O	General Purpose I/O pin
			Dig. Input	**HSSPI0_CLK** – High Speed SPI Peripheral, HSSPI0 Clock signal
GPIO1	B7	VDDIO	Dig. I/O	General Purpose I/O pin
			Dig. Output	**HSSPI0_PDO** – High Speed SPI Peripheral, SPI0 Data output. This pin will float in SLEEP and DEEPSLEEP mode preventing the host from receiving a predictive message when trying to communicate with the QM35825. HSSPI0_PDO defaults to an input when SPI is inactive, this allows it to be shared among other devices on the bus. When HSSPI0_CSn goes active (active low), then switch HSSPI0_PDO to be an output and drive the required data on it. HSSPIO0 can also be used for programming.
GPIO2	C7	VDDIO	Dig. I/O	General Purpose I/O pin
			Dig. Input	**HSSPI0_PDI** – High Speed SPI Peripheral, HSSPI0 Data input. HSSPIO0 can also be used for programming.
GPIO3	B8	VDDIO	Dig. I/O	General Purpose I/O pin
			Dig. Output	**HSS_IRQ** – High Speed SPI Peripheral, interrupt request. Notification to Host in HSSPIO mode. This pin will float in DEEP and DEEPSLEEP states and may cause spurious interrupts unless pulled low.
GPIO4	E9	VDDIO	Dig. I/O	General Purpose I/O pin
			Dig. Output	**SPI3_CSn** – SPI Controller, SPI3 Chip Select Signal, Active Low. The high-to-low transition on SPI_CSn signals the start of a new SPI transaction.
GPIO5	A6	VDDIO	Dig. I/O	General Purpose I/O pin
			Dig. Output	**SPI3_CLK** – SPI Controller, SPI3 Clock Signal
GPIO6	B6	VDDIO	Dig. I/O	General Purpose I/O pin
			Dig. Input	**SPI3_CDI** – SPI Controller, SPI3 Data Input
GPIO7	C6	VDDIO	Dig. I/O	General Purpose I/O pin
			Dig. Output	**SPI3_CDO** – SPI Controller, SPI3 Data Output. SPI3_CDO defaults to an input when SPI is inactive, this allows it to be shared among other devices on the bus. When SPI3_CSn goes active (active low), then switch SPI3_CDO to be an output and drive the required data on it.
GPIO8	A5	VDDIO	Dig. I/O	General Purpose I/O pin.
			Dig. Output	Interrupt **1** request output from the chip to the host processor.
GPIO9	A4	VDDIO	Dig. I/O	General Purpose I/O pin
GPIO10	B5	VDDIO	Dig. I/O	General Purpose I/O pin
GPIO11	C5	VDDIO	Dig. I/O	General Purpose I/O pin
GPIO12	D9	VDDIO	Dig. I/O	General Purpose I/O pin
GPIO13	C4	VDDIO	Dig. Output	General Purpose I/O pin. Interrupt **2** request output from the chip to the host processor.
GPIO14	C3	VDDIO	Dig. I/O	General Purpose I/O pin

Pin Name	Ball Nr	Supply	I/O Type (default)	Description
GPIO15	A3	VDDIO	Dig. I/O	General Purpose I/O pin
GPIO16	B4	VDDIO	Dig. I/O	Reserved – Do not connect.
GPIO23	D2	VDDIO	Dig. I/O	General Purpose I/O pin
			Dig. Input	**SWDIO/TMS – SWD/JTAG** Select signal
GPIO 24	C2	VDDIO	Dig. I/O	General Purpose I/O pin
			Dig. Input	**TRST/JRSTn** – JTAG Reset, Active low.
GPIO25	D1	VDDIO	Dig. I/O	General Purpose I/O pin
			Dig. Output	**SWO/TDO** – SWD/JTAG Data Output signal
GPIO26	C1	VDDIO	Dig. I/O	General Purpose I/O pin
			Dig. Input	**SWCLK/TCK** – SWD/JTAG Clock signal
GPIO27	E1	VDDIO	Dig. I/O	General Purpose I/O pin
			Dig. Input	**TDI** – JTAG Data Input Signal
GPIO28	A8	VDD5	Dig. I/O	General Purpose I/O pin
			Dig. Input	**HSSPI0_CSn** – High Speed SPI Peripheral, HSSPI0 Chip Select Signal, Active Low
GPIO29	D8	VDD5	Dig. I/O	General Purpose I/O pin
GPIO30	E2	VDDIO	Dig. I/O	General Purpose I/O pin

Note 1: **Warning**: There shall be no signals on any GPIO (including the RTCI) when the VDD1 / VDD5 is set to 0V.
Note 2: Max. acceptable voltage level on any GPIO pin should be: VDD5 + 0.7 V.
Note 3: Min. acceptable voltage level on any GPIO pin should be GND - 0.7 V.

7.2 Pin Functions – non-GPIO

Table 2: Pin Functions – Mode Independent

Pin Name	Ball Nr	Supply	I/O Type (default)	Description
RSTn	A9	VDD**5**	Digital In	Reset pin. Active Low. May be pulled low by external open-drain driver to reset the chip. Must not be pulled high by external source.
WAKEUP	B9	VDD**5**	Digital In	When asserted into its active high state, the WAKEUP pin brings the chip out of SLEEP or DEEPSLEEP states into operational mode. Connect to ground if not used.
EXTON	C8	VDD**5**	Digital Out	External devices enable. Asserted during wake-up process and held active until device enters sleep mode. It can be used to control external DC-DC converters or other circuits that are not required when the device is in sleep mode to minimize power consumption.
XTO	G11	VDD**2**	Analog Out	38.4 MHz reference crystal output. Requires 1 pF to ground, only if external clock is used, otherwise leave open.
XTI	H11	VDD**2**	Analog In	38.4 MHz reference crystal input or external reference overdrive pin.
RTCO	B11	VDD**1**	Analog Out	32.768 kHz reference crystal output for RTC. Note: Requires off-chip feedback resistor. If an ext. reference clock is used, tie to ground with 1 pF capacitor.
RTCI	C11	VDD**1**	Analog In	32.768 kHz reference crystal input for RTC. Note: Requires off-chip feedback resistor. Warning: there should be no signal when VDD1/VDD5 is set to 0V.
VSSTX	J2	VDD**2**	GND	RF ground pin for TX
VSSTXBAL	J1	VDD**2**	GND	RF ground pin for TX balun
ANT1	J3	VDD**2**	RF Tx/Rx	RF Input/Output 1. Connect to GND if not used.
ANT2	J5	VDD**2**	RF Tx/Rx	RF Input/Output 2. Connect to GND if not used.
ANT3	J7	VDD**2**	RF Rx	RF Input 3. Connect to GND if not used.
ANT4	J9	VDD**2**	RF Rx	RF Input 4. Connect to GND if not used.
VSSANT_A	J4	VDD**2**	GND	RF ground pin for antenna
VSSANT_B	J6	VDD**2**	GND	RF ground pin for antenna
VSSANT_C	J8	VDD**2**	GND	RF ground pin for antenna
VDD1	B10	VDD**1**	Power supply	VDD1 power supply (1.62 – 1.98 V)
VDD2	F11	VDD**2**	Power supply	VDD2 power supply (2.4 - 3.6 V)
VDD2a	H1	VDD**2**	Power supply	VDD2a power supply (2.4 - 3.6 V)
VDD3	D11	VDD**3**	Power supply	VDD3 power supply (1.5 - 3.6 V)
VDD3a	F1	VDD**3**	Power supply	VDD3a power supply (1.5 - 3.6 V)
VDD4	E11	VDD**4**	Power supply	VDD4 power supply (1.8 V +/-10%)
VDD5	A10	VDD5	Power supply	AON supply: 1.8 V +/- 10% for 1.8 V IO, 1.2 V +/-5% for 1.2 V IO
VDD2TX	G1	VDD**2**	Power decoupling	TX supply decoupling (2.2 V). Requires 220 nF cap. to GND.
VDDIO	A2	VDD**5**	Power supply	IO power supply decoupling. Internally connected to VDD5 with 2.5 Ω (typ.) switch to allow disconnect for ultra-low leakage mode. Requires 0.1 µF capacitor to ground.
RRVDD	F2	VDD**IO** or VDD**1**	Power supply	VDDIO for 1.8 V configuration. VDD1 for 1.2 V configuration. See chapter 12.
VSSDIG	B3	VDD**1**	GND	Ground return for internal digital core supply (VDDDIG). Star connect to VSS1. Recommended to bring out digital ground for noise isolation.
VSSIO	A1,B1,B2	VDD**1**	GND	Ground return for VDDIO. Normally (star) connected to VSS1.
VSS1	A11,J10, J11,H9	VDD**1**	GND	Ground return for VDD1, also PSUB connection.
VSS2	F9,F10,H2 G10,H10	VDD**2**	GND	Ground return for VDD2
VSS3	C9,C10, D10,G2	VDD**3**	GND	Ground return for VDD3
VSS4	E10	VDD**4**	GND	Ground return for VDD4
GND	E8,F8,G8, G9,H8	VDD**4**	GND	Connect to RF ground for functional (normal) mode

8 Electrical Characteristics

8.1 Absolute Maximum Ratings

Table 3: Absolute Maximum Ratings

Parameter	Min.	Max.	Units
Supply voltage VDD1, VDD2 and VDD3	-0.3	4.0	V
Supply Voltage VDD4 and VDD5	-0.3	2.5	V
Maximum input level on RF pins		15	dBm
Storage temperature	-65	+150	˚C
Operating temperature	-40	+85	
Junction temperature (T_J)	-	+125	
MSL (Moisture Sensitivity Level) for WLCSP packages (JEDEC-JSTD-020)	3	3	level
Tsol (Reflow soldering temperature)		+260	˚C
ESD HBM (Human Body Model)	all pins: 1750 V (Class 1C)		
ESD CDM (Charged Device Model)	all pins: 1000 V (Class C3)		

8.2 Nominal Operating Conditions

Table 4: Nominal Operating Conditions

Parameter	Min.	Typ.	Max.	Units	Condition / Note
Operating temperature	-40	-	85	˚C	
Supply voltage VDD1	1.62	1.8	1.98	V	Vmax limits of the RF circuit
Supply voltage VDD2	2.4	3.0	3.6	V	
Supply voltage VDD3	1.5	1.8	3.6	V	
Supply voltage VDD4	1.62	1.8	1.98	V	
Supply voltage VDD5	1.62	1.8	1.98	V	connected to VDD1 for 1.8 V support
Supply voltage VDD5	1.14	1.2	1.26	V	for 1.2 V IO

Note 1: Operation is guaranteed by design when operating within these ranges.
Note 2: Sufficient headroom for any power supply voltage ripple should be considered in system designs.

8.3 DC Characteristics – Current Consumption

Conditions: T_{amb} = 25 ˚C, MCU clock speed is 95 MHz.

Table 5: DC Characteristics - Current Consumption

Parameter	Min.	Typ.	Max.	Units	Condition / Note
Supply current DEEP SLEEP mode (S4) VDD1 = 1.8V VDD2 = 3.0V VDD3 = 1.8V VDD4 = 1.8V VDD5 = 1.2 V, 1.8 V		 1 0 0 1 0		µA	
Supply current SLEEP mode (S3A) VDD1 = 1.8V VDD2 = 3.0V VDD3 = 1.8V VDD4 = 1.8V VDD5 = 1.2 V, 1.8 V		 38 0 0 1 0		µA	SRAM Retention active
Supply current S0 (UWB Off) VDD1 = 1.8V VDD2 = 3.0V VDD3 = 1.8V VDD4 = 1.8V VDD5 = 1.2 V, 1.8 V		 1 1.6 17 0 0		mA	
SRAM retention S1 (UWB Off) VDD1 = 1.8V VDD2 = 3.0V VDD3 = 1.8V VDD4 = 1.8V VDD5 = 1.2 V, 1.8 V		 1 1.6 12 0 0		mA	
Supply current IDLE_PLL CH5, CH9 VDD1 = 1.8V VDD2 = 3.0V VDD3 = 1.8V VDD4 = 1.8V VDD5 = 1.2 V, 1.8 V		 1 2.6 24 0 0		mA	S0+IDLE_PLL
Supply current IDLE_RC mode VDD1 = 1.8V VDD2 = 3.0V VDD3 = 1.8V VDD4 = 1.8V VDD5 = 1.2 V, 1.8 V		 1 1.6 18 0 0		mA	S0+IDLE_RC
Peak Current Continuous Tx/Rx					
TX CH5 (max power) VDD1 = 1.8V VDD2 = 3.0V VDD3 = 1.8V VDD4 = 1.8V VDD5 = 1.8V		 4.6 30 30 90* 0		mA	BPRF-03 mode. Continuous TX only used as test mode. In typical operation TX is powered up for frame transmission then powered down. *PA On. In the case of PA Off; current @ VDD4 = 0 mA.
TX CH9 (max power) VDD1 = 1.8V VDD2 = 3.0V		 4.6 29		mA	* see comment above

Parameter	Min.	Typ.	Max.	Units	Condition / Note
VDD3 = 1.8V VDD4 = 1.8V VDD5 = 1.8V		27 90* 0			
RX CH5 (single RX) VDD1 = 1.8V VDD2 = 3.0V VDD3 = 1.8V VDD4 = 1.8V VDD5 = 1.8V		 4.5 4 85 9.9* 0		mA	Measured in preamble hunt mode. *LNA On. In the case of LNA Off; current @ VDD4 = 0 mA.
RX CH9 (single RX) VDD1 = 1.8V VDD2 = 3.0V VDD3 = 1.8V VDD4 = 1.8V VDD5 = 1.8V		 4.5 4 81 9.9* 0		mA	Measured in preamble hunt mode. *LNA On. In the case of LNA Off; current @ VDD4 = 0 mA.
Dual RX CH5 VDD1 = 1.8V VDD2 = 3.0V VDD3 = 1.8V VDD4 = 1.8V VDD5 = 1.8V		 4.5 4 137 18.5* 0		mA	Dual RX mode. *LNA On. In the case of LNA Off; current @ VDD4 = 0 mA.
Dual RX CH9 VDD1 = 1.8V VDD2 = 3.0V VDD3 = 1.8V VDD4 = 1.8V VDD5 = 1.8V		 4.5 4 137 18.5* 0		mA	Dual RX mode. *LNA On. In the case of LNA Off; current @ VDD4 = 0 mA.
Digital input voltage High	0.7*VDD5			V	
Digital input voltage Low			0.3*VDD5	V	
Digital output voltage	0.7*VDD5			V	assumes 500 Ω load
Digital output voltage			0.3*VDD5	V	assumes 500 Ω load
Digital output drive current		8			VDD5= 1.8 V
Digital output drive current		4			VDD5= 1.2 V
EXTON	3	4		mA	
Maximum Current					
VDD1			5	mA	
VDD2/VDD2a			110		applies to TX CW test mode only
VDD3/VDD3a			140		applicable in dual RX active mode
VDD4			110		nominal value when PA is active
VDD5			5		output pins shorted to ground

8.4 Receiver AC Characteristics

Conditions: T_{amb} = 25 ˚C, VDD2 = 3.0 V, VDD1=VDD3=VDD4 = 1.8 V unless otherwise stated.

Table 6: Operating Frequencies

Parameter	Min.	Typ.	Max.	Units	Condition / Note
Center Frequency - channel 5		6489.6		MHz	
Center Frequency - channel 9		7987.2		MHz	
Channel Bandwidth		499.2		MHz	programmable

Table 7: RX Blocking - Channel 5

Parameter	Min.	Typ.	Max.	Units	Condition / Note
Low Band 617 - 960 MHz		0		dBm	LTE Signal. Bandwidth: 20 MHz (100 RB)
Medium Band 1427 – 2200 MHz		-7		dBm	
High Band 2300 – 2690 MHz		0		dBm	
Ultra High Band (n77/n78) 3300 – 4200 MHz		-30		dBm	NR Signal Bandwidth: 20 MHz (30 kHz SCS, 51 RB)
Ultra High Band (n79) 4400 – 5000 MHz		-17		dBm	
Wi-Fi 5150 – 5500 MHz		-28		dBm	Wi-Fi Signal. Bandwidth: 20 MHz (802.11ax)
Wi-Fi 5500 – 5850 MHz		-34		dBm	

Note: Chip referred (power at the pin) to give 1% PER with useful signal 3 dB above reference sensitivity level.
Note: please refer to the plots in section 9.2 for details.

Table 8: RX Blocking - Channel 9

Parameter	Min.	Typ.	Max.	Units	Condition / Note
Low Band 617 - 960 MHz		4		dBm	LTE Signal. Bandwidth: 20 MHz (100 RB)
Medium Band 1427 – 2200 MHz		0		dBm	
High Band 2300 – 2690 MHz		-14		dBm	
Ultra High Band (n77/n78) 3300 – 4200 MHz		-32		dBm	NR Signal Bandwidth: 20 MHz (30 kHz SCS, 51 RB)
Ultra High Band (n79) 4400 – 5000 MHz		-20		dBm	
Wi-Fi 5150 – 5500 MHz		-24		dBm	Wi-Fi Signal. Bandwidth: 20 MHz (802.11ax)
Wi-Fi 5500 – 5850 MHz		-33		dBm	

Note: Chip referred (power at the pin) to give 1% PER with useful signal 3 dB above reference sensitivity level.
Note: please refer to the plots in section 9.2 for details.

8.5 Receiver Sensitivity Characteristics

Conditions: T_{amb} = 25 ˚C, VDD2 = 3.0 V and VDD1=VDD3=VDD4 = 1.8 V.
LNA ON. 20-byte payload. Carrier frequency offset = ±10 ppm. Reference Frequency = 38.4 MHz.
Sensitivity is measured at the 1% Packet Error Rate (PER). Applies to all antenna ports.

With reference frequency clock @ 26 MHz, RX sensitivity levels are degraded by 1 dB.

Note: For STS packet configuration 3 (SP3) where there is no PHY header and no payload, Rx Sensitivity is the same".

Table 9: Reference Sensitivity Level

Channel	HPRF/ BPRF	IEEE Subset/ LNA State/ RX Mode	Typical Receiver Sensitivity Level [dBm / 500 MHz]
CH5	BPRF	Set#03 (FiRa TC) Single RX mode	-98
		Set#03 (FiRa TC) Dual RX mode	-101
		Set#04 (FiRa TC) Single RX mode	-103.5
		Set#04 (FiRa TC) Dual RX mode	-103.5
	HPRF	Set#06 (FiRa TC) Single RX mode	-98
		Set#06 (FiRa TC) Dual RX mode	-101.3
		Set#14 (FiRa TC) LNA ON Single RX mode	-94.5
		Set#14 (FiRa TC) LNA ON Dual RX mode	-97
CH9	BPRF	Set#03 (FiRa TC) Single RX mode	-97.5
		Set#03 (FiRa TC) Dual RX mode	-100.5
		Set#04 (FiRa TC) Single RX mode	-103.5
		Set#04 (FiRa TC) Dual RX mode	-103.5
	HPRF	Set#06 (FiRa TC) Single RX mode	-98
		Set#06 (FiRa TC) Dual RX mode	-101.3
		Set#14 (FiRa TC) Single RX mode	-94
		Set#14 (FiRa TC) Dual RX mode	-96.5

Parameter	Min.	Typ.	Max.	Units
Rx Sensitivity variation over temperature		0.025		dB/°C

8.6 Reference Clock Characteristics

Conditions: T_{amb} = 25 ˚C, VDD1 = 1.8 V, VDD2 = 3.0 V, VDD3 = 1.8 V, VDD5 = 1.2 V.
Here VDD2 is both VDD2 and VDD2a combined. VDD3 is both VDD3 and VDD3a combined.

Table 10: Reference Clock Characteristics

Parameter	Min.	Typ.	Max.	Units	Condition / Note
Crystal oscillator reference frequency		38.4		MHz	A reference frequency can be provided from an external reference in place of a crystal if desired. Also supports 19.2, 26 and 52 MHz reference frequencies.
Crystal specifications					
Load capacitance	10			pF	depends on crystal used and PCB parasitics
Shunt capacitance	0		4	pF	
Drive level			200	µW	depends on crystal & load capacitance used
Equivalent Series Resistance (ESR)			60	Ω	
Frequency tolerance			±20	ppm	QM35825 includes circuitry to trim the crystal oscillator to reduce the initial frequency offset.
Crystal trimming range	-20		+20	ppm	Trimming range provided by on-chip circuitry. Value depends on the crystal used and PCB design.
External Reference (e.g.: TCXO)					
Amplitude	0.8		VDD2	Vpp	Must be AC coupled. A coupling capacitor value of 10 nF is recommended.
SSB Phase Noise Power Density			-107	dBc/Hz	@100 Hz offset
			-127		@1 kHz offset
			-137		@10 kHz offset
			-142		@100 kHz offset
			-147		@1 MHz offset
Duty Cycle	40		60	%	
External RTC clock 32.768 kHz					
Temperature range	-40	25	85	°C	
Nominal Frequency		32.768		kHz	buffer checked at nominal frequency +/- 10% across PVT
Input High Voltage	0.65* VDD1		VDD1	V	
Input Low voltage		0	0.4	V	
Duty Cycle	40	50	60	%	
Frequency Tolerance				+/- 100 ppm	over all conditions (initial frequency tolerance aging and temperature)
Internal Fast and Slow Oscillators					
Slow RC - default freq.		21		kHz	
32 kHz RC – default freq.		32.768		kHz	
32 kHz RC Frequency Tolerance		150		ppm	over 5 ms
32 kHz RC frequency over temp.		250		ppm/°C	
Fast RC – Default Frequency		95		MHz	

8.7 Transmitter Characteristics

Conditions: T_{amb} = 25 ˚C, VDD2 = 3.0 V, VDD1=VDD3=VDD4 = 1.8 V, VDD5 = 1.2 V.

Table 11: Transmitter AC Characteristics

Parameter	Condition / Note	Min.	Typ.	Max.	Units
Center Frequency	channel 5		6489.6		MHz
	channel 9		7987.2		MHz
Channel Bandwidth			499.2		MHz
Maximum Mean Power Spectral Density	channel 5, for BPRF-3 (Fira TC)		-19.6		dBm / MHz
	channel 9, for BPRF-3 (Fira TC)		-20.8		
	channel 5, for HPRF-14 (Fira TC)		-15.5		
	channel 9, for HPRF-14 (Fira TC)		-18		
Maximum Output Channel Power	channel 5, for BPRF-3 (Fira TC)		6		dBm / 500 MHz
	channel 9, for BPRF-3 (Fira TC)		4.5		
	channel 5, for HPRF-14 (Fira TC)		9		
	channel 9, for HPRF-14 (Fira TC)		7.5		
Peak Power	BPRF Set #3		13		dBm
Load Impedance	single ended		50		Ω
Power Level Range			30		dB
Output Power Variation with temperature			0.025		dB / °C
Output Power Variation with voltage	internally regulated		0		dB / V
Transmit Bandwidth Variation with temperature	with internal calibration enabled		0.2		MHz / °C

8.8 Temperature and Voltage Monitor Characteristics

Table 12: Temperature and Voltage Monitor Characteristics

Parameter	Min.	Typ.	Max.	Units
VDD1 Voltage Monitor Range	1.62		1.98	V
VDD1 Voltage Monitor Accuracy		5		%
Temperature Monitor Range	-40		85	°C
Temperature Monitor Accuracy (using customer's single point calibration)		+/- 4		°C

8.9 Location Accuracy Characteristics

Table 13: Location Accuracy Characteristics

Parameter	Min.	Typ.	Max.	Units	Condition / Note
Ranging mean accuracy (after applied calibration)	-5		5	cm	BPRF3 and BPRF4 packets. In line-of-sight conditions.
Ranging standard deviation		3		cm	
PDoA accuracy (*) low power, single RX mode	-12.5		12.5	deg	tested in conducted mode across full dynamic range of the receiver
PDoA standard deviation low power, single RX mode		5		deg	
PDoA accuracy (*) low power, dual RX mode	-4		4	deg	
PDoA standard deviation low power, dual RX mode		4		deg	

Note (*): in a typical PDoA based system the computed Angle of Arrival (AoA) accuracy is better than the PDoA accuracy by a factor of ~ 2, i.e., if PDoA accuracy is ± 12.5° then AoA accuracy is ± 6.25°.
See also section 6.2.

9 Typical Performance

9.1 Transmit Spectra

The maximum transmit spectra for channel 5 and channel 9, for BPRF03 and HPRF14, are shown in the plots below.

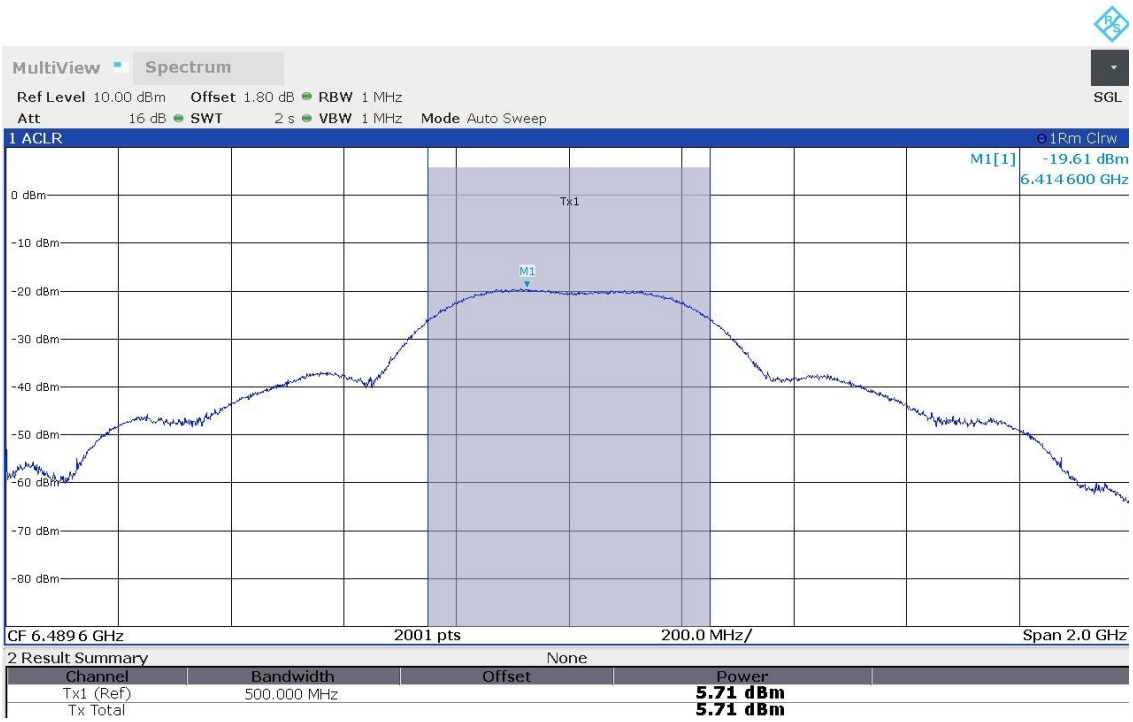


Figure 2: Tx spectrum BPRF3 – ch5

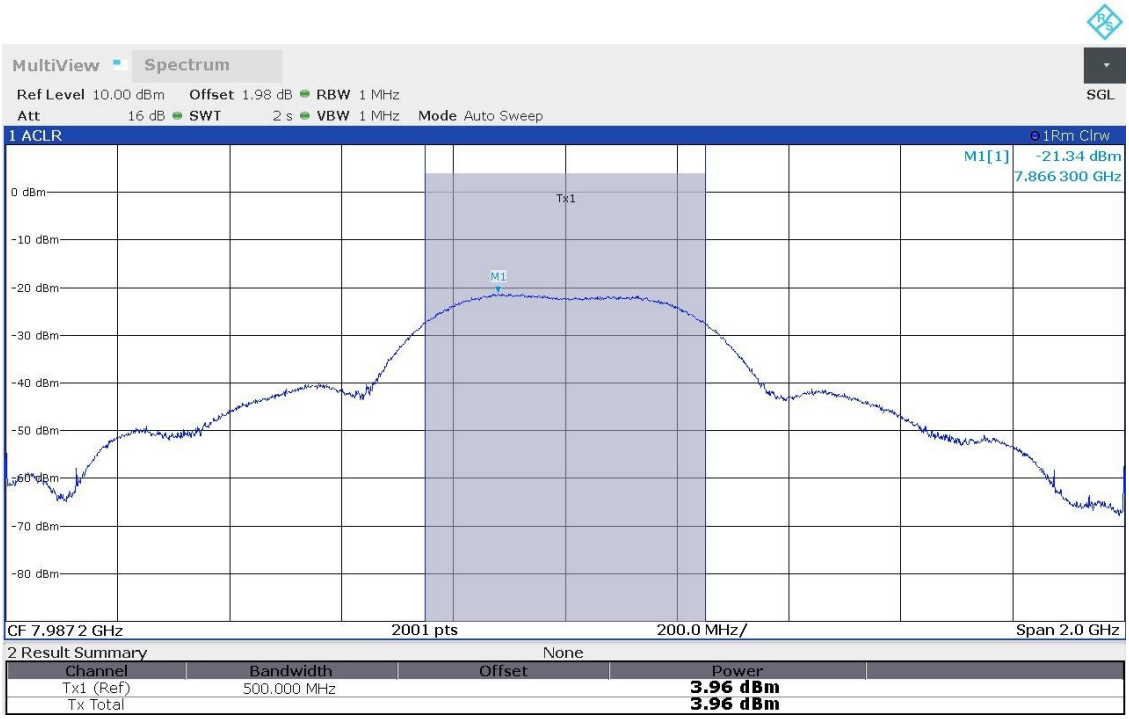


Figure 3: Tx Spectrum BPRF3 – ch9

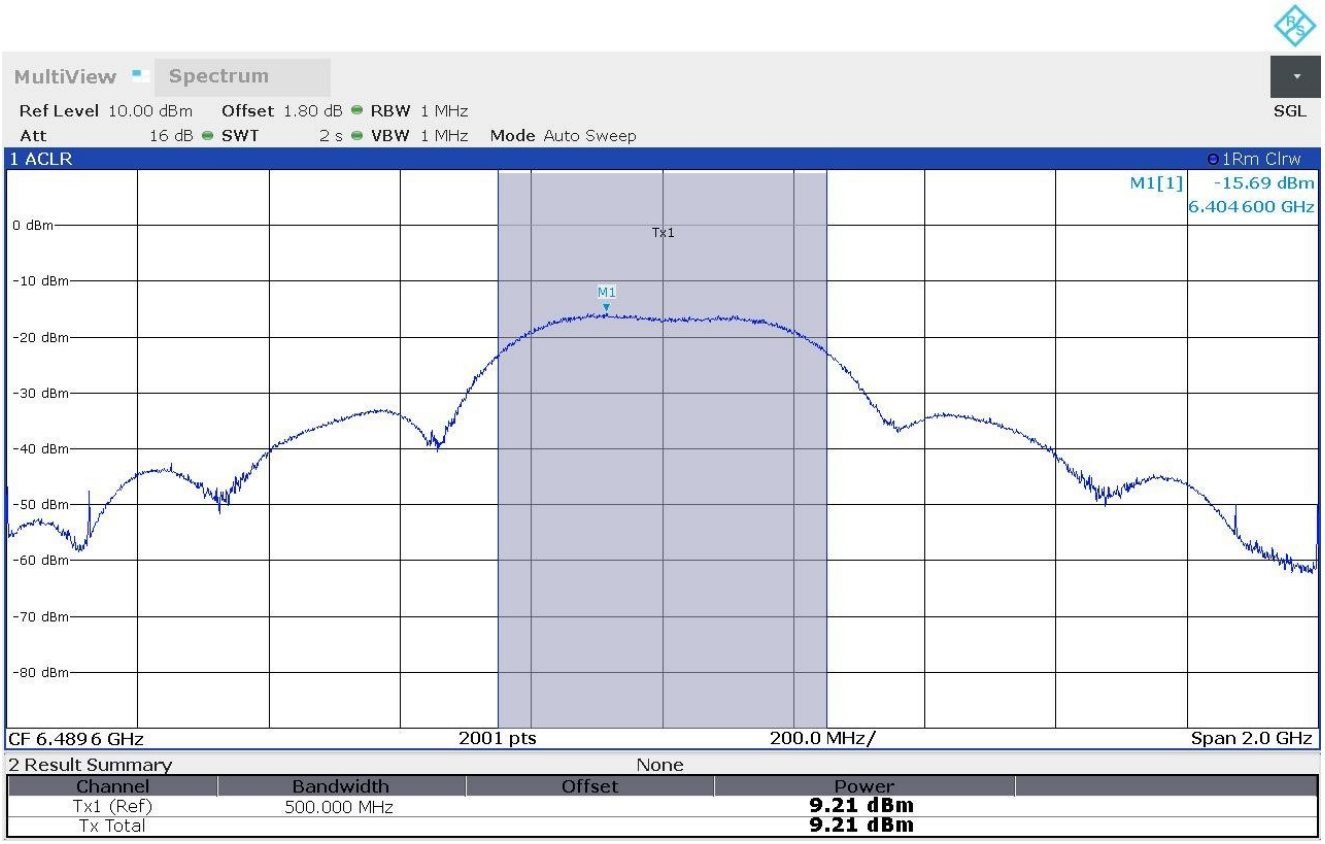


Figure 4: Tx spectrum HPRF14 – ch5

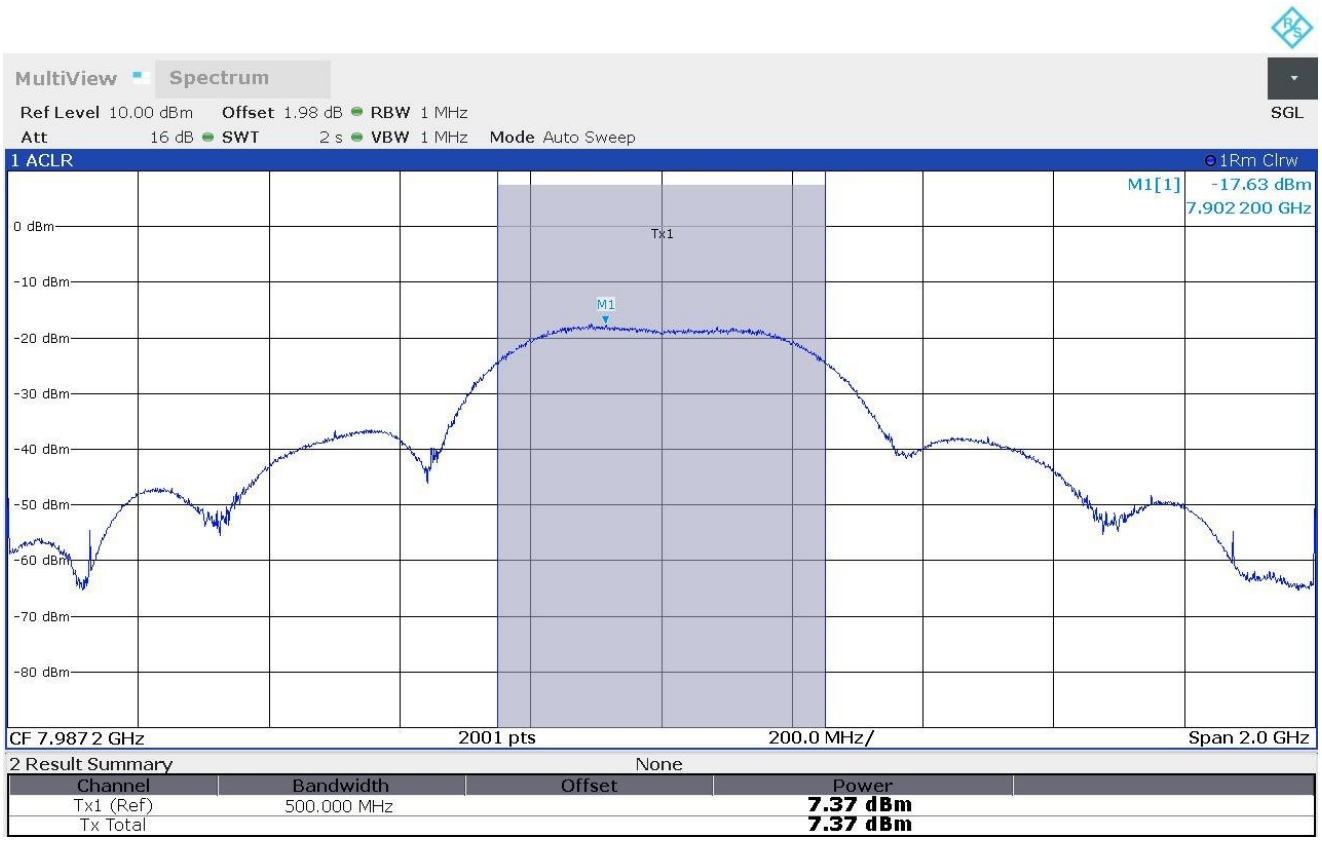


Figure 5: Tx spectrum HPRF14 – ch9

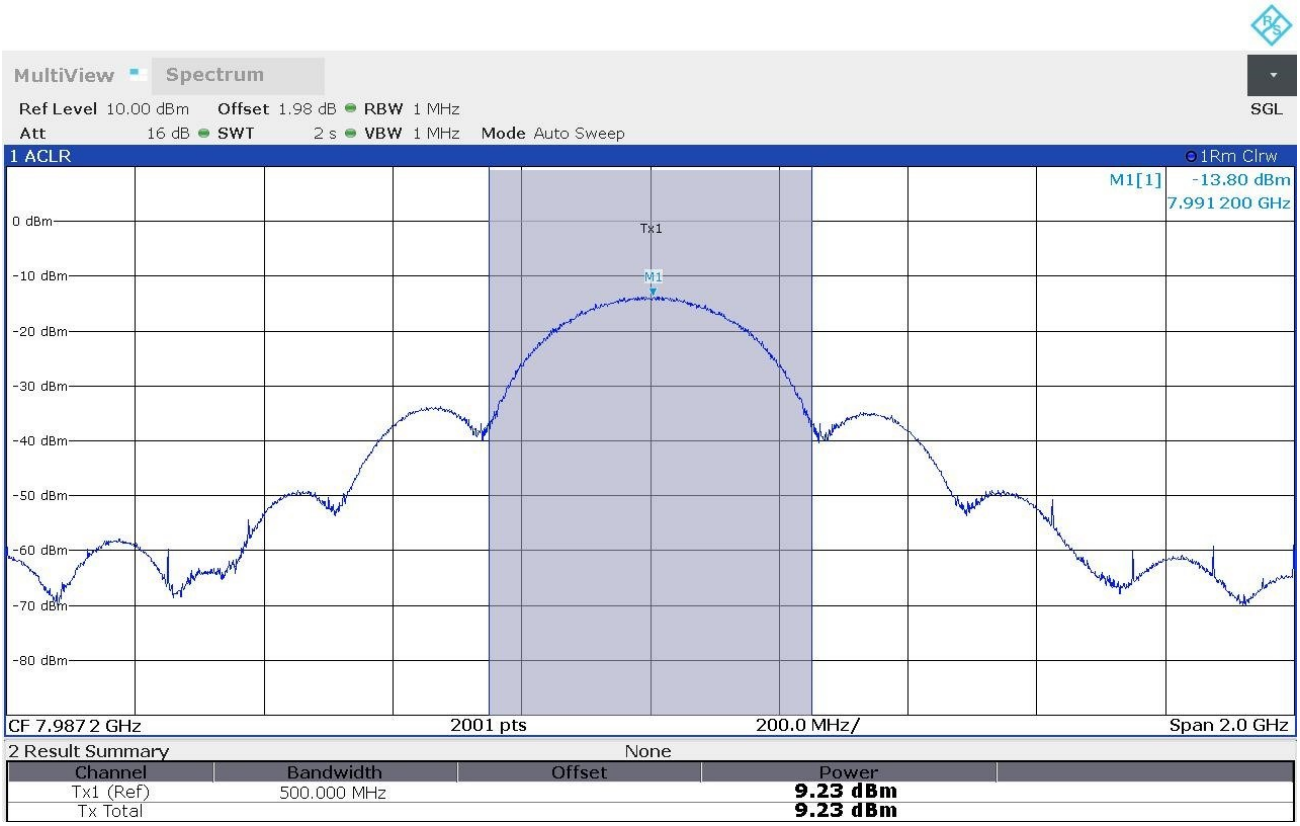


Figure 6: Tx Spectrum HPRF14 – ch9 – Japan

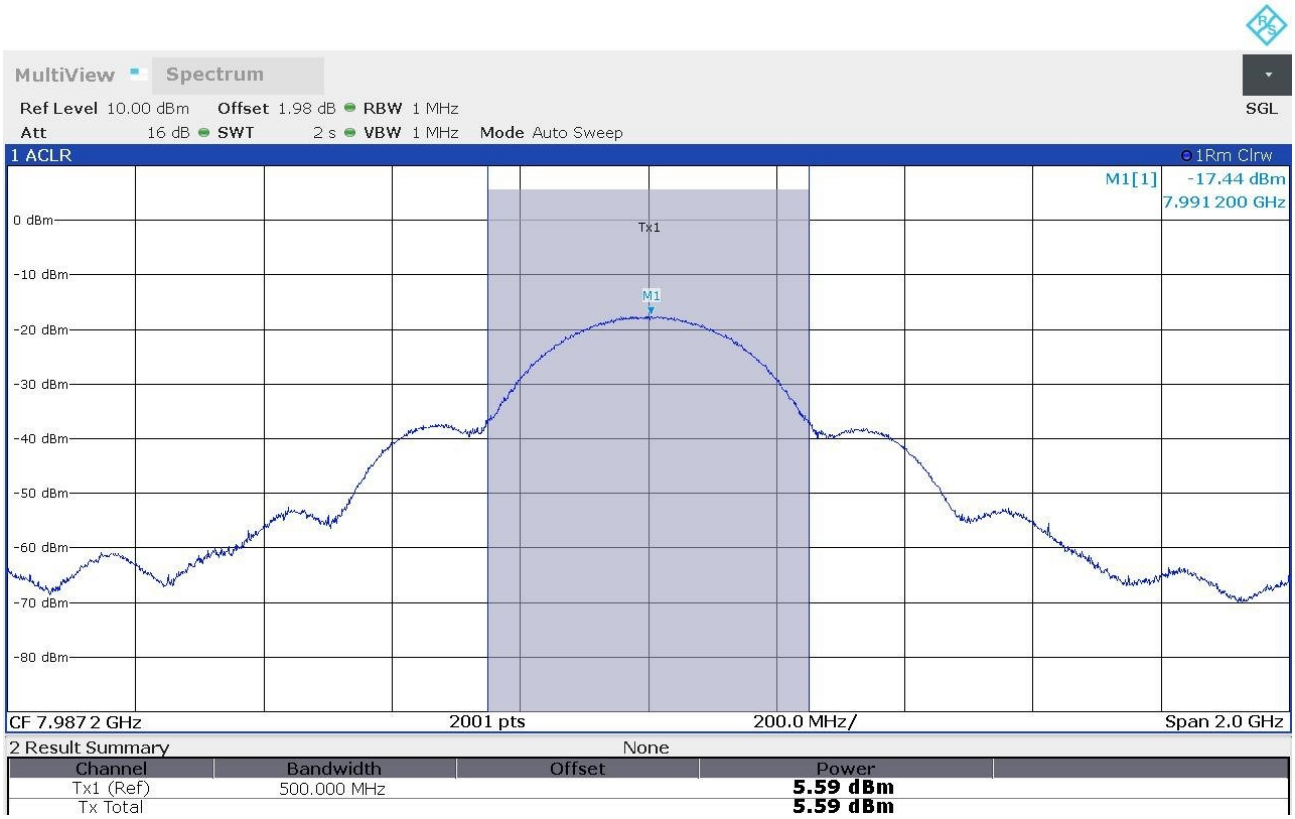


Figure 7: Tx Spectrum BPRF3 – ch9 – Japan

9.2 Receiver Blocking

The following plots show typical blocking levels to give 1% UWB PER at 3 dB back-off from the sensitivity point.
Note that the flat responses are due to test limitations.
For more information regarding the measured bands please refer to section 8.4.

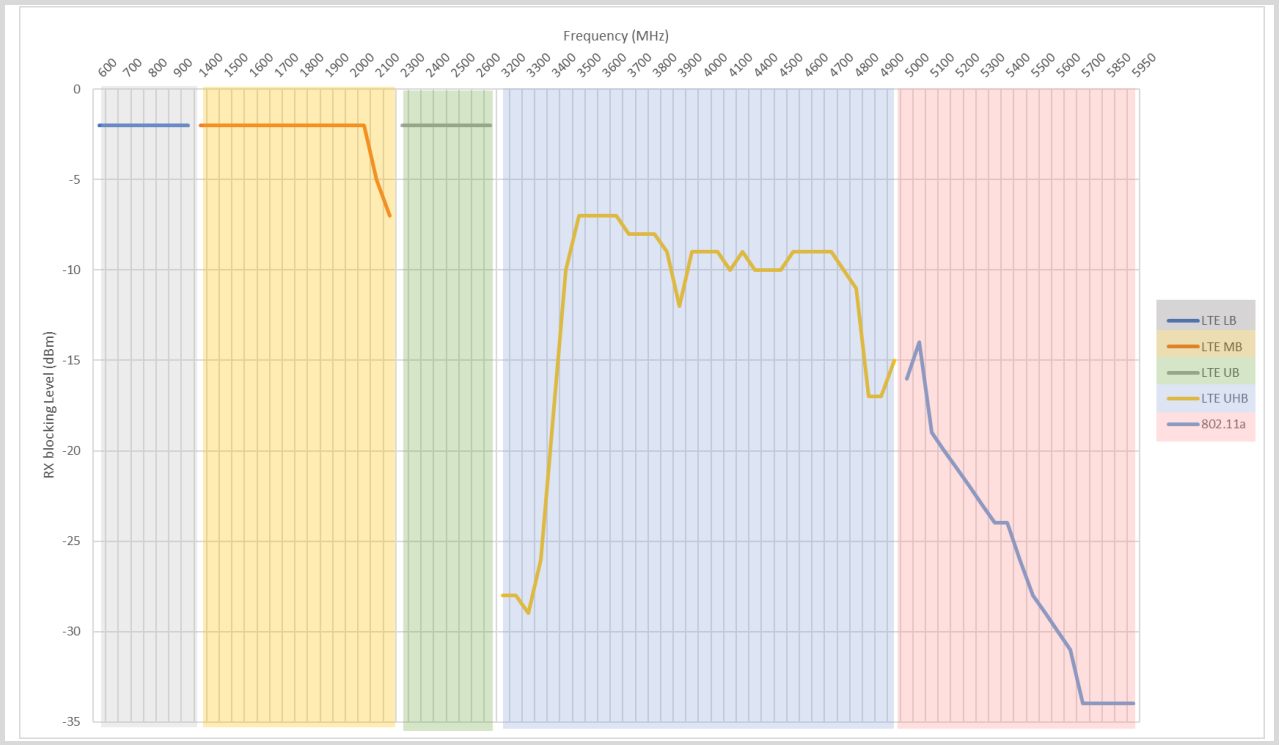


Figure 8: Rx Blocking BPRF3 – Ch5

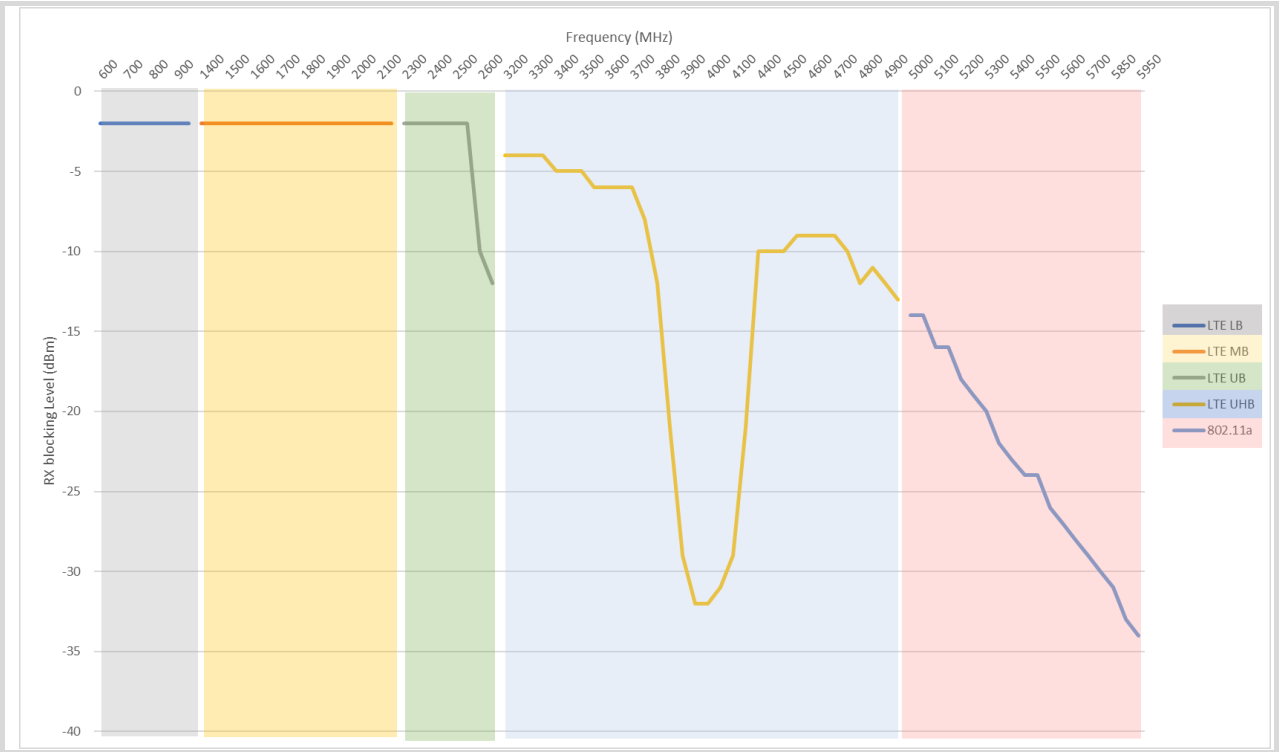


Figure 9: Rx Blocking BPRF3 – Ch9

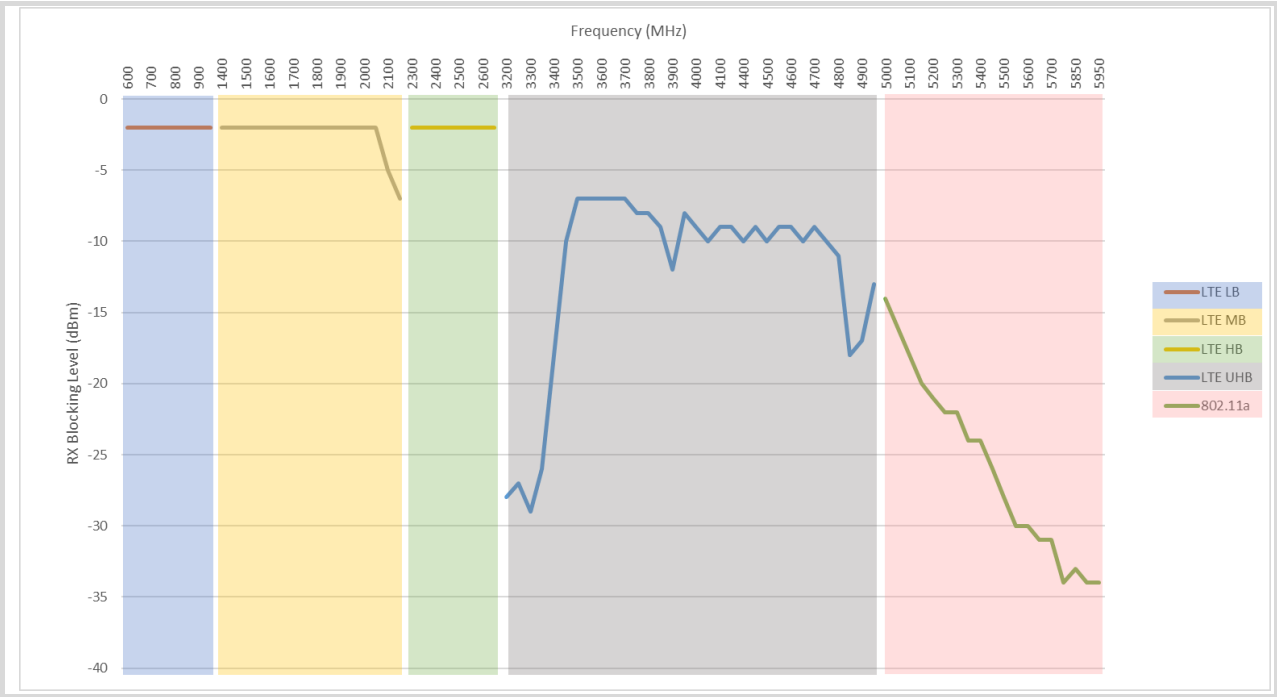


Figure 10: Rx Blocking HPRF14 – Ch5

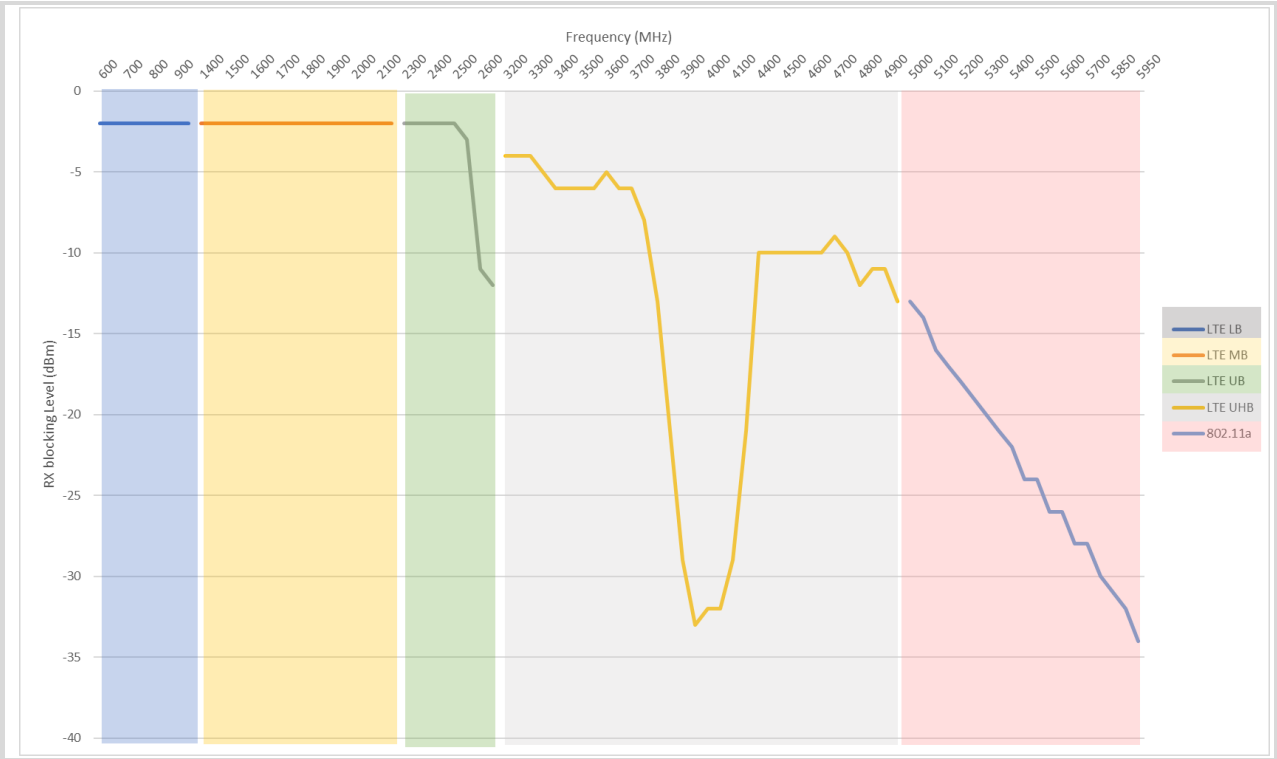


Figure 11: Rx Blocking HPRF14 – Ch9

9.3 Ranging Performance

The Range Error Histogram shown below is based on 4000 samples (BPRF4 configuration).

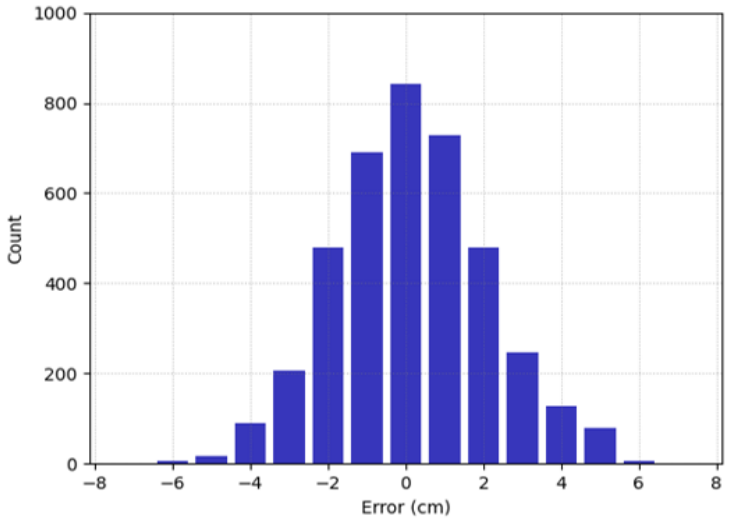


Figure 12: Range Error Histogram

10 Functional Description

10.1 Physical Layer Modes

Please refer to [3] and [4] for the PHY specification.

10.2 Supported Channels and Bandwidths

The QM35825 supports the following IEEE 802.15.4 UWB channels:

Table 14: Supported Channels and Bandwidth

UWB Channel Nr	Center Frequency [MHz]	Bandwidth [MHz]
5	6489.6	499.2
9	7987.2	499.2

10.3 Supported Bit Rates

The QM35825 supports IEEE 802.15.4-2011 and IEEE 802.15.4-2020 UWB standard bit rates.
A full list is shown on the table below.

Table 15: Supported Bit Rates

Bit Rate	Mode	Preamble Code	Remark
850 kbps	BPRF	<25	
6.8 Mbps	BPRF	<25	K=3 Viterbi and RS for ECC
6.8 Mbps	HPRF	>=25	K=3 Viterbi and RS for ECC
7.2 Mbps	HPRF	>=25	
27 Mbps	HPRF	>=25	K=3 Viterbi and RS for ECC
31.2 Mbps	HPRF	>=25	
62.4 Mbps	Proprietary	>=25	

In general, lower data rates give; increased receiver sensitivity, increased link margin and longer range but due to longer frame lengths they result in increased air occupancy per frame and a reduction in the number of individual transmissions that can take place per unit time.

10.4 Frame Format IEEE 802.15.4-2015 and IEEE 802.15.4-2020

Frames, as initially defined in IEEE 802.15.4-2015 and IEEE 802.15.4-2020, are structured as shown in Figure 12 below. Detailed descriptions of the frame format are given in the standards. The frame consists of a Synchronization header (SHR) which includes the preamble symbols and Start Frame Delimiter (SFD), followed by the PHY header (PHR) and data. The data frame is usually specified in number of bytes and the frame format will include 48 Reed-Solomon parity bits following each block of 330 data bits (or less).

While zero length payloads and zero length PHR is supported, the maximum frame length is 1023-bytes, including the 2-byte FCS.

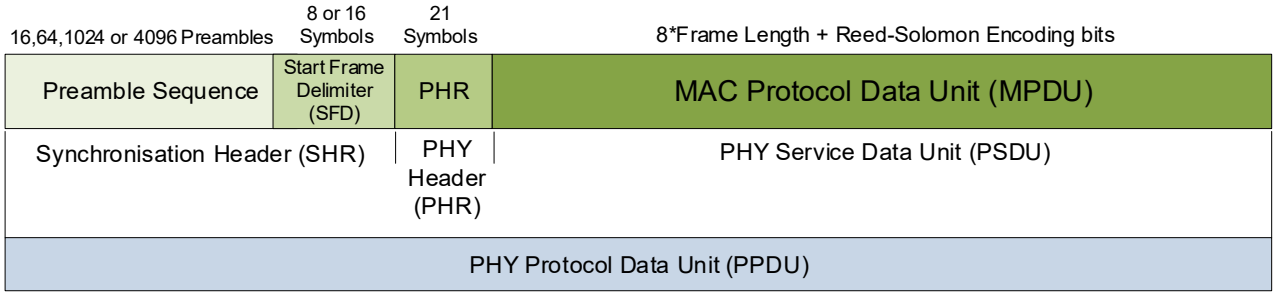


Figure 13: IEEE 802.15.4-2015 PPDU Structure Frame

10.5 Formats of IEEE 802.15.4z-2020

The 4z amendment added new packet formats to HRP UWB PHY incorporating a Scrambled Timestamp Sequence (STS) into the packet structure, defining four STS Packet Configurations as shown in Figure 14 below.

- Packet configuration SP**0** is a standard IEEE 802.15.4-2015 UWB packet structure. This ensures backward compatibility with Qorvo's DW1000 chip, see frame format above.
- Packet configuration SP**1** includes Scrambled Timestamp Sequence (STS) between the start of frame delimiter (SFD) and the PHY header (PHR).
- Packet configuration SP**2** contains the STS after the payload is complete (there is a short configurable gap between the end of the payload and the start of the STS). The gap can be any integer value from 1 to 127 symbols.
- Packet configuration SP**3** is when there is no PHR and no payload.

The STS is a random sequence of positive and negative pulses generated using an AES-128 based Deterministic Random Bit Generator (DRBG). Only valid transmitters and receivers have the correct seed (e.g., the key) to generate the sequence for transmission and to validly cross correlate in the receiver to determine the receive timestamp. The STS provides secure receive timestamping and secure ranging.

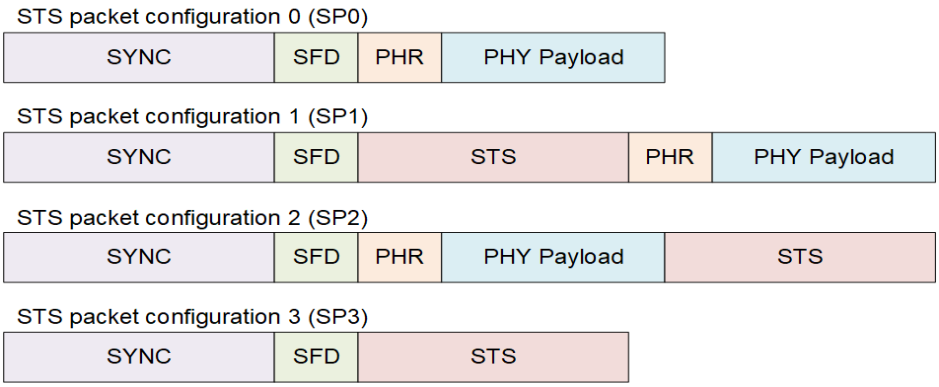


Figure 14: IEEE 802.15.4z-2020 HRP UWB PHY PPDU Formats

10.6 Proprietary Long Frames

The QM35825 offers a proprietary long frame mode where frames of up to 1023 bytes may be transferred.

10.7 No Data Frames

The QM35825 offers zero-length payloads and zero-length PHR. This is for use cases where an alternative method of data communication is available.

10.8 Reference Crystal Oscillator

With the addition of an external crystal and appropriate loading capacitors, the on-chip crystal oscillator generates the reference frequency for the integrated frequency synthesizer's PLL. A trim facility is provided which can be used to trim out crystal initial frequency error. Typically, a trimming range of ± 20 ppm is possible using a 6-bit trim value. This trimming, in 0.125 pF steps, provides for up to 8 pF additional capacitance on the XTI and XTO crystal connections.

10.8.1 Calculation of External Capacitor Values for Frequency Trim

Ideally, the value of external loading capacitors (Cext) should be calculated to give an equal trim range about the center trim value. To do this, one needs to estimate the parasitic capacitance (Cpar) between the crystal pads XTI/XTO and the crystal pads.

A good starting estimate for Cext is approximately 3.6 pF. However, some trial and error may be required initially. The values of Cm, Lm, Rm and Co, obtained from the crystal manufacturer, are also required (see Figure 15).

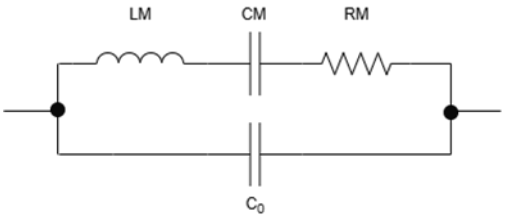


Figure 15: Crystal Equivalent Model

A typical crystal trimming plot is shown in Figure 16.

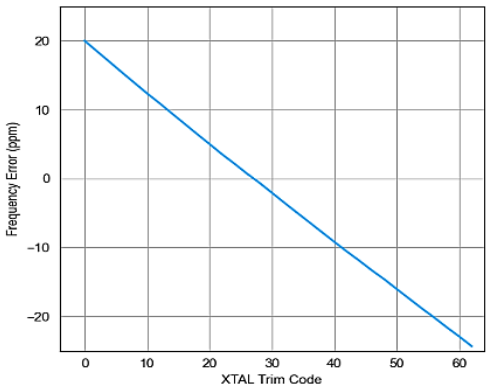


Figure 16: Crystal Trim Plot

Using the following formula, the required Cext and trim range can be estimated where:

$$f_s = \frac{1}{2\pi\sqrt{C_M L_M}}$$

$$f_p = f_s\left(\sqrt{1+\frac{C_M}{C_0}}\right)$$

$$f_L = f_s\left(\sqrt{1+\frac{C_M}{C_L}}\right)$$

$$C_L = C_0 + \frac{1}{2}(C_{TRIM} + C_{PAR} + C_{EXT})$$

$$\Delta f_{ppm} = 10^6 \times \frac{f_L - f_{L_{nom}}}{f_{L_{nom}}}$$

f_s = series frequency
f_p = parallel frequency
f_L = loaded (desired) frequency

11 Operational States

11.1 Overview

The QM35825 has several basic operating states as described in the table below.

Table 16: Operational States

ACPI state	UWB state	Description
S5 (OFF)	OFF	All the device blocks are powered off, the digital core and CPU is off. The reset line is held low.
BOOT	OFF	After power up, the secure ROM boot image starts executing and following image verification will execute the application image in NVM.
S0 (CPU_ON / ACTIVE)	*	The CPU is active, clocks are not gated. FCLK at 64 MHz or 100 MHz XTAL (38.4 MHz)/FOSC enabled.
S1 (SUSPENDED – WAIT FOR INTERRUPT)	*	The CPU has gated clocks (WFI). The wake-up time is very fast. In S1, the UWBS remains in the same state it was when the CPU enters the S1 state. As an example, if UWBS is in IDLE_PLL when the CPU enters S1, it remains in IDLE_PLL while the CPU is in S1.
S3a (SLEEP/ RETENTION)	OFF	The CPU retention sleep (S3a) state. The S3a mode is entered under command from the AON driver. The CPU is powered down. The content of the I-cache and the CPU context is lost. XTAL (38.4 MHz) is shut down. Only the data in SRAM is saved. The wake-up time can be long and can involve restoring some CPU context from the SRAM.
S4 (SLEEP without RETENTION)	OFF	CPU and SRAM are powered off, Always On (AON) memory is still powered. The sleep timer is running and configured to wake up the device. As the SRAM is off the application will be fully restarted on wakeup.
S4 (DEEP SLEEP)	OFF	CPU and SRAM are powered off, AON memory is still powered. When entering S4, the CPU is powered off by the AON. It means the firmware context is totally lost and the user code must be reloaded from the NVM. It comes with a big exit latency which makes this S4 usable only when the UWB subsystem is not used for long periods.
S0/S1	RESET	UWB system is held in reset, UWB clock is turned off.
S0/S1	UWB_RC (IDLE_RC)	UWB system is clocked at FOSC (~120 MHz).
S0/S1	UWB_IDLE (IDLE_PLL)	UWB system is clocked from the PLL at 124.8 MHz
S0/S1	UWB_LPTB	UWB system is clocked from the XTAL (38.4 MHz), PLL is off.
S0/S1	TX_WAIT	TX blocks are sequenced on as required. Includes DELAYED_TX mode.
S0/S1	TX	Active TX state. Automatically reverts to IDLE_PLL after transmission.
S0/S1	RX_WAIT	RX blocks are sequenced as required. Includes DELAYED RX mode.
S0/S1	RX	Active RX state. Can revert to IDLE_PLL if packet received or timeout triggers.
S0/S1	TRX	Both receiver and transmitter are enabled. Used in sensing use cases.
S5 (OFF)	OFF	All the device blocks are powered off, the digital core is off, CPU is off. The reset line is held low.

Note (*): WARNING: there shall be no signals on any GPIO (including the RTCI in this case) when VDD1/VDD5 is set to 0 V.

11.2 Operating State Transitions

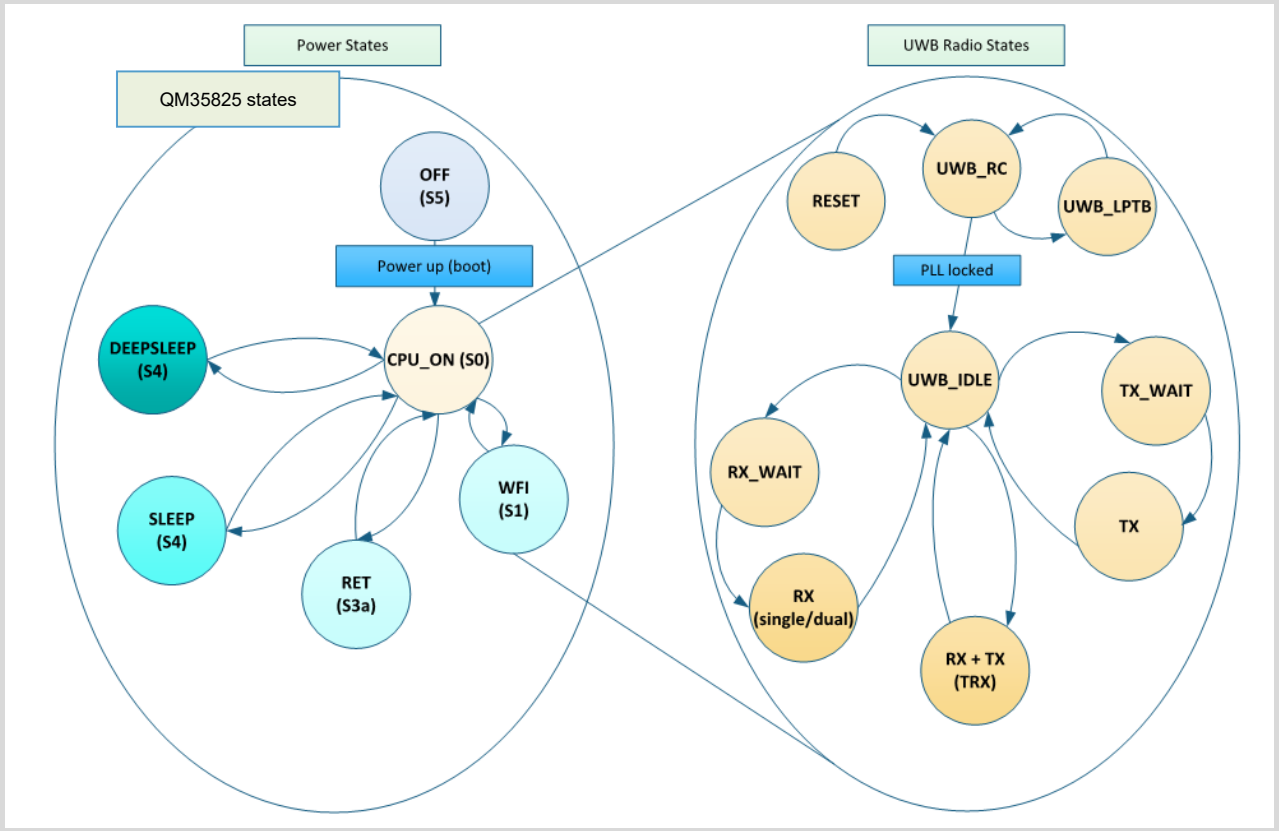


Figure 17: Operating State Transitions

12 Peripheral Description

12.1 UART Interface

Table 17: UART Configuration Summary

Parameter	Value / Comment
UART FIFO depth	16 bytes
Maximum Baud rate	115.2 kBd
Baud rate	Serial Clock Frequency / (16 * Divisor)
9-bit Mode Support	not supported
Asynchronous Clock	supported
RTC Flow Control Trigger	RX FIFO Threshold Trigger
FIFO Access Mode	supported
Fractional Baud rate Divisor Support	supported
Fractional Divisor Width	6
Additional DMA signal on I/F	supported
DMA signal	supported - active high

12.2 SPI Controller and Peripheral Interface

SPI peripheral timing parameters are stated in the tables and figure below.

Table 18: SPI Timing Specifications (High Speed / Peripheral)
Conditions: VDDIO @ 1.8 V +/-10%, typical drive strength, Tamb = 25 ˚C.

Parameter	Min.	Typ.	Max.	Units	Condition / Note
Frequency	-	-	35	MHz	dependent on load capacitance
SCLK High	14.28	-	-	ns	
SCLK Low	14.28	-	-	ns	
trSCLK	-	-	5	µs	
CSn	-	-	-	ns	Firmware dependent
CS Lead	7	-	-	ns	
CS Trail	0	-	-	ns	
MOSI Setup	0	-	-	ns	
MOSI Hold	2	-	-	ns	
CSn to MISO Driven, tACCESS	16.5	-	-	ns	
CSn to MISO disabled, tDISABLE	-	-	100	ns	
MISO Data Valid Time, tVD	-	-	14.28	ns	

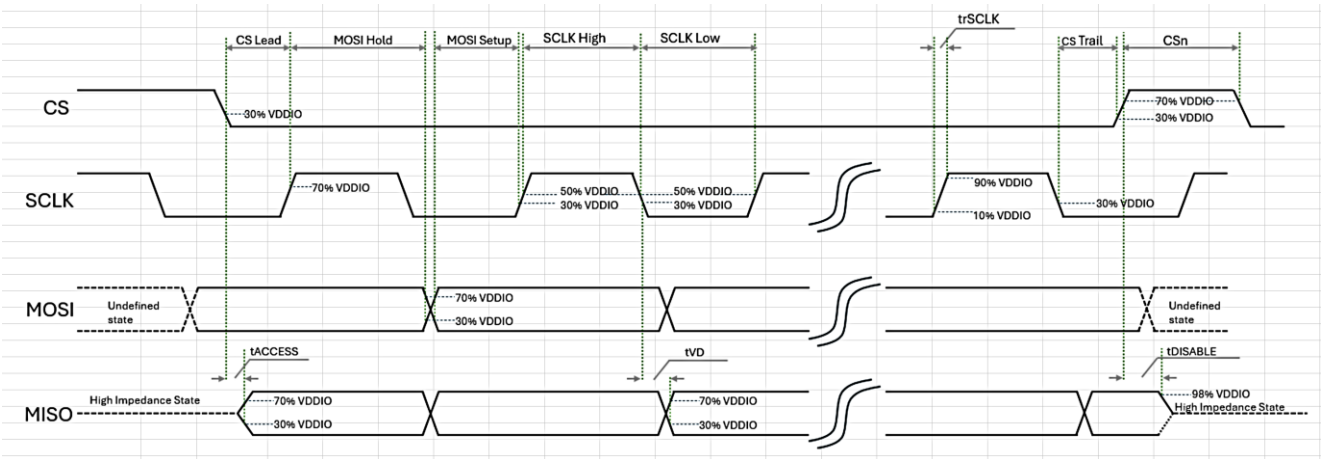


Figure 18: SPI Timing Diagram (mode 0)

Table 19: SPI Timing Specifications (Low Speed / Peripheral)
Conditions: VDDIO @ 1.2 V +/-5%, max. drive strength, Tamb = 25 ˚C.

Parameter	Min.	Typ.	Max.	Units	Condition / Note
Frequency	-	-	25	MHz	dependent on load capacitance
SCLK High	20	-	-	ns	
SCLK Low	20	-	-	ns	
trSCLK	-	-	5	µs	
CSn	-	-	-	ns	firmware dependent
CS Lead	7	-	-	ns	
CS Trail	0	-	-	ns	
MOSI Setup	0	-	-	ns	
MOSI Hold	3	-	-	ns	
CSn to MISO Driven, tACCESS	28	-	-	ns	
CSn to MISO disabled, tDISABLE	-	-	200	ns	
MISO Data Valid Time, tVD	-	-	20	ns	

12.2.1 Clock SPI Clock Sources

Table 20: SPI Clock Sources

Clock	Frequency			
	Min.	Typ.	Max.	Unit
SPI_CLK (Controller)		30		
SPI_CLK (Peripheral)	3		10	

12.2.2 SPI Operating Modes

SPI mode 0/0 (POL=0/PHA=0) is supported as defined in the Motorola SPI protocol.

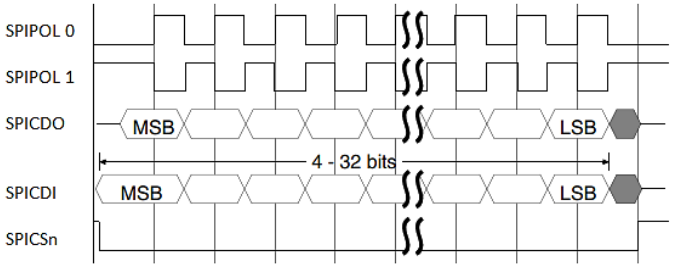


Figure 19: Timing Diagram for SPI Transfer with SPIPHA=0

12.3 I²C Interface

12.3.1 I²C Configuration Summary

Table 21: I²C Configuration Summary

Parameter	Comment
High Speed Mode	supported (I²C bus loading 100 pF)
10-bit addressing in both Master and Slave Mode	supported
Depth of both transmit and receive buffer	8 bytes
Asynchronous FIFO Mode	supported
Status bit	included

12.3.2 I²C Clock Frequencies

Table 22: I²C Clock Frequencies

Parameter	Min.	Typ.	Max.	Unit	Conditions
SCL clock frequency	0	-	100	kHz	Standard Mode
	0	-	400	kHz	Fast Mode
	0	-	1	MHz	Fast Mode Plus
	0	-	3.4	MHz	High Speed Mode

12.3.3 I²C Protocol

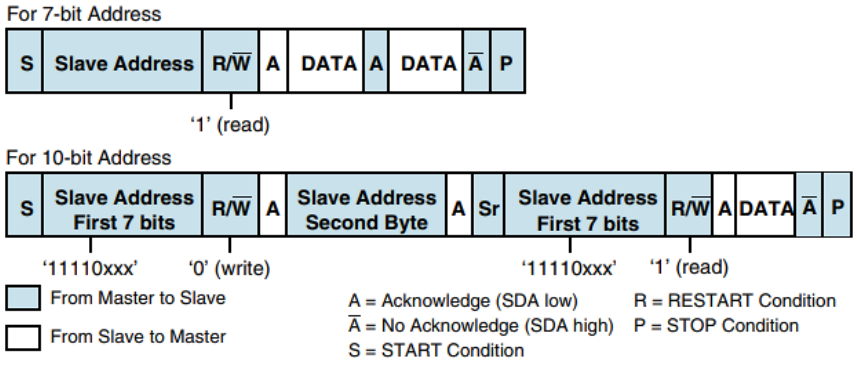


Figure 20: Master Receiver

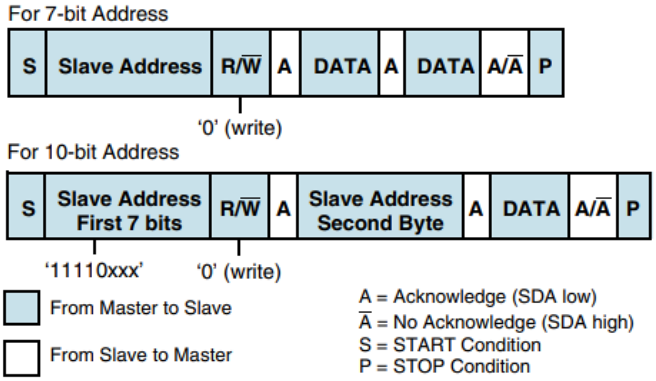


Figure 21: Master Transmitter

12 QM35825 Powering

QM35825 is designed such that it can be powered in several different configurations depending on the application. When the external power source is applied to the QM35825 for the first time, the internal Power On Reset (POR) circuit compares the externally applied supply voltage (VDD1) to an internal power-on threshold and once this threshold is passed, the AON block is released from reset and the external device enable pin EXTON is asserted.

After that, the VDD2a/b and VDD3 supplies are monitored and once they are above the required voltage, as specified in the datasheet, the fast RC oscillator (FAST_RC) and crystal (XTAL Oscillator) will come on within 500 µs and 1 ms, respectively. Once the digital reset is de-asserted, the digital core wakes up and enters the BOOT state and starts to execute the primary boot ROM image.

12.1 Powering Diagrams

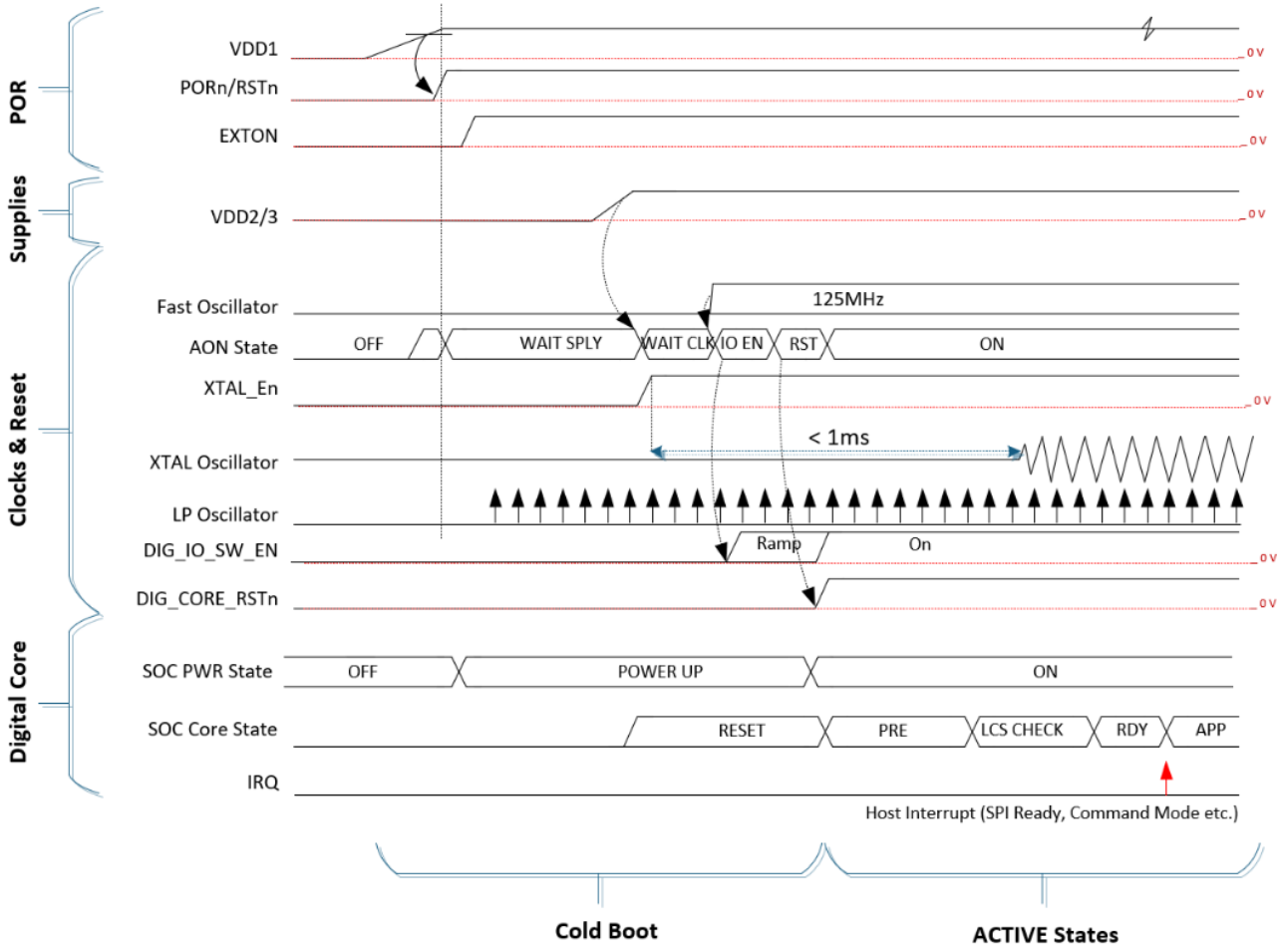


Figure 22: QM35825 Powering Diagram Cold Start

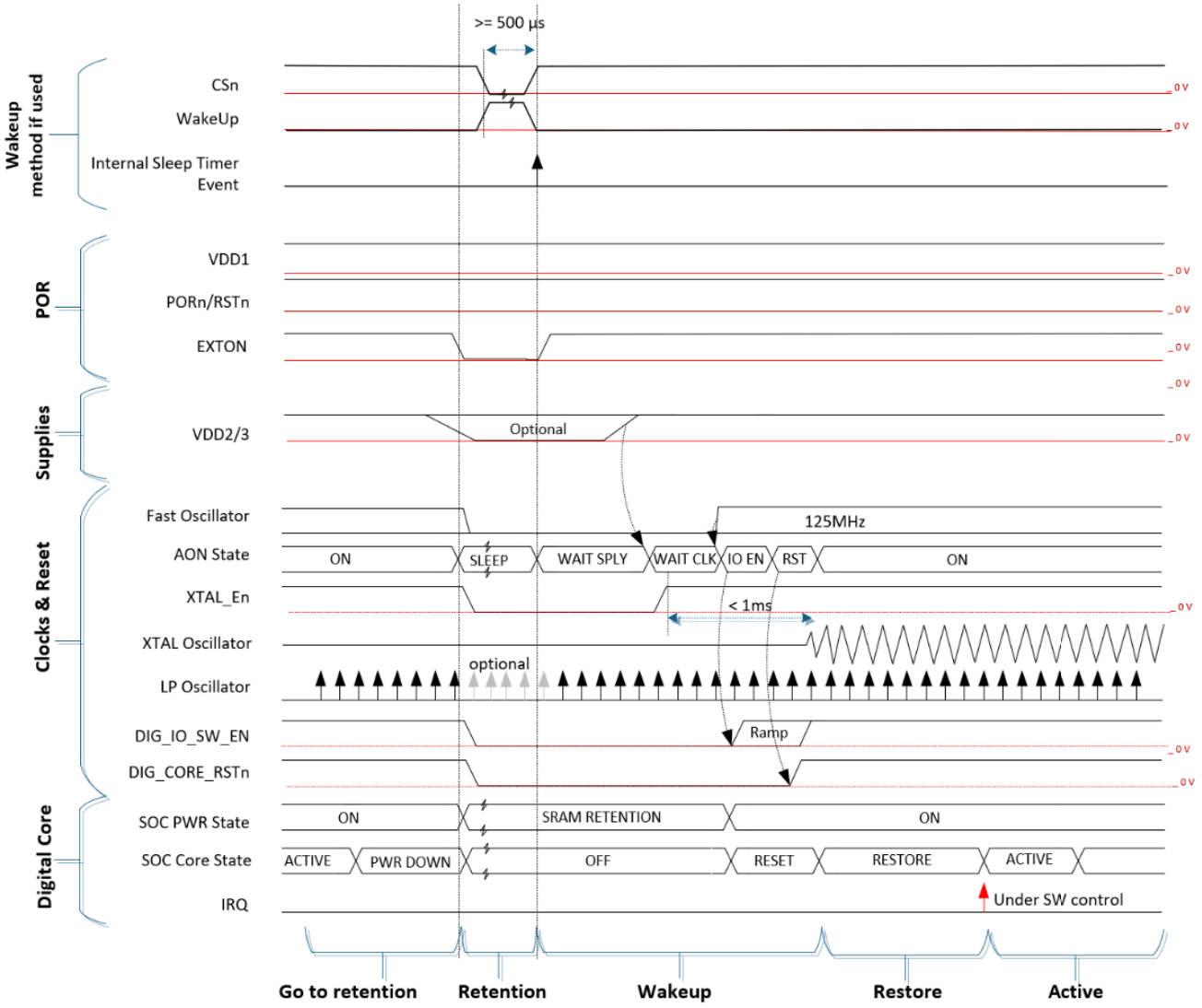


Figure 23: QM35825 Powering Diagram Warm Start

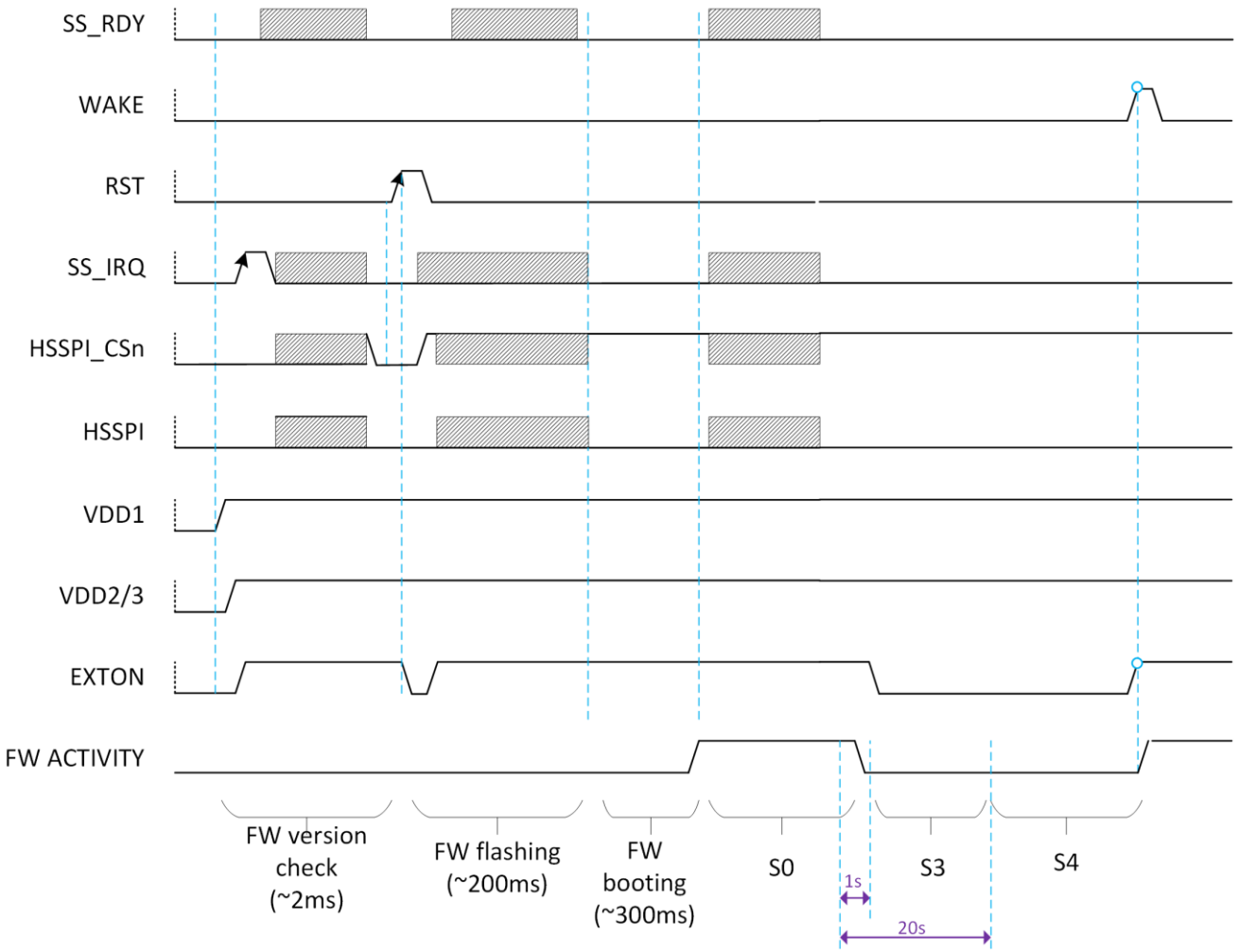


Figure 24: MCU Power State Timing Diagram after Device Boot

12.2 Internal Power Supply Distribution

The following block diagram shows the power distribution within the QM35825 SoC.

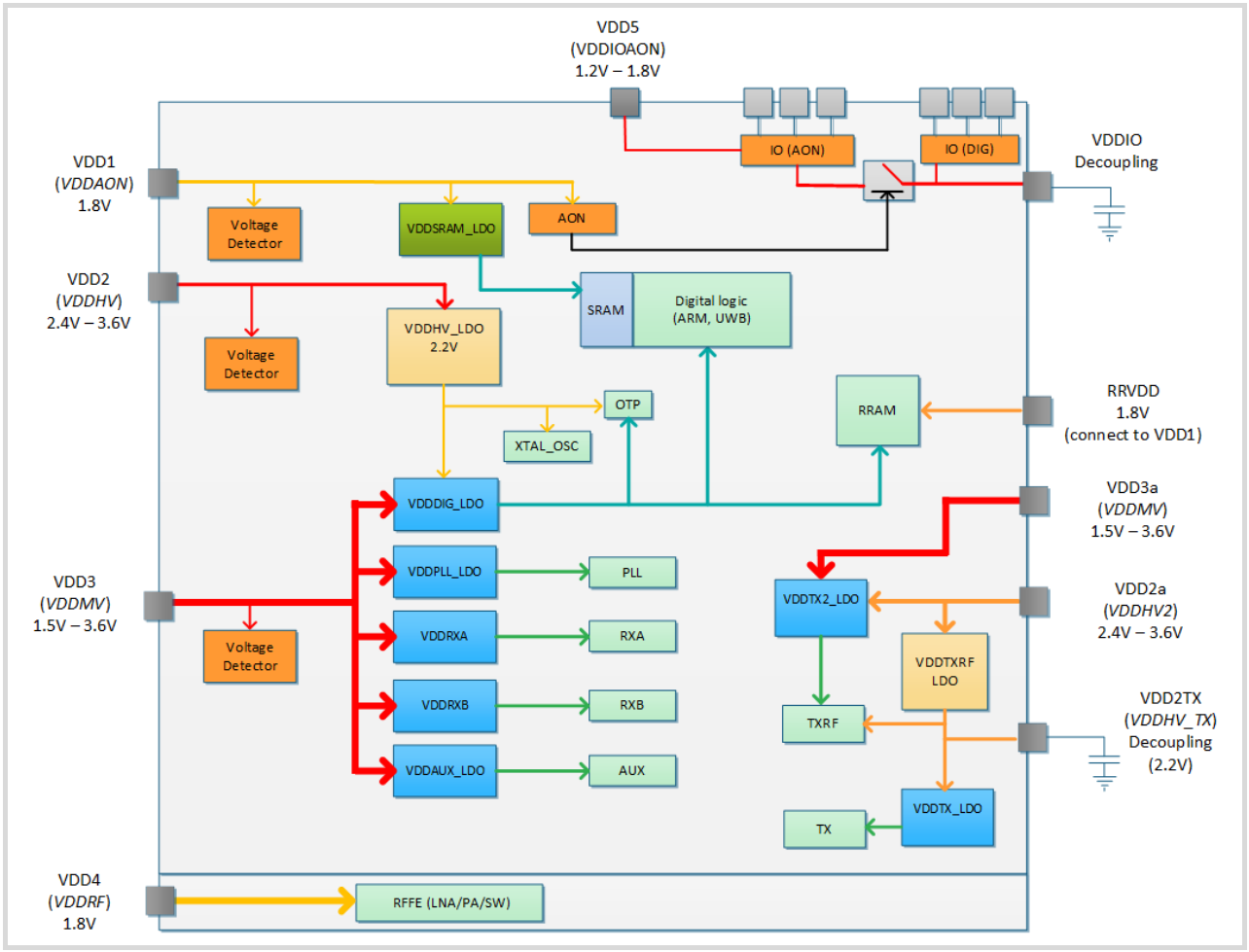


Figure 25: Internal Power Distribution

13 Application Information

13.1 Application Circuit Diagram – VDDIO = 1.2 V

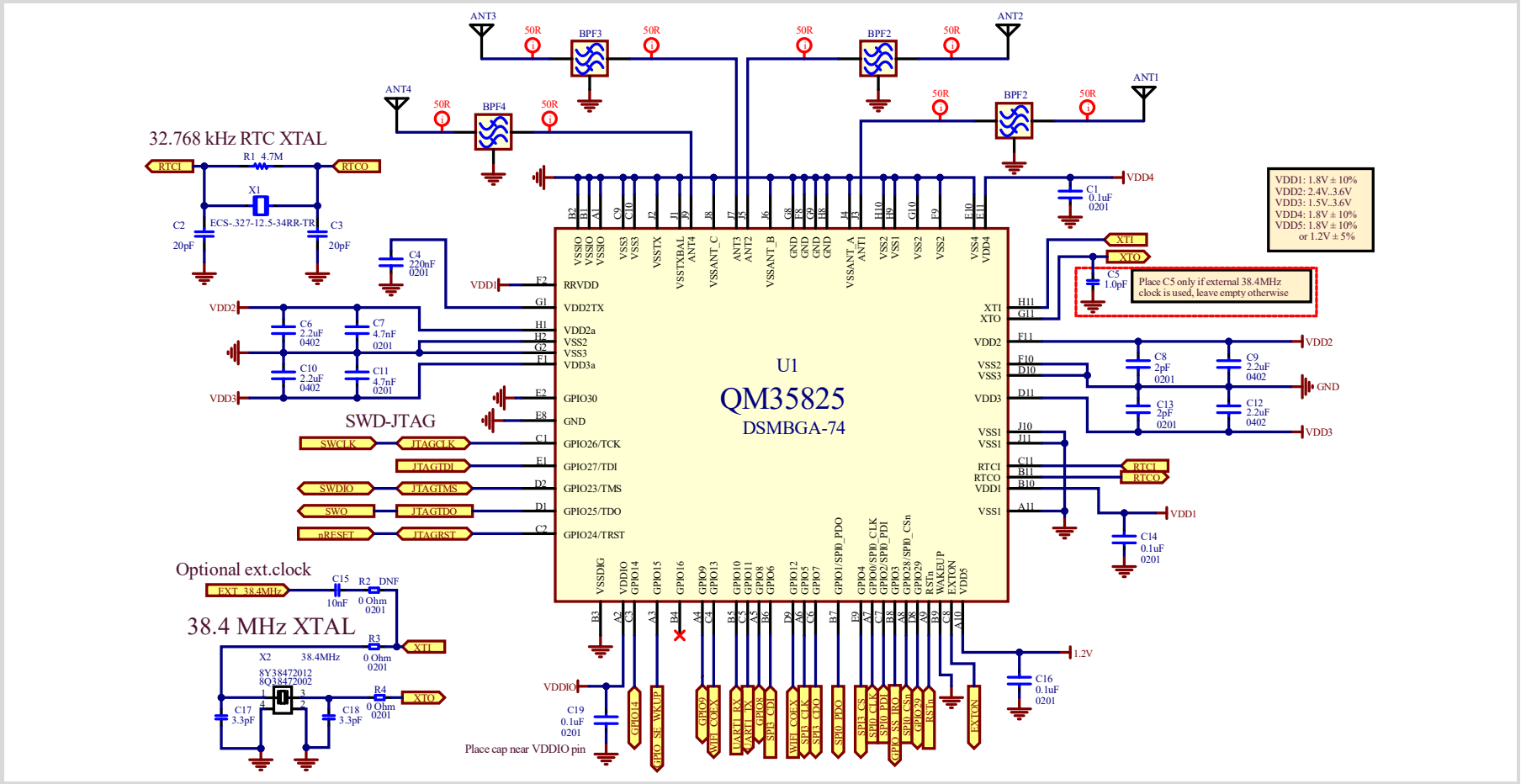


Figure 26: QM35825 Typical Application Circuit Diagram, VDDIO = 1.2 V

13.2 Application Circuit Diagram – VDDIO = 1.8 V

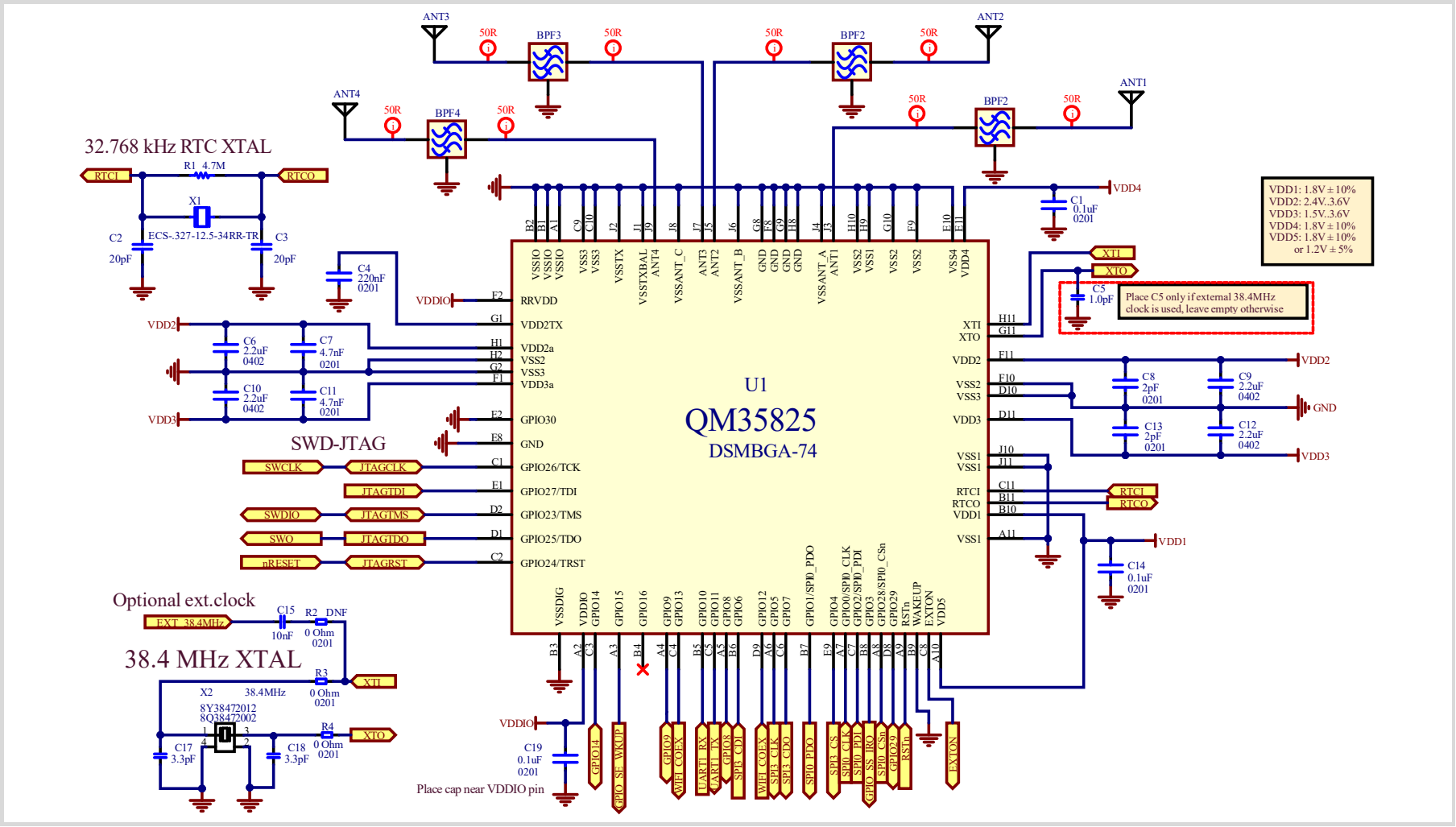


Figure 27: QM35825 Typical Application Circuit Diagram, VDDIO = 1.8 V

14 Packaging and Packing Information

14.1 Package Dimensions (74-Ball BGA)

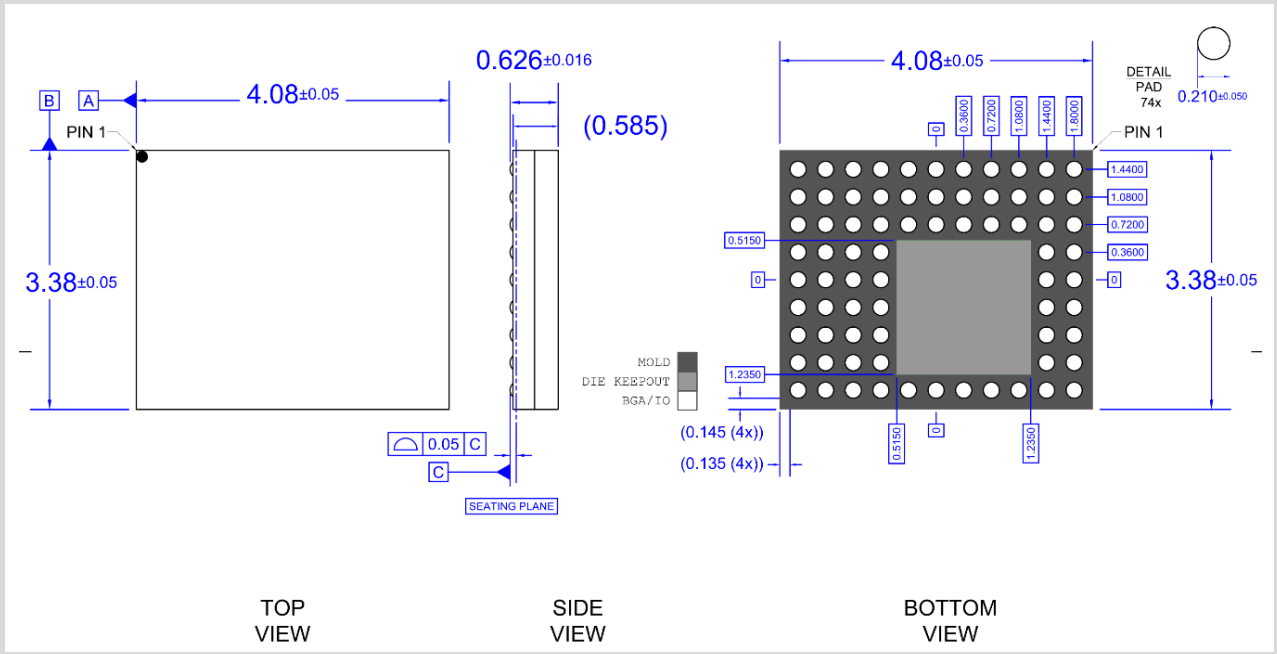


Figure 28: Package Dimensions [mm]

14.2 Recommended Land Pattern and Land Pattern Mask

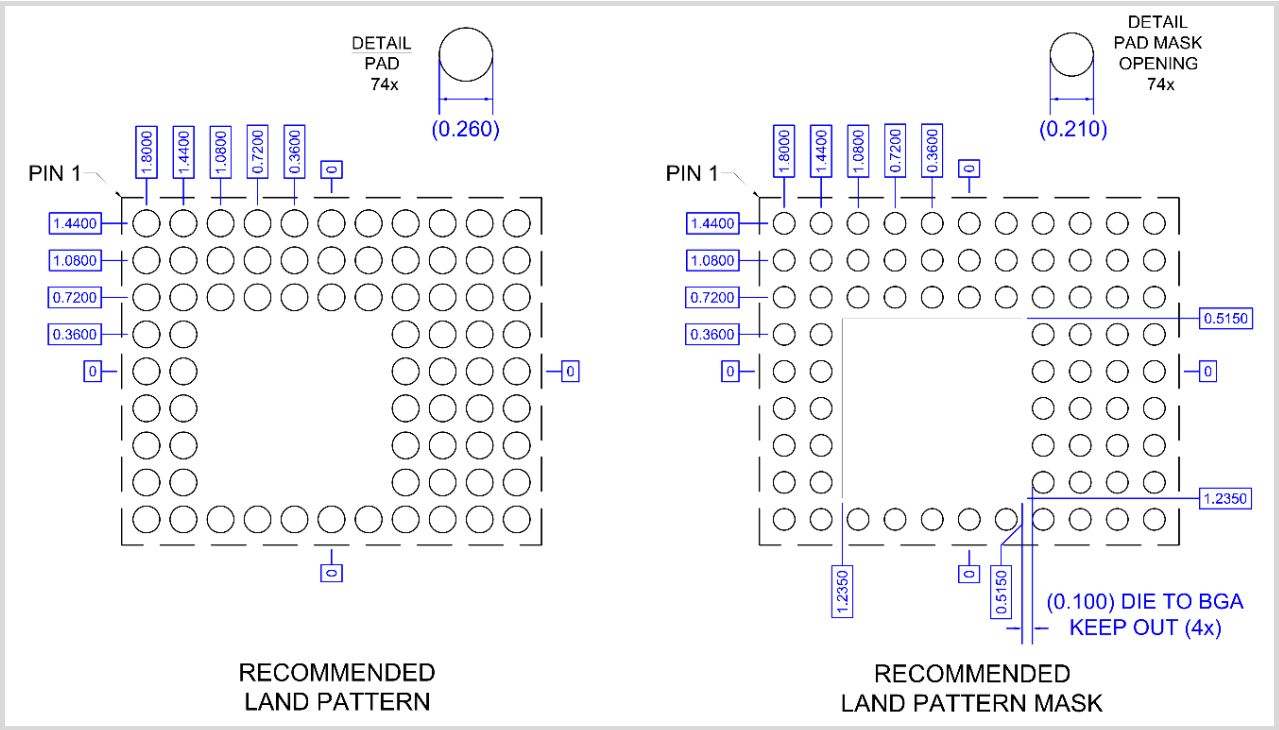


Figure 29: Recommended Land Pattern and Land Pattern Mask [in mm]

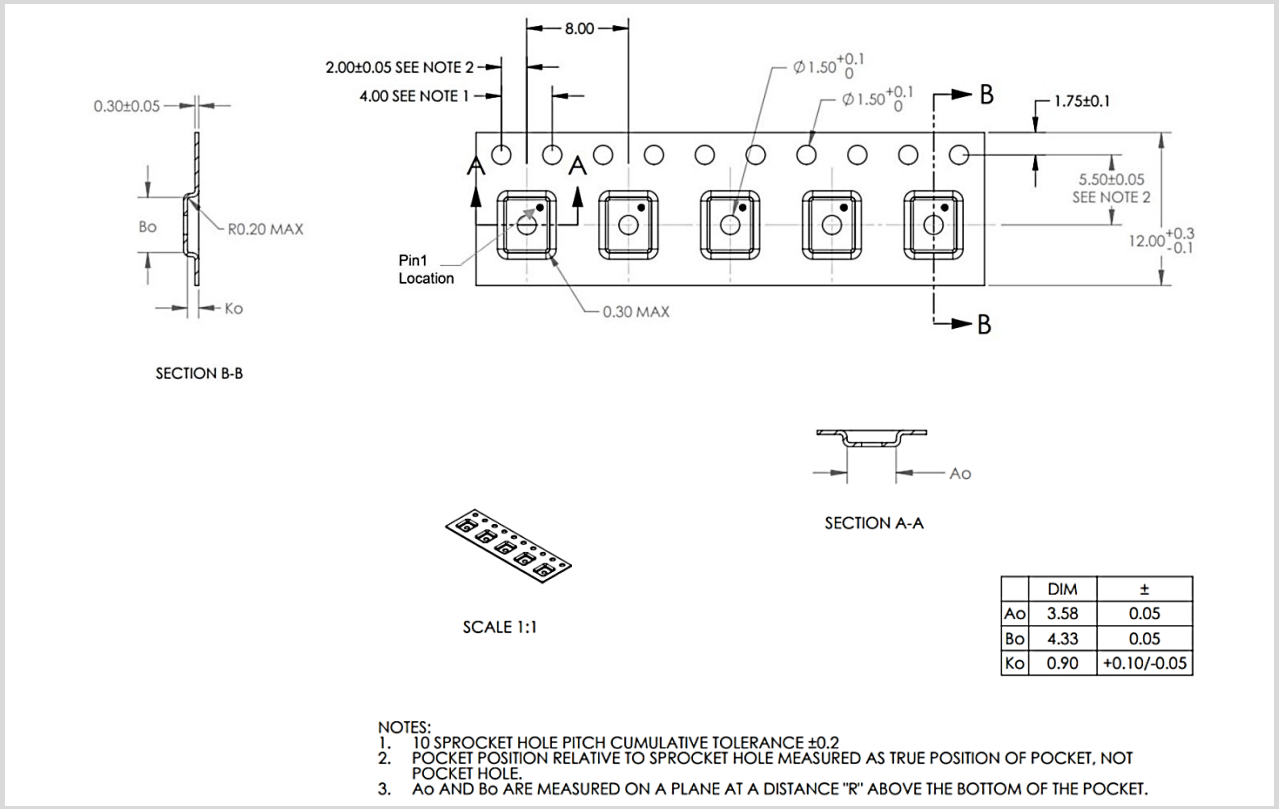
14.3 Device Package Marking

The image and table below shows the package markings for the QM35825.

Legend	
5825	Part number
Tr(ace) Code	XXXXXX

Figure 30: Device Package Marking

14.4 Tape & Reel Packaging Information



	DIM	±
Ao	3.58	0.05
Bo	4.33	0.05
Ko	0.90	+0.10/-0.05

Figure 31: Tape & Reel Orientation with Dimensions [mm]

Packaging reels are used to prevent damage to devices during shipping and storage, loaded carrier tape is typically wound onto a plastic take-up reel. The reels are made from high-impact injection-molded polystyrene (HIPS), which offers mechanical and ESD protection to packaged devices.

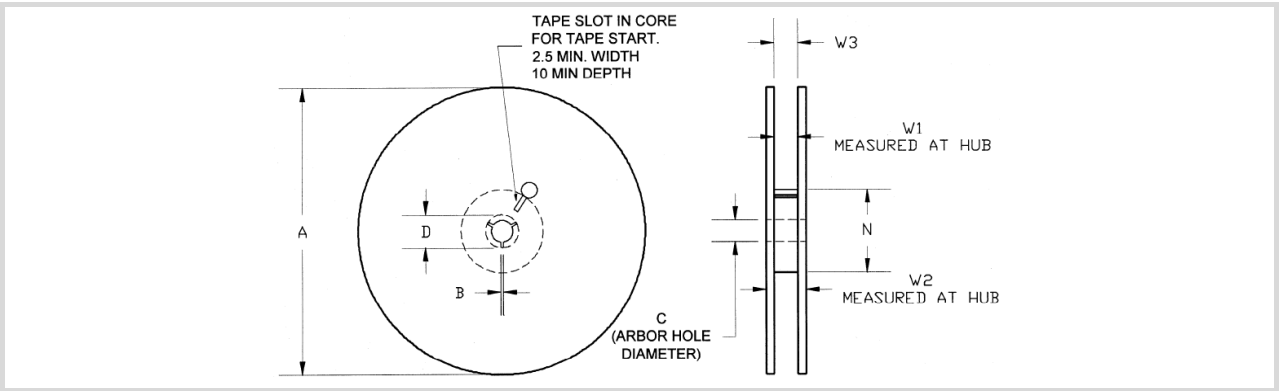


Figure 32: Reel Dimensions

Table 23: Reel Dimensions

Feature	Measure	Symbol	Size (mm)	Size (in)
Flange	Diameter	A	330	12.992
	Thickness	W2	18.4	.724
	Space Between Flange	W1	12.4	.488
Hub	Outer Diameter	N	102.0	4.016
	Arbor Hole Diameter	C	13.0	0.512
	Key Slit Width	B	2.0	0.079
	Key Slit Diameter	D	20.2	.795

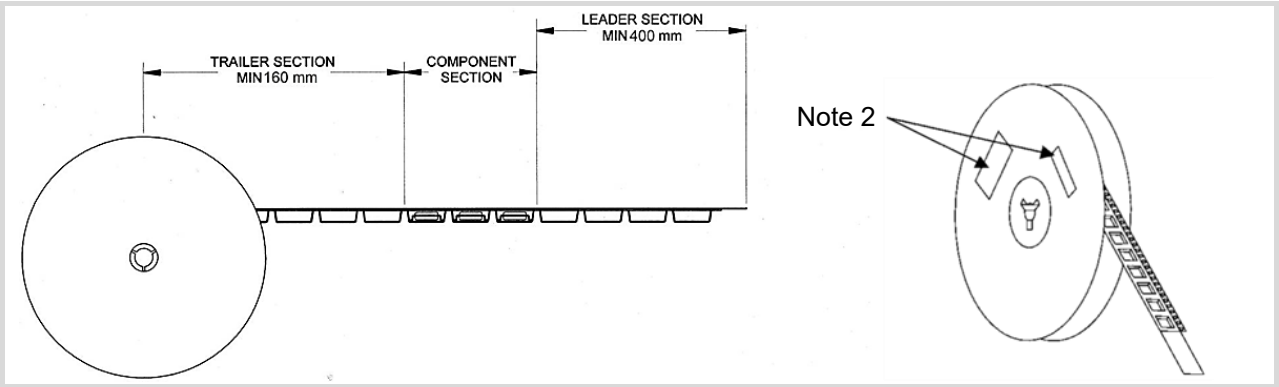


Figure 33: Tape Sections and Label Placement

Note 1: Empty part cavities at the trailing and leading ends are sealed with cover tape. See EIA 481.
Note 2: Labels are placed on the flange opposite the sprockets in the carrier tape.

Table 24: Other Data

Package Size	Units per Reel
3.38 x 4.08 mm	3000

14.5 Thermal Characteristics

Table 25: Thermal Characteristics

Symbol	Parameter	Conditions	Value	Unit
Theta JA ($R_{\theta JA}$)	Thermal resistance from junction to ambient		40	K/W

16 Recommended PCB Layout

16.1 PCB Technology

The following technology has been implemented in the QM35825 evaluation boards,

Table 26: PCB Stack-up Example

Parameter	Notes
Number of layers	6 layers
Substrate material	FR4
Minimum trace width	0.125 mm
Minimum line spacing	0.125 mm
QM35825 pad geometry	SMD (Solder Mask Defined - the solder mask opening is smaller than the metal pad). See dimensions in section 16.2 (Recommended Land Pattern).
Via	**L1 to L6:** drill hole diameter: 0.254 mm, pad diameter: 0.61 mm.
Micro via	**L1 to L2, L2 to L3** (see Figure 35Figure 35 below). Drill hole diameter: 0.1 mm, pad diameter: 0.2 mm, via in pad and via filling under the BGA.
Pad finish	ENIG (Electroless Ni Immersion Gold)

#	Name	Type	Material	Thickness	Dk	Weight
	Top Overlay	Overlay				
	Top Solder	Solder Mask	Solder Resist	0.02mm	3.7	
1	L1-Top	Signal		0.035mm		1oz
	ISO-1	Prepreg	S1000HB (3313)	0.094mm	4.48	
2	L2	Signal		0.035mm		1/2oz
	ISO-2	Prepreg	S1000HB (3313)	0.092mm	4.48	
3	L3-SignalNS	Signal		0.035mm		1/2oz
	ISO-3	Core	S1000H	1.03mm	4.74	
4	L4-Ground	Signal		0.035mm		1/2oz
	ISO-4	Prepreg	S1000HB (3313)	0.094mm	4.48	
5	L5-Power	Signal		0.035mm		1/2oz
	ISO-5	Prepreg	S1000HB (3313)	0.094mm	4.48	
6	L6-Bottom	Signal		0.035mm		1/2oz
	Bottom Solder	Solder Mask	Solder Resist	0.02mm	3.7	
	Bottom Overlay	Overlay				

Figure 34: QM35825 HDK Stack-up

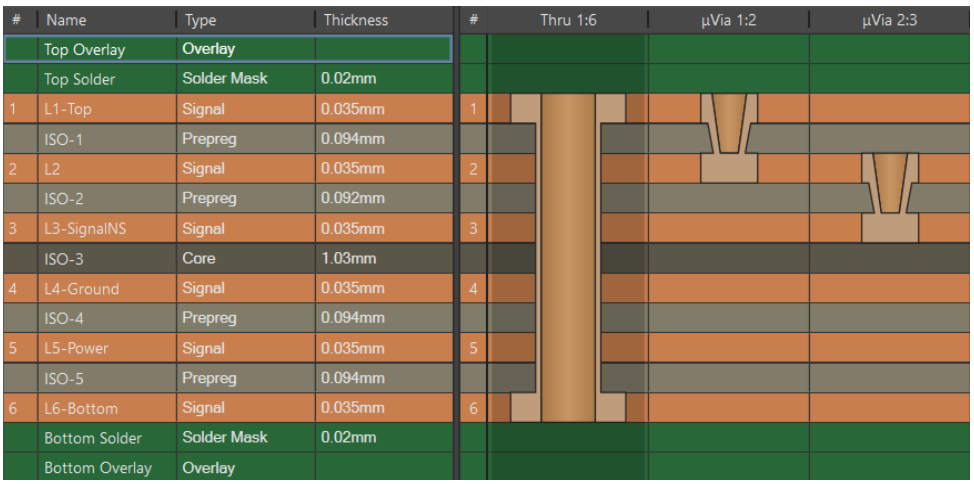


Figure 35: QM35825 HDK Via Structure

16.2 Recommended PCB Layout and Pad Geometry

In the areas shown below, copper, tracks and via's should be removed to a depth of 100 µm from the bottom of the chip once soldered. In most of the case, this means removing copper from the top layer in the area in question.

An opening should also be created in the solder mask as indicated in the image below.

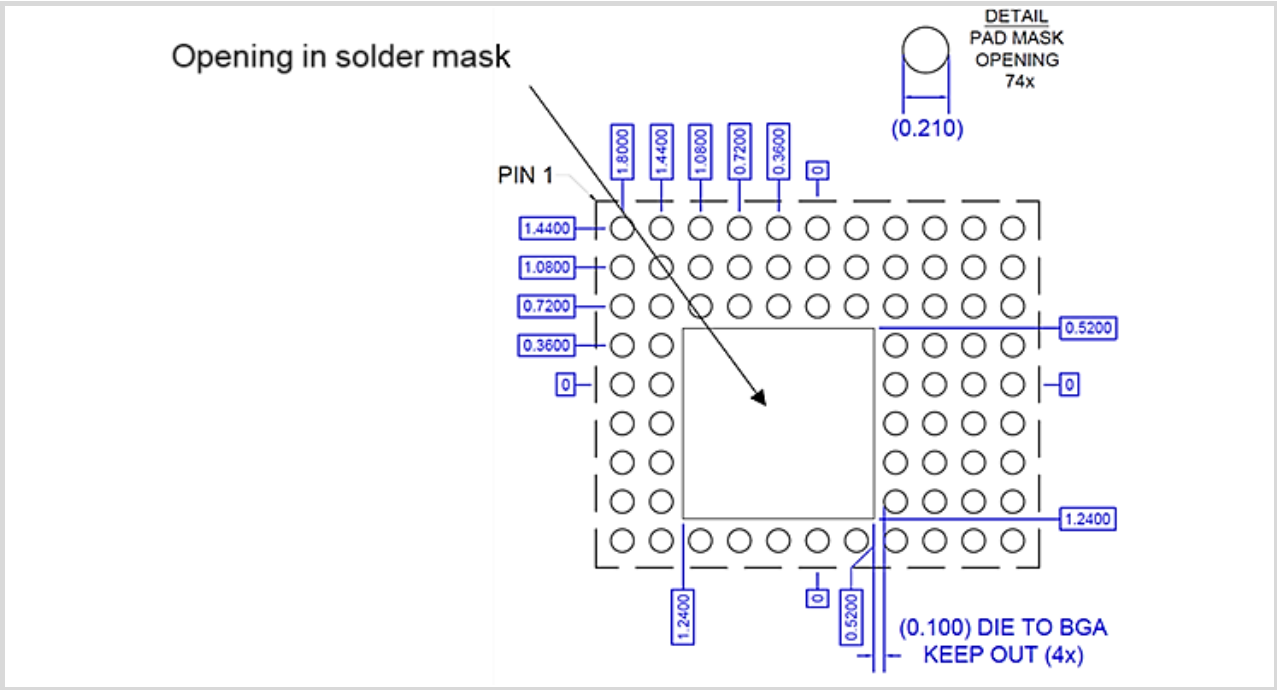


Figure 36: Recommended Land Pattern Mask

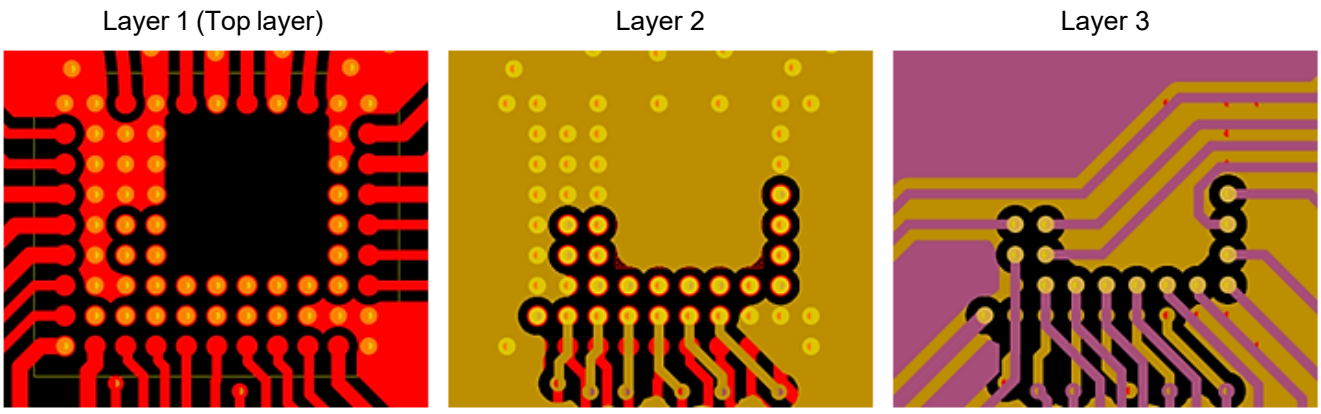


Figure 37: BGA Escape Routing Example

17 Glossary

Table 27: Glossary of Terms

Abbreviation	Meaning	Explanation
EIRP	Equivalent Isotropic Radiated Power	The amount of power that a theoretical isotropic antenna (which evenly distributes power in all directions) would emit to produce the peak power density observed in the direction of maximum gain of the antenna being used.
BPRF	Base PRF mode	64 MHz PRF Mode.
GPIO	General Purpose Input / Output	Pin of an IC that can be configured as an input or output under software control and has no specifically identified function.
IEEE	Institute of Electrical and Electronic Engineers	The world's largest technical professional society. It is designed to serve professionals involved in all aspects of the electrical, electronic and computing fields and related areas of science and technology.
LoS	Line of Sight	Physical radio channel configuration in which there is a direct line of sight between the transmitter and the receiver.
Open Drain	Open Drain	A technique allowing a signal to be driven by more than one device. Generally, each device is permitted to pull the signal to ground but when not doing so it must allow the signal to float. Devices should not drive the signal high so as to prevent contention with devices attempting to pull it low.
NLoS	Non-Line of Sight	Physical radio channel configuration in which there is no direct line of sight between the transmitter and the receiver.
PLL	Phase Locked Loop	Circuit designed to generate a signal at a particular frequency whose phase is related to an incoming "reference" signal.
PPM	Parts Per Million	Used to quantify very small relative proportions. Just as 1% is one out of a hundred, 1 ppm is one part in a million.
RTLS	Real Time Location System	System intended to provide information on the location of various items in real-time.
SFD	Start of Frame Delimiter	Defined in the context of the IEEE 802.15.4-2011 standard.
SPI	Serial Peripheral Interface	An industry standard method for interfacing between IC's using a synchronous serial scheme first introduced by Motorola.
TWR	Two Way Ranging	Method of measuring the physical distance between two radio units by exchanging messages between the units and noting the times of transmission and reception. More information available here: https://www.qorvo.com/innovation/ultra-wideband/technology
TDoA	Time Difference of Arrival	Method of deriving information on the location of a transmitter. The time of arrival of a transmission at two physically different locations whose clocks are synchronized is noted and the difference in the arrival times provides information on the location of the transmitter. A number of such TDoA measurements at different locations can be used to uniquely determine the position of the transmitter. More information available here: https://www.qorvo.com/innovation/ultra-wideband/technology
PDoA	Phase Difference of Arrival	Method of determining the direction of propagation of an RF wave incident on an antenna array using the phase difference between the signal received on each antenna array element.
LNA	Low Noise Amplifier	An amplifier designed to amplify very low-power signals without significantly degrading their signal-to-noise ratio.

18 References

[1] IEEE 802.15.4-2011. IEEE Standard for Local and metropolitan area networks – Part 15.4: Low-Rate Wireless Personal Area Networks (LR-WPANs). IEEE Computer Society Sponsored by the LAN/MAN Standards Committee. Available from https://standards.ieee.org/.

[2] IEEE 802.15.4-2015. IEEE Standard for Local and metropolitan area networks – Part 15.4: Low-Rate Wireless Personal Area Networks (LR-WPANs). IEEE Computer Society Sponsored by the LAN/MAN dStandards Committee. Available from https://standards.ieee.org/.

[3] IEEE 802.15.4-2020. IEEE Standard for Low-Rate Wireless Networks. IEEE Computer Society Sponsored by the LAN/MAN Standards Committee. Available from https://standards.ieee.org/.

[4] IEEE 802.15.4z-2020 (Amendment to IEEE 802.15.4-2020). Amendment 1: Enhanced Ultra-Wideband (UWB) Physical Layers (PHYs) and Associated Ranging Techniques". IEEE Computer Society Sponsored by the LAN/MAN Standards Committee. Available from https://standards.ieee.org/.

19 Approvals and Compliance

19.1 Radio Regulatory Requirements

The QM35822S is compliant with relevant FCC (USA/Canada), ETSI (EU) and ARIB (Japan) radio regulatory requirements (pending external testing).

19.2 Regulatory Approvals

All (**end**)**-products** developed by the manufacturer (or importer) incorporating the QM35825 must obtain approval/certification from the relevant authority governing radio emissions, including spectrum usage, in any given jurisdiction prior to the marketing or sale of such products in that jurisdiction.

19.3 Environmental Compliance

This part is compliant with 2011/65/EU RoHS directive (Restrictions on the Use of Certain Hazardous Substances in Electrical and Electronic Equipment) as amended by Directive 2015/863/EU.

Symbol	Attribute	Compliant
RoHS	Restrictions on the Use of Certain Hazardous Substances in Electrical and Electronic Equipment; Directives 2011/65/EU and 2015/863/EU.	✓
Pb	Lead Free	✓
	Halogen Free (Chlorine, Bromine)	✓
	Antimony Free	✓
	TBBP-A ($C_{15}H_{12}Br_4O_2$) Free	✓
	PFOS Free	✓
	SVHC Free	✓

20 Ordering Information

Part No.	Description
QM35825TR13	13” T&R with 3000 pcs
QM35825SR	7” sample reel, 100 pcs

21 Contact Information

For the latest specifications, additional product information, worldwide sales and distribution locations:

Web: www.qorvo.com **Tel:** 1-844-890-8163 **Support:** https://www.qorvo.com/support

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Data Sheet Information Status

	Data Information Status Label	Product Life Cycle Status	Definition
	TARGET DATA SHEET	Preview	Data sheet contains early design specifications for a product under development.
	PRELIMINARY DATA SHEET	Preview	Data sheet contains preliminary specifications for a product under development.
►	PRODUCTION DATA SHEET	Production	Data sheet contains production product specifications.

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Revision History

Revision	Date	Description
~~B1~~	~~Feb 29 2024~~	~~Released version (Advance Information).~~
~~B3~~	~~Jun 7 2024~~	~~SR version.~~
A	Jul 5 2024	SR version.
B1	Feb 20 2025	Block diagram updated.
		IEEE 802.15.4 names updated.
		T&R section updated. Figure 30: reel pin1 locations added.
		I^3C section removed.
	Mar 14 2025	Table 3: ESD test results updated.
		Section 12.1: UART Interface text updated.
		Chapter 1: Key Features text updated.
B1a	Mar 19 2025	Intermediate version
B	Apr 25 2025	Released Version.
		Section 5: Package dimensions added.
		Section 12.4: Timing Diagram for SPI Transfer with SPIPHA=1 removed.
		Section 15.1 and 15.2: format of drawings changed.
C	Aug 5 2025	FiRa 3.0 certified stated (chapter 1).
		Default levels (L/H) after Reset removed (Table 1).
		Max. Tx channel Power, Peak Power and PSD updated (Table 11).
		Supported bit rates updated (chapter 1 and section 10.3).
		Secure Asset location accuracy updated (page 1 and 5).
		Functional Block diagram updated (chapter 2).
		UWB positioning with radar sensing methods updated (chapter 4).
		RRAM text updated (chapter 5).
		Note added for STS packet configuration 3 (section 8.5).
		Transmit spectra updated (section 9.1).
		Transition State Diagram updated (section 11.2)
D	Sep 19 2025	Receiver blocking plots and data updated (section 8.4 and 9.2).