

# QPL9503 – 3.4-3.6GHz Reference Design

## Product Overview

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The QPL9503 is a flat-gain, high-linearity, ultra-low noise amplifier in a small 2 x 2 mm surface-mount package. The LNA provides a gain flatness of 2 dB (peak-to-peak) over a wide bandwidth from 3 to 6 GHz. At 5.5 GHz, the amplifier typically provides 21.6 dB gain, +35.5 dBm OIP3 at a 56mA bias setting, and 0.95 dB noise figure. The LNA can be biased from a single positive supply ranging from 3.3 to 5 volts. The device is housed in a green/RoHS-compliant industry-standard 2x2 mm package.

The QPL9503 is internally matched using a highperformance E-pHEMT process and only requires five external components for operation from a single positive supply: an external RF choke and blocking/bypass capacitors and a bias resistor going to pin 1. This LNA integrates a shut-down biasing capability to allow for operation in TDD applications.

The QPL9503 is optimized for linear performance across the 3 to 6 GHz frequency band but can operate down to 600 MHz.

## Referenced Documents

The reference documents below take precedence over the contents of this application note and should always be consulted for the latest information.

QPL9503 Data Sheet.

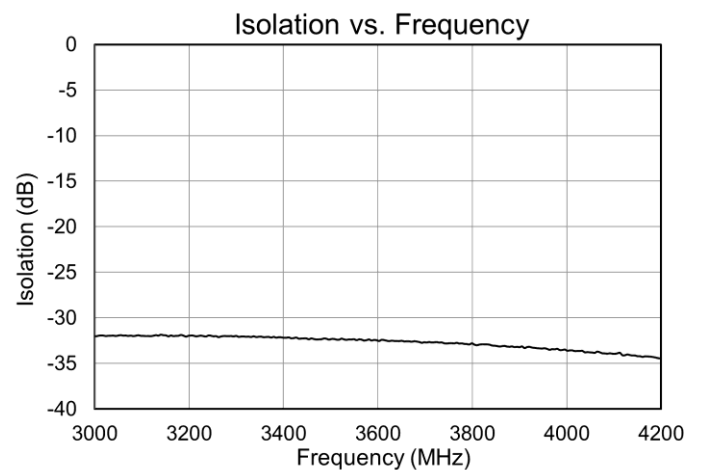
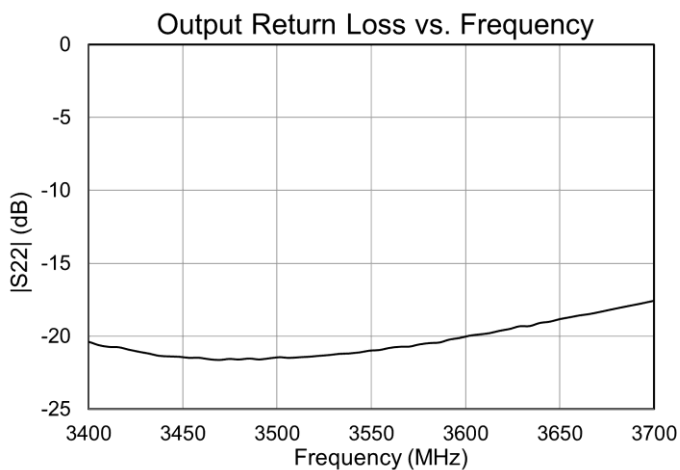
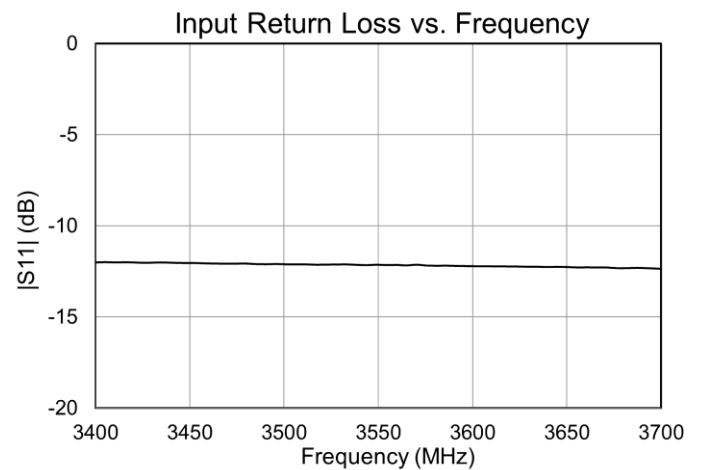
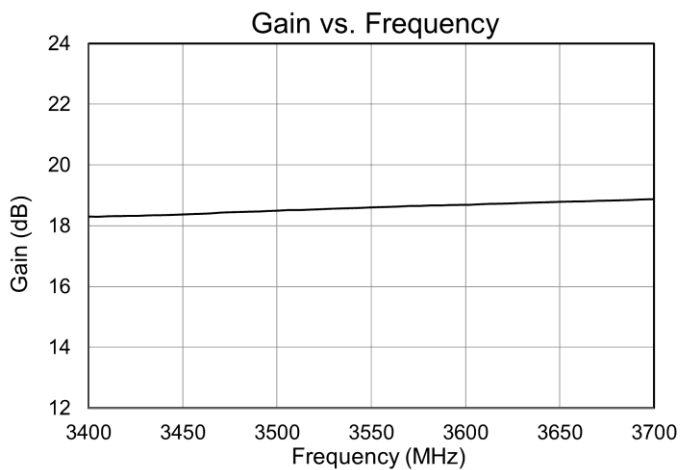
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## Application Electrical Performance

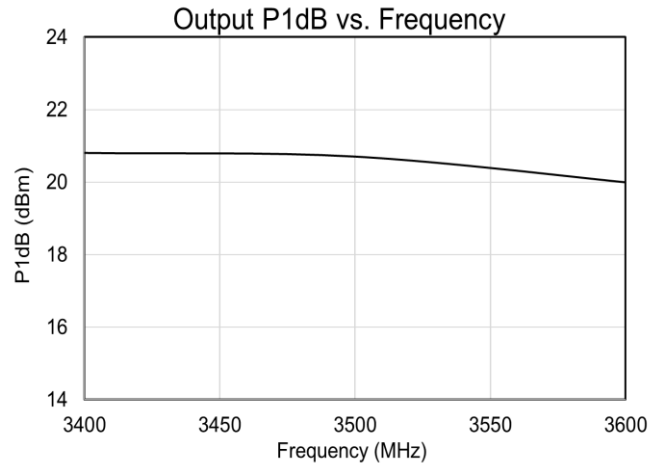
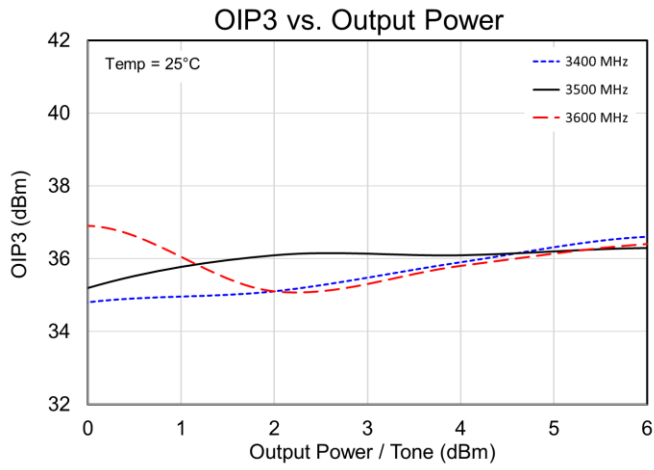
Qorvo Field and Factory Applications Engineers are available to provide technical assistance for determining appropriate matching networks for a particular application.

Parameter	Conditions	Typical Value			Units
		3400	3500	3600	
Frequency		3400	3500	3600	MHz
Gain		18.3	18.5	18.7	dB
Input Return Loss		12.0	12.0	12.1	dB
Output Return Loss		20.4	21.4	20.1	dB
Noise Figure	EVB Trace Loss De-embedded	0.90	0.98	0.95	dB
Output P1dB		20.8	20.7	20.0	dBm
OIP3	Pout = +5dBm/tone, $\Delta f = 1$ MHz	36.3	36.2	36.1	dBm
Device Current, I <sub>DD</sub>	On State	56			mA
	Off State	3			mA

Test conditions unless otherwise noted: V<sub>DD</sub> = +5V, Temp = +25 °C, 50 Ω system.



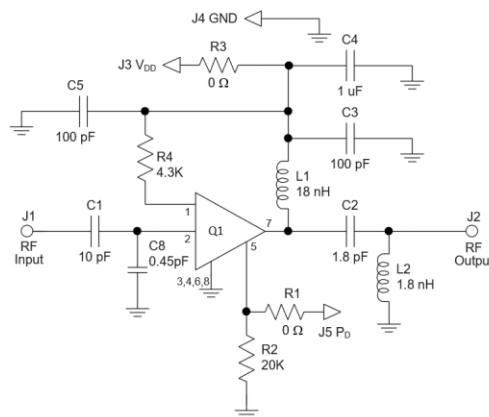
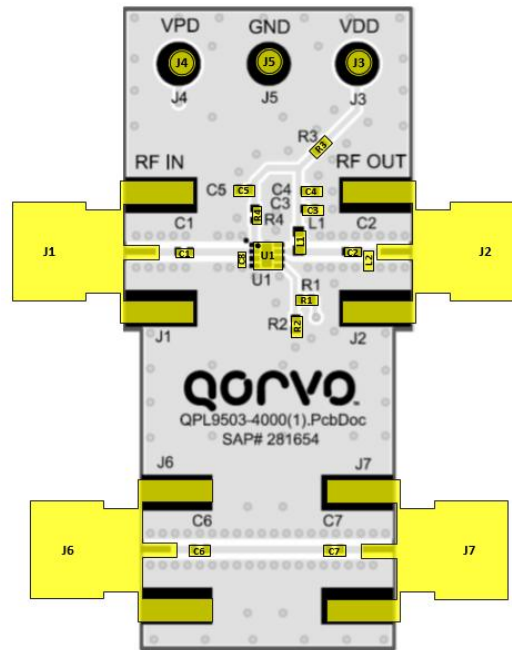
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## Evaluation Board Information

### Evaluation Board and Schematic



#### Notes:

1. See Evaluation Board PCB Information section for material and stack-up.
2. All components are of 0402 size unless stated on the schematic.
3. For TDD Applications: R2 = 20K & R1 = 0Ω
4. For FDD Applications: R2 = 20K 'OR' Pin 5 tied to ground. R1 = DNP/Omitted
5. A through line is included on the evaluation board to de-embed the board losses.
6. R4 sets the current draw. Can be changed for the desired bias point. Critical component placement locations:
7. Distance between U1 (right edge) and C8 (left edge):20 mils

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## Evaluation Board – Bill of Material

Reference Des.	Value	Description	Manuf.	Part Number
n/a	n/a	Printed Circuit Board		
U1	n/a	Ultra Low Noise, Flat Gain LNA	Qorvo	QPL9503
R4	4.3K	Resistor, Chip, 0402, 5%, 1/16W	various	
R2	20K	Resistor, chip, 0402, 5%, 1/16W	various	
R1, R3	0 $\Omega$	Resistor, Chip, 0402, 5%, 1/16W	various	
L1	18 nH	Inductor, 0402, 5%, coil	Coilcraft	0402CS-18NXJL
C1	10 pF	CAP, 0402, +/-1%, 50V	Murata	GJM1555C1H100FB01D
C2	2.2 pF	CAP, 0402, +/-0.1pF, 25V	AVX	04023J series
C8	0.4 pF	CAP, 0402, +/-0.05pF, 50V	AVX	04023J series
L2	2.2 nH	Inductor, 0402	AVX	04023J series
C4	1.0 uF	Cap., Chip, 0402, 10%, 10V, X5R	various	
C3, C5, C6, C7	100 pF	Cap., Chip, 0402, 5%, 50V, NPO/COG	various	

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## Additional Information

For information on ESD, Soldering Profiles, Packaging Standards, Handling and Assembly, please contact Qorvo for general guidelines.

## Contact Information

For the latest specifications, additional product information, worldwide sales and distribution locations:

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