QPC5330

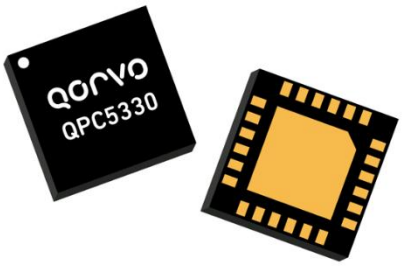
0.02 – 15 GHz SOI 6-Bit Digital Attenuator

Product Overview

Qorvo's QPC5330 is an ultra-wide band SOI 6-bit digital step attenuator (DSA). It operates from 0.02 to 15 GHz and provides a 31.5 dB attenuation range with an LSB of 0.5 dB. It also achieves a low step error of less than 0.1 dB typically.

The QPC5330 also offers multiple control options including parallel, SPI, or I2C as well as the ability to control multiple DSAs simultaneously using either addressing or daisy chaining.

The QPC5330 is housed in a 3.5 x 3.5 mm laminate-based package. This, along with the minimal DC power consumption, allows for easy system integration.



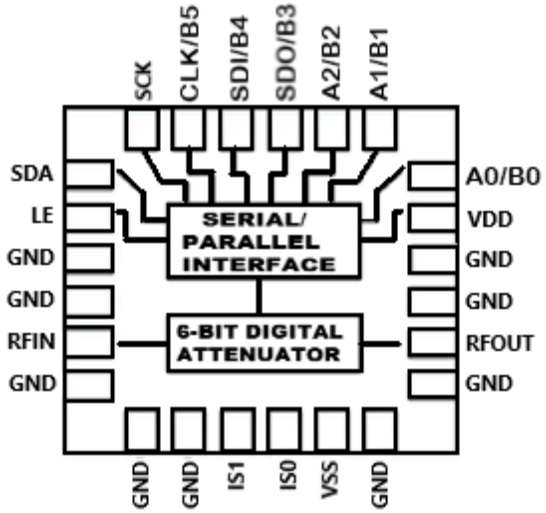
3.5 x 3.5 mm OVM Package

Key Features

- Frequency Range: 0.02 – 15 GHz
- 6-Bit Digital Attenuator
- DSA Attenuation Range: 31.5 dB
- Attenuation Step Size (LSB): 0.5 dB
- Insertion Loss (Ref. State): 3.0 dB Typical @15 GHz
- Step Error: 0.1 dB Typical
- RF Settling Time: 250 ns Typical
- Switching Time: 140 ns Typical
- Control Voltage: 1.8 V Logic, 5.5 V Max
- Package Size: 3.5 x 3.5 x 0.912 mm
-

Performance is typical across frequency. Please reference the electrical specification table and data plots for more details.

Functional Block Diagram



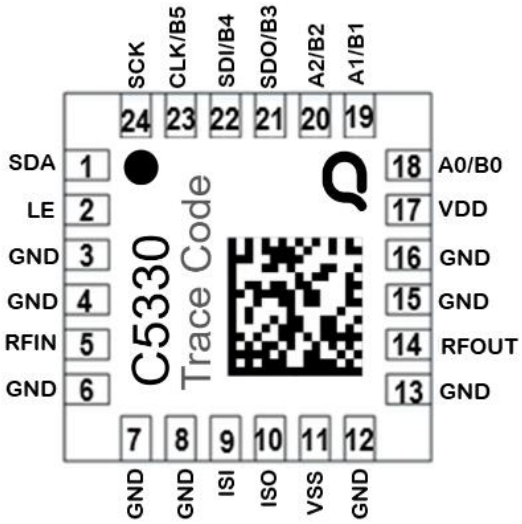
Applications

- Commercial and Military Radar
- Satellite Communications
- Electronic Warfare
- General Purpose

Ordering Information

Part No.	Description
QPC5330TR7	QPC5330 0.02 - 15 GHz SOI 6-Bit Digital Attn. 500 Piece 7" Reel
QPC5330SR	100 Piece 7" Reel
QPC5330EVB01	QPC5330 EVAL BOARD

Pin Configuration



Top view of package base

Pin Description

Pin No.	Label	Description
1	SDA	I2C data pin, should be tied down if I2C mode is not used.
2	LE	Latch Enable
3,4,6-8,12,13,15,16	GND	Ground. On PCB, multiple vias should be employed under 25 (center pad) to minimize inductance and thermal resistance.
5	RFIN (*)	RF Attenuator input, no DC block required if voltage is not present (DC coupled); Interchangeable with RFOUT.
9	IS1	Mode set pin 2
10	IS0	Mode set pin 1
11	V_{SS}	Negative supply pin / Ground for internal Negative Voltage generation (NVG)
14	RFOUT (*)	RF Attenuator Output, no DC block required if voltage is not present (DC coupled); Interchangeable with RFIN.
17	V_{DD}	Positive Supply Pin
18	A0/B0	SPI address bit or parallel bit
19	A1/B1	SPI address bit or parallel bit
20	A2/B2	SPI address bit or parallel bit
21	SDO/B3	SPI serial output or parallel bit
22	SDI/B4	SPI serial input or parallel bit
23	CLK/B5	SPI clock input or parallel bit
24	SCK	I2C clock pin, should be tied down if I2C mode is not used.

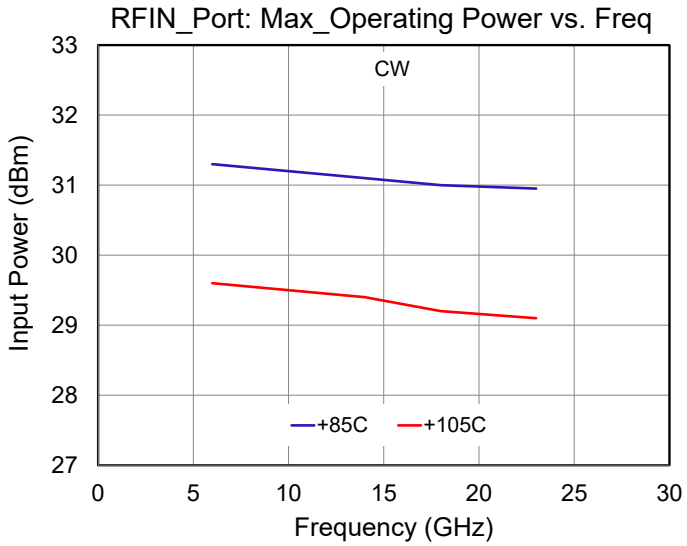
Notes:
(*) RFOUT port can be used as RF input port with slightly degraded input power handling as indicated from max operating power graphs on page 3.

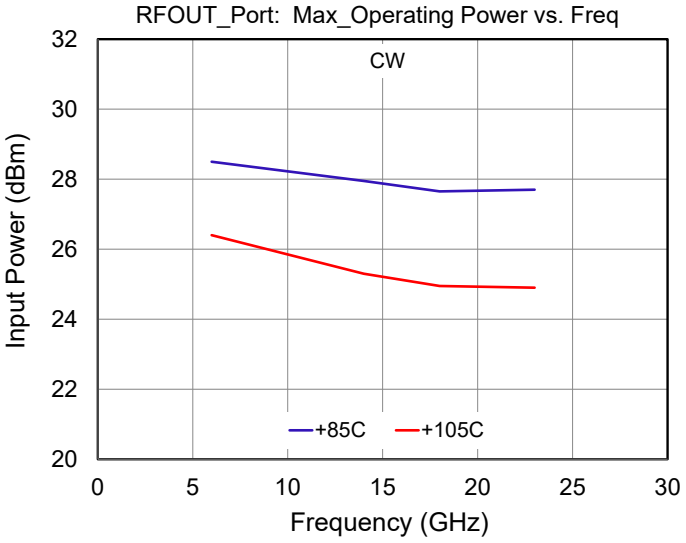
Absolute Maximum Ratings

Parameter	Value
Supply Voltage (V_{DD})	-0.3V to +6V
Negative Supply Voltage (V_{SS})	-6V to +0.3V
RFIN Port Steady State Average, 50 Ω, 105°C	34 dBm
RFIN Port Steady State Peak (1), 50 Ω, 105°C	36 dBm
RFIN Port, Hot Switching Average, 50 Ω, 105°C	34 dBm
RFOUT Port Steady State Average, 50 Ω, 105°C	31 dBm
RFOUT Port Steady State Peak (1), 50 Ω, 105°C	36 dBm
RFOUT Port, Hot Switching Average, 50 Ω, 105°C	31 dBm
Input Power Port Unbiased, 50 Ω, 25°C	21 dBm
Output Power Port Unbiased, 50 Ω, 25°C	21 dBm
Max Junction Temperature	150 °C
Mounting Temperature (30 Seconds)	260 °C
Storage Temperature	-65 to 150 °C

Operation of this device outside the parameter ranges given above may cause permanent damage. These are stress ratings only, and functional operation of the device at these conditions is not implied.

(1) Peak power refers to the peaks present in a modulated signal with a specified peak to average ratio.





Normal Operating Conditions

Parameter [1]	Min	Typ.	Max	Units
Power Supply Voltage (V_{DD})	3.15	-	5.5	V
Power Supply Current (I_{DD})	-	150	-	µA
Negative Power Supply (V_{SS}) [2]	-5.5	-	-3.15	V
Negative Power Supply Current (I_{SS})	-	-25	-	µA
DSA Control Logic Low (“0”)	-0.3	0	+0.63	V
DSA Control Logic High (“1”)	1.17	-	V_{DD}	V
DSA Control Current	-20	-	+20	µA
Serial Output Logic (Low)	-	0 ± 0.3	-	V
Serial Output Logic (High)	-	V_{DD} ± 0.3	-	V
Serial Output Current	-	-	0.5	mA
Steady State Average Power [3] (Input Power @ RFIN), 105°C	-	-	29	dBm
Steady State Peak Power [4] (Input Power @ RFIN), 105°C	-	-	34	
Hot Switching Average Power (Input Power @ RFIN), 105°C	-	-	29	
Hot Switching Peak Power (Input Power @ RFIN), 105°C	-	-	34	
Steady State Average Power [3] (Input Power @ RFOUT), 105°C	-	-	25	dBm
Steady State Peak Power [4] (Input Power @ RFOUT), 105°C	-	-	34	
Hot Switching Average Power (Input Power @ RFOUT), 105°C	-	-	25	
Hot Switching Peak Power (Input Power @ RFOUT), 105°C	-	-	34	
Operating Temperature Range	−40	-	+105	°C
Junction Temperature for > 10^6 Hours MTTF	-	-	125	°C

1 Electrical specifications are measured at specified test conditions. Specifications are not guaranteed over all recommended operating conditions.
2. Apply V_{SS} to deactivate internal negative voltage generator (NVG). To reactivate NVG, connect V_{SS} to ground and then cycle V_{DD}.
3. See Average Power graphs for temperature and frequency dependance on page 3.
4. Peak power refers to the peaks present in a modulated signal with a specified peak to average ratio. Note that the average power should not exceed the value from max operating power graphs on page 3.

Electrical Specifications

Test conditions unless otherwise noted: 50 Ω, 25 °C, V_{SS} = 0 V or -3.3 V, V_{DD} = +3.3 V.

Parameter		Test conditions	Min	Typ.	Max	Units
Operational Frequency Range			0.02	-	15	GHz
Insertion Loss (Ref-State)		Frequency: 1 GHz	-	1.8	2.2	dB
		Frequency: 10 GHz	-	2.4	2.8	
		Frequency: 15 GHz	-	3.0	3.4	
Input Return Loss (All States)		Frequency = 5 GHz	-	17	-	dB
		Frequency = 10 GHz	-	18	-	
		Frequency = 15 GHz	-	18	-	
Output Return Loss (All States)		Frequency = 5 GHz	-	17	-	dB
		Frequency = 10 GHz	-	16	-	
		Frequency = 15 GHz	-	15	-	
Attenuation	Range	Between minimum and maximum attenuation states	-	31.5	-	dB
	Step Size	Between any successive attenuation states	-	0.5	-	dB
	Accuracy (Reference to Insertion Loss)	Frequency: 10 MHz to 10 GHz	±(0.1 + 0.4% of state)			dB
		Frequency: 10 to 15 GHz	±(0.15 + 0.5% of state)			
Step Error Loss		Frequency: 0.1 to 10 GHz	-	±0.1	-	dB
		Frequency: 10 to 15 GHz	-	±0.1	-	

Electrical Specifications (Cont.)

Test conditions unless otherwise noted: 50 Ω, 25 °C, V_{SS} = 0 V or -3.3 V, V_{DD} = +3.3 V.

Parameter	Test Conditions	Min	Typ.	Max	Units
Operational Frequency Range		0.02	-	15	GHz
Relative Phase (Max Attenuation)	Frequency = 10 GHz	-	11	-	deg
	Frequency = 15 GHz	-	21	-	
Worst Case Overshoot	Decrease in loss during switching	-	2.5	-	dB
Input Power ($P0.1_{dB}$)	Ref State	-	40	-	dBm
	All Other States	-	36	-	
Input IP3	P_{IN} = 14dBm per tone, 1MHz tone spacing	-	57	-	dBm
Switch Time	50% control to 10/90% RF	-	140	-	ns
Settling Time (RF Settling 0.1 dB)	50% control to 0.1dB to final RF output	-	250	-	
Settling Time (RF Settling 0.05 dB)	50% control to 0.05dB to final RF output	-	300	-	
Thermal Resistance (θ_{JC}) (1), T_{BASE} = 105 °C		-	23	-	C °/W

Notes:
1. Measured to the back of the package.

Optional External V_{SS}

For proper operation, V_{SS} supply pin must be grounded or tied to the V_{SS} voltage specified in the Normal Operating Conditions table. When the V_{SS} pin is grounded, an internal negative voltage generator (NVG) is implemented. The spur levels generated by internal NVG are very low due to spread-spectrum architecture. For applications that require the lowest possible spur performance, V_{SS} can be applied externally to bypass the internal negative voltage generator. Applying V_{SS} disables internal NVG. To reactivate NVG, V_{SS} must be removed and then V_{DD} cycled.

Switching Frequency

The QPC5330 has a switching frequency of 100kHz. Switching frequency is defined to be the speed at which the DSA can be toggled across attenuation states.

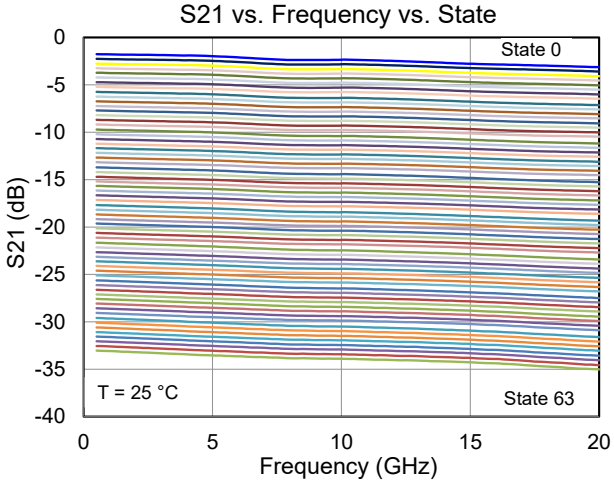
Glitch-safe Operation

The QPC5330 provides safe transition behavior when changing attenuation states. When RF input power is applied, positive output power spikes are minimized during attenuation state changes by design.

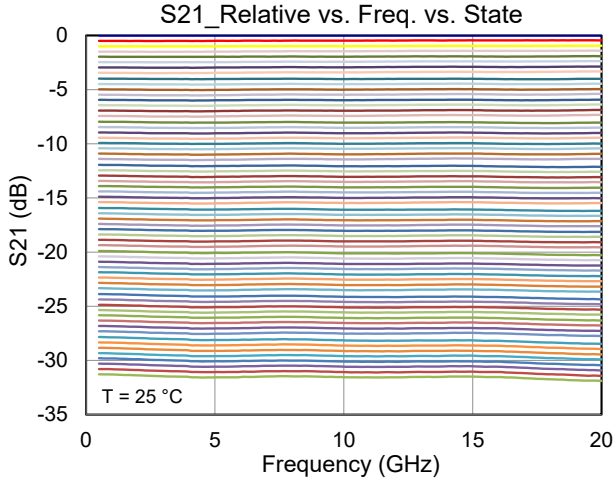
Performance Plots – Small Signal

Test conditions unless otherwise noted: 50 Ω, 25 °C, V_{SS} = 0 V or -3.3 V, V_{DD} = +3.3 V. RF reference plans at package leads.

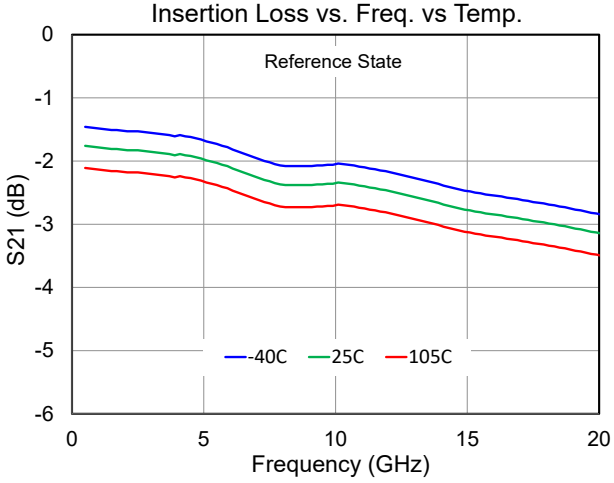
S21 vs. Frequency vs. State



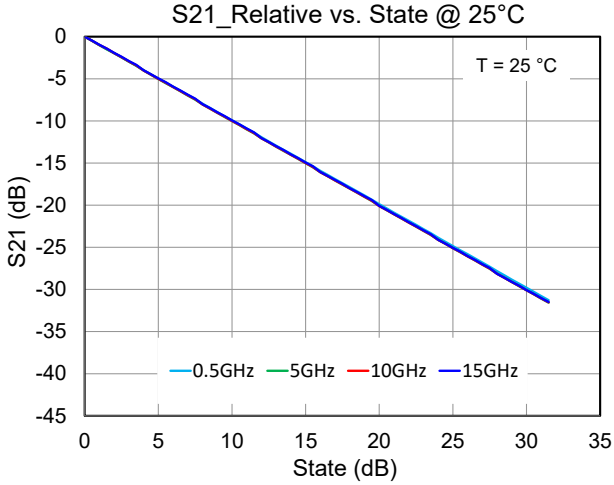
S21_Relative vs. Freq. vs. State



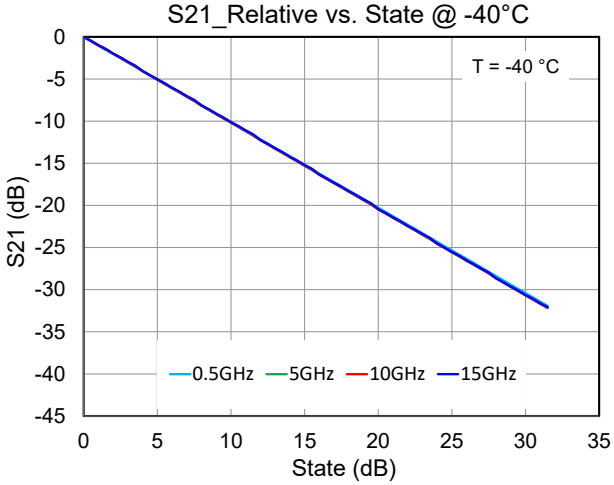
Insertion Loss vs. Freq. vs Temp.



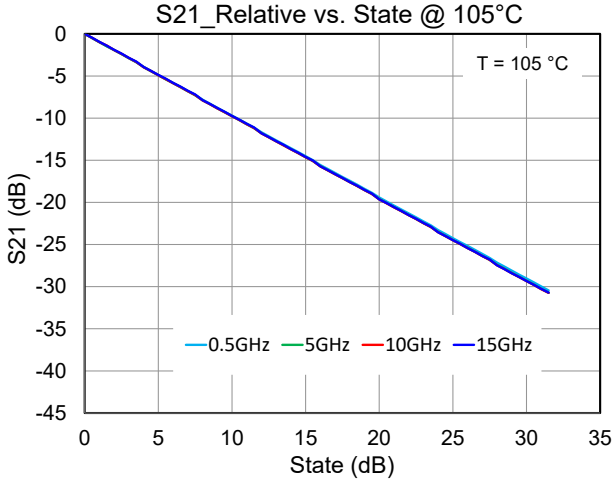
S21_Relative vs. State @ 25°C



S21_Relative vs. State @ -40°C



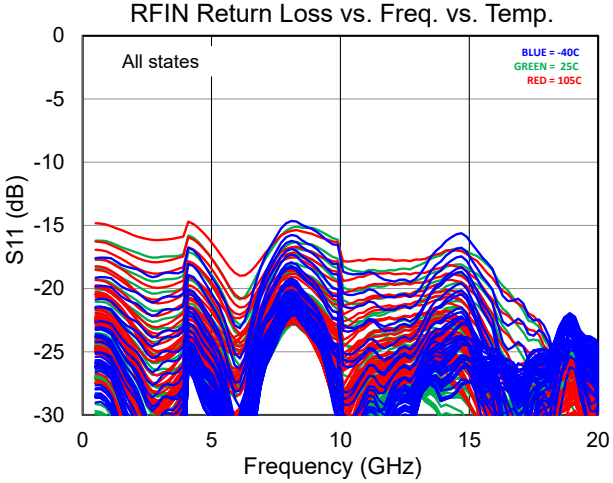
S21_Relative vs. State @ 105°C



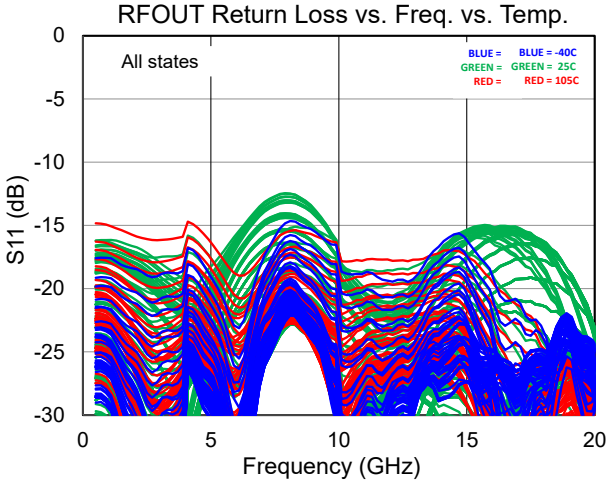
Performance Plots – Small Signal

Test conditions unless otherwise noted: 50 Ω, 25 °C, V_{SS} = 0 V or -3.3 V, V_{DD} = +3.3 V. RF reference plans at package leads.

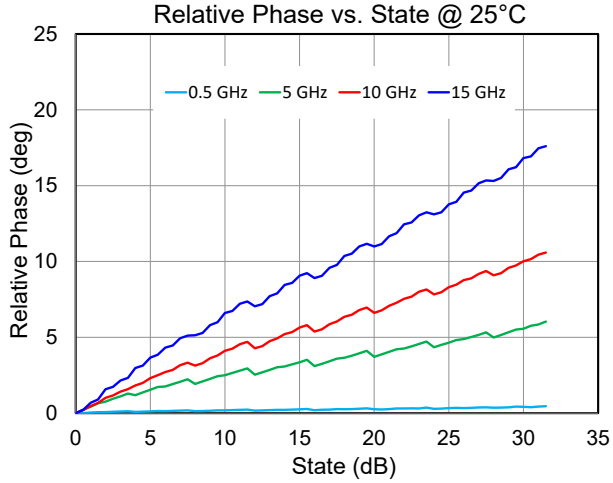
RFIN Return Loss vs. Freq. vs. Temp.



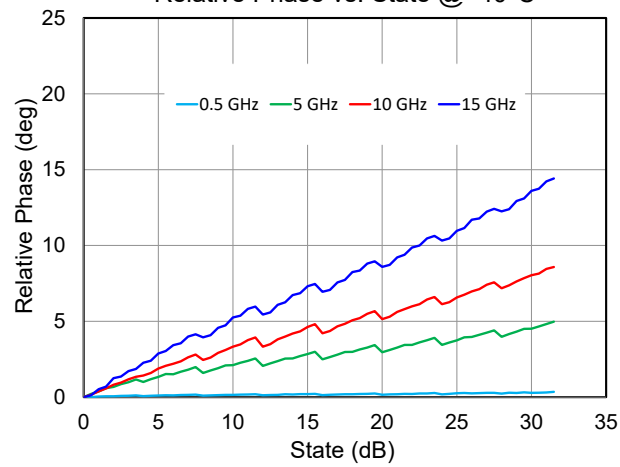
RFOUT Return Loss vs. Freq. vs. Temp.



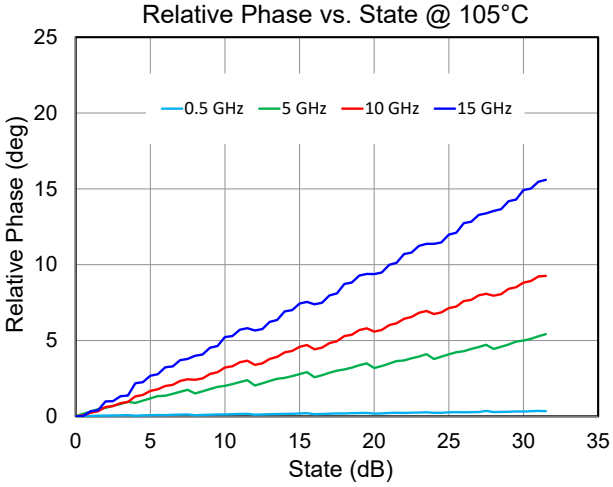
Relative Phase vs. State @ 25°C



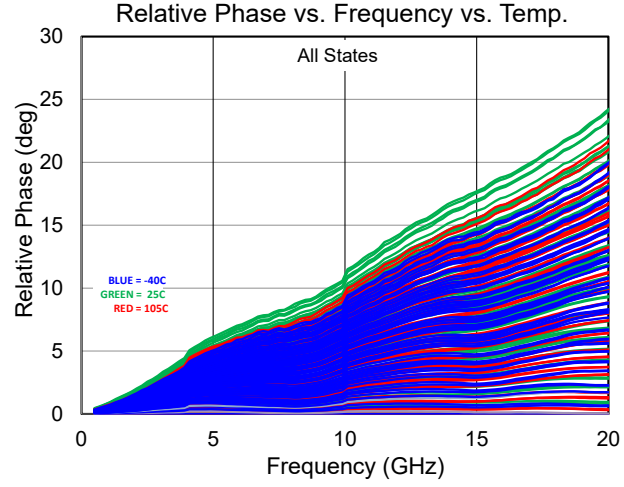
Relative Phase vs. State @ -40°C



Relative Phase vs. State @ 105°C



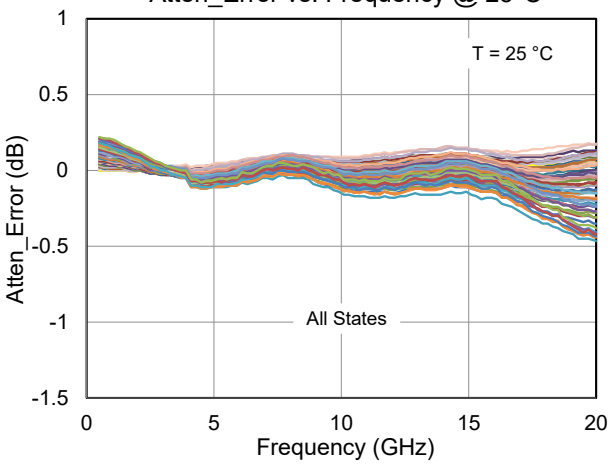
Relative Phase vs. Frequency vs. Temp.



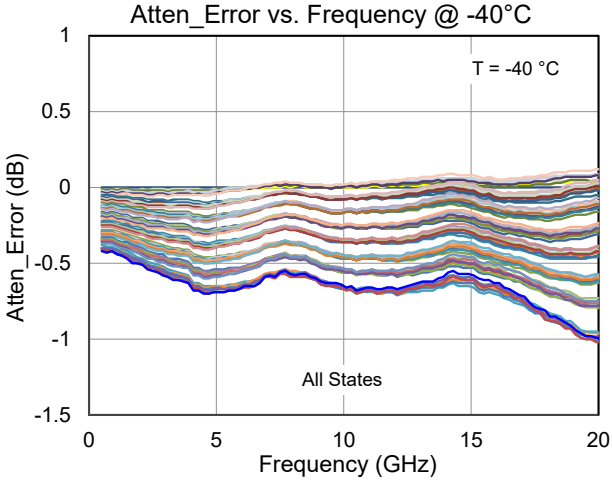
Performance Plots – Small Signal

Test conditions unless otherwise noted: 50 Ω, 25 °C, V_{SS} = 0 V or -3.3 V, V_{DD} = +3.3 V. RF reference plans at package leads.

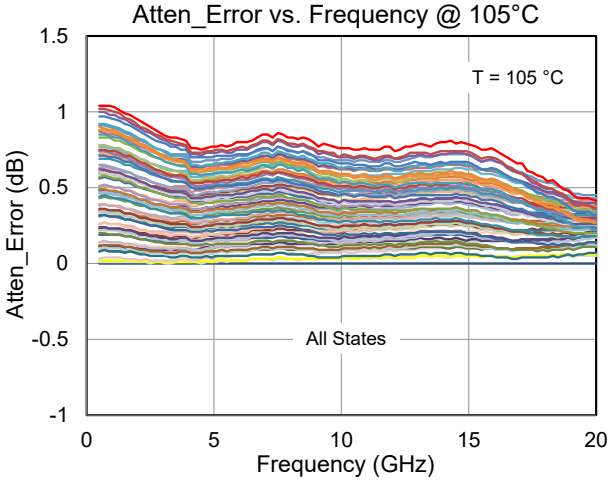
Atten_Error vs. Frequency @ 25°C



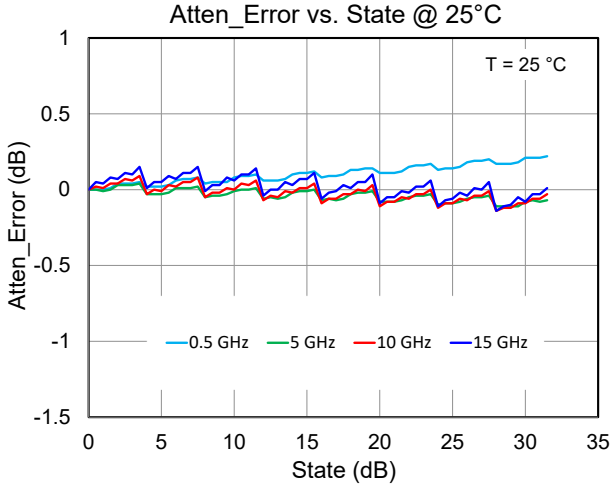
Atten_Error vs. Frequency @ -40°C



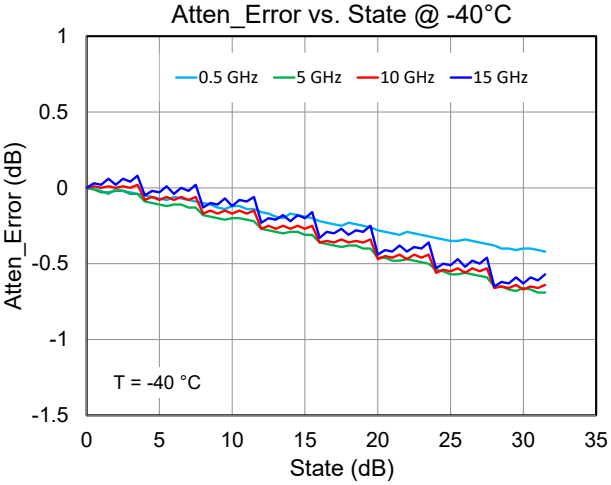
Atten_Error vs. Frequency @ 105°C



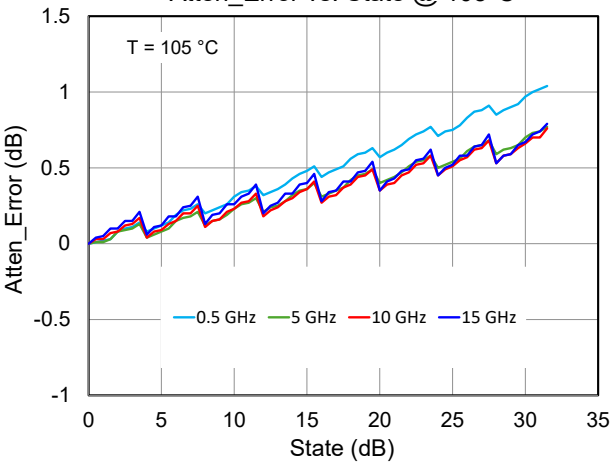
Atten_Error vs. State @ 25°C



Atten_Error vs. State @ -40°C

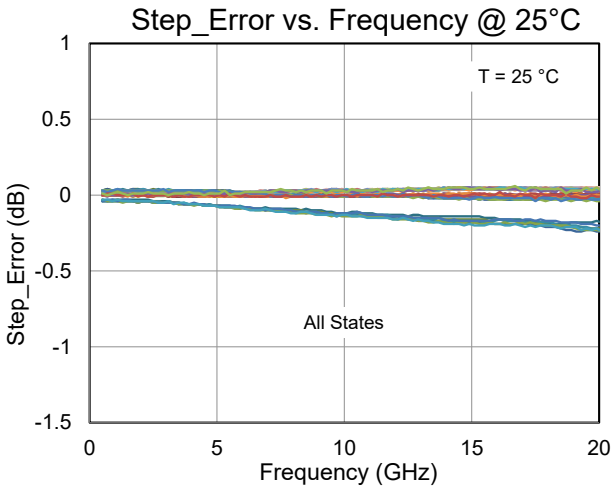


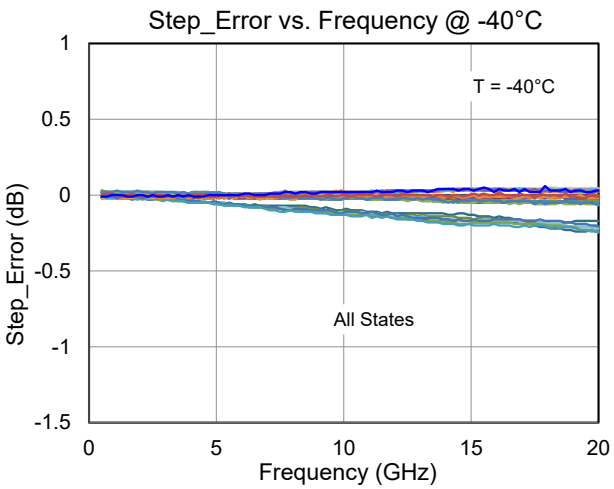
Atten_Error vs. State @ 105°C

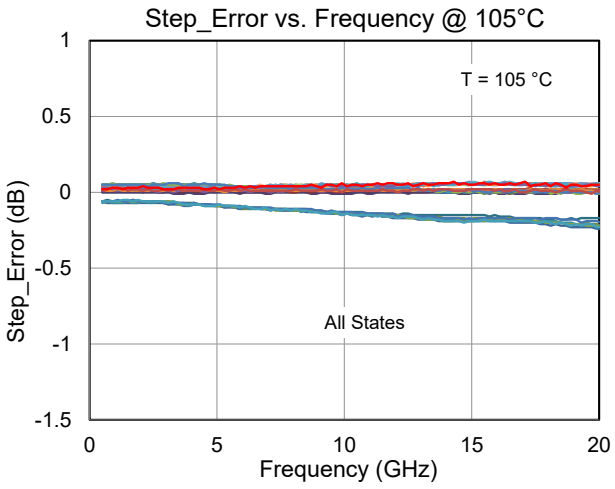


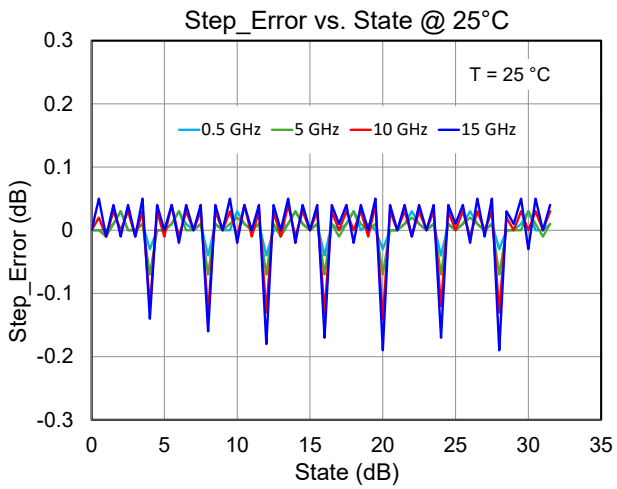
Performance Plots – Small Signal

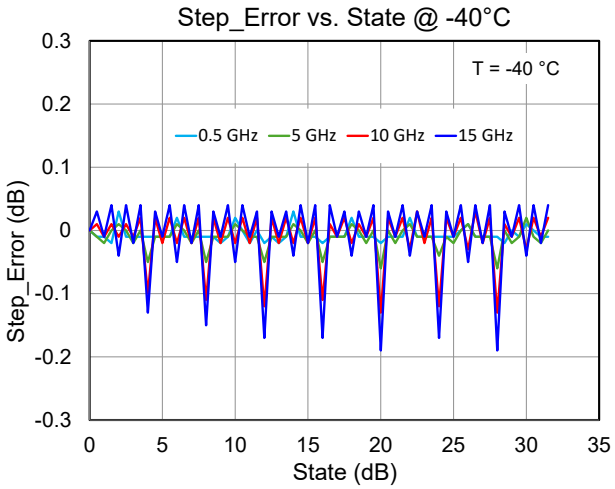
Test conditions unless otherwise noted: 50 Ω, 25 °C, V_{SS} = 0 V or -3.3 V, V_{DD} = +3.3 V. RF reference plans at package leads.
Monotonicity is maintained if Step Error is < +0.5 dB

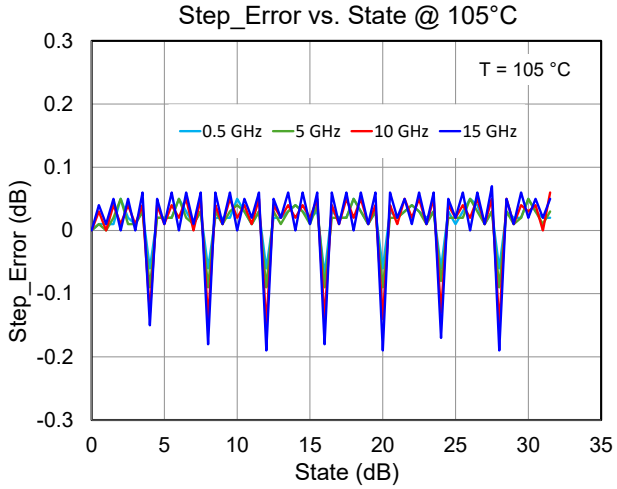






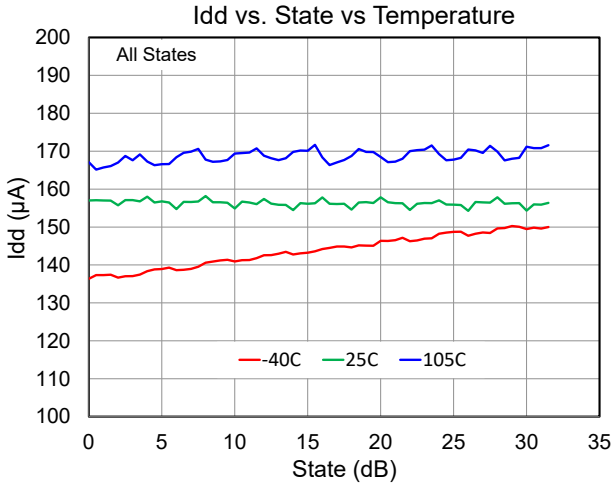


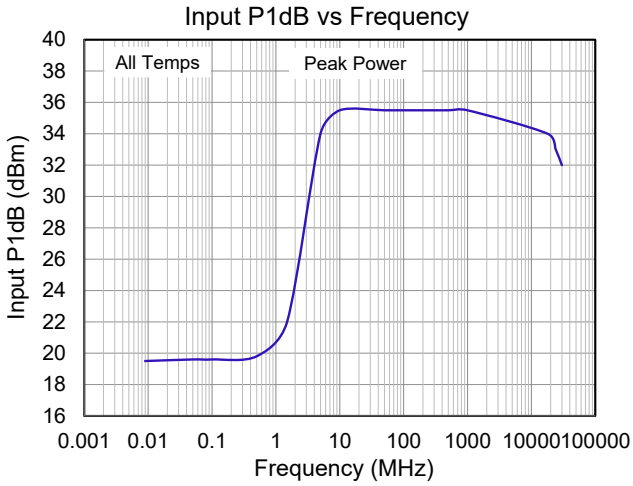


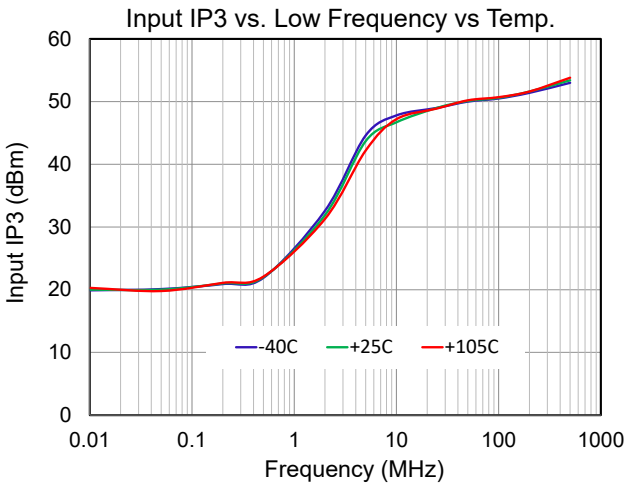


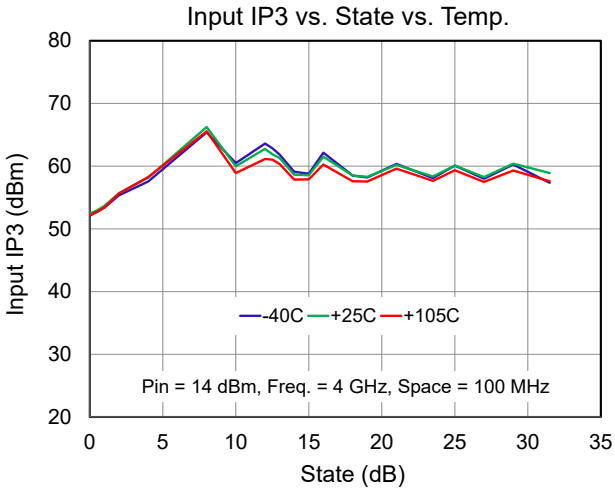
Performance Plots – Small Signal, Compression Power & Linearity

Test conditions unless otherwise noted: 50 Ω, 25 °C, V_{SS} = 0 V or -3.3 V, V_{DD} = +3.3 V. RF reference plans at package leads.









DSA Attenuation State Logic Table for Major States - (Applicable to all Modes)

Attenuation States	B5 (MSB)	B4	B3	B2	B1	B0 (LSB)
0.0 dB / Reference State	0	0	0	0	0	0
0.5 dB	0	0	0	0	0	1
1 dB	0	0	0	0	1	0
2 dB	0	0	0	1	0	0
4 dB	0	0	1	0	0	0
8 dB	0	1	0	0	0	0
16 dB	1	0	0	0	0	0
31.5 dB	1	1	1	1	1	1

Note: For logic “0” and logic “1” levels, refer to Nominal Operating Conditions Table

Control Interface

QPC5330 supports 4 different control interfaces - parallel, 6/8-bit non-addressable SPI, 16-bit addressable SPI and I2C. The two pins SCK and SDA for I2C mode should be tied down if I2C interface is not used. Please see table below for selection logic table and default power-up states for these control modes.

Interface-Select Table & Default Power-Up State

Operation Modes		IS0	IS1	LE (During Power-Up)	D[5:0] (During Power-Up)	DSA Power-Up State
Parallel	Latched	0	0	0	X	Max Attenuation
	Directed			1 or Floating	Data Present	Defined by Data
					Floating	Max Attenuation
6/8-bit SPI		1	0	0	-	Max Attenuation
				1 or Floating	-	Min Attenuation
16-bit Addressable SPI		0	1	0	-	Max Attenuation
				1 or Floating	-	Min Attenuation
I2C		1	1	0	-	Max Attenuation
				1 or Floating	-	Min Attenuation

Note:
a. For logic “0” and logic “1” levels, refer to Nominal Operating Conditions Table
b. Dynamic operation between different interface modes is not supported.

Parallel Mode Interface (1)

The QPC5330 has six digital control inputs B0 (LSB) to B5 (MSB), to select the desired attenuation state in the parallel mode, as shown in the Logic Table above. The parallel control interface is activated when IS0 and IS1 are set to low.

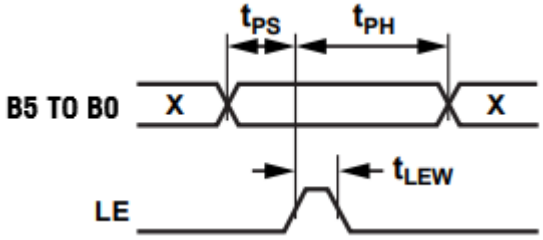
There are two modes of parallel operation: direct parallel and latched parallel.

Direct Parallel Mode

To enable direct parallel mode. The LE pin must be kept high. The attenuation state is changed by control voltage inputs (B0 to B5) directly. This mode is ideal for manual control of the attenuator.

Latched Parallel Mode

To enable latched parallel mode, the LE pin must be kept low when changing the control voltage inputs (B0 to B5) to set the attenuation state. When the desired state is set, LE must be toggled high to transfer the 6-bit data to the bypass switches of the attenuator array and then toggled low to latch the change into the device until the next desired attenuation change. See the timing diagram below:



Timing Specifications for Parallel Mode

Parameter	Min	Typ.	Max	Units
t_{PS} Control setup time	2	-	-	ns
t_{PH} Control hold time	2	-	-	
t_{LEW} Minimum LE pulse width	-	1	3.4	

Notes:
1. See Interface-Select Table on page 12 for details on Mode selection and Default Power-Up State.

SPI Mode Interface (1)

The QPC5330 supports a 3-wire SPI (CLK, LE and SDI) interface with serial data output (SDO) in 2 different modes. The attenuation states can be controlled using 6/8-bit non-addressable SPI mode or 16-bit addressable SPI mode. Modes are selected using Interface-Select pins (See Interface-Select table on page 6).

In non-addressable SPI mode, data is clocked in MSB first on the rising CLK edges into the shift register. Then, LE must be toggled high to latch the new attenuation state into the device. LE must be set back to low to clock new data. SDI data can be 6 bits or 8 bits with D6 and D7 as "don't care" bits. The control bits B5-B0 in attenuation state table are assigned to SDI data D[5:0].

In addressable SPI mode, 16-bit SDI is clocked in LSB first. The 16-bit word contains 8-bit attenuation word (D[7:0]), followed by 8-bit address word (A[7:0]). Bits D[7], D[0] and A[7:3] are not used and must be set low. The control bits B5-B0 in attenuation state table are assigned to SDI data D[6:1]. Bits A[2:0] contain the address and must match the logical states of the address pins (A2, A1 and A0) for the DSA to change state. The address pins A0, A1, and A2 can be set low or left floating (internally pulled up) depending upon the address decided by the user.

Using SDO

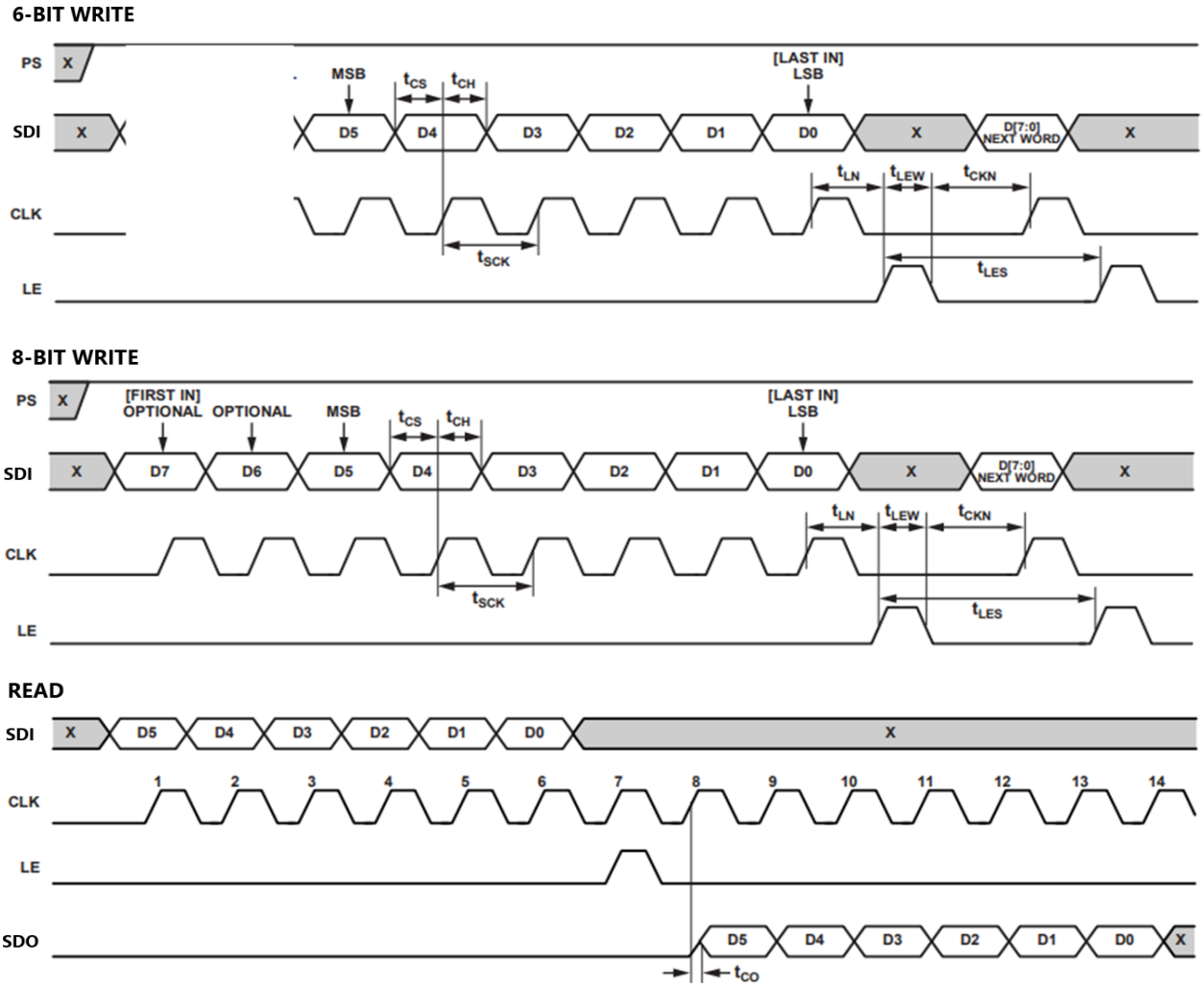
The QPC5330 features a serial data output, SDO, for daisy-chain operation using a single SPI bus. This pin does not support high-impedance mode. A tristate buffer can be used to interface a shared bus.

In non-addressable mode, 8-bit SDI data must be used and SDO outputs the serial input data at the 8th clock cycle. See the serial out timing diagrams on page 15.

In addressable mode, SDO outputs serial input data delayed by 16 clock cycles. See the serial out timing diagrams on page 16.

Notes:
1. See Interface-Select Table on page 12 for details on Mode selection and Default Power-Up State.

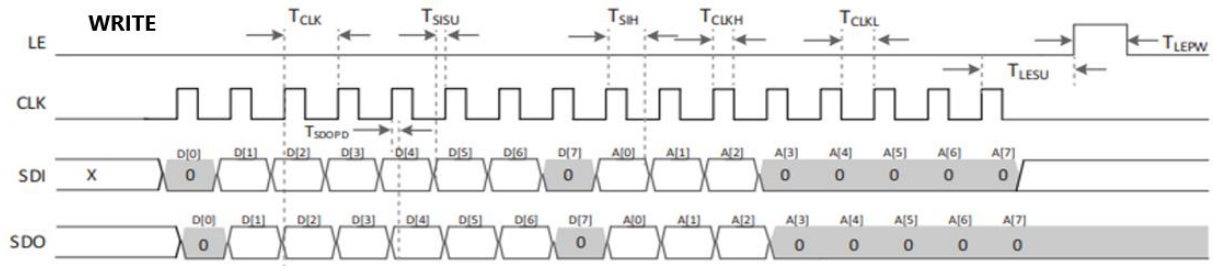
Timing Diagram for 6/8-Bit - SPI



Timing Specifications for 6/8-Bit - SPI

Parameter	Min	Typ.	Max	Units
t_{CLK} Minimum serial period	20	-	-	ns
t_{CS} Control setup time	1.5	-	-	
t_{CH} Control hold time	0.2	-	-	
t_{LN} LE Setup time	5	-	-	
t_{LEW} Minimum LE pulse width	-	1	-	
t_{LES} Minimum LE pulse spacing	-	180	-	
t_{CKN} Serial clock hold time from LE	5	-	-	
t_{PH} Hold time	-	10	-	
t_{PS} Setup time	-	2	-	
t_{CO} Clock to output (SDO) time	5.5	-	13.6	

Timing Diagram for 16-Bit - SPI



READ for 16-Bit: Continue wave form above with additional 16 extra clock cycles (Serial Cascaded Devices Table)

	D[0]	D[1]	D[2]	D[3]	D[4]	D[5]	D[6]	D[7]	A[0]	A[1]	A[2]	A[3]	A[4]	A[5]	A[6]	A[7]	D[0]	D[1]	D[2]	D[3]	D[4]	D[5]	D[6]	D[7]	A[0]	A[1]	A[2]	A[3]	A[4]	A[5]	A[6]	A[7]
CLK	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
SDI	1	1	1	1	1	1	0	0	0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
SDO	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	1	1	1	1	1	1	0	0	0	1	0	1	0	0	0	0

Timing Specifications for 16-Bit - SPI

Parameter	Min	Typ.	Max	Units
F_{CLK} Serial CLOCK frequency	-	-	50	MHz
T_{CLK} Serial CLOCK time period	20	-	-	ns
T_{CLKH} Serial CLOCK HIGH time (50% & 20% duty cycles)	9 / 4	-	-	
T_{CLKL} Serial CLOCK LOW time (50% & 20% duty cycles)	10 / 16	-	-	
T_{TLSU} Last serial clock rising edge setup time to LE rising edge	5	-	-	
T_{LEPW} LE pulse width		1	-	
T_{SISU} Serial DATA setup time	1.5	-	-	
T_{SIH} Serial DATA hold time	0.2	-	1.8	
T_{SDOPD} Clock to SDO delay	5.5	-	13.6	

I2C Mode Interface (1)

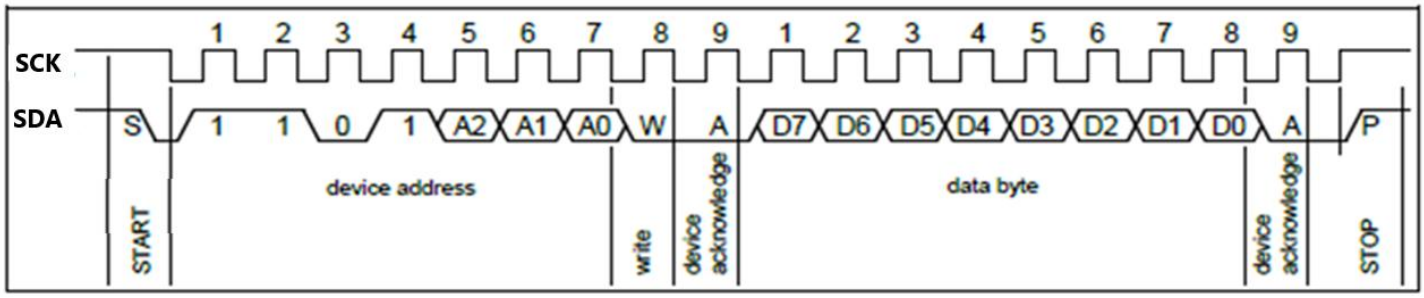
The QPC5330 supports a 2-wire I2C interface to control the attenuation setting. Write command is initiated by toggling SDA low before toggling SCK low. The data on SDA pin is then clocked in MSB first and starts with 7-bit address code. Address bits A[6:4] are reserved as [1101], A[2:0] must match the logic states of address pins (A2, A1, A0) for QPC5330 to respond to the write command and change DSA state. The address pins A0, A1, and A2 can be set low or left floating (internally pulled up) depending upon the address decided by the user.

Address bits are followed by R/W bit, ACK/NACK bit and 8-bit attenuation code (D[7:0]) and another ACK/NACK bit. Bits D[7] and D[0] are not used and must be set low. The control bits B5-B0 in attenuation state table are assigned to bits D[6:1].
Write command is finished by toggling SDA high after SCK is toggled high.

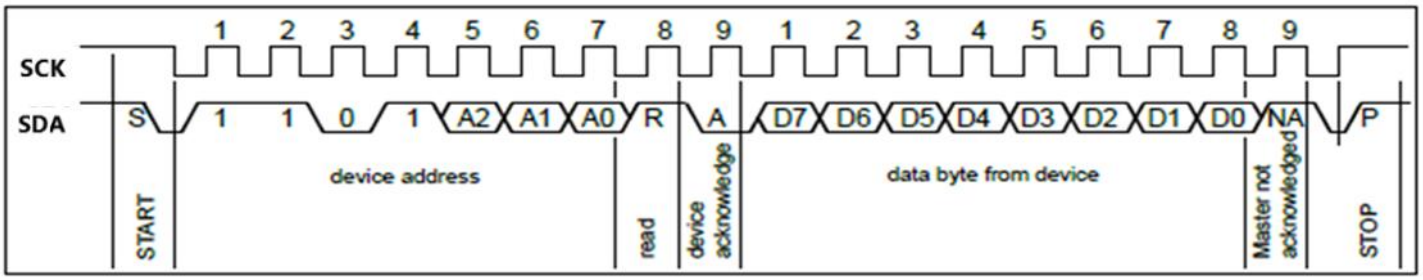
I2C interface also supports read operation. Please see the following timing diagrams and table for details.

Timing Diagram

WRITE

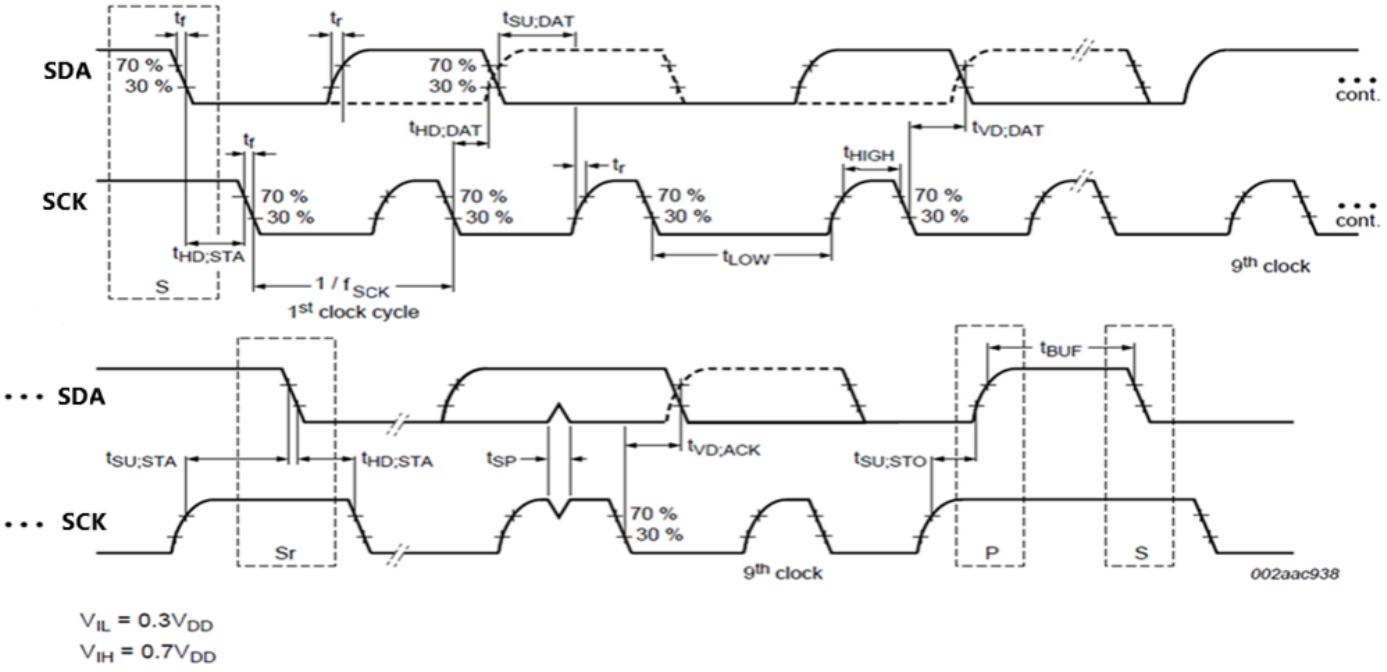


READ



Notes:
1. See Interface-Select Table on page 12 for details on Mode selection and Default Power-Up State.

Timing Diagram - Continued



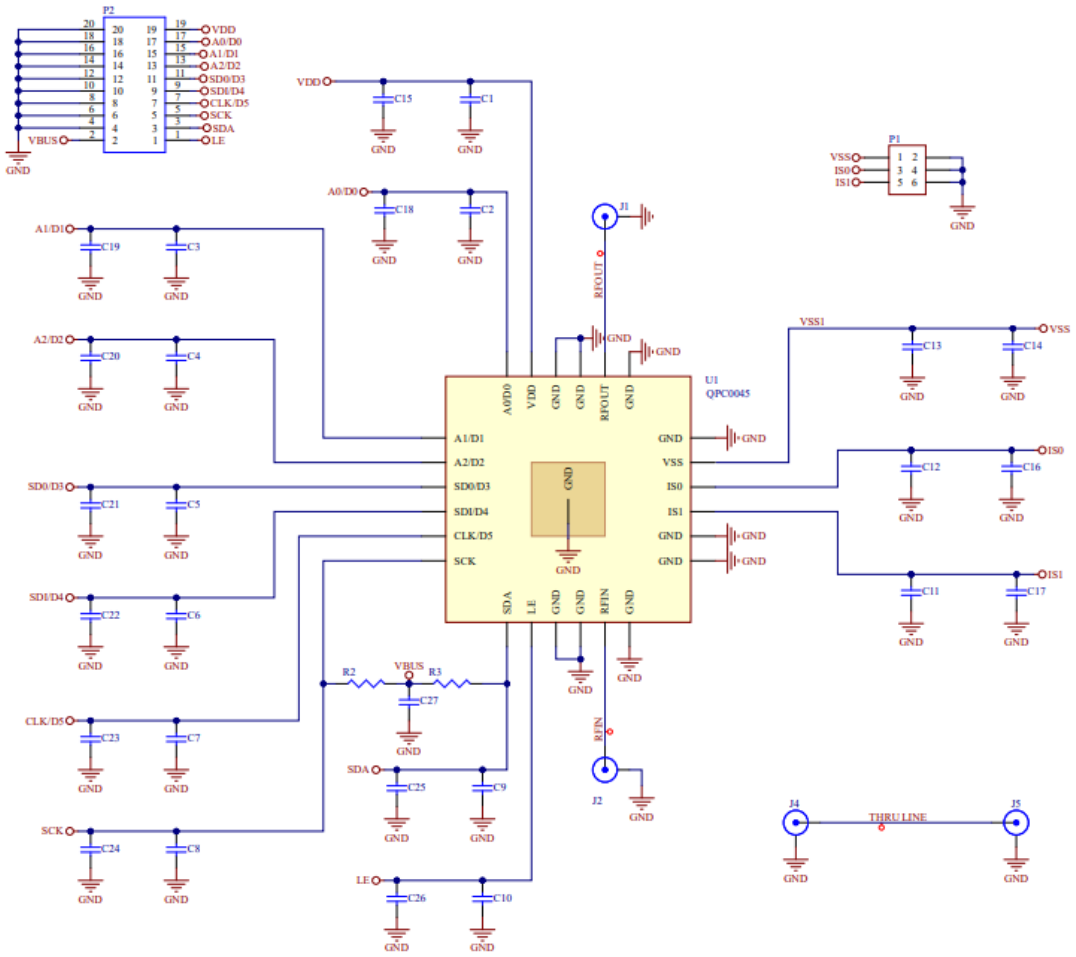
$V_{IL} = 0.3V_{DD}$
$V_{IH} = 0.7V_{DD}$

I2C Control Interface Timing Specifications (1)

Parameter	Min	Typ.	Max	Units
f_{SCK} CLOCK frequency	-	-	100	kHz
$t_{HS;STA}$ Hold time (repeated) START condition	2	-	-	ns
t_{LOW} LOW period of SCK clock	-	6000	-	
t_{HIGH} HIGH period of the clock	-	4000	-	
$t_{SU;STA}$ Setup time for repeated START condition	2			
$t_{HD;DAT}$ DATA hold time	2	-	-	
$t_{SU;DAT}$ DATA setup time	2	-	-	
t_r Rise time of both DATA and CLOCK	-	123	-	
t_f Fall time of both DATA and CLOCK	-	8	-	
$t_{SU;STO}$ setup time for STOP condition	-	-	2	
t_{BUF} bus free time between as STOP and START condition	-	-	5000	
C_b capacitive load for each bus line	-	-	400	
$t_{VD;DAT}$ DATA valid time (fall)	106	-		
$t_{VD;DAT}$ DATA valid time (rise)	-	-	406	
$t_{VD;ACK}$ DATA valid acknowledge time (fall)	106	-	-	
$t_{VD;ACK}$ DATA valid acknowledge time (rise)	-	-	406	
V_{nL} Noise margin at LOW level	-	0.6	-	V
V_{nL} Noise margin at HIGH level	-	-	-	

Notes:
1. For 1.8V bus voltage with 400pF load and 360 Ohm pullup.

Applications Circuit

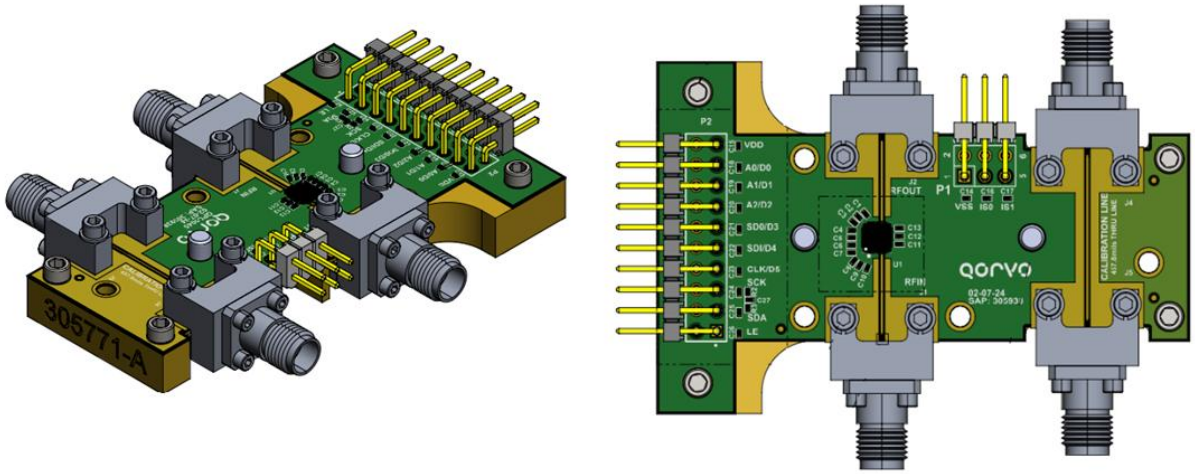


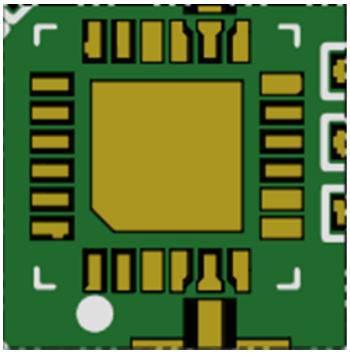
Bill of Materials for EVB

Reference Des.	Value	Description	Mfg.	Part Number
C1-C13, C27	100 pF	CAP, 0201, 25 V, 5%, C0G	Various	–
C14-C26	N/A	Not Populated		
R2, R3 (*)	510 Ohms	RES, 0402, 5%, 1/10W	Various	–

Note:
(*) These pullup resistors to VBus voltage are for Qorvo I2C controller setup. In most cases these already exist in I2C system.

Evaluation Board (EVB) Layout





Landing Pattern

Notes:

1. RFIN and RFOUT are interchangeable. RFOUT port can be used as RF input port with slightly degraded input power handling as indicated from max operating power graphs on page 3.
2. No DC blocking capacitor is necessary when the RF line potential is <0.1V DC. Ports are pulled down to ground.
3. The pad pattern shown has been developed and tested for optimized assembly at Qorvo Inc. The PCB land pattern has been developed to accommodate lead and package tolerances. Since surface mount processes vary from company to company, careful process development is recommended.

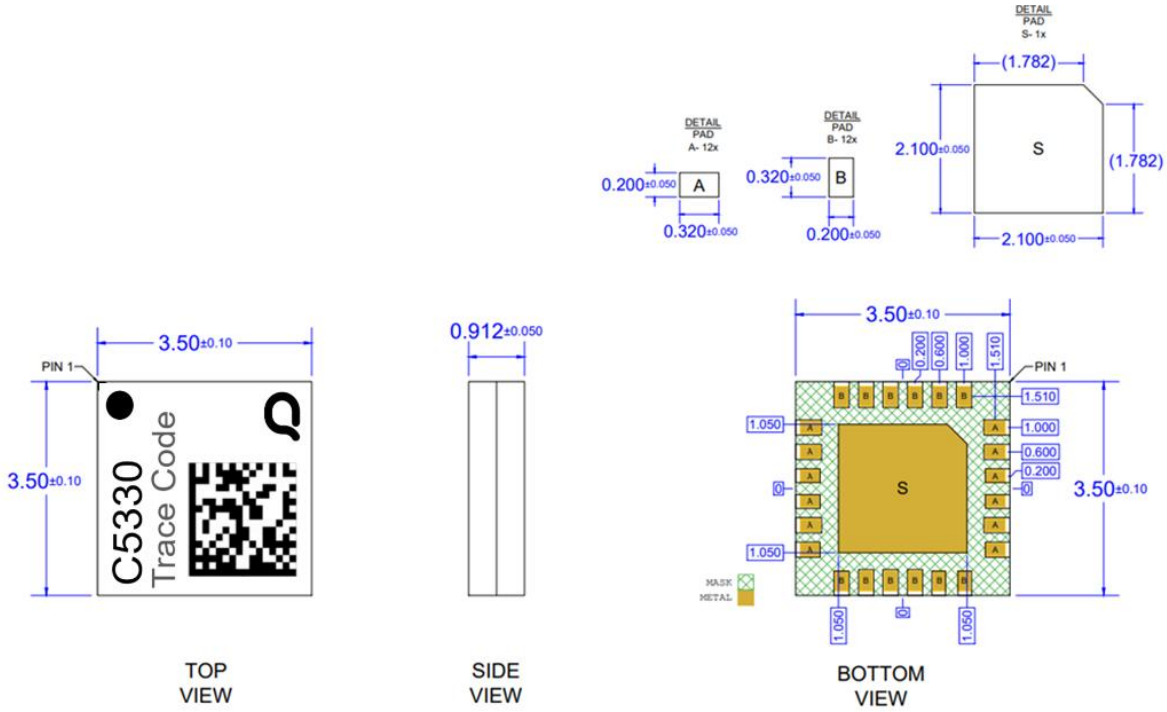
Evaluation Board PCB Information

LAYER STACK LEGEND

Material	Layer	Thickness	Dielectric Material	Type	Comment
	Top Overlay			Legend	HIGH TEMPERATURE, NON-CONDUCTIVE, WHITE EPOXY BASED INK.
Surface Material	Top Solder	0.0004	Solder Resist	Solder Mask	LPI (LIQUID PHOTO-IMAGEABLE) OR LDI (LASER DIRECT IMAGEABLE), GREEN.
Copper	**Top Layer**	**0.0018**		**Signal**	**FINISH THICKNESS=0.5oz COPPER CLADDING + SURFACE PLATING/VIA PLATING/FINISH**
Core		*0.0080*	*Rogers 4003*	*Dielectric*	
Copper	**Bottom Layer**	**0.0018**		**Signal**	**FINISH THICKNESS=0.5oz COPPER CLADDING + SURFACE PLATING/VIA PLATING/FINISH**

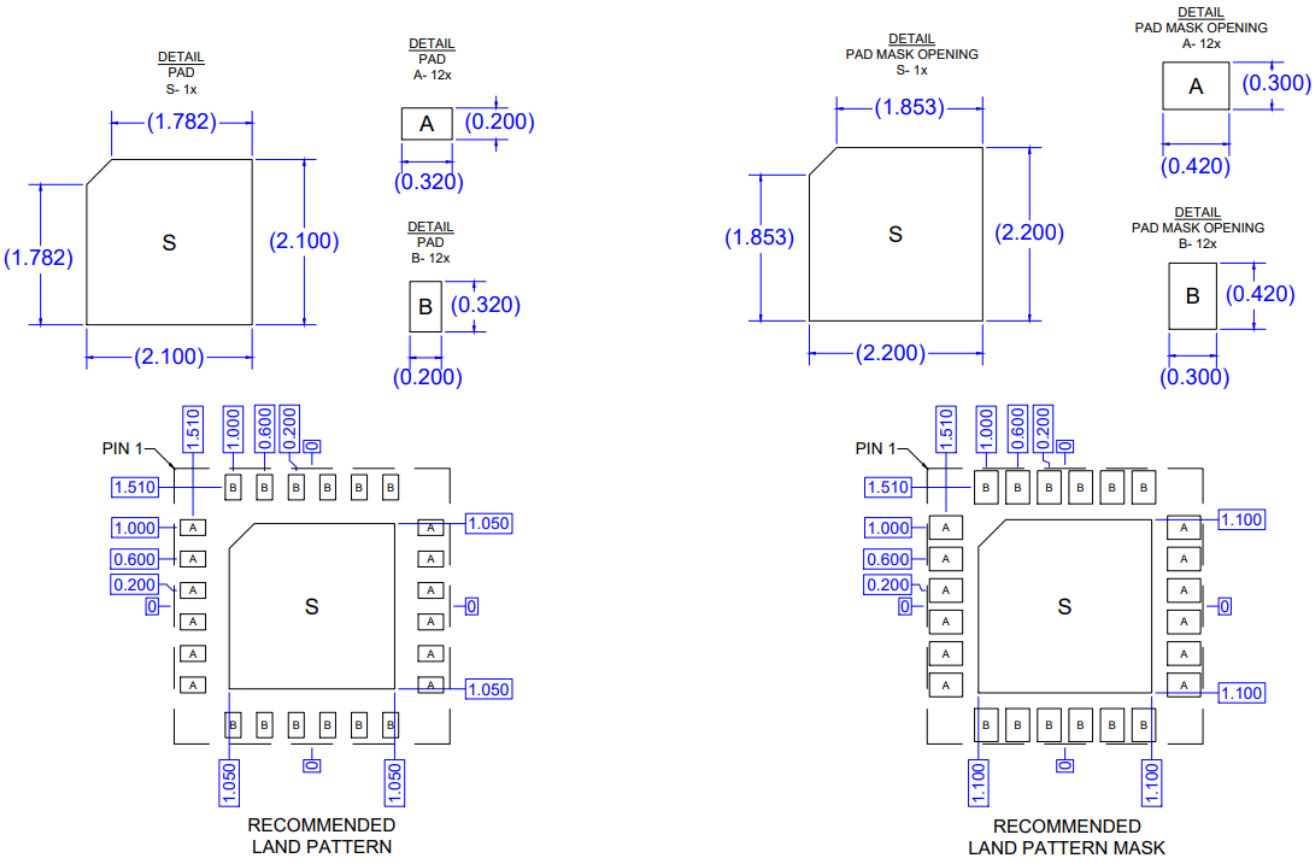
Finished board thickness: 0.0120

Mechanical Information



NOTES: UNLESS OTHERWISE SPECIFIED:
1. PART IS MOLD ENCAPSULATED
2. PACKAGE LEADS ARE GOLD PLATE
3. PART MARKING:
   5330: PART NUMBER
   TRACE CODE TO BE ASSIGNED BY SUBCON
4. ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.
5. DIMENSIONS AND TOLERANCE FORMATS CONFORM TO SPE-000677.

PCB Mounting Pattern



Notes:

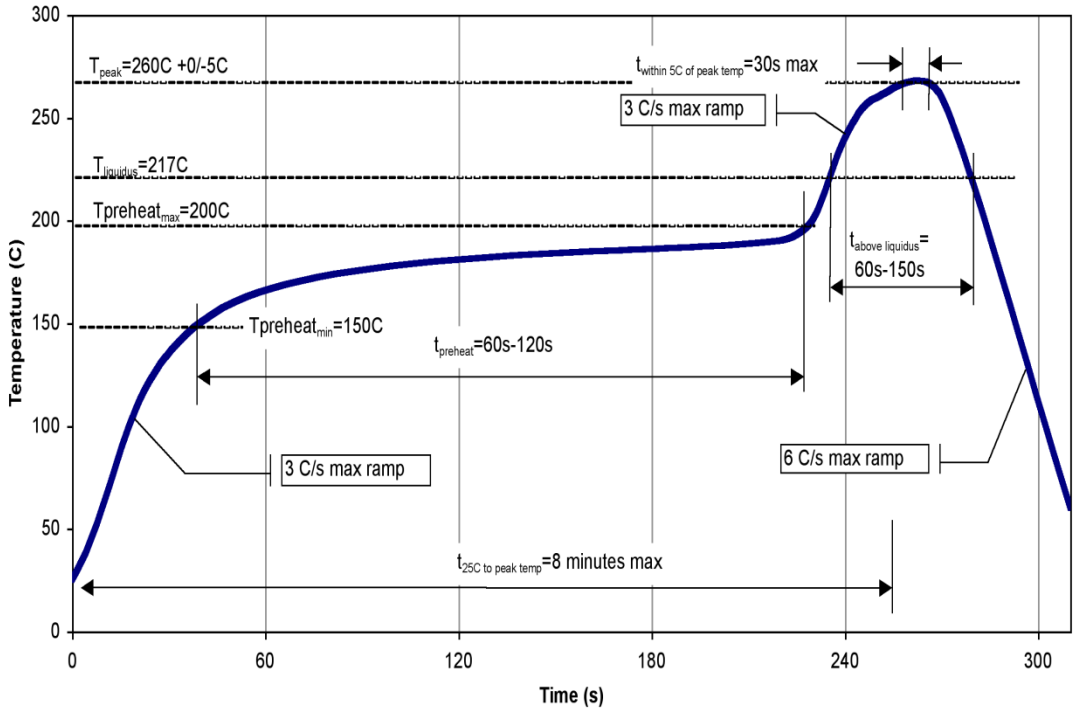
1. All dimensions are in millimeters. Angles are in degrees.
2. This drawing specifies the mounting pattern used on the Qorvo evaluation board for this product. Some modification may be necessary to suit end user assembly materials and processes.

Solderability

Compatible with both lead-free (260 °C max. reflow temperature) and tin/lead (245 °C max. reflow temperature) soldering processes.

Contact plating: OSP - Thin NiENEPIG .

Recommended Soldering Profile



Handling Precautions

Parameter		Rating	Standard
ESD – Human Body Mode (HBM)	All Pins	Class 1B	ANSI/ESD/JEDEC JS-001
	Excluding: RFIN & RFOUT	Class 1C	ANSI/ESD/JEDEC JS-001
ESD – Charge Device Model (CDM)		Class C3	JESD22-C101
MSL – Moisture Sensitivity Level		Level 3	IPC/JEDEC J-STD-020

Caution!
ESD-Sensitive Device

Environmental Compliance

This part is compliant with 2011/65/EU RoHS directive (Restrictions on the Use of Certain Hazardous Substances in Electrical and Electronic Equipment) as amended by Directive 2015/863/EU.

This product also has the following attributes:

- Lead Free
- Halogen Free (Chlorine, Bromine)
- Antimony Free
- TBBP-A ($C_{15}H_{12}Br_40_2$) Free
- PFOS Free
- SVHC Free

Contact Information

For the latest specifications, additional product information, worldwide sales and distribution locations:

Web: www.qorvo.com

Tel: 1-844-890-8163

Email: customer.support@qorvo.com

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