QP8817

Advanced PMIC with 5 Bucks, 2 Buck-Boost, and 10 LDO/LSWs

BENEFITS and FEATURES

- **Wide Input Voltage Range**
  - Vin = 2.7V to 5.5V
- **Complete Integrated Power Solution**
  - SW 1, 2: Configurable Single/Dual Phase 6A Buck Switching Regulators
  - SW 3, 4, 5: 2A Buck Switching Regulators
  - SW 6, 7: 1.5A Buck-Boost Switching Regulators
  - LDO 1, 2: 200mA High PSRR LDOs
  - LDO/LSW 3, 4, 5: 400mA Generic LDOs, Configurable as a Load Switch
  - LDO/LSW 6: 400mA Generic LDO, Configurable as 1.5A Load Switch
  - LSW 7/8: 1.5A Load Switches
  - LDO 9, 10: Low Quiescent Current Always-on 30mA and 15mA LDOs
  - Proprietary ACOT Control for Buck and Buck-Boost Regulators
- **Space Savings**
  - Fully Integrated
  - All Buck Regulators Work with 0.22 ~ 0.47µH Inductors
- **Ultra-low Quiescent Current**
- **Excellent Efficiency at Very Light Load**
- **Easy System Level Design**
  - Configurable Power ON/OFF Sequencing
  - Seamless Sequencing of External Supplies
  - Configurable Sleep Modes
  - I²C Watch Dog timer.
  - UV, OV, OTS & OC Fault Monitoring.
  - Pin Configurable I²C Addresses.
  - 4 Levels of Thermal Warnings with Register bit Read Out.
- **12X GPIOs**
  - Autonomous LED Modes for 2X GPIOs.
  - Multiple Wake up Triggers with GPIOs
  - Low Power Mode Control.
  - Dynamic Voltage Scaling (DVS) Control.
  - Power Good, nRESET Output Signals.
  - Interrupt Request Output (nIRQ).
  - General Purpose Input / Output Control Pins.
  - Sync Input to Synchronize Sequencing with a Second PMIC (PWREN pin)
  - Autonomous LED Blink and Breathe
  - I²C Interface – up to 3.4MHz

APPLICATIONS

- Computer Vision
- Portable Audio / Video
- AI / AR / VR
- FPGA

GENERAL DESCRIPTION

The QP8817 PMIC is an integrated ActiveCiPS™ power management integrated circuit. It powers a wide range of processors, including video processors, FPGA's, peripherals, and microcontrollers. The QP8817 is highly flexible and can be reconfigured via I²C for multiple applications without the need for PCB changes. The low external component count and high configurability significantly speed time to market. Examples of configurable options include output voltage, startup time, slew rate, system-level sequencing, switching frequency, sleep modes, operating modes, etc. QP8817 is programmed at the factory with a default configuration. These settings can be optimized for a specific design through the I²C interface. The QP8817 is available in several default configurations. Contact the factory for specific default configurations.

The core of the device includes five DC/DC step-down and two DC/DC Buck-Boost regulators, all with integrated power FETs; two low noise, high PSRR low-dropout regulators (LDO), three configurable LDOs than can be configured as low switches; and three high current LSWs that can support up to 1.5A current, and two low quiescent current always-on LDOs that support 30mA and 15mA. All Bucks and Buck-Boosts regulators use an ACOT control architecture to optimize the load transient response with 0.22 ~ 0.47uH inductor and smaller output capacitors. Buck 1 and Buck 2 support dual-phase operation to support up to 10A typ. / 12A peak currents. The LDO/LSWs only require small ceramic capacitors. All outputs are highly configurable via the I²C interface.

In addition to the two I2C pins, the QP8817 has 12 configurable GPIOs. These GPIOs can be configured for multiple purposes, like enable signals for external regulators, interrupts, PWREN, DVS control, LED drive, push button, etc. For the LED driver, the QP8817 supports configurable single/double blink and breathe modes and LED drive current.

The QP8817 PMIC is available in a 3.77 x 4.17 mm 90-ball WLCSP package.

TYPICAL APPLICATION DIAGRAM

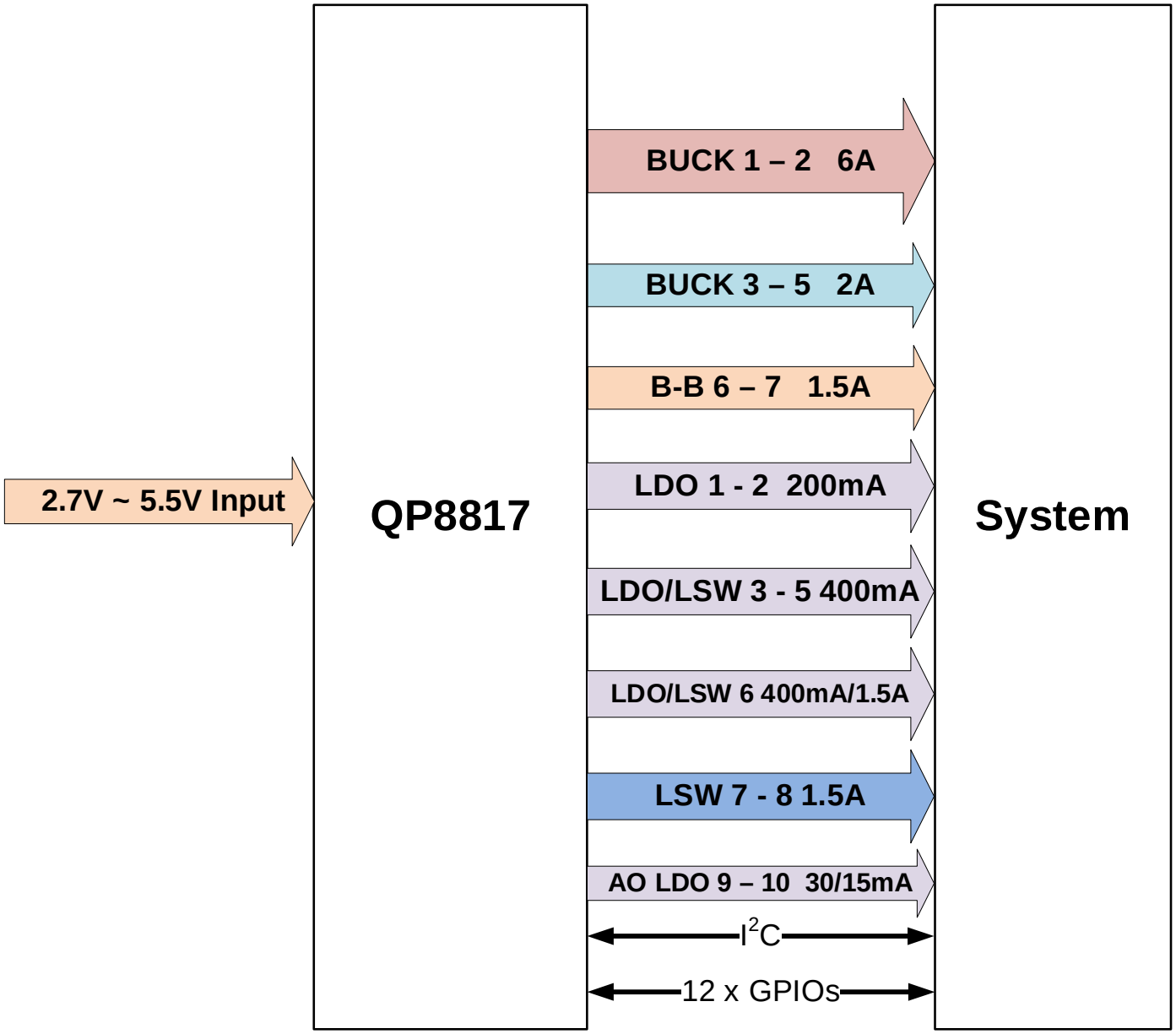


Figure 1: Typical Application Diagram

APPLICATION BLOCK DIAGRAM

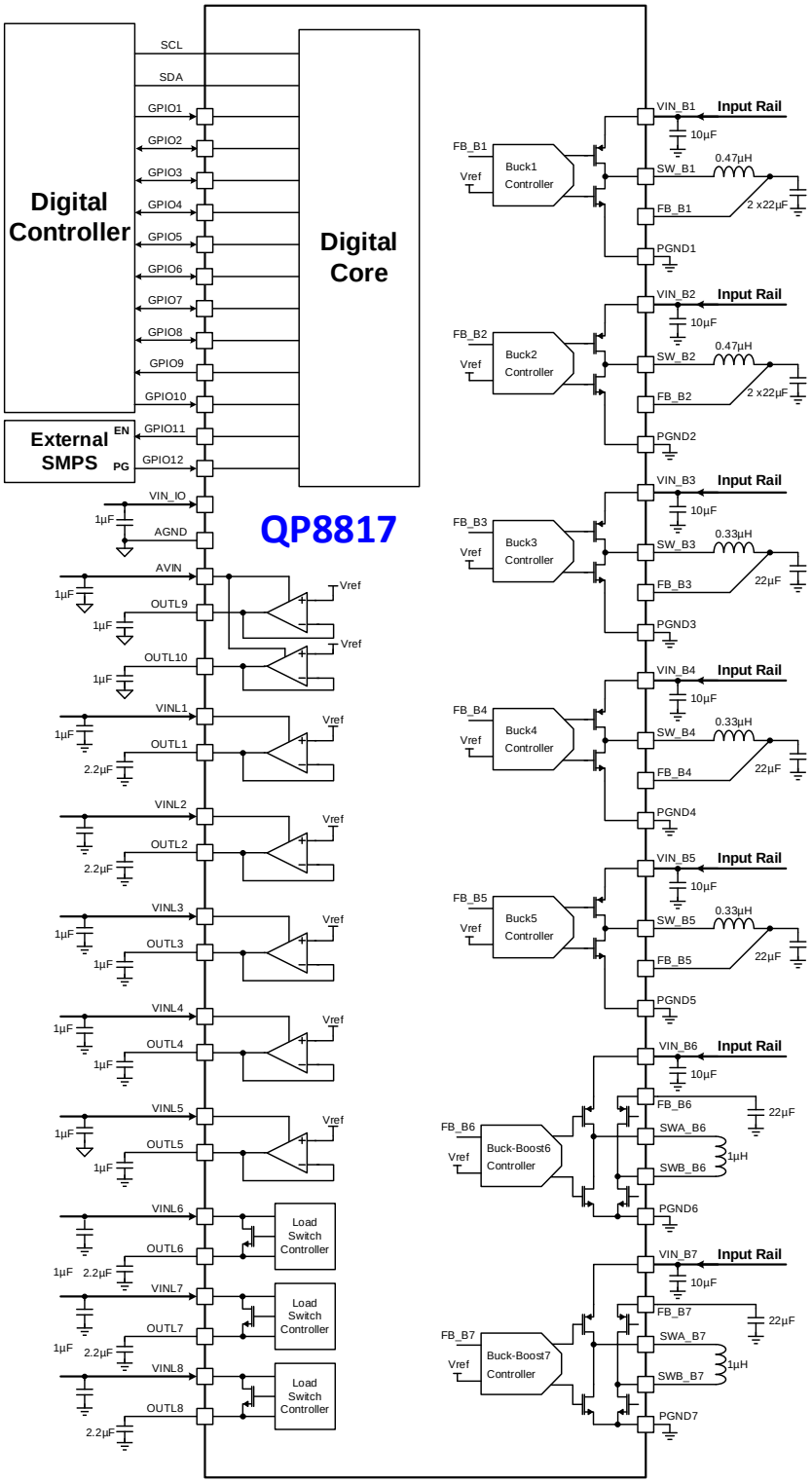


Figure 2: QP8817 Block Diagram & Application Schematic (Buck-Boost *6/7* in Buck-Boost Mode)

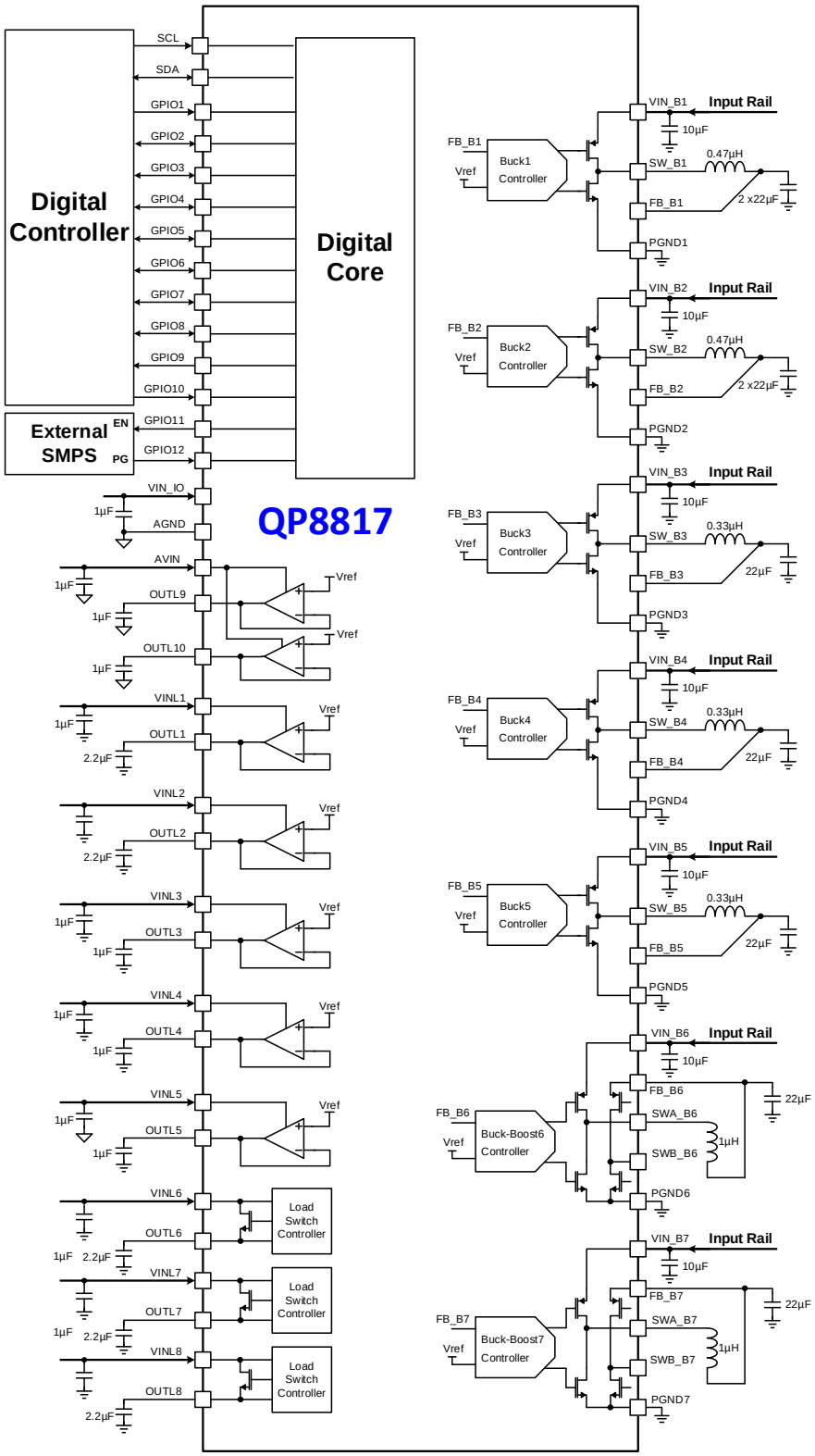
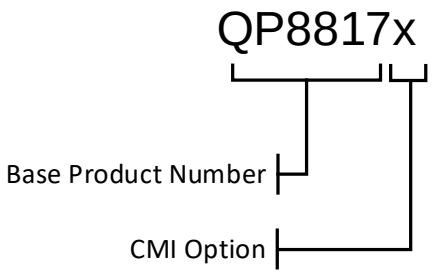


Figure 3: QP8817 Block Diagram & Application Schematic (Buck-Boost 6/7 in Buck Mode)

ORDERING INFORMATION

PART NUMBER	V_{OUT1}	V_{OUT2}	V_{OUT3}	V_{OUT4}	V_{OUT5}	V_{OUT6}	V_{OUT7}	V_{LDO1}	
QP8817A	0.725V	0.725V	1.8V	1.2V	0.725V	3.3V	3.3V	1.9V	
	V_{LDO2}	V_{LDO3}	V_{LDO4}	V_{LDO5}	V_{LDO6}	V_{LDO7}	V_{LDO8}	V_{LDO9}	V_{LDO10}
	1.8V	LSW	1.8V	1.05V	LSW	LSW	LSW	1.8V	3.3V



Note 1: Standard product options are identified in this table. Contact the factory for custom options. Minimum order quantity is required.

Note 2: “x” represents the CMI (Code Matrix Index) option The CMI identifies the IC’s default register settings.

PIN CONFIGURATION - WLCSP

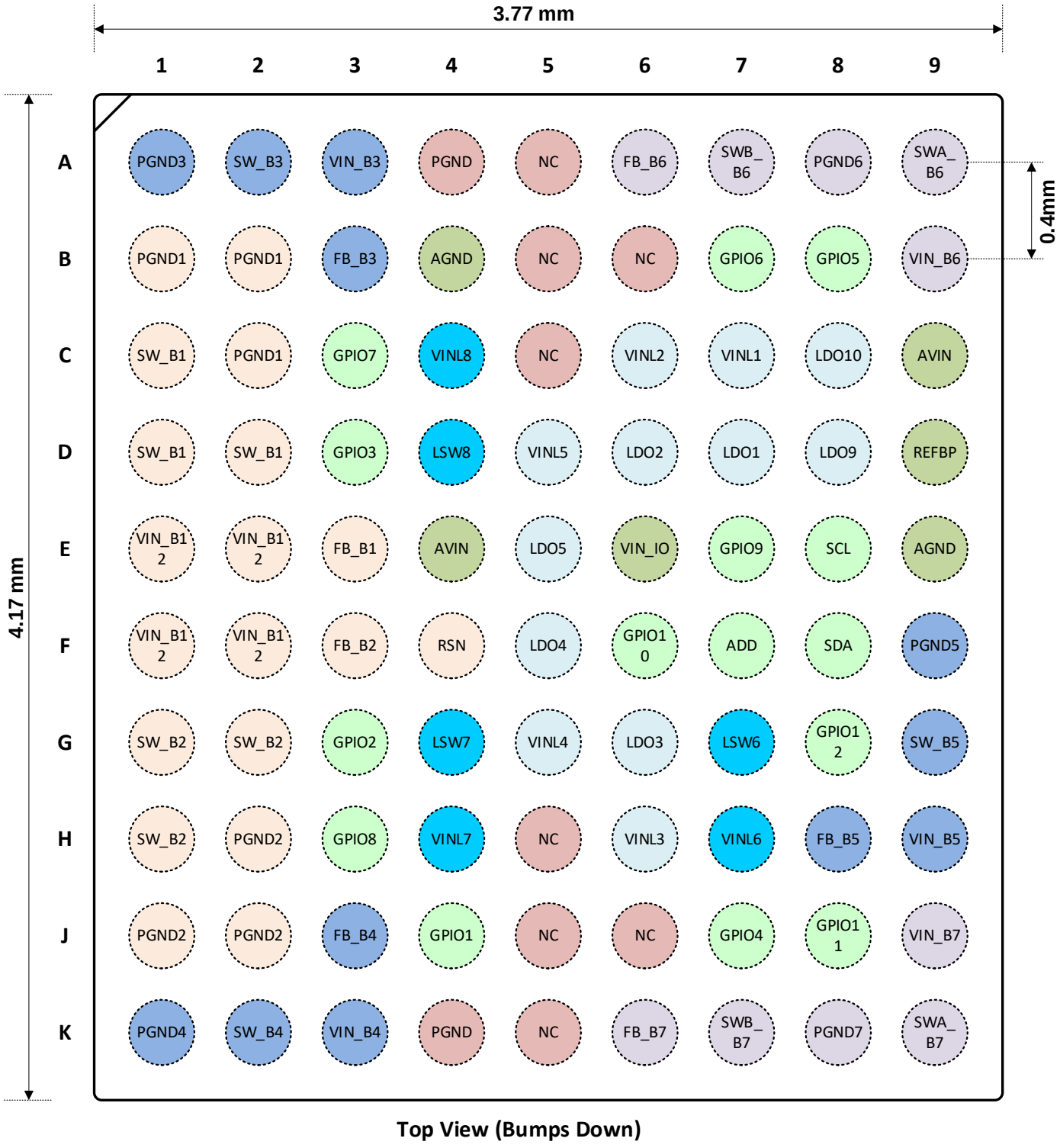


Figure 4: QP8817 Pin Configuration – Top View (bumps down) – WLCSP- 90

PIN DESCRIPTIONS

Ball (CSP)	NAME	DESCRIPTION
E1, E2	VIN_B1	Buck1 Input. Connect a bypass capacitor between this pin and PGND.
C1, D1, D2	SW_B1	Buck1 switch node
B1, B2, C2	PGND1	Buck1 power ground
E3	FB_B1	Buck1 feedback
F4	RSN	Buck1 remote sense, it is also the remote sense pin for Buck 1/2 dual-phase operation. Can be used with FB_B1 as a differential pair for remote voltage sensing.
F1, F2	VIN_B2	Buck2 Input. Connect a bypass capacitor between this pin and PGND.
G1, G2, H1	SW_B2	Buck2 switch node
H2, J1, J2	PGND2	Buck2 power ground
F3	FB_B2	Buck2 feedback
A3	VIN_B3	Buck3 Input. Connect a bypass capacitor between this pin and PGND.
A2	SW_B3	Buck1 switch node
A1	PGND3	Buck3 power ground
B3	FB_B3	Buck3 feedback
K3	VIN_B4	Buck4 Input. Connect a bypass capacitor between this pin and PGND.
K2	SW_B4	Buck4 switch node
K1	PGND4	Buck4 power ground
J3	FB_B4	Buck4 feedback
H9	VIN_B5	Buck5 Input. Connect a bypass capacitor between this pin and PGND.
G9	SW_B5	Buck5 switch node
F9	PGND5	Buck5 power ground
H8	FB_B5	Buck5 feedback
B9	VIN_B6	Buck-Boost6 Input. Connect a bypass capacitor between this pin and PGND.
A9	SWA_B6	Buck-Boost6 Buck side switch node
A7	SWB_B6	Buck-Boost6 Buck side switch node
A8	PGND6	Buck-Boost6 power ground
A6	FB_B6	Buck-Boost6 feedback
J9	VIN_B7	Buck-Boost7 Input. Connect a bypass capacitor between this pin and PGND.
K9	SWA_B7	Buck-Boost7 Buck side switch node
K7	SWB_B7	Buck-Boost7 Buck side switch node
K8	PGND7	Buck-Boost7 power ground
K6	FB_B7	Buck-Boost7 feedback

C7	VINL1	LDO1 input. Connect a bypass capacitor between this pin and AGND.
D7	LDO1	LDO1 output
C6	VINL2	LDO2 input. Connect a bypass capacitor between this pin and AGND.
D6	LDO2	LDO2 output
H6	VINL3	LDO3 input. Connect a bypass capacitor between this pin and AGND.
G6	LDO3	LDO3 output
G5	VINL4	LDO4 input. Connect a bypass capacitor between this pin and AGND.
F5	LDO4	LDO4 output
D5	VINL5	LDO5 input. Connect a bypass capacitor between this pin and AGND.
E5	LDO5	LDO5output
H7	VINL6	Load switch 6 input. Connect a bypass capacitor between this pin and AGND.
G7	LSW6	Load switch 6 output
H4	VINL7	Load switch 7 input. Connect a bypass capacitor between this pin and AGND.
G4	LSW7	Load switch 7 output
C4	VINL8	Load switch 8 input. Connect a bypass capacitor between this pin and AGND.
D4	LSW8	Load switch 8 output
D8	LDO9	Low quiescent current LDO9 output
C8	LDO10	Low quiescent current LDO10 output
J4	GPIO1	GPIO
G3	GPIO2	GPIO
D3	GPIO3	GPIO
J7	GPIO4	GPIO
B8	GPIO5	GPIO
B7	GPIO6	GPIO
C3	GPIO7	GPIO
H3	GPIO8	GPIO
E7	GPIO9	GPIO
F6	GPIO10	GPIO
J8	GPIO11	GPIO
G8	GPIO12	GPIO
F8	SDA	I2C Data
E8	SCL	I2C Clock
C9, E4	AVIN	Analog input

B4, E9	AGND	Analog output
E6	VIN_IO	IO Voltage Pin
D9	REFBP	Internal reference bypass pin. Connect a capacitor between this pin and AGND.
F7	ADD	I2C address program pin. Connect a resistor between this pin and AGND to set the I2C address.
A4, K4	PGND	Power ground
A5, B5, B6, C5, H5, J5, J6, K5	NC	No connect. This pin must be left floating.

ABSOLUTE MAXIMUM RATINGS (NOTE1)

PARAMETER	VALUE	UNIT
All I/O and Power pins unless stated otherwise below	-0.3 to 6	V
Grounds: Any PGND referenced to AGND	-0.3 to +0.3	V
RSN to AGND	-0.3 to +0.3	V
VIN_Bx to PGNDx, x = 1, 2, 3, 4, 5, 6, 7	-0.3 to 6	V
SW_Bx to PGNDx, x = 1, 2, 3, 4, 5, 6, 7	-1 to VIN_Bx + 1	V
FB_Bx to PGNDx , x = 1, 2, 3, 4, 5, 6, 7	-0.3 to AVIN + 0.3	V
VINLx to AGND, x = 1, 2, 3, 4, 5, 6, 7	-0.3 to 6	V
LDOx to AGND, x = 1, 2, 3, 4, 5, 6, 7, 8, 9, 10	-0.3 to Min (6.0 or VINLx + 0.3V)	V
GPIOx, x = 1, 2, 3, 4, 5, 6, 7, 8, 9, 10	-0.3 to 6.0V	V
SDA, SCL to AGND	-0.3 to Min (6.0 or AVIN + 0.3V)	V
Junction to Ambient Thermal Resistance, CSP (Note2)	21.6	°C/W
Junction to Case Thermal Resistance, CSP (Note2)	4.5	°C/W
Operating Junction Temperature	-40 to 150	°C
Storage Temperature	-55 to 150	°C
HBM ESD (Note3)	2000	V
MSL rating	1	

Note1: Do not exceed these limits to prevent damage to the device. Exposure to absolute maximum rating conditions for long periods may affect device reliability.
Note2: Measured on Qorvo Evaluation Kit.

Note3: JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	VALUE	UNIT
All Pins to GND unless stated otherwise below	0 to 5.0	V
AGND	0 to + 0.3	V
PGNDx, x = 1, 2, 3, 4, 5, 6, 7, 8, 9	0 to + 0.3	V
VIO to AGND	0 to 1.8	V
AVIN to AGND	0 to 5.0	V
VIN_Bx, x = 1, 2, 3, 4, 5, 6, 7 to AGND (VIN_Bx = AVIN is required) (Note 1)	2.7 to 5.0	V
FB_Bx, x = 1, 2, 3, 4, 5, 6, 7 to AGND	0 to 5.0	V
SW_Bx, x = 1, 2, 3, 4, 5, 6, 7 to PGND	-0.8 to VIN_Bx + 0.8	V
BOOT_Bx to PGNDx, x = 8, 9	-0.3 to 23	V
FB_Bx to PGNDx, x = 8, 9	-0.3 to 20	V
SW_Bx to PGNDx, x = 8, 9	-0.3 to 20	V
VINLx, x = 1, 2, 3, 4, 5, 9, 10 to AGND	0 to 5.0	V
LDOx, x = 1, 2, 3, 4, 5, 9, 10 to AGND	0 to VINLx	V
VINLx, x = 6, 7, 8 to AGND	Min of (AVIN-1 or 3.6V)	V
GPIOx, x = 1, 2, 3, 4, 5, 6, 7, 8, 9, 10	0 to 5.0	V
nPB / PWREN / PWRON to AGND	0 to 5.0	V
SDA, SCL to AGND	0 to 5.0	V
Operating Junction Temperature	-10 to 125	°C

Note1: AVIN must always be the highest input voltage to the IC.

DIGITAL I/O ELECTRICAL CHARACTERISTICS

(AVIN = VIN_Bx = 3.8V, VIO = 1.8V, T_j = -40°C to +125°C, unless otherwise specified.)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
GPIO Pins					
VIO, GPIO Reference Voltage	Operating Voltage Range	1.62	1.8	AVIN	V
VIL, GPIOX, X = 1-8, 11, 12 Input Low	GPIO_VCC = AVIN = 2.7V - 5.0V, Input mode			0.3	V
VIL, GPIOX, X = 1-8, 11, 12 Input Low	GPIO_VCC = VIO = 1.8V Input mode			0.3	V
VIH, GPIOX, X = 1-8, 11, 12 Input High	GPIO_VCC = AVIN = 2.7V - 5.0V, Input mode	1.0			V
VIH, GPIOX, X = 1-8, 11, 12 Input High	GPIO_VCC = VIO = 1.8V Input mode	1.0			V
VIL, GPIOX, X = 9-10 Input Low	VIO = 1.8V Input mode			0.4	V
VIH, GPIOX, X = 9-10 Input High	VIO = 1.8V Input mode	1.35			V
GPIOX, X = 1-12 Input Deglitch Time (falling)				30	µs
GPIOX, X = 1-12 Input Deglitch Time (rising)				30	µs
GPIOX, X = 1-8, 11, 12 Delay time	GPIOX DEL [1:0] = 00 GPIOX DEL [1:0] = 01 GPIOX DEL [1:0] = 10 GPIOX DEL [1:0] = 11		0 1 2 4		ms
VOHPP, GPIOX, X = 1-8, 11, 12 Output High (Not GPIO5)	AVIN = 5.0V, VIO = 1.8V, I_{OL} = 0.1mA, GPIO configured as push-pull output type.	1.5			V
VOHPP, GPIOX, X = 1-8, 11, 12 Output High (Not GPIO5)	AVIN = 5.0V, VIO = 3.3V, I_{OL} = 0.1mA, GPIO configured as push-pull output type.	3.0			V
VOLPP, GPIOX, X = 1-8, 11, 12 Output Low (Not GPIO5)	AVIN = 5.0V, VIO = 1.8V, I_{OL} = 0.1mA, GPIO configured as push-pull output type.			0.3	V
VOLPP, GPIOX, X = 1-8, 11, 12 Output Low (Not GPIO5)	AVIN = 5.0V, VIO = 3.3V, I_{OL} = 0.1mA, GPIO configured as push-pull output type.			0.2	V
IOOD, GPIOX, X = 1-12 Open Drain Output High	VO = AVIN = 5.0V, VIO = 1.8 – 5.0V. Output Leakage Current, T_J = 25°C			1	µA
VOLOD, GPIOX, X = 1-12 Open Drain Output Low	I_{OL} = 1mA, AVIN = 5.0V, VIO = 1.8 – 5.0V			0.2	V
LED Current Sink Programming (Analog GPIO Pin Only – See GPIO table for Analog GPIO Pin List)					
ISINK range	ILEDX [3:0]	0	15	21	mA
ISINK, LED Current Sink Settings	ILEDX1, 2 = 0000 (LED disabled)		0		mA
	ILEDX1, 2 = 0001		1		mA
	ILEDX1, 2 = 0010		2		mA
	ILEDX1, 2 = 0011		3		mA
	ILEDX1, 2 = 0100		4		mA
	ILEDX1, 2 = 0101		5		mA

	ILEDX1, 2 = 0110		6		mA
	ILEDX1, 2 = 0111		7		mA
	ILEDX1, 2 = 1000		8		mA
	ILEDX1, 2 = 1001		9		mA
	ILEDX1, 2 = 1010		10		mA
	ILEDX1, 2 = 1011		11		mA
	ILEDX1, 2 = 1100		12		mA
	ILEDX1, 2 = 1101		13		mA
	ILEDX1, 2 = 1110		14		mA
	ILEDX1, 2 = 1111		15		mA
nPB – Push Button Pin Characteristics (Applicable when IC is configured for Push Button Function, nPB pin)					
nPB De-bounce Time	Push button presses shorter than this time are ignored.		50		ms
nPB Power Off Time (duration for successful turn-off)	EN_PB_OFF = 1 PB OFF TIME [1:0] = 00 PB OFF TIME [1:0] = 01 PB OFF TIME [1:0] = 10 PB OFF TIME [1:0] = 11		 1<t<4 4<t<8 8 12		s
nPB Power Cycle with Push Button	EN_PB_CYCLE = 1 PB CYCLE TIME [1:0] = 00 PB CYCLE TIME [1:0] = 01 PB CYCLE TIME [1:0] = 10 PB CYCLE TIME [1:0] = 11		 1<t<4 4<t<8 8 12		s
PWREN – Power Enable Pin Characteristics (Applicable when IC is configured for Power Enable Function, PWREN pin)					
PWREN Input Low	AVIN = 3.0V			0.3	V
PWREN Input High	AVIN = 3.3V	1			V
PWREN Input Low	AVIN > 2.7V, VIO = 1.8V (VIO used for I/O)			0.3	V
PWREN Input High	AVIN > 2.7V, VIO = 1.8V (VIO used for I/O)	1			V
PWREN, EXT_PG Deglitch Time (falling)			1	30	µs
PWREN, EXT_PG Deglitch Time (rising)			1	30	µs

SYSTEM CONTROL ELECTRICAL CHARACTERISTICS

(AVIN = 3.8V, T_j = -40°C to +125°C, unless otherwise specified.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
AVIN Operating Voltage Range		2.7		5.5	V
VIO Operating Voltage Range		1.62	1.8	AVIN	V
AVIN UVLO Threshold Falling	AVIN Shutdown Voltage	2.5	2.6	2.7	V
AVIN UVLO Hysteresis	Rising threshold higher than falling threshold	50			mV
System Monitor (SYSMON) Falling Threshold. Programmable Range. (AVIN Voltage)	Generate interrupt or turn off regulators when AVIN < SYSMON Threshold. Option to send SYSMON output via GPIO. Configurable in 100mV steps from 2.7 to 4.8V	-2.5	SET POINT	2.5	%
System Monitor (SYMON) Hysteresis - Programming Value. (AVIN Voltage)	AVIN must exceed the rising threshold for power up.		100		mV
System Warning (SYSWARN) Programmable Range– Falling Threshold	In 25mV steps	2.7		3.3	V
System Warning (SYSWARN) Accuracy	In 25mV steps	-2.5	SET POINT	2.5	%
System Monitor (SYSWARN) Hysteresis			100		mV
OV Threshold Rising	AVIN OV setting from 3.7V to 5.8V with 0.3V steps	3.7		5.8	V
OV Threshold Accuracy	AVIN OV Threshold, AVINOV = 1	-3		3	%
OV Hysteresis		80	200	320	mV
AVIN Deglitch Time for UV	UV Detection deglitch time Falling – Enter UV condition Rising – Exit UV condition		5 100		µs
AVIN Deglitch Time for OV	OV Detection deglitch time Falling – Enter OV condition Rising – Exit OV condition		5 200		µs
Operating Supply Current	All Regulators Disabled I2C is always available		12.5		µA
	Buck 3 (ULPM Mode) is on, other Regulators Disabled		61		µA
	Buck 3 and Buck 4 are on ULPM Mode, other Regulators Disabled		78		µA
	Buck 3 (ULPM Mode) and LDO3 (in LDO mode) are on, other Regulators Disabled		80		µA
	Buck 3 (ULPM Mode), LDO1, and LDO3 (in LDO mode) are on, other Regulators disabled		130		µA
	Buck 3 (ULPM Mode), Buck 4 (ULPM Mode), and LDO3 (in LSW mode) are on, other Regulators disabled		82		µA
	Buck 3 (ULPM Mode), Buck-Boost 6, and		295		µA

	LDO3 (in LDO mode) are on, other Regulators Disabled				
	All Regulators Enabled – No load (not in ultra-low power mode)		2		mA
Thermal Warning Threshold	TWARN0 Register Bit, TWARN = 00	TWARN1-30	TWARN1-20	TWARN1-10	°C
	TWARN1 Register Bit, TWARN = 01	TWARN2-30	TWARN2-20	TWARN2-10	°C
	TWARN2 Register Bit, TWARN = 10	TWARN3-30	TWARN3-20	TWARN3-10	°C
	TWARN3 Register Bit, TWARN = 11	TSD-35	TSD-25	TSD-15	°C
TSD, Thermal Shutdown	Temperature rising	135	155	175	°C
Thermal Shutdown Hysteresis			30		°C
Power Up Delay after initial AVIN applied	Time from AVIN > UVLO threshold to Internal Power-On Clear (POR)		475	800	µs
Startup Delay after initial AVIN Applied	Time from AVIN > UVLO threshold to start of first regulator turning On. (zero delay)		650	1000	µs
Main Oscillator Frequency	Master Clock reference for digital logic and control in the PMIC.		2.25		MHz
Slow Oscillator Frequency	Master Clock reference for digital logic and control in the PMIC.	29.6	32	34.4	kHz
Transition time from Deep Sleep (DPSLP) State to Active State	Time from GPIOx pin transition to time when the first regulator turns ON with minimum turn on delay configuration.			1	ms
Transition time from Sleep State (SLEEP) to Active State	Time from I2C command to clear sleep mode to time when the first regulator starts to turn ON with minimum turn on delay configuration.			200	µs
Time to first power rail turn off when entering SLEEP / DPSLP	Time from turn Off event to when the first power rail turns off with minimum off delay.			200	µs
Startup Delay Programmable Range (Does not count internal propagation delay, which is ~112us)	MSB setting of 0/1 is only factory accessible register bit and requires factory programming ONDLY= 0_000 ONDLY= 0_001 ONDLY= 0_010 ONDLY= 0_011 ONDLY= 0_100 ONDLY= 0_101 ONDLY= 0_110 ONDLY= 0_111 ONDLY= 1_000 ONDLY= 1_001 ONDLY= 1_010 ONDLY= 1_011 ONDLY= 1_100 ONDLY= 1_101 ONDLY= 1_110 ONDLY= 1_111		 28.5 57 114 228 456 912 1824 3648 0 500 1000 2000 4000 8000 16000 32000		µs
Turn Off Delay Programmable Range (Does not count internal propagation delay, which is ~112us)	MSB setting of 0/1 is only factory accessible register bit and requires factory programming OFFDLY = 0_000 OFFDLY = 0_001 OFFDLY = 0_010 OFFDLY = 0_011		 28.5 57 114 228		µs

	OFFDLY = 0_100 OFFDLY = 0_101 OFFDLY = 0_110 OFFDLY = 0_111 OFFDLY = 1_000 OFFDLY = 1_001 OFFDLY = 1_010 OFFDLY = 1_011 OFFDLY = 1_100 OFFDLY = 1_101 OFFDLY = 1_110 OFFDLY = 1_111		456 912 1824 3648 0 500 1000 2000 4000 8000 16000 32000		
nRESET Programmable Delay	nRST [1:0] = 000 nRST [1:0] = 001 nRST [1:0] = 010 nRST [1:0] = 011 nRST [1:0] = 100 nRST [1:0] = 101 nRST [1:0] = 110 nRST [1:0] = 111		2.5 5 10 20 40 60 80 100		ms

BUCK 1, 2 ELECTRICAL CHARACTERISTICS, REGULATOR:

(VIN_Bx = 3.8V, T_j = -40°C to +125°C, unless otherwise specified.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
VIN_BX Operating Voltage Range		2.7		AVIN	V
V_{FB_BX} Output Voltage Range	Configurable in 5mV steps, RANGE = 0 Configurable in 25mV steps, RANGE = 1	0.5 0.5		1.135 3.675	V
V_{FB_BX}, Output Voltage Accuracy	V_{OUT} = 1.0V, I_{OUT} = 2000mA (continuous PWM mode), 25°C < T_J < 85°C	-1%	V_{NOM}	1%	V
	V_{OUT} = 1.0V, I_{OUT} = 2000mA (continuous PWM mode), -40°C < T_J < 125°C	-1.5%	V_{NOM}	1.5%	V
	V_{OUT} = 1.0V, I_{OUT} = 10mA (discontinuous PFM mode), Buck ULPM = 0 (Ultra Low Power Mode Disabled), 25°C < T_J < 85°C	-1%	V_{NOM}	1%	V
	V_{OUT} = 1.0V, I_{OUT} = 10mA (discontinuous PFM mode), Buck ULPM = 0 (Ultra Low Power Mode Disabled), -40°C < T_J < 125°C	-1.5%	V_{NOM}	1.5%	V
	V_{OUT} = 1.0V, I_{OUT} = 10mA (discontinuous PFM mode operation), Buck ULPM = 1, (Ultra Low Power Mode Enabled), 25°C < T_J < 85°C	0%	V_{NOM} + 1.5%	2.5%	V
	V_{OUT} = 1.0V, I_{OUT} = 10mA (discontinuous PFM mode operation), Buck ULPM = 1, (Ultra Low Power Mode Enabled), -40°C < T_J < 125°C	0%	V_{NOM} + 1.5%	3%	V
I_{OUT}, Maximum ORutput Current ULPM = 1 (Ultra Low Power Mode)	Output current, ILIM = X	15			mA
Maximum Operation Duty Cycle		99			%
I_{SHUT}, Shutdown Current	V_{SW} = V_{IN} / 0V, Regulator Disabled, T_J = 25ºC		0.1	1	µA
I_{Q2}, Standby Supply Current, Buck Low Power Mode Enabled	Regulator Enabled, No Load		40		µA
I_{QLPM1}, Standby Supply Current, Buck Ultra Low Power Mode Enabled	Regulator Enabled, No Load, Buck ULPM = 1 & Fixed On-Time Enabled.		15		µA
$I_{LOADREG}$, Load Regulation	V_{OUT} = Default CMI Setting PWM mode.		0.05		%/A
$I_{LINEREG}$, Line Regulation	V_{IN} = 3.2V to 5.5V		0.05		%/V
P_{GOOD}, Power Good Threshold	V_{OUT} Rising	89	92	95	%
Power Good Hysteresis	V_{OUT} Falling		3		%
OV_{FLT}, Overvoltage Threshold	V_{OUT} Rising	109	112	115	%
Overvoltage Hysteresis	V_{OUT} Falling		3		%
Switching Frequency	FSET=00 FSET=01 FSET=10 FSET=11		1.5 2.0 2.5 3.3		MHz
T_{SS}, Soft-Start Period	10% to 90% ramp time of V_{OUT}		50 100 200 300		µs

			400 500 750 1000		
ILIM, Internal High Side Peak Current Limit (Cycle-by-Cycle)	ILIMSET=00 ILIMSET=01 ILIMSET=10 ILIMSET=11		4.0 5.5 7.0 8.5		A
Internal High Side Peak Current Limit (Cycle-by-Cycle) Tolerance	At Default ILIMSET	-12.5		12.5	%
IWARN, Internal High Side Peak Current Limit Warning Threshold.	Warning threshold as % of ILIM threshold	-12.5	-22.5	-32.5	%
Low Side On-Resistance, NMOS	I_{SW} = 1A, V_{IN} = 3.3V, T_J = 25°C		10		mΩ
High Side On-Resistance, PMOS	I_{SW} = 1A, V_{IN} = 3.3V, T_J = 25°C		30		mΩ
SW Leakage Current – NMOS	V_{IN} = 5V, V_{SW} = 5V, T_J = 25°C			1	µA
SW Leakage Current – PMOS	V_{IN} = 5V, V_{SW} = 0V, T_J = 25°C			1	µA
Output Pull Down Resistance	Enabled when regulator disabled, V_{OUT}=0.1V		6.7		Ω
Dynamic Voltage Scaling Rate	RANGE = 0 DVS SLEW = 00 DVS SLEW = 01 DVS SLEW = 10 DVS SLEW = 11		11.26 5.63 2.82 1.41		mV/ µs
	RANGE = 1 DVS SLEW = 00 DVS SLEW = 01 DVS SLEW = 10 DVS SLEW = 11		56.31 28.15 14.08 7.04		mV/ µs
C_{OUTMIN}, Minimum Output Cap	Minimum output capacitance with voltage de-rating	20			µF

BUCK 1/2 DUAL-PHASE ELECTRICAL CHARACTERISTICS:

(VIN_Bx = 3.8V, T_j = -40°C to +125°C, unless otherwise specified.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
VIN_BX Operating Voltage Range		2.7		AVIN	V
V_{FB_BX} Output Voltage Range	Configurable in 5mV steps, RANGE = 0 Configurable in 25mV steps, RANGE = 1	0.5 0.5		1.135 3.675	V
V_{FB_BX}, Output Voltage Accuracy	V_{OUT} = 1.0V, I_{OUT} = 2000mA (continuous PWM mode), 25°C < T_J < 85°C	-1%	V_{NOM}	1%	V
	V_{OUT} = 1.0V, I_{OUT} = 2000mA (continuous PWM mode), -40°C < T_J < 125°C	-1.5%	V_{NOM}	1.5%	V
	V_{OUT} = 1.0V, I_{OUT} = 10mA (discontinuous PFM mode), Buck ULPM = 0 (Ultra Low Power Mode Disabled), 25°C < T_J < 85°C	-1%	V_{NOM}	1%	V
	V_{OUT} = 1.0V, I_{OUT} = 10mA (discontinuous PFM mode), Buck ULPM = 0 (Ultra Low Power Mode Disabled), -40°C < T_J < 125°C	-1.5%	V_{NOM}	1.5%	V
	V_{OUT} = 1.0V, I_{OUT} = 10mA (discontinuous PFM mode operation), Buck ULPM = 1, (Ultra Low Power Mode Enabled), 25°C < T_J < 85°C	0%	V_{NOM} + 1.5%	2.5%	V
	V_{OUT} = 1.0V, I_{OUT} = 10mA (discontinuous PFM mode operation), Buck ULPM = 1, (Ultra Low Power Mode Enabled), -40°C < T_J < 125°C	0%	V_{NOM} + 1.5%	3%	V
I_{OUT}, Maximum Output Current ULPM = 1 (Ultra Low Power Mode)	Output current, ILIM = X	30			mA
Maximum Operation Duty Cycle		99			%
I_{SHUT}, Shutdown Current	V_{SW} = V_{IN} / 0V, Regulator Disabled, T_J = 25ºC		0.2	2	µA
I_{Q2}, Standby Supply Current, Buck Low Power Mode Enabled	Regulator Enabled, No Load		80		µA
I_{QLPM1}, Standby Supply Current, Buck Ultra Low Power Mode Enabled	Regulator Enabled, No Load, Buck ULPM = 1 & Fixed On-Time Enabled.		30		µA
$I_{LOADREG}$, Load Regulation	V_{OUT} = Default CMI Setting PWM mode.		0.05		%/A
$I_{LINEREG}$, Line Regulation	V_{IN} = 3.2V to 5.5V		0.05		%/V
P_{GOOD}, Power Good Threshold	V_{OUT} Rising,	89	92	95	%
Power Good Hysteresis	V_{OUT} Falling		3		%
OV_{FLT}, Overvoltage Threshold	V_{OUT} Rising,	109	112	115	%
Overvoltage Hysteresis	V_{OUT} Falling		3		%
Switching Frequency	FSET=00 FSET=01 FSET=10 FSET=11		1.5 2.0 2.5 3.3		MHz
T_{SS}, Soft-Start Period	10% to 90% ramp time of V_{OUT}		50 100 200 300		µs

			400 500 750 1000		
ILIM, Internal High Side Peak Current Limit per phase (Cycle-by-Cycle)	ILIMSET=00 ILIMSET=01 ILIMSET=10 ILIMSET=11		4.0 5.5 7 8.5		A
Internal High Side Peak Current Limit per phase (Cycle-by-Cycle) Tolerance	At default ILIMSET	-12.5		12.5	%
IWARN, Internal High Side Peak Current Limit Warning Threshold per phase.	Warning threshold as % of ILIM threshold	-12.5	-22.5	-32.5	%
Low Side On-Resistance, NMOS, per phase	I_{SW} = 1A, V_{IN} = 3.3V, T_J = 25°C		10		mΩ
High Side On-Resistance, PMOS, per phase	I_{SW} = 1A, V_{IN} = 3.3V, T_J = 25°C		30		mΩ
SW Leakage Current – NMOS, per phase	V_{IN} = 5V, V_{SW} = 5V, T_J = 25°C			1	µA
SW Leakage Current – PMOS, per phase	V_{IN} = 5V, V_{SW} = 0V, T_J = 25°C			1	µA
Output Pull Down Resistance	Enabled when regulator disabled, V_{OUT}=0.1V		3.35		Ω
Dynamic Voltage Scaling Rate	RANGE = 0 DVS SLEW = 00 DVS SLEW = 01 DVS SLEW = 10 DVS SLEW = 11		 11.26 5.63 2.82 1.41		mV/ µs
	RANGE = 1 DVS SLEW = 00 DVS SLEW = 01 DVS SLEW = 10 DVS SLEW = 11		 56.31 28.15 14.08 7.04		mV/ µs
C_{OUTMIN}, Minimum Output Cap	Minimum output capacitor with voltage de-rating	50			µF

BUCK 3, 4, 5 ELECTRICAL CHARACTERISTICS, REGULATOR:

(VIN_Bx = 3.8V, T_j = -40°C to +125°C, unless otherwise specified.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
VIN_BX Operating Voltage Range		2.7		AVIN	V
V_{FB_BX} Output Voltage Range	Configurable in 5mV steps, RANGE = 0 Configurable in 25mV steps, RANGE = 1	0.5 0.5		1.135 3.675	V
V_{FB_BX}, Output Voltage Accuracy	V_{OUT} = 1.0V, I_{OUT} = 1000mA (continuous PWM mode), 25°C < T_J < 85°C	-1%	V_{NOM}	1%	V
	V_{OUT} = 1.0V, I_{OUT} = 1000mA (continuous PWM mode), -40°C < T_J < 125°C	-1.5%	V_{NOM}	1.5%	V
	V_{OUT} = 1.0V, I_{OUT} = 10mA (discontinuous PFM mode), Buck ULPM = 0 (Ultra Low Power Mode Disabled), 25°C < T_J < 85°C	-1%	V_{NOM}	1%	V
	V_{OUT} = 1.0V, I_{OUT} = 10mA (discontinuous PFM mode), Buck ULPM = 0 (Ultra Low Power Mode Disabled), -40°C < T_J < 125°C	-1.5%	V_{NOM}	1.5%	V
	V_{OUT} = 1.0V, I_{OUT} = 10mA (discontinuous PFM mode operation), Buck ULPM = 1, (Ultra Low Power Mode Enabled), 25°C < T_J < 85°C	0%	V_{NOM} + 1.5%	2.5%	V
	V_{OUT} = 1.0V, I_{OUT} = 10mA (discontinuous PFM mode operation), Buck ULPM = 1, (Ultra Low Power Mode Enabled), -40°C < T_J < 125°C	0%	V_{NOM} + 1.5%	3%	V
I_{OUT}, Maximum Output Current (normal mode)	Output current, ILIM = 1	1.2			A
I_{OUT}, Maximum Output Current ULPM = 1 (Ultra Low Power Mode)		15			mA
Maximum Operation Duty Cycle		99			%
I_{SHUT}, Shutdown Current	V_{SW} = V_{IN} / 0V, Regulator Disabled, T_J = 25ºC		0.1	1	µA
I_{Q2}, Standby Supply Current, Low Power Mode Enabled	Regulator Enabled, No Load		40		µA
I_{QLPM1}, Standby Supply Current, Ultra Low Power Mode Enabled	Regulator Enabled, No Load, Buck ULPM = 1 & Fixed On-Time Enabled.		15		µA
$I_{LOADREG}$, Load Regulation	V_{OUT} = Default CMI Setting PWM mode.		0.05		%/A
$I_{LINEREG}$, Line Regulation	V_{IN} = 3.2V to 5.5V		0.05		%/V
P_{GOOD}, Power Good Threshold	V_{OUT} Rising,	89	92	95	%
Power Good Hysteresis	V_{OUT} Falling		3		%
OV_{FLT}, Overvoltage Threshold	V_{OUT} Rising,	109	112	115	%
Overvoltage Hysteresis	V_{OUT} Falling		3		%
Switching Frequency	SWFREQ = 00 SWFREQ = 01 SWFREQ = 10 SWFREQ = 11		1.5 2.0 2.5 3.3		MHz

T_{SS}, Soft-Start Period	10% to 90% ramp time of V_{OUT}		50 100 200 300 400 500 750 1000		µs
ILIM, Internal High Side Peak Current Limit (Cycle-by-Cycle)	ILIMSET=0 ILIMSET=1		2.0 3.0		A
Internal High Side Peak Current Limit (Cycle-by-Cycle) Tolerance	At default ILIMSET	-12.5		12.5	**%**
IWARN, Internal High Side Peak Current Limit Warning Threshold.	Warning threshold as % of ILIM threshold	-12.5	-22.5	-32.5	%
Low Side On-Resistance, NMOS	I_{SW} = 0.5A, V_{IN} = 3.3V, T_J = 25°C		45		mΩ
High Side On-Resistance, PMOS	I_{SW} = 0.5A, V_{IN} = 3.3V, T_J = 25°C		80		mΩ
SW Leakage Current – NMOS	V_{IN} = 5V, V_{SW} = 5V, T_J = 25°C			1	µA
SW Leakage Current – PMOS	V_{IN} = 5V, V_{SW} = 0V, T_J = 25°C			1	µA
Output Pull Down Resistance	Enabled when regulator disabled, V_{OUT}=0.1V		6.7		Ω
Dynamic Voltage Scaling Rate	RANGE = 0 DVS SLEW = 00 DVS SLEW = 01 DVS SLEW = 10 DVS SLEW = 11		11.26 5.63 2.82 1.41		mV/ µs
	RANGE = 1 DVS SLEW = 00 DVS SLEW = 01 DVS SLEW = 10 DVS SLEW = 11		56.31 28.15 14.08 7.04		mV/ µs
C_{OUTMIN}, Minimum Output Cap	Minimum output capacitor with voltage de-rating	12			µF

BUCK-BOOST 6, 7 ELECTRICAL CHARACTERISTICS, REGULATOR:

(VIN_Bx = 3.8V, T_j = -40°C to +125°C, unless otherwise specified.)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IN_Bx}, x = 6, 7, Buck-Boost Operating Input Voltage		2.7		AVIN	V
Output Voltage Range	Configurable in 25mV steps, Buck-Boost Mode	1.8		5.0	V
	Configurable in 25mV steps, Buck Mode	0.8		3.6	V
V_{BBST_STEP}, Output Step Size			25		mV
V_{BBST_ACC}, Output Voltage Accuracy	V_{OUT} = 3.3V, (continuous PWM mode), 25°C < T_J < 85°C	-1.5%	V_{NOM}	1.5%	V
	V_{OUT} = 3.3V, (continuous PWM mode), -40°C < T_J < 125°C	-2%	V_{NOM}	2%	V
	V_{OUT} = 3.3V, I_{OUT} = 10mA (discontinuous PFM mode), 25°C < T_J < 85°C	-2%	V_{NOM}	2%	V
	V_{OUT} = 3.3V, I_{OUT} = 10mA (discontinuous PFM mode), -40°C < T_J < 125°C	-3%	V_{NOM}	3%	V
V_{BUCK_ACC}, Output Voltage Accuracy	V_{OUT} = 1.8V, I_{OUT} = 500mA (continuous PWM mode), 25°C < T_J < 85°C	-1%	V_{NOM}	1%	V
	V_{OUT} = 1.8V, I_{OUT} = 500mA (continuous PWM mode), -40°C < T_J < 125°C	-1.5%	V_{NOM}	1.5%	V
	V_{OUT} = 1.8V, I_{OUT} = 10mA (discontinuous PFM mode), 25°C < T_J < 85°C	-1.5%	V_{NOM}	1.5%	V
	V_{OUT} = 1.8V, I_{OUT} = 10mA (discontinuous PFM mode), -40°C < T_J < 125°C	-2%	V_{NOM}	2%	V
Line Transient	V_{OUT} = 3.3V, VIN = 3.0V to 4.2V, 0.1V/us		±5%		
	V_{OUT} = 1.8V, VIN = 3.0V to 4.2V, 0.1V/us		±5%		
I_{OMAX}, Maximum Allowable Continuous Output Current	V_{IN_Bx} = 3.3V, V_{OUT} = 3.3V, L = 1µH	1			A
	V_{IN_Bx} = 3.3V, V_{OUT} = 5.0V, L = 1µH	0.6			A
	V_{IN_Bx} = 3.3V, V_{OUT} = 1.8V, L = 1µH	1.8			A
I_{Q1BB}, Supply Current	V_{IN_Bx} = 3.3V, V_{OUT} = 103% of V_{OUT_NOM}, Buck-Boost Mode		200		µA
I_{SHUT}, Shutdown Current	Regulator Disabled			1	µA
ISWA_Bx_LEAK, Leakage from SWA_Bx	SWA_Bx = 0V, VIN_Bx = 3.3V, TJ = 25°C			1.5	µA
	SWA_Bx = 3.3V, VIN_Bx = 3.3V, TJ = 25°C			1.5	µA
ISWB_Bx_LEAK, Leakage from SWB_Bx	SWB_Bx = 0V, VIN_Bx = 3.3V, TJ = 25°C			1.5	µA
	SWB_Bx = 3.3V, VIN_Bx = 3.3V, FB_Bx = 3.3V, TJ = 25°C			1.5	µA
$I_{LOADREG}$, Load Regulation	V_{OUT} = Default CMI Setting PWM mode.		0.1		%/A
$I_{LINEREG}$, Line Regulation	V_{IN} = 3.2V to 5.5V		0.15		%/V
P_{GOOD}, Power Good Threshold	V_{OUT} Rising	89	92	95	%
Power Good Hysteresis	V_{OUT} Falling		3		%
OV_{FLT}, Overvoltage Threshold	V_{OUT} Rising	109	112	115	%
Overvoltage Hysteresis	V_{OUT} Falling		3		%
F_{SWBB}, Switching Frequency, CCM - Continuous Conduction Mode.	Frequency V_{IN_Bx} = 3.3V, V_{OUT} = 3.3V		2		MHz

$T_{BBMINON}$, SW5 and SW6 Minimum On-time	Note 2		125		ns
T_{SS}, Soft-Start Period	10% to 90% ramp time of V_{OUT}		500 1000 2000 3000		µs
$ILIM_{CBC}$, Cycle-by-Cycle Current Limit	ILIM set = 00, Boost Mode		1.7		A
	ILIM set = 01, Boost Mode		2.1		A
	ILIM set = 10, Boost Mode		2.5		A
	ILIM set = 11, Boost Mode		3.2		A
$ILIM_{SHUT}$, Current Limit for Shutdown	% compared to cycle-by-cycle Current Limit. Buck-Boost region		140		%
	% compared to cycle-by-cycle Current Limit. Buck region or Boost region	110	122	135	%
Current Limit, Warning	% compared to cycle-by-cycle Current Limit.	70	80	90	%
HS1 PMOS FET On-Resistance	I_{SW3} = 0.2A, V_{IN_Bx} = 3.3V		75		mΩ
HS2 NMOS FET On-Resistance	I_{SW3} = 0.2A, V_{IN_Bx} = 3.3V		70		mΩ
LS1 PMOS FET On-Resistance	I_{SW4} = 0.2A, V_{IN_Bx} = 3.3V		75		mΩ
LS2 NMOS FET On-Resistance	I_{SW4} = 0.2A, V_{IN_Bx} = 3.3V		70		mΩ
Output Pull Down Resistance	Buck - Boost Disabled		10		Ω
C_{OUTMIN}, Minimum Output Cap	Minimum output capacitance with voltage de-rating	12			µF

LDO 1, 2 ELECTRICAL CHARACTERISTICS

(VINLx = 3.8V, T_j = -40°C to +125°C, unless otherwise specified.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
Operating Voltage Range	AVIN Voltage	2.7		5.5	V
V_{INLX}, Operating Input Voltage		1.08		AVIN	V
V_{LDOX}, Output Voltage Range	Configurable in 12.5mV steps, RANGE = 0 Configurable in 50mV steps, RANGE = 1	0.5 1.2		1.2875 3.6	V
Output Voltage Accuracy	At Default CMI Output Setting, LPM = 0	-3	V_{NOM}	3	%
	At Default CMI Output Setting, LPM = 1 (Low Power Mode is Enabled)	-3	V_{NOM}	3	%
Line Regulation	V_{INLX} – V_{LDOX} > 400mV AVIN > 3.3V, I_{OUT} = 10mA			0.25	% / V
Load Regulation	V_{INLX} – V_{LDOX} > 400mV AVIN > 3.3V, I_{OUT} = 10mA to 200mA			0.25	% / A
I_{Q1}, Supply Current	Regulator Enabled, VOUT > 1.0V, No Load		160		µA
I_{Q1}, Supply Current	Regulator Enabled, VOUT < 1.0V, No Load		52		µA
I_{SD}, Shut Down Current	Regulator Disabled, T_J = 25ºC			1	µA
I_{OUT} Maximum Output Current	LPM = 0 (normal mode)	200			mA
I_{LIM}, Output Current Limit	LPM = 0 (normal mode)	210	252		mA
I_{SHORT}, Shorted Output Foldback Current			30		%
V_{DO}, Drop Out Voltage	I_{OUT} = 150mA, AVIN – V_{OUTL} > 2.0V			150	mV
Soft-Start Period	LDO_SS=1, Default V_{OUTL}, 10% to 90%		320	500	µs
	LDO_SS=0, Default V_{OUTL}, 10% to 90%		160	250	µs
Power Good Threshold	VLDO1 Rising, % of V_{NOM}	89	92	95	%
Power Good Hysteresis	VLDO1 Falling, % of V_{NOM}		3		%
Overvoltage Fault Threshold	VLDO1 Rising, % of V_{NOM}	109	112	115	%
Overvoltage Fault Hysteresis	VLDO1 Falling, % of V_{NOM}		3		%
PSRR, Power Supply Rejection Ratio	f = 1kHz, I_{OUT} = 10mA, V_{OUTL} = 0.8V, V_{INL1} = 1.2V, LPM=0		75		dB
	f = 10kHz, I_{OUT} = 10mA, V_{OUTL} = 0.8V, V_{INL1} = 1.2V, LPM=0		65		dB
	f = 100kHz, I_{OUT} = 10mA, V_{OUTL} = 0.8V, V_{INL1} = 1.2V, LPM=0		55		dB
	f = 2000kHz, I_{OUT} = 10mA, V_{OUTL} = 0.8V, V_{INL1} = 1.2V, LPM=0		40		dB
V_{LTR}, Transient Response	I_{OUT} 10mA to 250mA in 10us, V_{OUTL} = 1.8V, V_{INL} = 2.7V		1	2.5	%
Discharge Resistance	On When regulator disabled, VOUT = 0.1V		9.4		Ω

Allowable Output Capacitance (Effective)	Effective capacitance after voltage derating	1.5		10	µF

LDO 3, 4, 5, 6 ELECTRICAL CHARACTERISTICS (LSW MODE = 0 FOR LDOX)

(VINLx = 3.8V, T_j = -40°C to +125°C, unless otherwise specified.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
Operating Voltage Range	AVIN Voltage	2.7		5.5	V
V_{INLX}, Operating Input Voltage		1.62		AVIN	V
V_{LDOX}, Output Voltage Range	Configurable in 12.5mV steps, RANGE = 0 Configurable in 50mV steps, RANGE = 1	0.5 1.2		1.2875 3.6	V
Output Voltage Accuracy	At Default CMI Output Setting, LPM = 0	-1	V_{NOM}	1	%
	At Default CMI Output Setting, LPM = 1 (Low Power Mode is Enabled)	-3	V_{NOM}	3	%
Line Regulation	V_{INLX} – V_{LDOX} > 400mV AVIN > 3.3V, I_{OUT} = 10mA			0.25	% / A
Load Regulation	V_{INLX} – V_{LDOX} > 400mV AVIN > 3.3V, I_{OUT} = 10mA to 400mA			0.25	% / A
I_{Q1}, Supply Current	Regulator Enabled, Normal Mode		15	25	µA
I_{SD}, Shut Down Current	Regulator Disabled, T_J = 25ºC			1	µA
I_{OUT} Maximum Output Current	LPM = 0 (normal mode), 2.7V < VINLX	400			mA
	LPM = 0 (normal mode), 1.62V < VINLX < 2.7V	300			mA
I_{LIM}, Output Current Limit	LPM = 0 (normal mode), Range = 0, 2.7V < VINLX	410			mA
	LPM = 0 (normal mode), Range = 0, 1.62V < VINLX < 2.7V	310			mA
I_{SHORT}, Shorted Output Foldback Current			30		%
V_{DO}, Drop Out Voltage	I_{OUT} = 150mA, V_{INL} > 2.7V			150	mV
	I_{OUT} = 300mA, V_{INL} > 2.7V			300	mV
Soft-Start Period	LDO_SS=1, Default V_{OUTL}, 10% to 90%		320	500	µs
	LDO_SS=0, Default V_{OUTL}, 10% to 90%		160	250	µs
Power Good Threshold	VLDO1 Rising, % of V_{NOM}	89	92	95	%
Power Good Hysteresis	VLDO1 Falling, % of V_{NOM}		3		%
Overvoltage Fault Threshold	VLDO1 Rising, % of V_{NOM}	109	112	115	%
Overvoltage Fault Hysteresis	VLDO1 Falling, % of V_{NOM}		3		%
PSRR, Power Supply Rejection Ratio	f = 1kHz, I_{OUT} = 10mA, V_{OUTL} = 0.8V, V_{INLx} = 2.7V, LPM=0		70		dB
	f = 10kHz, I_{OUT} = 10mA, V_{OUTL} = 0.8V, V_{INLx} = 2.7V, LPM=0		60		dB
	f = 100kHz, I_{OUT} = 10mA, V_{OUTL} = 0.8V, V_{INLx} = 2.7V, LPM=0		40		dB
	f = 2000kHz, I_{OUT} = 10mA, V_{OUTL} = 0.8V, V_{INLx} = 2.7V, LPM=0		20		dB

V_{LTR}, Transient Response	I_{OUT} 10mA to 250mA in 10us, V_{OUTL} = 1.8V, V_{INL} = 2.7V		2.7		%
Discharge Resistance	On When regulator disabled, VOUT = 0.1V		9.4		Ω
Allowable Output Capacitance (Effective)	Effective capacitance after voltage derating	0.8		10	µF

LDO 3, 4, 5 ELECTRICAL CHARACTERISTICS – LOAD SWITCH

(AVIN = 3.8V, T_j = -40°C to +125°C, unless otherwise specified.)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Load Switch Operation Range	AVIN (Input Voltage)	2.7		AVIN	V
PMOS On-Resistance			200		mΩ
Internal PMOS Current Detection	Triggers Interrupt on nIRQ Pin	330	500		mA
Internal PMOS Current Detection De-glitch Time			10		µs
Load Switch Supply Current	PLSW Mode. Load Switch Enabled. No Load, normal power mode (Option no OV protection)		9		µA
	Load Switch Disabled		0.1	1	
Output Current Limit	@Current Foldback & VINL – VOUT = 0.7V, LDOx_ILIM = 0 @Current Foldback & VINL – VOUT = 0.7V, LDOx_ILIM = 1	0.3 0.4	0.45 0.55		A
Internal PMOS Current Shutdown De-glitch Time			5		µs
Internal PMOS Current Shutdown Off time (Retry time)			14		ms
Internal PMOS Soft start	Only used with 3.3V Input, Cout = 1uF, Default Setting ISS [1:0] = 00.		10		mV/ µs
OV Deglitch Time			45		µs

LSW 6, 7, 8 ELECTRICAL CHARACTERISTICS – LOAD SWITCH

(AVIN = 3.8V, T_j = -40°C to +125°C, unless otherwise specified.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
Operating Voltage Range	AVIN Voltage	2.7		5.5	V
V_{INLX}, Operating Input Voltage		0.5		3.3	V
Output Current Capability	$V_{LDOX} < V_{INLX}$ – 0.25V, Note [1]	1.5			A
Current Limit Shutdown		2			A
Current Limit Shutdown deglitch time	Minimum time for current limit signal to be valid.	10			µs
On Resistance (T_J = 25°C)	V_{INLX} = 1.2V, I_{LSX} = 250mA, AVIN= 3.8V to 5.0V		12		mΩ
	V_{INLX} = 1.8V, I_{LSX} = 250mA, AVIN= 3.8V to 5.0V		18.5		mΩ
	V_{INLX} = 3.3V, I_{LSX} = 250mA, AVIN= 3.8V to 5.0V		52		mΩ
Soft start time	V_{INLSX} = 1.2V, AVIN = 3.8V, V_{OUTLSX} 10 – 90%		160		µs
Output Discharge Resistance	LSW6 On When regulator disabled		9.4		Ω
	LSW7/8, AVIN = 3.6V, V_{OUTLS1} = 0.1V.		25		Ω
Startup Delay	Time from Enable to Power Good (PG/ POK)		250		µs
I_{Q1}, Total Current Condition 1	AVIN=3.8V, V_{INL}=1.2V, I_{SYS}+I_{VINLS1} with no load current, Current Limit Enabled, LPM = 0		100		µA
I_{SD}, Disable Current	Load Switch Disabled, T_J = 25ºC			1	µA

LDO 9 ELECTRICAL CHARACTERISTICS

(VINL9 = 3.8V, T_j = -40°C to +125°C, unless otherwise specified.)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Operating Voltage Range	AVIN	2.7		AVIN	V
Output Voltage Range		1.2		3.6	V
Maximum Output Current		30			mA
Output Voltage Accuracy	Iout = 5mA, VIN >= VOUT + 0.25V	-3	V_{NOM}	3	%
Line Regulation	Δ(VOUT)/VIN I_{OUT} = 5mA		0.6		%
Load Regulation	Δ(VOUT)/IOUT I_{OUT} = 0.1mA to 20mA		0.6		%
Dropout Voltage	I_{OUT} = 5mA		150	250	mV
Supply Current	I_{OUT} = 0mA		5		µA
Current Limit	V_{OUT} = 95% of the regulation voltage	30	40		mA

LDO 10 ELECTRICAL CHARACTERISTICS

(VINL10 = 3.8V, T_j = -40°C to +125°C, unless otherwise specified.)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Operating Voltage Range	AVIN	2.7		AVIN	V
Output Voltage Range		1.2		3.6	V
Maximum Output Current		15			mA
Output Voltage Accuracy	Iout = 5mA, VIN >= VOUT + 0.25V	-3	V_{NOM}	3	%
Line Regulation	Δ(VOUT)/VIN I_{OUT} = 5mA		0.6		%
Load Regulation	Δ(VOUT)/IOUT I_{OUT} = 0.1mA to 20mA		0.6		%
Dropout Voltage	I_{OUT} = 5mA		150	250	mV
Supply Current	I_{OUT} = 0mA		5		µA
Current Limit	V_{OUT} = 95% of the regulation voltage	16	20		mA

I²C INTERFACE ELECTRICAL CHARACTERISTICS

(AVIN = 3.8V, T_j = -40°C to +125°C, unless otherwise specified.)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
SCL, SDA Input Low	AVIN = 3.3V			0.4	V
SCL, SDA Input High	AVIN = 3.3V	1.05			V
SDA Leakage Current	SDA=5V			1	µA
SDA Output Low	I_{OL} = 5mA			0.35	V
SCL Clock Frequency, f_{SCL}		0		3400	kHz
SCL Low Period, t_{LOW}		0.125			µs
SCL High Period, t_{HIGH}		0.100			µs
SDA Data Setup Time, t_{SU}		10			ns
SDA Data Hold Time, t_{HD}	(Note1)	0			ns
Start Setup Time, t_{ST}	For Start Condition	65			ns
Stop Setup Time, t_{SP}	For Stop Condition	65			ns
Capacitance on SCL or SDA Pin				10	pF
SDA Rise Time SDA, T_r	Device requirement			30	ns
SDA Fall Time SDA, T_f	Device requirement			30	ns
Pulse Width of spikes must be suppressed on SCL and SDA		0		50	ns

Note1: Comply to I²C timings for 3.4MHz operation - “Fast Mode Plus”.

Note2: No internal timeout for I²C operations, however, I²C communication state machine will be reset when entering RESET, IDLE, OVUVFLT, and THERMAL states to clear any transactions that may have been occurring when entering the above states.

Note3: This is an I²C system specification only. Rise and fall time of SCL & SDA not controlled by the device.

Note4: Device Address is 7’h5A

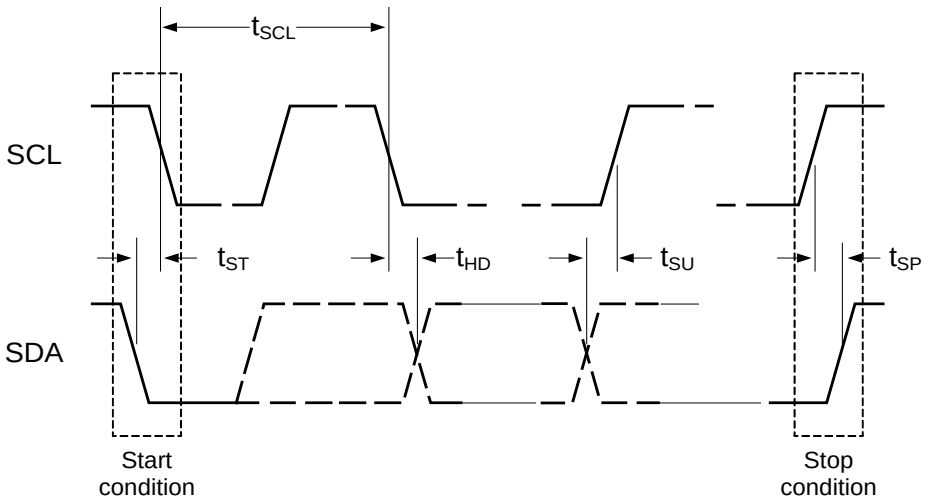


Figure 5: I2C Data Transfer

SYSTEM CONTROL INFORMATION

General

The QP8817 is a highly integrated PMIC that is designed to be flexible and work with many system controllers and processors. It combines seven switching regulators and a combination of ten linear regulators (LDO) and load switches (LSW) into a small form factor package. The switching regulators' high frequency minimizes the inductor size and reduces the overall solution size. The PMIC also integrates a master controller that provides startup sequencing to both the integrated power supplies and external regulators. The master controller manages startup and power-off sequencing, timing, voltages, slew rates, sleep states (Low Power Modes or LPM), and fault conditions. I²C configurability allows system level changes without the need for costly PCB changes.

The QP8817 contains five Buck regulators. Two Buck regulators can support 5A average and 6A peak current; three Bucks support 1.5A and 2A peak current. The QP8817 Buck regulators are optimized to work with 0.22 ~ 0.47µH inductors. The regulators are designed for high efficiency and high current for microprocessor core supply voltages that are typically below 1.0V. The regulators are fully compensated internally and require just the inductor and output capacitor for operation. Buck1/2 can be operated in parallel to supply a 12A load.

In addition, QP8817 has two Buck-Boost switching regulators that can support 1.5A output current. Each Buck-Boost regulator has four integrated FETs that can regulate the output to be lower, higher, or equal to input voltage.

LDO1 and LDO2 are 200mA LDOs with high PSRR. LDO3, LDO4, and LDO5 are general-purpose LDOs that support up to 400mA of output current. These LDOs can be configured as load switches as well. LSW6, LSW7, and LSW8 are 1.5A low R_{ON} load switches. In addition, QP8817 also has two low quiescent current LDOs. LDO9 can support up to 30mA, and LDO10 can support up to 15mA output currents.

The QP8817 has ten integrated GPIO pins. The GPIO pins are highly configurable and typically can be configured either as an input or output pin. The GPIO output drive, open drain or push-pull, and voltage level are configurable. Each GPIO can be configured for several different functions such as power good signals, interrupt requests, fault monitoring, sequencing, and controlling external regulators, LED drivers, Dynamic voltage scaling, Low Power Modes LPM entry and exit etc.

Many of the QP8817s functions are configurable. The IC's default functionality is defined by the default CMI (Code Matrix Index), but much of this functionality can be changed via I²C. The first part of the datasheet describes basic IC functionality and default pin functions. The end of the datasheet provides the configuration and functionality specific to each CMI version. Contact sales@qorvo.com for additional information about other configurations.

I²C Serial Interface

To ensure compatibility with a wide range of systems, the QP8817 uses standard I²C commands. The QP8817 always operates as a slave device and is addressed using a 7-bit slave address followed by an eighth bit, which indicates whether the transaction is a read-operation or a write-operation. Refer to each specific CMI for the IC's slave address.

The IC contains two sets of configurable I²C addresses. Master, GPIOs, Buck 1-5 operate from one I²C address and the rest of the regulators have a different I²C address.

The I2C addresses can be set by the external resistor on the ADD pin.

There is no timeout function in the I²C packet processing state machine, however, any time the I²C state machine receives a start bit command, it immediately resets the packet processing, even if it is in the middle of a valid packet.

I²C commands are communicated using the SCL and SDA pins. SCL is the I²C serial clock input. SDA is the data input and output. SDA is open drain and must have a pullup resistor. Signals on these pins must meet timing requirements in the Electrical Characteristics Table.

Table 1: QP8817 I²C Addresses

ADD Pin Resistance	I2C Address 7bit	7bit Adds	8-bit write	8-bit read
	(MSTR+BK1,3+BB1, LDO85, LDO12)			
Float	0x67h	110 0111b	0xCEh	0xCFh
200k +/-7.5%	0x6Bh	110 1011b	0xD6h	0xD7h
100k +/-7.5%	0x62h	110 0010b	0xC4h	0xC5h
51k +/-7.5%	0x64h	110 0100b	0xC8h	0xC9h
	(Remain tiles)			
Float	0x68h	110 1000b	0xD0h	0xD1h
200k +/-7.5%	0x6Ch	110 1100b	0xD8h	0xD9h
100k +/-7.5%	0x63h	110 0011b	0xC6h	0xC7h
51k +/-7.5%	0x65h	110 0101b	0xCAh	0xCBh

I2C Registers

The QP8817 has an array of internal registers that contain the IC's basic instructions for setting up the IC configuration, output voltages, switching frequency, fault thresholds, fault masks, etc. These registers give the IC its operating flexibility. The two types of registers are described below.

Basic Volatile – These are R/W (Read and Write) and RO (Read only). After the IC is powered, the user can modify the R/W register values to change IC functionality. Changes in functionality include things like masking certain faults. The RO registers communicate IC status such as fault conditions. Any changes to these registers are lost when power is recycled. The default values are fixed and cannot be changed by the factory or the end user.

Basic Non-Volatile – These are R/W and RO. After the IC is powered, the user can modify the R/W register values to change IC functionality. Changes in functionality include things like output voltage settings, startup delay time, and current limit thresholds. Any changes to these registers are lost when power is recycled. The default values can be modified at the factory to optimize IC functionality for specific applications. Please contact Qorvo for custom options and minimum order quantities.

When modifying only certain bits within a register, take care to not inadvertently change other bits. Inadvertently changing register contents can lead to unexpected device behavior.

State Machine

The QP8817 contains three independent state machines. Each state machine includes startup, low power modes, operating, and fault modes. One of the key features is the SLEEP and DPSLP states which are two configurable states that allow the user to optimize their system for low-power modes. The output voltages can be adjusted or turned off to achieve the lowest system-level power consumption. These states can be entered and exited with GPIOs and I^{2}C commands. Each of the three state machines is defined by the factory-configured CMI and cannot be changed by the user.

The QP8817 can be configured to operate in either the PWREN, PWRON, or Push Button state machines. Only one mode of operation is allowed. Only one of the three modes of operation is allowed in any IC. The details of the PWREN mode, the PWRON mode of operation and the Push Button mode of operation can be seen in the separate state diagrams illustrated below. The state diagrams show the different states possible within each mode of operation.

PWREN State Machine

The PWREN state machine allows the IC to automatically startup when input power is applied. After the outputs are turned on per the programmed startup sequence, either an I^{2}C command or the PWREN pin can be used to move the IC to the DPSLP state.

PWRON State Machine

The PWRON state machine is very similar to PWREN with two main differences. The outputs do not automatically turn on unless the PWRON pin is pulled high. The PWRON pin is used as an enable input in the PWRON state machine. Also, the PWRON pin cannot be used to move the state machine into the DPSLP state, but another GPIO or an I^{2}C command can be used to enter and exit DPSLP mode.

Push Button State Machine

The Push Button state machine uses the nPB pin to control the outputs turn on and turn off. The nPB input pin is a unique, multi-function push button input. Refer to the nPB pin functionality for more details.

In any states, as long as the Push Butten is push-hold for more than 8s, the PMIC will enter power cycle where all the outputs will be turned off and start again as in the configured sequence.

RESET State

In the RESET, or "cold" state, the QP8817 is waiting for the input voltage on AVIN to be within a valid range defined by the AVIN_UV and AVIN_OV thresholds. All volatile registers are reset to defaults and Non-Volatile registers are reset to programmed defaults. The IC transitions from RESET to the VROFF (PWRON configuration) or POWER SEQUENCE START (PWREN configuration) state when the input voltage is in the correct operating range.

The IC transitions from any other state to RESET if the input voltage drops below the UVLO threshold voltage. It is important to note any transition to RESET returns all volatile and non-volatile registers to their default states.

VROFF State

The VROFF state is only used in the PWRON configuration. The IC enters VROFF from RESET when VIN rises above UVLO or falls below OVLO. It also enters VROFF when the PWRON pin is de-asserted. When entring the VROFF state using the PWRON pin, the IC can be configured to the register settings as-is, or it can be configured to reset them to their default settings. This is a stable state (not transitional state) where the IC waits for a GPIO input trigger to start sequencing on the output. When it receives this trigger, it transitions to the

POWER SEQUENCE START state. The IC returns to this state to turn off all the regulators if the PWRON pin is de-asserted at any time during operation. The IC then turns of all the regulators in proper order and waits in the VROFF state for the trigger to restart. If the IC is in the VROFF state and the input voltage drops below the UV threshold or goes over the OV threshold, the IC moves to the RESET state from this state. I²C is active in this state.

POWER SEQUENCE START State

The POWER SEQUENCE START state is a transitional state while the regulators are starting. The outputs are enabled and are starting up in this state. Depending on the IC's configuration and GPIO inputs, it immediately transitions to the POWER ON, SLEEP, or DPSLP states states when the regulators go into regulation.

The QP8817 fault mask bits ILIM_FLTMSK, ILIM_WARN_FLTMSK, OV_FLTMSK and UV_FLTMSK default to 1 at startup, so if one regulator has a fault at startup, all other regulators still turn on.

POWER ON (Active) State

The ACTIVE state is the normal operating state when the input voltage is within the allowable range, all outputs are turned on, and no faults are present. The IC only enters the ACTIVE State from the POWER SEQUENCE START State with the PWREN and nPB configurations. It enters from the VROFF State in the PWRON configuration.

SLEEP State

The SLEEP state is a configurable low power state. Based on the system's low power operational requirements, the user can configure the SLEEP state by defining which internal and external regulators are kept on or turned off during the SLEEP state. Buck1/2/7 can be programmed to be either ON or OFF. Buck3/4/5/6 can be programmed to be either ON, OFF, or regulate to one of its two VSETx register values. The VSETx registers effectively provide a dynamic voltage scaling (DVS) function. The LDOs can be programmed to be either ON or OFF. The regulators follow their programmed sequencing delay times when turning on or off as they exit or enter the SLEEP state.

The IC can enter SLEEP state via the I²C register SLEEP bit or by a GPIO input. Figure 3 shows how the NVM SLEEP_MODE factory bit sets the I²C and GPIO requirements to enter and exit the SLEEP state.

When the I²C bit SLEEP_MODE = 0, the IC enters SLEEP State with the logical AND of the I²C SLEEP bit and the GPIOs. If more than one GPIO is configured as a SLEEP State input, then all the GPIOs must be asserted. If no GPIOs are configured to control the SLEEP State, then only the SLEEP bit controls SLEEP State entry and exit. The IC immediately exits the SLEEP State when the SLEEP bit or a GPIO is de-asserted.

When the I²C bit SLEEP_MODE = 1, the IC enters SLEEP State with the logical OR of the I²C SLEEP bit and the GPIOs. If no GPIOs are configured to control the SLEEP state, then only the SLEEP bit controls the SLEEP State. The IC exits SLEEP State when both I²C and GPIO are de-asserted.

If the OK_START bit is cleared to 0 within 512ms after the IC exits Sleep state, the IC turns off and the POWER_OFF bit is set. The OK_START bit should not be cleared to 0 until at least 538ms after the IC exits SLEEP mode. 538ms includes a 5% tolerance buffer across temperature and process.

If a fault occurs within 500 ms after the IC exits SLEEP mode and causes nRESET to go low, and it does not clear after the the 500 ms duration ends, the POWER_OFF bit will be set to 1.

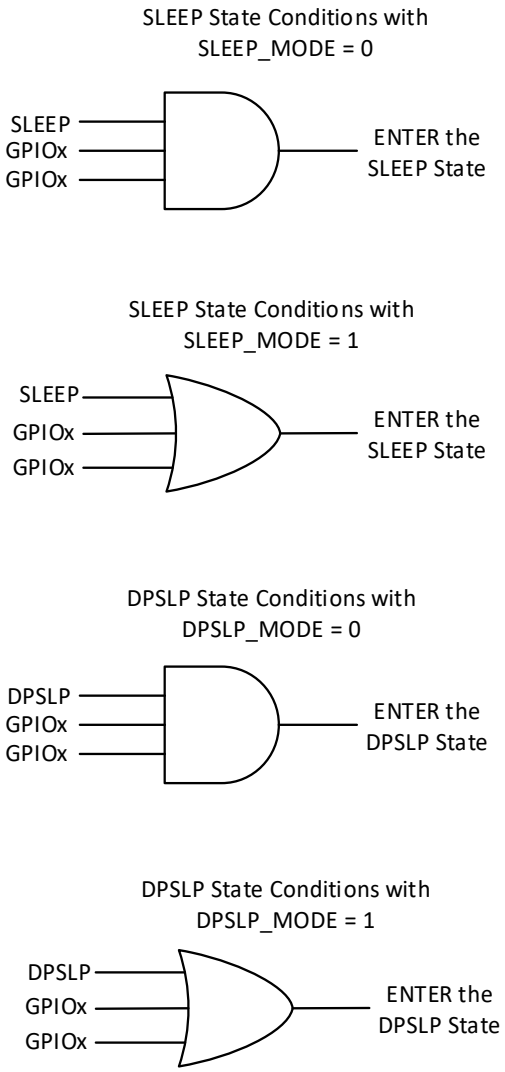


Figure 3. SLEEP and DPSLP State Truth Tables

DPSLP State

The DPSLP State is another low power operating mode for the operating system. It is intended to be used in a lower power configuration than the SLEEP state. It is identical to the SLEEP state, but DPSLP uses slightly different configurations to enter and exit this mode. Buck1/2/7 can be programmed to be either ON or OFF. Buck3/4/5/6 can be programmed to be ON, OFF, or regulate to one of its VSETx register voltages (the DVS function). The LDOs can be programmed to be either ON or OFF.

The DPSLP state programming or configuration can be different and independent from the SLEEP state programming. Each output can be programmed to have different functionality between the SLEEP and DPSLP states. The outputs follow their programmed sequencing delay times when turning on or off as they enter or exit the DPSLP state. The IC can enter DPSLP state via the I²C register DPSLP bit or by a GPIOs input. Figure 3 shows how the NVM DPSLP factory bit sets the I²C and GPIO requirements to enter and exit the DPSLP state.

Any GPIO can be configured to control the DPSLP state without requiring an I²C command. This GPIO hardware function is called PWREN

The PWREN pin activates DPSLP State in one of two ways. The PWREN function can be configured to be either edge triggered or level triggered. The difference between these configurations only affects DPSLP Mode at power up.

Level triggered: If PWREN is low at startup, the IC enters DPSLP immediately after VIN goes above the UV threshold. Pulling PWREN high exits DPSLP.

Edge triggered: If PWREN is low at startup, the IC ignores PWREN and starts up normally. PWREN must be pulled high and then pulled low to generate a negative going edge to enter DPSLP Mode. If PWREN is high at startup, the IC starts up normally and then immediately enters DPSLP Mode when PWREN is pulled low.

Like the SLEEP state, an NVM factory bit DPSLP_MODE sets the logic OR or AND logic between I²C and GPIOs for entering and exiting the DPSLP state.

When DPSLP_MODE = 0, the IC enters DPSLP State with the logical AND of the I²C DPSLP bit and the GPIOs. If more than one GPIO is configured as a DPSLP State input, then all the GPIOs must be asserted. If no GPIOs are configured to control the DPSLP State, then only the DPSLP bit controls DPSLP State entry and exit. The IC immediately exits the DPSLP State when the DPSLP bit or a GPIO is de-asserted.

When the I²C bit DPSLP_MODE = 1, the IC enters DPSLP State with the logical OR of the I²C DPSLP bit and the GPIOs. If no GPIOs are configured to control the DPSLP state, then only the DPSLP bit controls the DPSLP State. The IC exits DPSLP State when both I²C and GPIO are de-asserted.

GPIOs can also be programmed to individually turn one or multiple outputs on and off. This on/off GPIO functionality in addition to the PWREN functionality. It provides a wide range of configurability for setting different DPSLP on/off patterns. Note that the GPIOs have four delay time options for both the rising and falling edges. These settings are 0ms, 1ms, 2ms, and 4ms.

For example, in SSD applications, the host can use these GPIOs and PWREN to enter different power save modes like PS3.5 and PS4.

In video applications, the GPIOs can be connected to sensor inputs to trigger the IC to exit the DPSLP mode when a sensor input triggers. The GPIO polarity can be programmed as active HIGH or LOW. GPIOs also have a programmable 0ms, 1ms, 2ms, and 4ms deglitch times.

Note that if an OV, UV, or THERMAL fault occurs when in DPSLP state, the PMIC transitions to the appropriate fault state and then transitions to the POWER ON state when the fault clears.

THERMAL State

In the THERMAL state, the IC has exceeded the thermal shutdown temperature. The IC shuts down all regulators and asserts the nRESET pin low to protect the IC in this condition. The THERMAL interrupt can be masked by setting register 0x01h bit 5 (TMSK) = 1. Note that thermal shutdown fault bit, TWARN, still provides the thermal status even if TMSK = 1. The THERMAL state can be disabled by setting register DIS_OTS in Factory level to 1.

OVUVFLT State

If one of the regulators exceed an OV or UV level at any time after the soft start ramp has completed, and the corresponding OV_FLTMSK or UV_FLTMSK volatile bits are set to low, the IC moves to UVOVFLT state. In this state, all regulators shutdown and the IC asserts the nRESET pin. After entering the OVUVFLT state, the IC stays there for 100ms and then goes back to the ACTIVE state. If the OV or UV condition still exists in the ACTIVE state, the IC returns to the OVUVFLT state. The cycle continues until the OV or UV fault is removed, or the input power is removed. The IC does not directly enter OVUVFLT in an overcurrent condition but does enter this state due to the resulting UV condition.

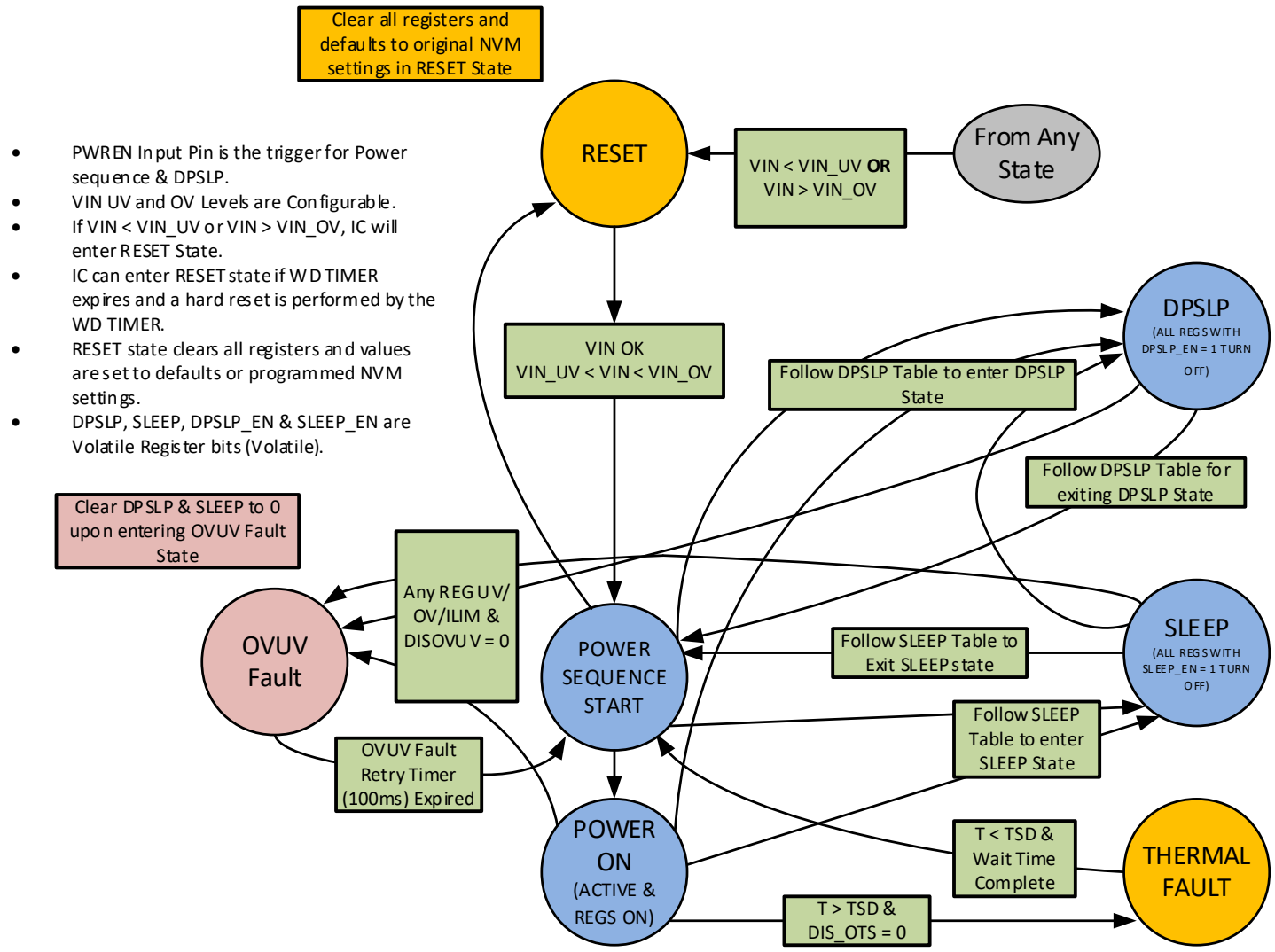


Figure 4: PWREN State Machine

- GPIO 6 can be used as the PWRON Input.
- VIN UV and OV Levels are Configurable.
- If VIN < VIN_UV or VIN > VIN_OV, IC will enter RESET State.
- IC can enter RESET state if WD TIMER expires and a hard reset is performed by the WD TIMER.
- RESET state clears all registers and values are set to defaults or programmed NVM settings.
- DPSLP, SLEEP, DPSLP_EN & SLEEP_EN are Volatile Register bits (Volatile).

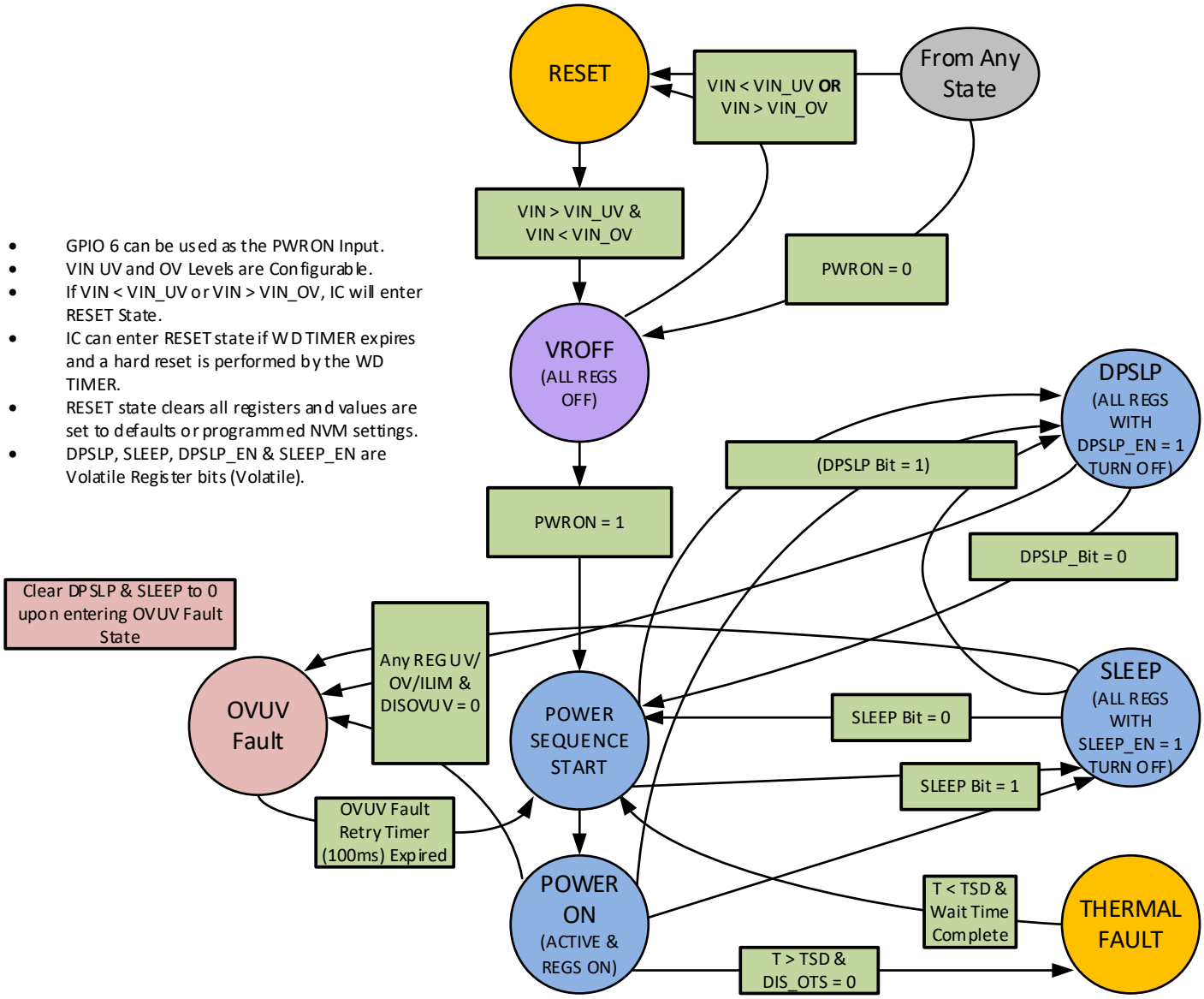


Figure 5: PWRON State Machine

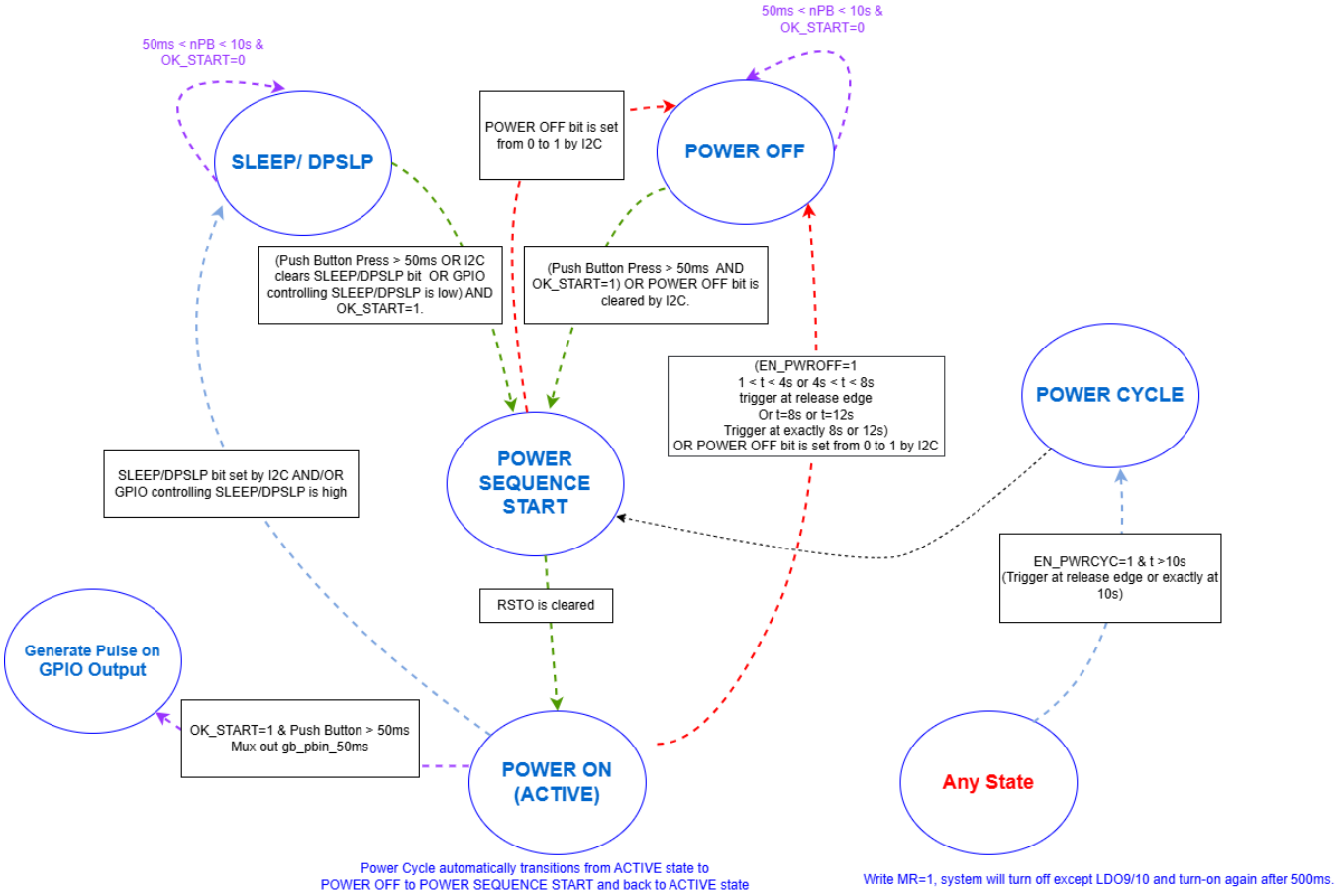


Figure 6: Push Button State Machine

PMIC OPERATION

The following sections describe the available QP8817 functionality. Much of this functionality is configurable and can be mapped to different IC pins with a different CMI.

Sequencing

The QP8817 provides the end user with extremely versatile sequencing capability that can be optimized for many different applications. Each of the 17 outputs has five basic sequencing parameters: input trigger, turn-on delay, turn-off delay, soft-start time, and output voltage. Each of these parameters is controlled via the ICs internal registers. Contact Qorvo for custom sequencing configurations. Refer to the Qorvo Application Note describing the Register Map for full details on I²C functionality and programming ranges.

Turn on and Turn off Options. The QP8817 provides several options for enabling the IC. These include automatic power-up when input power is applied as well as power-up with a digital input signal to a GPIO. The GPIO can be configured to latch the IC on with an input pulse or to be level-triggered. Once powered on, the IC can be turned off with either the GPIO or an I²C command.

Input trigger. The input trigger for a regulator is the event that turns that regulator on. Each output can have a separate input trigger. The input trigger can be the internal power OK (POK) signal from one of the other regulators, the internal VIN POK signal, or an external signal applied to the IC's nPB/PWREN or GPIO pins. This flexibility allows a wide range of sequencing possibilities, including having some of the outputs be sequenced with another external power supply or a control signal from the host. As an example, if the LDO1 input trigger is Buck1, LDO1 will not turn on until Buck1 is in regulation. Input triggers are defined at the factory and can be changed with a custom CMI configuration. The GPIOs can be internally connected to a power supply's internal POK signal and used as an output to turn on external supplies in the overall sequencing scheme. A GPIO configured as the enable signal to turn on an external power supply is called the EXT_EN function.

Turn-on Delay. The turn-on delay is the time between an input trigger going active and the output starting to turn on. Each output's turn-on delay is configured via its I²C bit ONDLY[2:0]. Turn-on delays can be changed after the IC is powered on, but they are volatile and reset to the factory defaults when power is recycled.

Turn-off Delay. The turn-off delay is the time between the input trigger for SLEEP or DPSLP Mode being asserted and when each output starts to turn off. Each output's turn-off delay is configured via its I²C bit OFFDLY[2:0]. Turn-off delays can be changed after the IC is powered on, but they are volatile and reset to the factory defaults when power is recycled.

Softstart Time. The softstart time is the time it takes an output to ramp from 10% to 90% to its programmed voltage. Each output's softstart time is configured separately via its I²C softstart bits. Softstart times can be changed after the IC is powered on, but they are volatile and reset to the factory defaults when power is recycled.

Output Voltage. Each regulator's voltage is programmed via its I²C bits VSETx. The Buck1/2/5 have four VSETx registers, Buck3/4 have two VSETx registers while the Buck-Boosts, and LDOs only have one. Note that in all conditions a Buck's VSET0 register must be programmed to the highest voltage setting of all its VSETx registers. VSET1/2/3 settings do not have any restrictions other than they must all be lower than VSET0. A Buck converter typically regulates to its VSET0 voltage in ACTIVE mode, but a GPIO can be configured to have the regulator regulate to one of its other voltages. The Buck converter can be programmed to DVS to different VSETx values via a GPIO or by I²C. The LDOs do not support DVS.

All Buck regulators can change between VSETx values on-the-fly (true DVS). If a system requires two different voltage options at startup, a GPIO can be programmed as a Voltage Select function. The Voltage Select input acts as an individual DVS control input to a Buck converter. The Voltage Select input is typically tied high or low before output voltage is enabled and then does not change after the output is turned on. However, the QP8817's does allow the Voltage Select to be changed on-the-fly for small output voltage changes that are less than 25%. For larger voltage changes, Qorvo recommends changing the voltage via I²C in small increments so the output voltage does not trigger an OV or UV condition.

Each output's Bx_VSET0 and Bx_VSET1 voltage can be changed via I²C after the IC is powered on, but the new setting is volatile and is reset to the factory defaults when power is recycled. All Bucks and LDO output voltages can be changed on-the-fly by writing a new value into their I²C registers. If a large voltage change is needed, change the output voltage by multiple smaller steps. Qorvo recommends minimizing the step size change to prevent the IC from detecting an instantaneous over or under-voltage condition due to fault thresholds being immediately changed, but output voltage taking time to respond.

Dynamic Voltage Scaling

On-the-fly dynamic voltage scaling (DVS) for all Buck regulators is available via the I²C interface. DVS allows systems to save power by quickly adjusting the microprocessor performance level when the workload changes. Note that DVS is not a different operating state. The IC operates in the ACTIVE state, but just regulates the outputs to a different voltage as specified by VSETx. For fault free operation, the user must ensure output load conditions plus the current required to charge the output capacitance during a DVS rising voltage condition does not exceed the current limit setting of the regulator. As with any power supply, changing an output voltage too fast can require a current higher than the current limit setting. The user must ensure that the voltage step, slew rate, and load current conditions do not result in an instantaneous loading that results in a current limit condition.

Buck1/2/5 have four DVS settings. Buck3/4 have two DVS settings. Buck1/2/5 enter DVS differently from Buck3/4. Entering DVS by a GPIO pin, I²C, or when entering SLEEP/DPSLP are CMI dependent, so contact Qorvo for details.

Buck1/2/5 enter DVS by using GPIO pins (Table 2) or via I²C using the BKxDvsI2C[1:0] bits in register 0x44h. Note that Buck1/2/5 cannot automatically enter DVS when the IC enters SLEEP or DPSLP mode.

Buck3/4 enter DVS by using a single GPIO pin or via I²C using the DVS_FROM_I2C_DBx bits in register 0x02h. They can also be programmed to automatically enter DVS when the IC enters SLEEP or DPSLP mode.

Table 2: Buck1/2/5 DVS Control

Buckx_I2C_DVS_EN bit	Control Input - BKxDvs	Control Input - GPIOx, GPIOy	Buck1/2/7 Voltage Control Register
0	xx	00	VSET0
0	xx	01	VSET1
0	xx	10	VSET2
0	xx	11	VSET3
1	00	xx	VSET0
1	01	xx	VSET1
1	10	xx	VSET2
1	11	xx	VSET3

Input Voltage Monitoring (SYSMON)

The QP8817 monitors the input voltage on the AVIN pin to ensure it is within specified limits for system level operation. The IC “wakes up” and allows I²C communication when AVIN rises above the UVLO threshold. The UVLO falling threshold can be set to either 2.7V or 3.6V by a factory programmable bit, VIN_LVL. VIN_LVL is not user adjustable. However, the outputs do not turn on until AVIN rises above the SYSMON threshold. The SYSMON rising threshold is programmable between 2.6V and 4.7V with 100mV steps. The SYSMON falling threshold has 100mV hysteresis.

If AVIN drops below the SYSMON falling threshold, the QP8817 operates in one of two modes, which are programmable via a factory bit. This bit is not user adjustable. When SYSMON_SD=0 the outputs continue to operate normally while AVIN is still above UVLO. A GPIO can be programmed to output an active low SYSMON signal to indicate the SYSMON threshold has been crossed. The IC also asserts the nIRQ interrupt when AVIN < SYSMON. The nIRQ interrupt can be masked by an NVM register bit. The SYSMON signal output is a real-time signal. The IC also has a real-time status bit, SYSDAT in register 0x02h that follows the internal SYSMON signal. Note that the nIRQ output is latched until the SYSSTAT bit in register 0x00h is read via I²C.

When SYSMON_SD=1 the outputs immediately turn off when AVIN drops below the SYSMON falling threshold. Note that the outputs do not follow their programmed turn of delay. Figure 7 shows the SYSMON details when SYSMON_SD=0 (not programmed to turn off the outputs). If programmed to turn off the outputs, Figure 8 would show the outputs turning off when AVIN dropped below SYSMON.

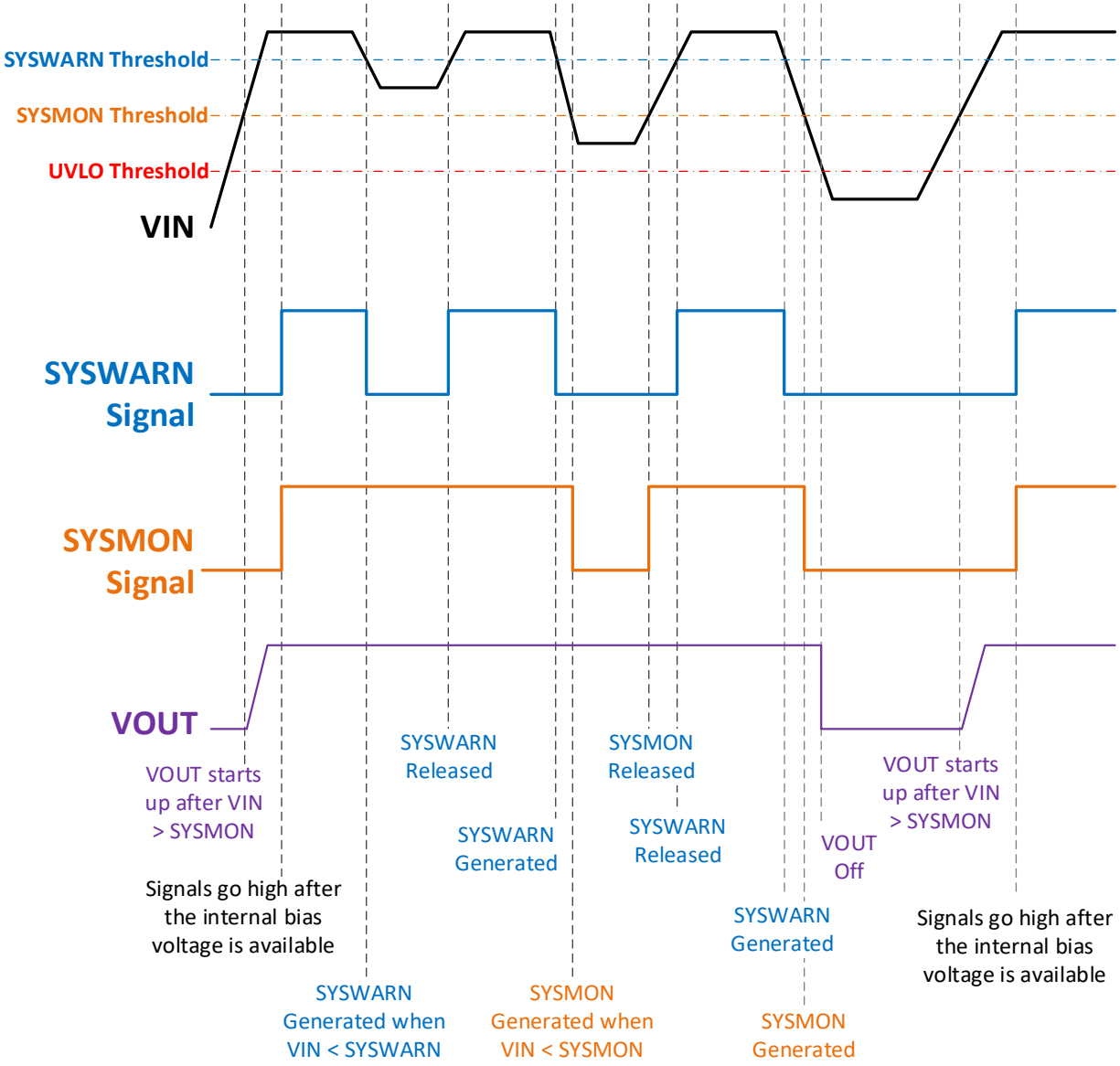


Figure 7: SYSMON and SYSWARN Signals when SYSMON_SD=0

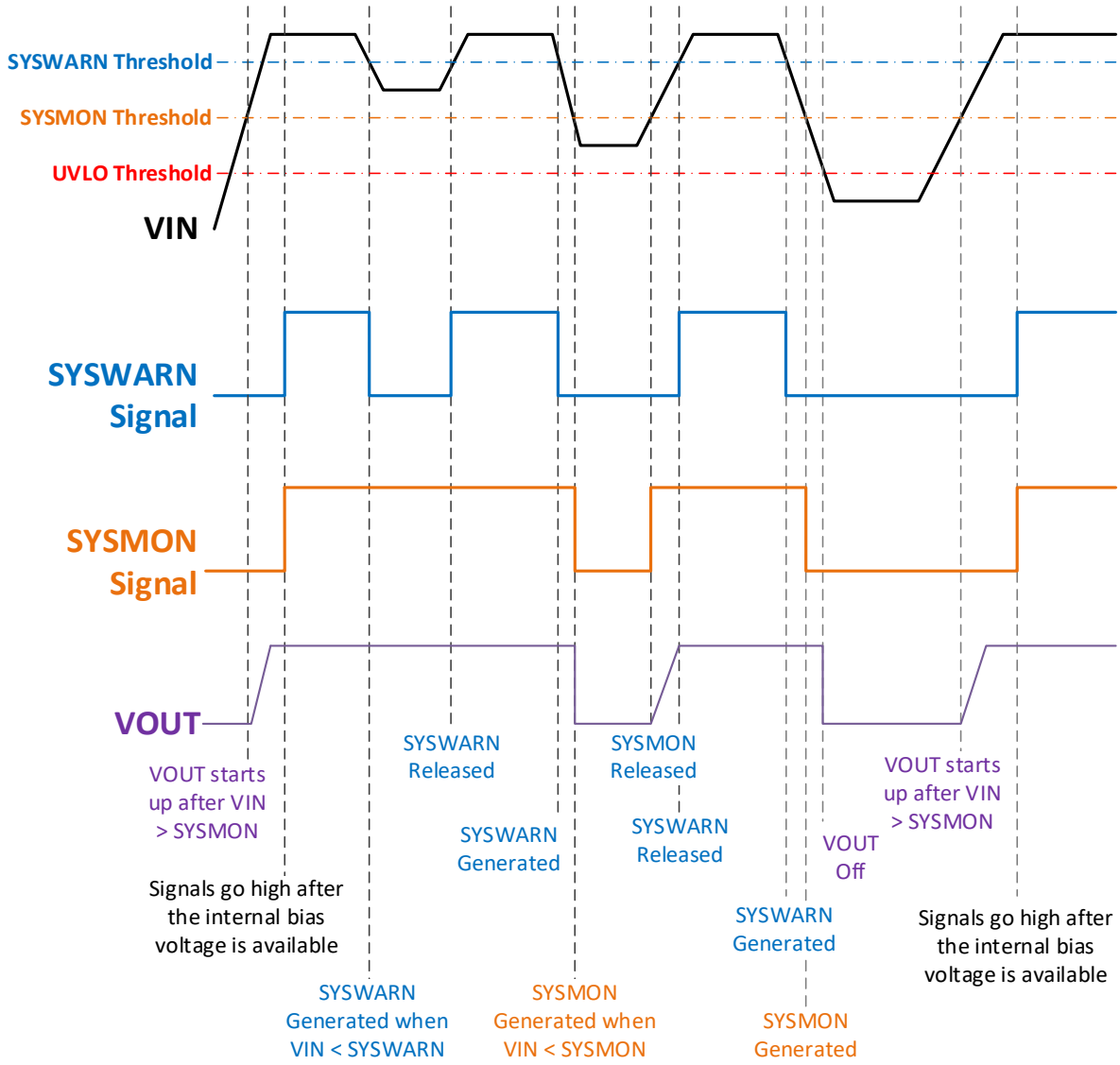


Figure 8: SYSMON and SYSWARN Signals when SYSMON_SD=1

Input Voltage Warning (SYSWARN)

The QP8817 also has a second level of input voltage monitoring, SYSWARN. SYSWARN provides another level of low input voltage warning to the host. The rising threshold is programmable between 2.725V and 3.1V with 25mV steps by the SYSWARN bits. It should not be programmed lower than the SYSMON threshold. A GPIO can be programmed to output an active low SYSWARN signal so the host can use it for system control purposes. In the meantime, the IC asserts the nIRQ interrupt when VIN < SYSWARN. The nIRQ interrupt can be masked in the NVM register bit. The SYSWARN signal output is a real-time signal. The IC also has a real-time status bit, SYSWARN, that follows the internal SYSWARN signal. Note that the nIRQ output is latched until the SYSWARN bit in register 0x00h is read via I²C.

Fault Protection

The QP8817 contains several levels of fault protection, including the following:

- System Monitor (SYSMON) – UV and OV detection

- System Warning (SYSWARN) – UV and OV detection
- Output Overvoltage
- Output Undervoltage
- Output Current Limit and Short Circuit
- 4 Levels of Thermal Warning
- Thermal Shutdown

There are three types of I²C register bits associated with each fault condition: fault flag bits, fault bits, and mask bits. The fault flag bits display the real-time fault status. Their status is valid regardless of whether that fault is masked. The mask bits either block or allow the fault to affect the fault bit. Each potential fault condition can be masked via I²C if desired. Any unmasked fault condition results in the fault bit going high, which asserts the nIRQ pin. nIRQ is typically active low. The nIRQ pin only de-asserts after the fault condition is no longer present and the corresponding fault bit is read via I²C. Note that masked faults can still be read in the fault flag bit. Refer to the Qorvo Application Note describing the Register Map for full details on I²C functionality and programming ranges.

Input Voltage UVLO

The QP8817 monitors its input voltage at the AVIN pin for a UVLO condition. When the input voltage is below the UVLO threshold, the IC is in the RESET State, all outputs are turned off, and nRESET is asserted low. I²C functionality is not enabled until AVIN goes above the UVLO threshold. When the input voltage goes above UVLO, the IC transitions to the Power Sequence Start or the VROFF state. The UVLO threshold can be set to either 2.7V or 3.6V by a factory programmable bit, VIN_LVL. VIN_LVL is not user adjustable.

Input Voltage OV

The QP8817 monitors its input voltage at the AVIN pin for an OV condition. There are two overvoltage levels, POK_OV and VIN_OV. The first level is set by the POK_OV register, which is programmable between 3.5V and 5.6V in 300mV steps. When AVIN goes above the POK_OV threshold, an interrupt is generated on the nIRQ output, but all outputs stay on. If VIN_POK_OV_MASK = 0, the VIN_POK_OV register provides real-time status if. If it = 1, then VIN_POK_OV register is latched until read by I²C. The second level, VIN_OV, is programmable between 3.7V and 5.8V. VIN_OV should be programmed higher than POK_OV. When the input voltage is above the VIN_OV threshold, the IC is in the RESET State, all outputs are turned off, and nRESET is asserted low. I²C functionality is still enabled while AVIN is above the VIN_OV threshold. When the input voltage goes below the VIN_OV threshold, the IC transitions back to the Power Sequence Start State and starts up normally.

Output Under/Over Voltage

The QP8817 monitors the output voltages for under voltage and over voltage conditions. The Bucks' undervoltage bits are POK and the overvoltage bits are OV. The LDOs' undervoltage bits are PWRGOOD and the overvoltage bits are OV. The undervoltage thresholds are ~92% of the setpoint and the overvoltage thresholds are ~108% of the setpoint.

If the fault mask bits are set to 1, output UV/OV faults will not trigger interrupt, and the IC will not enter UV/OV shutdown.

If the fault mask bits (UV_FLTMSK and OV_FLTMSK) are set to 0, output UV/OV faults will trigger interrupt. And if the bit DisOvUvShdn in register 0x09h is set to 0, the IC will enter UV/OV shutdown. The IC can be configured to assert the nIRQ pin low when an output goes UV/OV to interrupt the system processor nIRQ remains asserted low until either the faulty regulator is turned off or it goes back into regulation, and the POK [-] bit (for Bucks) and PWRGOOD[-] bit (for LDOs) has been read via I²C to clear the interrupt. After the UV/OV condition is removed, an I²C read is required to clear the interrupt.

When it enters the UV/OV state, it shuts down all outputs for 100ms and restarts with the programmed power up sequence. If an output is in current limit, it is possible that its voltage can drop below the UV threshold which also shuts down all outputs. If that behavior is not desired, mask the appropriate fault bit.

POK[]/PWRGOOD[] are real-time status bits while OV[] is a latching status bit. POK[]/PWRGOOD[] are set to 1 when VOUT is over the POK/PWRGOOD levels and reset to 0 when VOUT is under POK/PWRGOOD level. Note that these bits are valid even if the UV/OV faults are masked. Masking an OV/UV fault just prevents the fault from being reported via the nIRQ pin. They still provide real-time UV/OV fault status via its fault flag, even if the fault is masked.

OV[] is set to 1 when VOUT is over the OV level and stays latched at 1 until readback by I²C OV[] and the output voltage has dropped below the OV threshold.

A UV/OV fault condition pulls the nRESET pin low. Note that nRESET output is configurable via CMI settings. Note that when the IC enters the UV/OV state due to an output UV/OV condition, all other outputs also turn off, even if their UV and OV faults are masked.

Output Current Limit

The QP8817 incorporates a three-level overcurrent protection scheme for the Buck converters and a single level scheme for the LDOs. For the Buck converters, the overcurrent current threshold refers to the peak switch current. The first protection level is when a Buck converter's peak switch current reaches 77.5% of the Cycle-by-Cycle current limit threshold for greater than 17 continuous switching cycles. Under this condition, the IC reports the fault via the appropriate fault flag bit. If the fault is unmasked, it asserts the nIRQ pin. This does not turn off that output or other outputs. The next level is when the current increases to the Cycle-by-Cycle threshold. The Buck converter limits the peak switch current in each switching cycle. This reduces the effective duty cycle and causes the output voltage to drop, potentially creating an undervoltage condition. When the overcurrent condition results in an UV condition, and UV is not masked, the IC turns off all supplies off for 100ms and restarts. The third level is when the peak switch current reaches HS or LS Cycle-by-Cycle current limit threshold for twenty-four continuous switching cycles. This immediately shuts down the regulator and waits 14ms before restarting. The IC also has LS current limit for protection from current run-away.

If the Buck regulator current limit fault causes a UV fault which is reported back to the master controller (unmasked), the PMIC may shutdown for 100ms by entering the OV/UV state, and the behavior of the PMIC in this case is similar to the behavior in the OV/UV state.

For LDOs, the overcurrent thresholds are set by each LDO's Output Current Limit setting. When the output current reaches the Current Limit threshold, the LDO limits the output current. This reduces the output voltage, creating an undervoltage condition, causing all supplies to turn off for 100ms before restarting.

The overcurrent fault limits for each output are adjustable via I^2C. Overcurrent fault reporting can be masked via I^2C, but the overcurrent limits are always active and will shut down the IC when exceeded.

Thermal Warning and Thermal Shutdown

The QP8817 monitors its internal die temperature and reports a warning via the nIRQ interrupt pin when the temperature rises above the Thermal Interrupt Warning Threshold of typically 125^{O}C. The QP8817 contains four levels of thermal warning. The thermal warning status bits can be individually read from their corresponding register bits. One of the four thresholds can be mapped to generate an interrupt on the nIRQ pin.

The IC can report a fault when the temperature rises above the Thermal Shutdown Temperature of typically 165^{O}C. An over-temperature condition moves the state machine to the THERMAL FAULT state and shuts down all outputs unless the fault is masked. Both the fault and the warning conditions can be masked via I^2C. The temperature warning and fault flags still provide real-time status even if the faults are masked. Masking just prevents the faults from being reported via the nIRQ pin and prevents the PMIC from automatically reacting to the condition.

PWREN

PWREN is one of the three operating modes. See the State Machine section for more information. The PWREN functionality is controlled by the PWREN pin, which can only be assigned to GPIO6. The PWREN functionality is only available when the IC is configured for PWREN.

PWRON

PWRON is one of the three operating modes. See the State Machine section for more information. The PWRON functionality is controlled by the PWRON pin, which can only be assigned to GPIO6. The PWRON functionality is only available when the IC is configured for PWRON.

Push Button

Push Button is one of the three operating modes. See the State Machine section for more information. The Push Button functionality is controlled by the nPB pin, which can only be assigned to GPIO6. The Push Button functionality is only available when the IC is configured for Push Button.

The nPB provides multiple system level functions which depend on both the length of time that nPB is asserted low and the I^2C register settings. Table 12 summarizes the available options.

Power On: When nPB is pressed for longer than its 50ms debounce time, the IC always enters the ACTIVE state from any previous state, including SLEEP/DPSLP, UV/OV/OC protection, and POWER OFF states, and it resets the SLEEP/DPSLP bits to "0". If the press time is less than 50ms, the debounce timer resets and the IC stays in its current state.

Power Off: nPB can be used to turn the outputs off and put the IC into the POWER OFF state. Enable this functionality by setting EN_PWROFF=1. Asserting nPB for longer than the time defined by PB_OFF_TIMER turns the outputs off with the programmed turn off sequencing. Note that the IC first enters the ACTIVE state after the 50ms debounce time. For the 1s<4s and 4s<8s settings, the IC turns off when nPB is deasserted. For the 8s and 12s settings, the IC turns the outputs off after nPB is pressed for either 8s or 12s. nPB does no need to be

released to turn the outputs off. The four timing options are below:

00: 1s < Tpress < 4s, trigger at release

01: 4s < Tpress < 8s, trigger at release

10: Tpress = 8s, trigger at exactly 8s

11: Tpress = 12s, trigger at exactly 12s

For the 1s<4s and 4s<8s timing, if nPB is deasserted before the programmed time, the IC goes to the ACTIVE state after the 50ms debounce time and stays in the ACTIVE state. When the timing is programmed for 8s or 12s, the IC immediately turn the outputs off when nPB is held for longer than the 8s or 12 programmed time.

Power Cycle: The IC also contains a Power Cycle function. This function turns all outputs off with their programmed power down sequencing and then automatically restarts them with their startup sequencing after a 500ms delay.

Asserting nPB for longer than the time defined by 10s turns the outputs off with the programmed turn off sequencing. Depends on the PC_ENRL_Wake bit setting, PMIC enters the power cycle either at exact 10s or at push button release edge after 10s. Note that firmeware should not block the 10s PB recycle.

PC_ENRL_Wake = 1: Enter Power Cycle at release edge

PC_ENRL_Wake = 0: Enter Power Cycle at exact 10s.

Generate Pulse: One GPIO can be configured as a PB_Pulse function to generate a 100ms pulse when push-button is asserted for > 50ms.

Table 12 describes the available nPB functions.

nPB FUNCTION SUMMARY				
Function	*nPB Time*	*nPB TIME Configuration*	*nPB Configuration*	*Tigger at*
Power On	*t > 50ms*		*EN_PWROFF = 0*	*50ms*
Generate Pulse on GPIO	*t > 50ms*		*EN_PB_PULSE = 1*	*50ms*
Power Off	*1s < t < 4s*	*PB_OFF_TIMER = 00*	*EN_PWROFF = 1*	*Release Edge*
	4s < t < 8s	*PB_OFF_TIMER = 01*		
	t = 8s	*PB_OFF_TIMER = 10*		*8s*
	t = 12s	*PB_OFF_TIMER = 11*		*12s*
Power Cycle	*t > 10s*			*Release Edge (PC_ENRL_Wake = 1)*
				10s (PC_ENRL_Wake = 0)

Table 12: Summary of nPB Functions

nIRQ

The QP8817 interrupt pin informs the host of any unmasked IC faults. In general, anything with a status change indicator can assert the nIRQ pin. The status changes can be masked by set the corresponding register bits. Note that all interrupts are masked by default and must be unmasked as needed. If interrupt bit is set, the fault must be read before it clears the interrupt bit. nIRQ stays asserted until both the fault clears and the interrupt bit is cleared by an I^2C read. If the fault remains after the I^2C read, the interrupt bit remains set.

The following status changes assert nIRQ:

- Input over-voltage, under-voltage
- Input voltage drops below SYSMON
- Input voltage drops below SYSWARN
- Thermal warning, thermal shutdown
- Buck operation faults
- Buck under-voltage shutdown
- Any Buck regulator exceeding peak current limit for 17 cycles after soft start or a UV/OV condition.
- Any regulator exceeding current limit for more than 20µs after soft start or a UV/OV condition.
- Watch Dog timer expiring.
- GPIOs wake up mode high to low transition

nRESET

The nRESET pin is an open drain 5V compatible output used to issue the main reset to the system's CPU/controller. The output monitors the input voltage and valid regulator outputs to trigger a reset if the input voltage or regulator output voltages are not valid. The nRESET delay time is controlled by the TRST_DLY control bits. The

delay time is programmable from 5ms to 100ms. nRESET is essentially the same as a Power Good (PG) function but with a fixed delay after all the supply rails go into regulation.

The nRESET output signal is typically tied to all regulators outputs that are necessary for the system controller and I/Os to function properly. Each regulator has a register bit, RST, that determines if that regulator's POK signal is used as an input to the nRESET output signal. In general, the behavior of the nRESET output is such that the nRESET output is low if any one of the Power Okay (POK) signals from the controlling regulators is low. In other words, if any one of the controlling regulator outputs is not okay, the nRESET output will be asserted low.

The POK signal for any regulator can only be low when the regulator is enabled and the output is not regulating at normal levels. When a regulator's RSTI_by_POK bit = 0, the disabled regulator does not affect the nRESET signal even if its POK signal were configured to control the nRESET output. When a regulator's RSTI_by_POK bit = 1, then the disabled regulator does assert nRESET low. Note that RSTI_by_POK bit is a factory bit and can not be changed by a user.

In most applications, RSTI_by_POK bit = 0 so that a disabled regulator's POK bit stays high. The POK bits only go low (not ok) when the regulator is enabled but the output is not at the target regulation voltage. When a regulator is enabled, its internal POK immediately goes low until the output voltage goes above 90% of its programmed voltage.

Note that if a regulator's POK is configured as one of the input triggers to the nRESET function and that regulator turns off, the nRESET pin gets momentarily asserted low. The regulator could be turned off due to a GPIO input or going into SLEEP or DPSLP modes. When the regulator turn off due to a GPIO input or existing SLEEP or DPSLP modes, its POK output momentarily goes low, which also asserts nRESET low. If this is not desired, that individual regulator can be reconfigured to not be a RESET trigger input. Another option is to use the PGOOD function as a RESET to the system microprocessor.

PGOOD

The PGOOD output is similar to nRESET, but with some key differences. At power up the RESET function drives the PGOOD output, and PGOOD is asserted high at the same time that nRESET is deasserted high. The key difference is that PGOOD does not momentarily deassert low when a regulator enters or exits SLEEP or DPSLP states or when it is enabled or disabled with a GPIO. The regulator's POK signal does not force the PGOOD output low. The PGOOD output is only de-asserted when a fault occurs on any of the regulators after its soft start time. PGOOD is also deasserted low when all regulators on the IC are turned off or when the master UVLO (MUVLO) signal triggers. The master UVLO is a signal that is triggered when the input voltage (AVIN Input) is removed or when it drops below the UVLO threshold to reset the IC. A factory bit (ILIMFLT_PG_MASK[]) controls whether or not an output's current fault deasserts PGOOD. If ILIMFLT_PG_MASK = 0, any output's current limit fault deasserts PGOOD. If ILIMFLT_PG_MASK = 1, then current faults do not affect PGOOD.

EXT_EN

The EXT_EN is a GPIO output function that is used to enable an external power supply. This function is useful for incorporating external power supplies into the overall system level startup sequencing. The EXT_EN output can be triggered by one of the regulator's POK signals. It can be programmed with a 0, 1, 2, or 4ms delay time.

EDGE_OUT

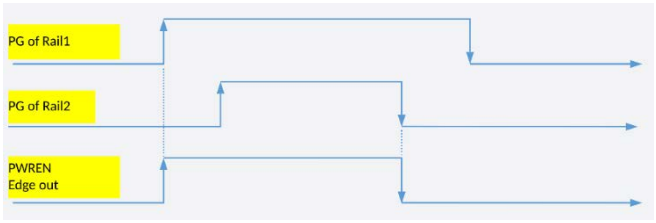


Figure 6: Edge-out diagram

Two GPIO can be configured as the output that triggered by two DC-DC/LDO/LSW rails PG signal. The edge-out rising edge is always triggered by the first rising edge of two input PG signal, and the falling edge is also triggered by the first falling edge of the two PG signals.

EXT_PG

The EXT_PG is a GPIO input function that is used to indicate that an external power supply has turned on and its output voltage is in regulation. This function is useful for incorporating external power supplies into the overall system level startup sequencing. The EXT_PG output can be used as an input trigger to turn on one of the QP8817 regulators.

POK

Any regulator's internal POK bit can be connected to a GPIO to provide an external POK signal. The POK function indicates that a regulator's output voltage is in regulation.

GPIO Wake up Mode

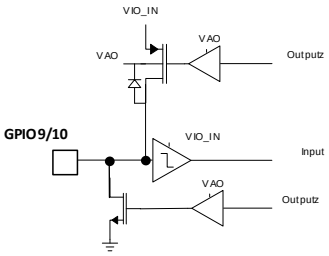
All GPIOs can be configured to force the IC into and out of DPSLP mode. Any number of GPIOs can be configured for this functionality. Please see the DPSLP State section for details. In addition, there are interrupt triggers that can be set up for GPIOs 1-11. The input status of the GPIOs can be read from the GPIOx_STAT bits, register 0x03h, 0x2Bh. Only the bits associated with the GPIOs that are configured as inputs are valid. The other bits are undefined and return a random value when read. For GPIOs configured as inputs, except PWRON, an input status change (1 to 0 or 0 to 1) can be configured to assert the nIRQ pin. For the PWRON input, a status change from 0 to 1 can be configured to assert the nIRQ pin, but a status change from 1 to 0 cannot. When the PWRON status changes from 1 to 0, all volatile and non-volatile registers are reloaded to their default settings, which masks the status change. The status change function is masked by default and must be unmasked to enable the function, except GPIO8 which is unmasked by default.

LED Driver

GPIO9/10 can be configured as LED sinks. They sink a constant current that is programmed by the ILEDx bits. These are configurable up to 15mA of current sink in 1mA steps. 0mA effectively turns the LED sink off.

Autonomous pattern control for programmable patterns include a configurable Period, Duty Cycle, Delay and single/double blink. There is also an autonomous “breath mode” that stair steps current up to the preset peak value and steps back down to emulate a breathing pattern smooth ramp up/down 0-3s in 0.1s increments.

The LED driver can work even when all the PMICs output are off. The LED driver enable/disable must be configured in a separated state from power-on/Sleep/Deep Sleep.



ILEDx [1:0]	ILEDx [3:2] (mA)			
	00	**01**	**10**	**11**
00	0	4	8	12
01	1	5	9	13
10	2	6	10	14
11	3	7	11	15

PWMFREQ<2:0>	LED TIME PERIOD (s)
000	0.233
001	0.466
010	0.932
011	1.398
100	1.864
101	2.795
110	3.725
111	5.592

PWMDUTY<3:0>	LED DUTY CYCLE (%)
0000	6.25
0001	12.5
0010	18.75
0011	25
0100	31.25
0101	37.5
0110	43.75
0111	50
1000	56.25
1001	62.5
1010	68.75
1011	75
1100	81.25
1101	87.5
1110	93.75
1111	100

LED_DELAY<1:0>	DELAY (%)
000	0
001	12.5
010	25
011	37.5
100	50
101	62.5
110	75
111	87.5

Discharge Function

The discharge function is used to quickly discharge a regulator's output voltage when the regulator is disabled. A GPIO can be configured as an open drain output and connected to the regulator's output through a resistor. When the output is turned off, all residual output capacitor energy is quickly discharged through the resistor to ground. The maximum discharge current is set by the discharge resistance and the output voltage. The discharge function is intended to quickly discharge the regulator's output voltage, but not to continuously sink current from an externally supplied voltage.

PIN DESCRIPTIONS

The QP8817 input and output pins are configurable via CMI configurations. The following descriptions refer to the basic pin functions and capabilities. Refer to the CMI Options section in the back of the datasheet for specific pin functionality for each CMI.

AVIN Input Pin

AVIN is the PMIC bias power input. AVIN provides bias power to the master controller, the control circuits for all the regulators, the voltage monitors and fault comparators for UV, OV, SYSMON, Current limits etc. AVIN must be connected to the same voltage source as the VIN_Bx pins. It requires a 10 µF bypass capacitor to AGND.

VIO Pin

The VIO output pin is a regulated voltage that can be set to 1.2V, 1.8V, 2.4V, or 3.3V. This voltage is used internally to power all GPIOs, and it sets the GPIO output voltage level when they are configured as push-pull outputs. The output voltage is powered from an integrated low quiescent current LDO. VIO requires a 1 µF capacitor to AGND. It can supply up to 20 mA of current to external circuity.

PWREN / PWRON / nPB Pin

This pin can be configured to only one of these three different functions. The pin's configuration is set by the ICs specific CMI. See the State Machine section of the datasheet for details on how this pin functions in each of the three available states: PWREN, PWRON, and Push Button.

SCL, SDA

These are the IC's I^2C clock and data pins. They have standard I^2C functionality. The SCL and SDA pins have dedicated functionality and cannot be used for other functionality. If I^2C is not needed, these pins should be tied to either ground or to AVIN. See the System Control section for the IC's available slave addresses. SCL and SDA can be configured as true open drain, or as open drain with internal 5kΩ pullup resistors. The pullup voltage can be configured to either VIO or AVIN.

PGNDx

The PGNDx pins are the Buck converter power ground pins. They connect directly to the Buck converters' low side FETs. Bypass VIN_Bx to PGNDx and place the bypass capacitors close to the IC with minimal trace distance and maximum trace width to minimize parasitic inductance.

VIN_Bx

VIN_Bx pins are the dedicated input power pins to the Buck converters. All VIN_Bx pins must be connected to the same voltage input. Each Buck converter's VIN_Bx pin must be bypassed directly to its PGNDx pin on the top PCB layer with high-quality ceramic capacitors. Refer to the Step-down DC/DC Converters section for more details on the capacitor requirements.

SW_Bx

SW_Bx are the Buck converter switch nodes. They connect directly to each Buck's inductor on the top layer.

FB_Bx

These are the feedback pins for each Buck converter. They should be kelvin connected to the Buck output capacitors.

VINLx

These are the dedicated LDOx input power pins. Each VINLx pin can be connected to a different input voltage to optimize system level efficiency. Each pin must be bypassed directly to AGND on the top PCB layer with a 1µF or greater ceramic capacitor.

LDOx

These are the LDO output pins. Each LDO output must be bypassed to AGND with an appropriate capacitor. See the LDO section for capacitor requirements.

GPIOx

The QP8817 has 12 GPIO pins. The GPIOs allow a variety of functions to be implemented. They can be used as inputs, open-drain outputs, or push-pull outputs. Their polarity can also be changed. These options allow implementation of a variety of system functions plus flexibility of functions tied to each pin. GPIOs can be configured for the following:

Reset output - nRESET

Power Good output - PG

Interrupt output – nIRQ

Power OK output – POK

External Regulator Enable output – EXT_EN

External Regulator Power Good input – EXT_PG

SLEEP Control input - SLEEP

DPSLP Control input - PWREN

Dynamic Voltage Scaling input – DVS

System Monitor output – SYSMON

System Warning output – SYSWARN

LED Driver input – LED

Not all GPIOs can support all available functions. The default GPIO configuration is defined by the IC's CMI. Some GPIOs can be reconfigured on-the-fly.

Some GPIOs that are configured as open drain outputs can be internally pulled up to either VIO or AVIN through an 86kΩ resistor. All GPIOs are 5V compliant and can be pulled to 5V regardless of their bias supply.

BUCK REGULATORS

General Description

The QP8817 contains five fully integrated step-down converters.

All Buck converters are Constant On Time (COT) mode controlled, synchronous PWM converters with peak efficiencies up to 96.5%. They switch at 1.5MHz, 2.0MHz 2.5MHz, or 3.3MHz, and are internally compensated, requiring only three small external components (Cin, Cout, and L) for operation. They ship with default output voltages that can be modified via I²C for systems that require advanced power management functions.

Buck1/2 support output currents up to 6A. Buck3/4/5 support output currents up to 2A. Buck1/2 can be configured to operate in parallel to provide a 2-phase operation with 10A (12A peak) currents. Buck3/4/5 do not support 2-phase operation.

Each Buck converter has a dedicated input pin and power ground pin. Each Buck converter must have a dedicated input capacitor that is optimally placed to minimize its power routing loops. Note that even though each Buck converter has separate inputs, all Buck converter inputs must be connected to the same voltage potential.

All QP8817 Buck regulators are highly configurable and can be quickly and easily reconfigured via I²C. This allows them to support changes in hardware requirements without the need for PCB changes. Examples of I²C functionality are given below:

Real-time power good, OV, and current limit status

Ability to mask individual faults

Dynamically change output voltage

On/Off control

Softstart ramp

DVS Slew rate control

Switching delay and phase control

Low power mode

Overcurrent thresholds

Refer to Qorvo's Register Map Definition application note for full details on I²C functionality and programming ranges.

Operating Mode

By default, Buck1-5 operate in PWM mode at medium to heavy loads, then transitions to a proprietary power-saving Low Power Mode, LPM, at light loads to save power. LPM mode reduces conduction losses by preventing the inductor current from going negative. Each Buck converter's LPM can be independently enabled or disabled via its DISLPM I²C bit. Setting DISLPM = 0 enables LPM while setting DISLPM = 1 disables LPM. Operating in LPM saves power and reduces the quiescent current by working in a fixed on-time hysteretic mode and by disabling unneeded IC functions when the LPM mode skips pulses. Disabling LPM mode reduces light load efficiency but improves load transient response during a light to heavy load transition.

LPM minimizes quiescent current in between switching cycles. This reduces input current to approximately 50µA in LPM mode. Light load output voltage ripple increases from approximately 5mV to 10mV when in LPM mode. Light load voltage droop when going from light load to heavier loads is only increased by 2-3mV when in LPM mode. LPM allows the customer to test the IC in their use case and optimize the balance between power consumption, voltage ripple, and transient response in their system. Setting DISLPM = 0 enables LPM while setting DISLPM = 1 disables LPM.

Many customers will program the Buck converters to LPM mode (LPM=1) after entering their system level low power mode and then program the IC back to PWM mode (LPM=0) just before leaving their system level low power mode. This provides the best load transient response while still taking advantage of reduced power dissipation in light load conditions. Note that when Vin=5V and operating in LPM mode, the output inductor should be 1µH.

ULPM (Ultra Low Power Mode)

The QP8817 incorporates an ultra-low power mode, ULPM, that provides significant efficiency improvements at very light loads. This improvement can be as much as 8% with a 2mA load. ULPM mode reduces the Buck converters quiescent current from ~50µA to ~10µA. The IC does this by turning off unused circuity and keeping only critical functionality enabled. Because ULPM is only used with extremely light loads, overcurrent protection is disabled to save quiescent current. ULPM mode helps systems like SSDs achieve very low power loss at extremely light loads, which is a requirement in their standby modes. ULPM mode regulates the output voltage between 99% to 101% of the setpoint. When the output voltage increases to 101%, the Buck converter shuts down to save quiescent current until the output voltage drops to 99%. It then turns back on and increases the output voltage to 101% again. ULPM mode should only be used when the load current is less than 15mA. With higher load currents, the output volt-

age drop can trigger UVLO before the converter can react. Using it with greater than 15mA results in much lower efficiencies than standard PWM or LPM mode operation.

If DVS mode is not needed when going into and out of DPSLP mode, program ULPM mode to automatically turn on when the IC enters SLEEP/DPSLP mode. If DVS is needed when going into and out of SLEEP/DPSLP mode, ULPM mode must be manually enabled after entering SLEEP/DPSLP mode and disabled before leaving SLEEP/DPSLP mode.

Synchronous Rectification

All Bucks feature integrated synchronous rectifiers (or LS FETs) to maximize efficiency and minimize the total solution size and cost by eliminating the need for external rectifiers.

Enable / Disable Control

When power is applied to the IC, all converters automatically turn on according to a pre-programmed sequence. Once in normal operation (ACTIVE state), each converter can be independently disabled via I²C. Each CMI version requires a different set of command to disable a converter, so contact the factory for specific instructions if needed. Each converter contains an optional integrated discharge resistor that actively discharges the output capacitor when the regulator is disabled. The discharge function is enabled via the I²C bit Dis_Pulldown.

Soft-Start

Each Buck regulator contains a softstart circuit that limits the rate of change of the output voltage, minimizing input inrush current and ensuring that the outputs power up monotonically. This circuitry is effective any time the regulator is enabled, as well as after responding to a short circuit or other fault condition. Each regulator's soft-start time is independently adjustable to either 50µs to 1000µs via its I²C SST register.

Output Voltage Setting

Buck1-5 regulate the voltage defined by I²C register VSET0 in normal operation. Buck1/2/5 have an additional three DVS settings defined by VSET1, VSET2, and VSET3. Buck3/4have one additional DVS setting, VSET1.

All Bucks have an Output-High and an Output-Low programming range.

Mode	Range	Step
Output-Low	0.5V-1.135V	5mV
Output-High	0.5V-3.675V	25mV

The Output-Low programming range is 0.5V to 1.135V in 5mV steps.

VBUCKx = 0.5V + VSETx * 0.005V

Where VSETx is the decimal equivalent of the value in I²C VSETx register. The VSETx registers contain an unsigned 7-bit binary value.

The Output-High programming range is 0.5V to 3.675V in 25mV steps.

VBUCKx = 0.5V + VSETx * 0.025V

Where VSETx is the decimal equivalent of the value in I²C VSETx register. The VSETx registers contain an unsigned 7-bit binary value. As an example, with Buck1 in the Output-Low setting and its VSET register contains 0111100b (60 decimal), the output voltage is 0.8V.

Qorvo recommends that a Buck converter's output voltage be kept within +/- 25% of the default output voltage to maintain accuracy. Voltage changes larger than +/- 25% may require different factory trim settings (new CMI) to maintain accuracy.

100% Duty Cycle Operation

All Buck regulators support 100% duty cycle operation. This allows operating conditions where the output voltage is very close to the input voltage. During 100% duty cycle operation, the P-ch high-side power MOSFET is turned on continuously, providing a direct connection from the input to the output (through the inductor), ensuring the lowest possible dropout voltage in battery powered applications.

As the input voltage drops, the converters have a transition between normal operation and 100% duty cycle mode. During normal switching, the minimum off-time is 40ns. If the operating conditions require < 40ns off-time, the switcher turns off for 40ns and then may skip the next switching cycle if the output voltage has not dropped to the point where the internal error amp commands another switching cycle. The output voltage is well regulated in this mode even though the IC skips pulses.

Dynamic Voltage Scaling

Each Buck converter supports Dynamic Voltage Scaling (DVS). DVS allows the user to optimize the processor's energy to complete tasks by lowering the processor's operating frequency and input voltage when lower performance is acceptable. In normal operation, all Buck regulators regulate to the voltage programmed in the I²C register Bx_VSET0. During automatic DVS initiated by SLEEP / DPSLP states, Buck3/4/5/6 regulate to Bx_VSET1. A GPIO can also be configured to change

an output's voltage between VSET0 and VSET1. Buck1/2/7 contain two additional VSETx registers, VSET2 and VSET3, to provide two additional DVS settings. When transitioning between VSETx settings, the control loop steps the output voltage through each step. The timing between steps is determined by the regulator's I²C SLEW bits. When going from a higher VSETx to a lower VSETx setting, the maximum output voltage transition rate may be limited by the rate determined by the output capacitance and the load current. When transitioning between a lower VSETx to a higher VSETx setting, the output transitions at the programmed slew rate.

VSET0 must always be programmed equal to or greater than the VSET1/2/3 setting. There is no programming limitations for VSET1/2/3 other than they must be programmed equal to or lower than VSET0.

During the transition between VSETx settings, the regulator's UV threshold is ignored to prevent incorrect fault triggering. The OV threshold is always relative to VSET0

For fault free operation, the user must ensure output load conditions plus the current required to charge the output capacitance during a DVS rising voltage condition does not exceed the current limit setting of the regulator. As with any power supply, changing an output voltage too fast can require a current higher than the current limit setting. The user must ensure that the voltage step, slew rate, and load current conditions do not result in an instantaneous loading that results in a current limit condition.

Qorvo recommends that a Buck converter's output voltage be kept within +/- 25% of the default output voltage to maintain accuracy. Voltage changes larger than +/- 25% may require different factory trim settings (new CMI) to maintain accuracy.

Optimizing Noise

Each QP8817 Buck converter contains several features available via I²C to further optimize functionality. The top P-MOSFET's turn-on timing can be shifted 100ns from the master clock edge via the PHASE I²C bit. It can also be aligned to the rising or falling clock edge via the PHASE I²C bit. The internal FET rise and fall times can be optimized to minimize switching noise at the cost of lower efficiency via the DRVADJ I²C bit.

Overcurrent and Short Circuit Protection

Each Buck converter provides overcurrent and short circuit protection. Overcurrent protection is achieved with cycle-by-cycle current limiting. The peak current threshold is set by the ILIM_SET I²C bits.

If the peak switch current reaches the programmed threshold (77.5% of ILIM_SET) for 17 consecutive switching cycles, the IC asserts that converter's ILIM_WARN bit and pulls nIRQ low. When DISOVUVShutdown = 0, a short circuit condition that results in a UV condition shuts down all supplies and then restarts the system in 100ms.

If a Buck converter reaches overcurrent or short circuit protection, the status is reported in that regulator's ILIM_REGx register. The contents of these registers are latched until read via I²C. Overcurrent and short circuit conditions can be masked via the I²C bit Bx_ILIM_FLTMSK. Note that ILIM_FLTMSK, ILIM_WARN_FLTMSK, OV_FLTMSK and UV_FLTMSK default to 1 (masked) at power up. The user can un-mask faults by setting these bits to 0 via I²C.

Compensation

The Buck converters utilize a proprietary internal compensation scheme to simultaneously simplify external component selection and optimize transient performance over their full operating range. No compensation design is required; simply follow a few simple guidelines described below when choosing external components.

Minimum On-Time

The QP8817 Buck regulators have a minimum on-time of 85ns. If the calculated on-time is less than the allowable minimum, then the user must configure the converter to switch at a lower frequency. The following equation calculates the on-time.

$$T_{ON} = \frac{V_{OUT}}{V_{IN} * F_{SW}}$$

Where V_{out} is the output voltage, V_{IN} is the input voltage, and F_{SW} is the switching frequency. The available switching frequencies are 1. 5MHz,2.0MHz, 2.5MHz, and 3.3MHz. The registers that set the switching frequency are in factory registers and are not user accessible.

Input Capacitor Selection

Each regulator requires a high quality, low-ESR, ceramic input capacitor. Note that even though each Buck converter has separate input pins, all input pins must be connected to the same voltage potential. 10µF capacitors are typically suitable, but this value can be increased without limit. Smaller capacitor values can be used with lighter output loads. Choose the input capacitor value to keep the input voltage ripple less than 50mV.

$$V_{ripple} = Iout * \frac{\frac{Vout}{Vin} * \left(1 - \frac{Vout}{Vin}\right)}{Fsw * Cin}$$

Be sure to consider the capacitor's DC bias effects and maximum ripple current rating when using capacitors smaller than 0805.

A capacitor's actual capacitance is strongly affected by its DC bias characteristics. The input capacitor is typically an X5R, X7R, or similar dielectric. Use of Y5U, Z5U, or similar dielectrics is not recommended. Input capacitor placement is critical for proper operation. Each Buck's input capacitor must be placed as close to the IC as possible. The traces from VIN_Bx to the capacitor and from the capacitor to PGNDx should as short and wide as possible.

Inductor Selection

The QP8817 Buck converters are optimized for operation with 0.47µH to 1µH inductors. Choose an inductor with a low DC resistance and avoid inductor saturation by choosing inductors with DC ratings that exceed the maximum output current by at least 30%. The following equation calculates the inductor ripple current.

$$\Delta I_L = \frac{\left(1 - \frac{V_{OUT}}{V_{IN}}\right) * V_{OUT}}{F_{SW} * L}$$

Where V_{OUT} is the output voltage, VIN is the input voltage, F_{SW} is the switching frequency, and L is the inductor value. Note that when Vin=5V and operating in LPM mode, the output inductor should be 1µH.

Output Capacitor Selection

The QP8817 is designed to use small, low ESR, ceramic output capacitors. Buck1/2 typically require 2x 22µF output capacitors while Buck3/4/5 typically requires a 22µF capacitor. To ensure stability, the actual Buck1/2 capacitance must be greater than 20µF while Buck3/4/5 must be greater than 12µF. There is no maximum output capacitance limitation. Design for an output ripple voltage less than 1% of the output voltage. The following equation calculates the output voltage ripple as a function of output capacitance.

$$\text{VRIPPLE} = \frac{\Delta I_L}{8 * F_{SW} * C_{OUT}}$$

Where ΔI_L is the inductor ripple current, F_{SW} is the switching frequency, and C_{OUT} is the output capacitance after taking DC bias into account.

Be sure to consider the capacitor's DC bias effects and maximum ripple current rating when using capacitors smaller than 0805.

A capacitor's actual capacitance is strongly affected by its DC bias characteristics. The output capacitor is typically an X5R, X7R, or similar dielectric. Use of Y5U, Z5U, or similar dielectrics are not recommended due to their wide variation in capacitance over temperature and voltage ranges.

Unused Buck Outputs

If a Buck converter is not used, connect the VIN_Bx pin to the other VIN_Bx pins. Connect FB_Bx to AGND. Leave SWx open. The input and output capacitors are not needed.

BUCK-BOOST REGULATORS

General Description

The QP8817 contains two fully integrated, Buck-Boost regulators. It can be configured for Buck-Boost mode or Buck mode only. In Buck-Boost mode, it provides up to 1000mA of output current with a 3.3V input and 3.3V output and can provide 600mA with a 5V output and a 3.3V input voltage. The output voltage of the Buck-Boost regulator can be programmed from 1.8V to 5V or from 0.8V to 3.6V in Buck-only mode. In Buck-only mode, it provides up to 2A of output current with a 3.3V input voltage.

The Buck-Boost regulator uses a proprietary COT-based control architecture to maximize efficiency. The base switching frequency is set at 2MHz. The integrated low RDS_{ON} (On-resistance) of the FETs help achieve up to 96% efficiency with a 3.3V output and 3.3V input voltage. It is internally compensated, requiring only three small external components (C_{IN}, C_{OUT}, L) for operation. The regulator has several settings that can be software controlled via the I^2C interface.

The Buck-Boost regulator is highly configurable and can be quickly and easily reconfigured via I^2C. This allows it to support changes in hardware requirements without the need for PCB changes. Examples of I^2C functionality are given below:

- Real-time power good output signal.
- UV, OV & Current Limit Status.
- Ability to mask individual faults.
- On/Off control.
- Low power mode.
- Overcurrent thresholds.
- Sequencing order and On/Off delay times.

Operating Modes

By default, the Buck-Boost regulator operates in a PWM mode at medium to heavy loads. It can then transition to a proprietary power-saving mode at light loads to save power and improve efficiency at light loads.

At light loads, the Buck-Boost operates in “burst” or “skip” mode. It automatically skips cycles to minimize switching losses. It enters this mode when the load current drops low enough that the inductor current drops to 0A. This is the transition between continuous conduction mode (CCM) and discontinuous conduction mode (DCM). It skips switching cycles as needed to maintain a regulated output voltage when the required duty cycle is less than the minimum on-time. In burst or skip mode, higher efficiency is maintained at light load conditions by operating the converter and switching only when necessary. The regulator automatically jumps out of skip or burst mode to PWM mode when the load current increases.

The Buck-Boost has two factory configurable operating modes: Buck-Boost mode or Buck only. Note that the operating mode is set at the factory and is not user adjustable.

Buck-Boost Mode: In this mode, the output voltage can be either higher or lower than the input voltage. All four internal FETs switch to achieve this functionality. In this mode, firstly the Boost portion (SWBB_2) operates with fixed off time. Then control loop modules the BUCK port tion (SWBB_1) to regulate output voltage

Synchronous Rectification

The Buck-Boost regulator features four fully integrated FETs and uses a full H-bridge for the power stage. It is therefore fully synchronous regulator. This maximizes efficiency and minimizes the total solution size and cost by eliminating the need for external rectifiers and FETs.

Enable / Disable Control

When power is applied to the IC, the Buck-Boost converter automatically turns on according to a pre-programmed sequence. Once in normal operation (ACTIVE state), it can be independently disabled via I^2C. Each CMI version (configuration of the IC) requires a different set of commands to disable the Buck-Boost, so contact the factory for specific instructions if needed. The Buck-Boost contains an optional integrated discharge resistor that actively discharges the output capacitor when the regulator is disabled. The discharge function is typically disabled. This function is user selectable and is turned on only for Buck-only operation.

Soft-Start

The Buck-Boost regulator includes a programmable (0.5/1/2/4 ms) internal soft-start ramp which limits the rate of change of the output voltage. This time is measured from 10% to 90% of the programmed output voltage. This minimizes input inrush current and ensures that the output powers up in a monotonic manner that is independent of current load on the outputs. This circuitry is effective any time the regulator is enabled, as well as during re-try after responding to a short-circuit or other fault condition.

Output Voltage Setting

The Buck-Boost converter regulates to the voltage defined by its I^2C register VSET0 in normal operation.

In Buck-Boost mode, the programming range is 1.8V to 5.0V in 25mV steps.

$V_{BUCK-BOOST}$ = 1.8V + VSET0 * 0.025V

In Buck-only mode, the programming range is 0.8V to 3.6V in 25mV steps and given by the following equation:

$V_{BUCK-BOOST}$ = 0.8V + VSET0 * 0.025V

Where VSET0 is the decimal equivalent of the value in Buck-Boost regulator's I²C VSET0 register. The VSET0 registers contain an unsigned 8-bit binary value.

Qorvo recommends that the Buck-Boost converter's output voltage be kept within +/- 25% of the default factory-set output voltage to maintain good accuracy. Voltage changes larger than +/- 25% using I²C may require different factory trim settings (new CMI) to maintain accuracy.

Overcurrent and Short Circuit Protection

The Buck-Boost converter provides overcurrent and short circuit protection. It provides cycle-by-cycle current limit on the VBBIN-to-SWBB_1x FET. The maximum current threshold is set by the ILIM I²C register bits.

Table 1: Buck-Boost Cycle-by-Cycle Current Limit Settings

ILIM [1:0]	Q_{SWBB_1x} FET Peak Current (A)
00	1.7
01	2.1
10	2.5
11	3.2

If the peak current reaches 80% of the programmed threshold for 16 consecutive switching cycles, the IC asserts nIRQ low if the IWARN_INT_MASK bit set to 0 and changes I²C bit ILIM_WARN = 1. The regulator continues to operate normally. If the peak current reaches the programmed threshold, the IC turns off the power FET for that switching cycle alone. If the peak current reaches the threshold 16 consecutive switching cycles, the IC asserts nIRQ low if the IFLT_INT_MASK bit set to 0. This condition typically results in shutdown due to an UV condition due to the shortened switching cycle and limited current capability of the regulator. A short circuit condition that results in the peak switch current being 125% of ILIM_SET for BUCK only mode and 140% for BUCK BOOST mode setting will immediately shut down the regulator and asserts the nIRQ output low if the ISHUT_INT_MASK bit set to 0. The regulator then attempts to restart in 14ms. If the fault condition is not masked, the IC transitions to the OVUV State, turns off all regulators, and restarts the system in 100ms.

Compensation

The Buck-Boost utilizes a proprietary internal compensation scheme to simultaneously simplify external component selection while optimizing transient performance over their full operating range. No external compensation design is required. Simply follow a few simple guidelines described below when choosing the output capacitor and inductor.

Input Capacitor Selection

The input requires a high quality, low-ESR, ceramic input capacitor. The Buck-Boost input voltage can be connected to the same or a different voltage rail from the other converters. Even if it is connected to the common voltage rail (V_{BUS}), it must have a dedicated input capacitor. 10uF capacitors are typically suitable, but this value can be increased when required. Smaller capacitor values can be used with lighter output loads. Choose the input capacitor value to keep the input voltage ripple less than 50mV. When in Buck-mode operating mode, the following equation calculates the input ripple.

$$V_{ripple} = Iout * \frac{\frac{Vout}{Vin} * \left(1 - \frac{Vout}{Vin}\right)}{Fsw * Cin}$$

Be sure to consider the capacitor's DC bias effects and maximum ripple current rating when using capacitors smaller than 0805.

A capacitor's actual capacitance is strongly affected by its DC bias characteristics. The input capacitor is typically an X5R, X7R, or similar dielectric. Use of Y5U, Z5U, or similar dielectrics is not recommended. Input capacitor placement is critical for proper operation. The input capacitor must be placed as close to the IC as possible. The traces from VBBST to the capacitor and from the capacitor to PGNDx should as short and wide as possible.

Inductor Selection

The Buck-Boost uses a proprietary internal compensation scheme to simultaneously simplify external component selection and optimize transient performance over its full operating range. The QP8817 Buck-Boost regulator is optimized for a 1µH inductor with a low DC-resistance (DCR), for higher efficiency and avoid inductor saturation by choosing inductors with DC current ratings that exceed the maximum current of the regulator by at least 30%. Additionally, the inductor peak-to-peak current ripple must be carefully considered along with the selected switching frequency before selecting appropriate inductor values with adequate current rating. The following equation calculates the inductor ripple current in the three operating modes.

$$\Delta I_{L(Buck-only)} = \frac{\left(1-\frac{V_{OUT}}{V_{IN}}\right) * V_{OUT}}{F_{SW} * L}$$

$$\Delta I_{L(Boost-only)} = \frac{\left(1-\frac{V_{IN}}{V_{OUT}}\right) * V_{IN}}{F_{SW} * L}$$

The Buck-Boost ripple current is the higher of the two following equations.

$$\Delta I_{L(buck-boost)} = \frac{\left(1-0.7*\frac{V_{IN}}{V_{OUT}}\right) * V_{IN}}{F_{SW} * L}$$

$$\Delta I_{L(buck-boost)} = \frac{(0.3 * V_{OUT})}{F_{SW} * L}$$

Where V_{OUT} is the output voltage, V_{IN} is the input voltage, F_{SW} is the switching frequency, and L is the inductor value.

Output Capacitor Selection

The Buck-Boost regulator is designed to take advantage of the benefits of ceramic capacitors, namely small size and very-low ESR capacitors. It is designed to operate with a 22µF capacitors. To ensure stability, ensure that the actual output capacitance is greater than 10µF. Design for an output ripple voltage less than 1% of the output voltage. The output capacitance can be increased to reduce output voltage ripple and improve load transients if needed. The following equations calculate the output voltage ripple as a function of output capacitance based on operating mode

$$V_{RIPPLE\ (Buck\text{-}only)} = \frac{\Delta I_L}{8 * F_{SW} * C_{OUT}}$$

$$V_{RIPPLE\ (Boost\text{-}only)} = \frac{I_{OUT} * \left(1-\frac{V_{IN}}{V_{OUT}}\right)}{F_{SW} * C_{OUT}}$$

$$V_{RIPPLE\ (Buck\text{-}Boost)} = \frac{I_{OUT} * \left(1-0.7*\frac{V_{IN}}{V_{OUT}}\right)}{F_{SW} * C_{OUT}}$$

Where ΔI_L is the inductor ripple current, F_{SW} is the switching frequency, and C_{OUT} is the output capacitance after taking DC bias into account and I_{OUT} is the load current.

Output capacitance affects low power mode behavior and the output capacitor discharge time at turnoff. System level evaluation should be performed to optimize the needed output capacitor value.

A capacitor's actual capacitance is strongly affected by its DC bias characteristics. The input capacitor is typically an X5R, X7R, or similar dielectric. Use of Y5V, Z5U, or similar dielectrics is not recommended. Be sure to consider the capacitor's DC bias effects and maximum ripple current rating when using capacitors smaller than 0805. Input capacitor placement is critical for proper operation. The input capacitor must be placed as close to the IC as possible. The traces from the input pin to the capacitor and from the capacitor to PGND should as short and wide as possible.

Buck-Boost PCB Layout Considerations

High switching frequencies and large peak currents make PC board layout an important part of step-down DC/DC converter design. A good design minimizes excessive EMI on the feedback paths and voltage gradients in the ground plane, both of which can result in instability or regulation errors. Follow these layout guidelines when designing the QP8817 PCB. Refer to the Active-Semi QP8817 Evaluation Kits for layout examples

1. Place the Buck-Boost input and output capacitors as close as possible to the IC. When operating in Buck-Boost mode, both the input and output capacitor placement are critical. In Boost-only mode, the output capacitor placement should have higher priority. In Buck-only mode, the input capacitor should have higher priority. Connect the input capacitors directly to VINBB and PGND. Connect the output capacitors directly to VBBST and PGND. Do not use vias to route power between the capacitors and the IC.
2. Minimize the switch node trace length between each SWx pin and the inductor. Avoid routing sensitive analog signals near these high frequency, high dV/dt traces.
3. The input capacitor and output capacitor grounds should be connected as close together as possible, with short, direct, and wide traces.
4. Connect the PGND ground pin and the AGND ground pin directly to the exposed pad under the IC. The AGND ground plane should be routed separately from the other ground planes and only connect to the main ground plane under the IC at the AGND pin.
5. Connect the exposed pad directly the top layer ground plane. Connect the top layer ground plane to both internal ground planes and the PCB backside ground plane with thermal vias. Provide ground plane routing on multiple layers that allows the IC's heat to flow into the PCB and then spread radially from the IC. Avoid cutting the ground planes and adding vias that re-

strict the radial flow of heat of operating conditions and are relatively insensitive to layout considerations.

Table 2: Buck-Boost Regulator Output Voltage Settings

B-B_VSET [3:0]	B-B_VSET [7:4]										
	0000	**0001**	**0010**	**0011**	**0100**	**0001**	**0110**	**0111**	**1000**	**1001**	**1010**
0000	0.8	1.2	1.6	2	2.4	2.8	3.2	3.6	4	4.4	4.8
0001	0.825	1.225	1.625	2.025	2.425	2.825	3.225	3.625	4.025	4.425	4.825
0010	0.85	1.25	1.65	2.05	2.45	2.85	3.25	3.65	4.05	4.45	4.85
0011	0.875	1.275	1.675	2.075	2.475	2.875	3.275	3.675	4.075	4.475	4.875
0100	0.9	1.3	1.7	2.1	2.5	2.9	3.3	3.7	4.1	4.5	4.9
0101	0.925	1.325	1.725	2.125	2.525	2.925	3.325	3.725	4.125	4.525	4.925
0110	0.95	1.35	1.75	2.15	2.55	2.95	3.35	3.75	4.15	4.55	4.95
0111	0.975	1.375	1.775	2.175	2.575	2.975	3.375	3.775	4.175	4.575	4.975
1000	1	1.4	1.8	2.2	2.6	3	3.4	3.8	4.2	4.6	5
1001	1.025	1.425	1.825	2.225	2.625	3.025	3.425	3.825	4.225	4.625	5
1010	1.05	1.45	1.85	2.25	2.65	3.05	3.45	3.85	4.25	4.65	5
1011	1.075	1.475	1.875	2.275	2.675	3.075	3.475	3.875	4.275	4.675	5
1100	1.1	1.5	1.9	2.3	2.7	3.1	3.5	3.9	4.3	4.7	5
1101	1.125	1.525	1.925	2.325	2.725	3.125	3.525	3.925	4.325	4.725	5
1110	1.15	1.55	1.95	2.35	2.75	3.15	3.55	3.95	4.35	4.75	5
1111	1.175	1.575	1.975	2.375	2.775	3.175	3.575	3.975	4.375	4.775	5

LDO/LSW

General Description

QP8817 features ten low drop out linear regulators (LDO) and load switches (LSW). The ten LDO/LSWs are separated into four sets, each with unique features that allow system level optimization. Each LDO also has a dedicated input voltage pin for system optimization.

LDO1 and LDO2

LDO1/2 are 200mA, high PSRR LDOs. They are optimized for high-PSRR. LDO1/2 feature a low power mode (LPM) that reduces quiescent current at light load conditions. LPM is enabled when bit DISCP is set to 1. DISCP is a factory bit that cannot be changed by the user.

LDO3, LDO4, LDO5 (LSW6, LSW7, LSW8)

LDO3/4/5 and LSW6/7/8 are 400mA, general-purpose LDOs. They are optimized for a low dropout voltage. LDO3/4/5 do not have a programmable LPM. LDO3/4/5 can also be configured as a 400mA load switch (LSW).

LSW6, LSW7, and LSW8

LSW6/7/8 are 1.5A load switches with overcurrent protection that can be configured as 400mA LDOs as well. However, overvoltage and undervoltage protection are disabled. LSW6/7/8 is an n-ch FET LSW. The input voltage between is 0.5V to 3.3V. Due to the lower n-ch FET Rdson, LSW can operate with up to 2A of bypass current while maintaining a low voltage drop. LSW has a fixed 100µs softstart time. The POK signal is asserted when the switch is enabled and is not in current limit. The gate driver circuit for the NMOS switch is ramped to control the soft start time for the output.

LDO9 and LDO10

LDO9/10 are low-quiescent current LDOs that optimized for always-on applications. LDO9 can support 30mA output current and LDO10 can support 15mA output current. Note that they will toggle off and on during power cycle events.

LDO9/10 require only a small ceramic capacitor with a minimum capacitance of 0.47µF for stability and typical output capacitor of 1uF. For best performance, the output capacitor should be connected directly between the output and ground, with a short and direct connection. LDO9/10 feature a constant current-limit, which protects the IC under output short-circuit conditions.

Enable / Disable Control

When power is applied to the IC, all LDO/LSWs automatically turn on according to a pre-programmed sequence. Once in normal operation (ACTIVE state), each converter can be independently disabled via I²C or GPIO. Each CMI version requires a different set of commands to disable a converter, so contact the factory for specific instructions if needed.

Each converter contains an optional integrated discharge resistor that actively discharges the output capacitor when the regulator is disabled. Each LDO's discharge function is enabled via I²C by setting the DIS_PULLDOWN_Lx = 0.

Soft-Start

Each LDO contains a softstart circuit that limits the rate of change of the output voltage, minimizing input inrush current and ensuring that the outputs power up monotonically. This circuitry is effective any time the LDO is enabled, as well as after responding to a short circuit or other fault condition. Each LDO's softstart time is adjustable to either 160µs or 320µs via its I²C bits SST_LDOx.

Output Voltage Setting

Each LDO regulates to the voltage defined by their VSET I²C register. The LDOs do not have additional VSETx registers.

Each LDO has an Output-High and an Output-Low programming range. The following tables define LDO voltage ranges and steps for each setting

Mode	Range	Step	LDO
Output-Low	0.5V-1.2875V 1.2V – 3.6V	12.5mV 50mV	1/2/3/4/5/6
Output-High	1.2V-3.6V	50mV	9/10

For LDO1/2/3/4/5, the Output-Low programming range is 0.5V to 1.2875V in 12.5mV steps or 1.2V to 3.6V in 50mV steps

VLDOx = 0.5V + VSET * 0.0125V

VLDOx = 1.2V + VSET * 0.05V

Where VSET is the decimal equivalent of the value in I²C VSET register. The VSET registers contain an unsigned 6-bit binary value.

For LDO9/10, the output programming range is 1.2V to 3.6V in 50mV steps.

VLDOx = 1.2V + VSET * 0.05V

Qorvo recommends that an LDO's output voltage be kept within +/- 25% of the default output voltage to maintain accuracy. Voltage changes larger than +/- 25% may require different factory trim settings (new CMI) to maintain accuracy.

Overcurrent and Short Circuit Protection

Each LDO provides overcurrent and short circuit protection. The overcurrent threshold is set by the LDOx_ILIM I^2C bits. In both an overload and a short circuit condition, the LDO limits the output current which causes the output voltage to drop. This can result in an undervoltage fault in addition to the current limit fault. If an LDO reaches current limit protection, the status is reported in the ILIM_REG[x] I^2C registers. The contents of these registers are latched until read via I2C. When the current limiting results in a drop-in output voltage that triggers an undervoltage condition, the IC shuts down all power supplies, asserts nIRQ low, and enters the UVLOFLT state. The IC restarts in 100ms and starts up with default sequencing. Overcurrent and short circuit conditions can be masked via the I^2C bits LDOx_ILIM_FLTMSK and LDOx_UV_FLTMSK.

The LDO contains current-limit circuitry featuring a current-limit fold-back function. During normal operation and moderate overload conditions, the regulator can support more than its rated output current. During sustained extreme overload conditions when current limit is triggered however, the current limit is reduced by approximately 30%, reducing power dissipation within the IC. The current limit has a fold back behavior in this regard where the triggering condition is higher than the regulated current value during overload.

Input Capacitor Selection

Each LDO requires a high quality, low-ESR, ceramic input capacitor. A 1uF is typically suitable, but this value can be increased without limit. Connect the input capacitor between the LDO input pin and AGND. The input capacitor should be a X5R, X7R, or similar dielectric.

Output Capacitor Selection

Each LDO requires a high quality, low-ESR, ceramic output capacitor.

LDO1/2/3/4/5 output capacitance is typically 1uF with a 0.8uF minimum capacitance value and a 10uF maximum capacitance value.

Connect the output capacitor between the LDO output pin and AGND. A capacitor's actual capacitance is strongly affected by its DC bias characteristics. The output capacitor is typically an X5R, X7R, or similar dielectric. Use of Y5U, Z5U, or similar dielectrics are not recommended due to their wide variation in capacitance over temperature and voltage ranges.

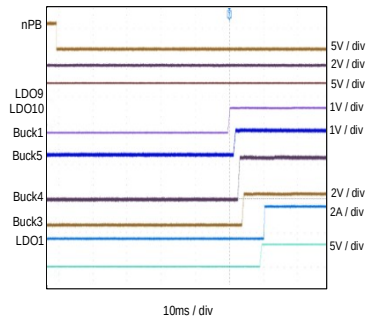
Unused LDO Outputs

If an LDO is not used, connect the VINLx pin to either GND or AVIN. Connect the LDOx output to AGND. The input and output capacitors are not needed.

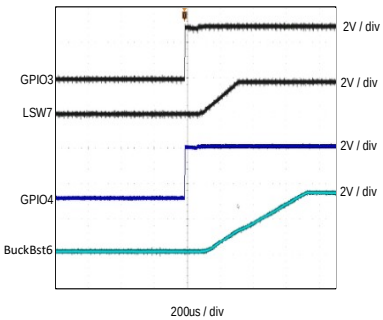
TYPICAL OPERATING CHARACTERISTICS

(VIN = 3.8V, CMI101)

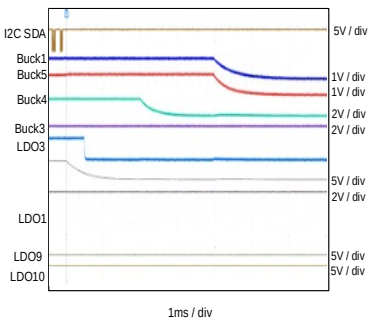
Startup Sequence



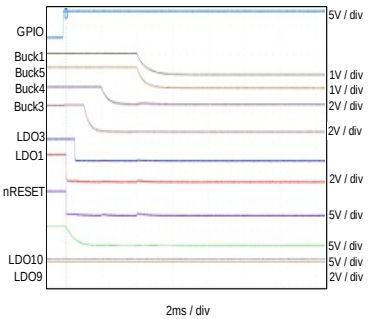
Turn-On By GPIOs



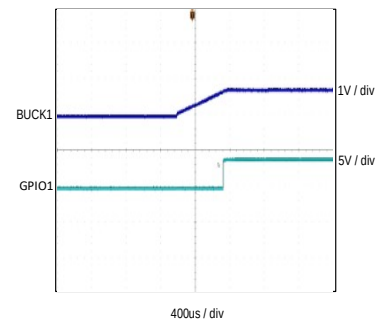
Entering Sleep Mode by I2C



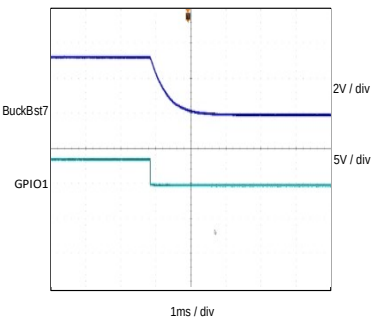
Entering DPSP Mode by GPIO



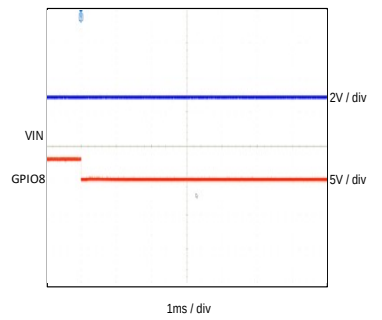
GPIO1 Edge Out with Buck1 Turned On



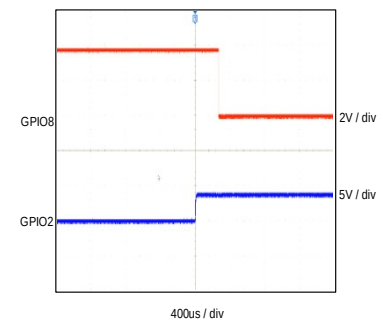
GPIO1 Edge Out with BB7 Turned Off



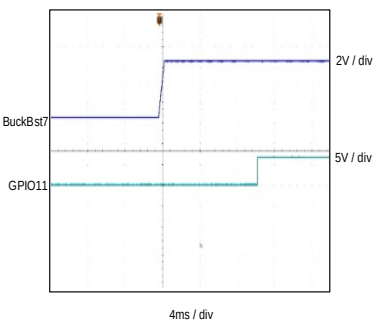
GPIO8 Interrupt Ouput by VIN Drop



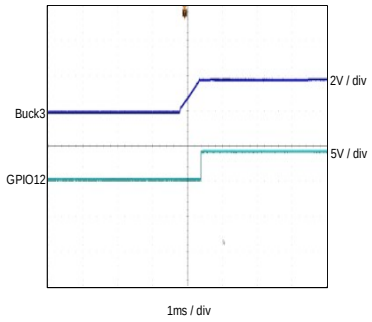
GPIO8 Interrupt Ouput by VIN Drop



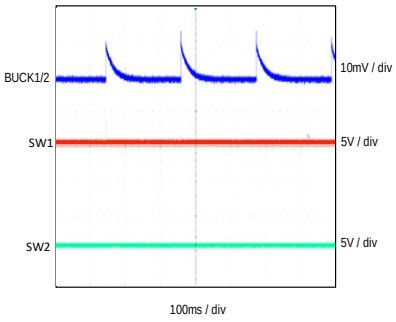
GPIO11 nRESET by BuckBoost7



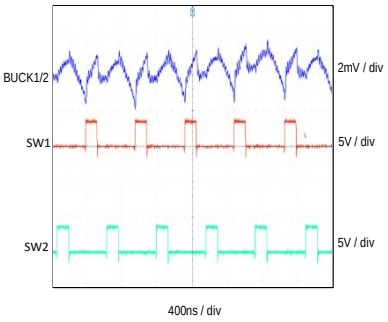
GPIO12 PowerGood of Buck3



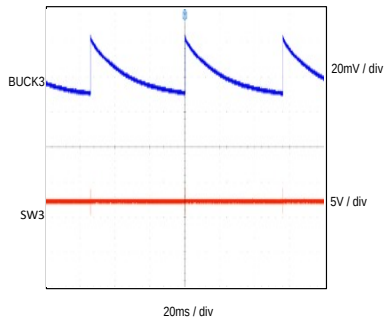
Buck1/2 Ripple (No Load)



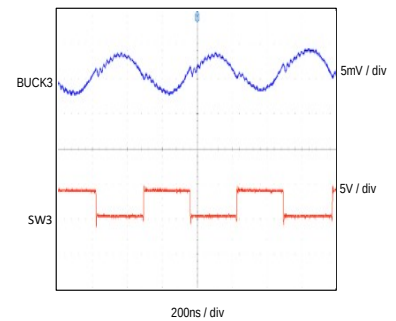
Buck1/2 Ripple (Load=10A)



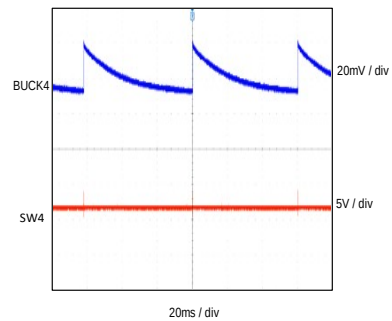
Buck3 Ripple (No Load)



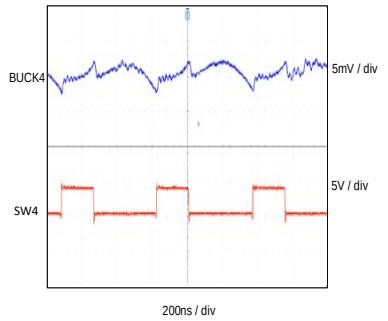
Buck3 Ripple (Load=1A)



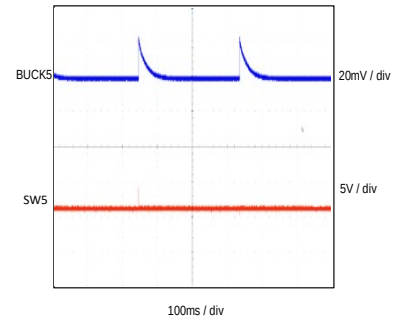
Buck4 Ripple (No Load)



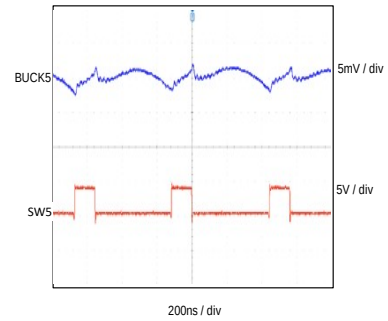
Buck4 Ripple (Load=1A)

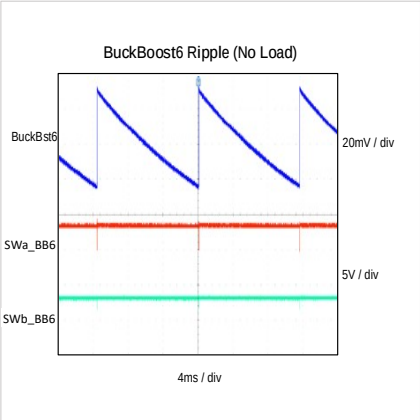


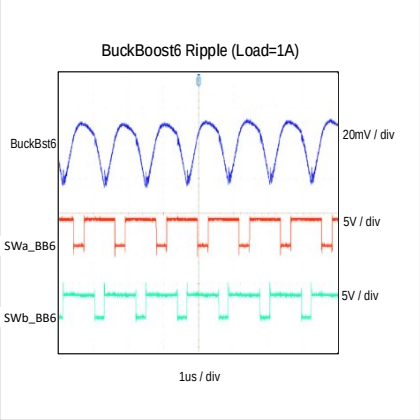
Buck5 Ripple (No Load)

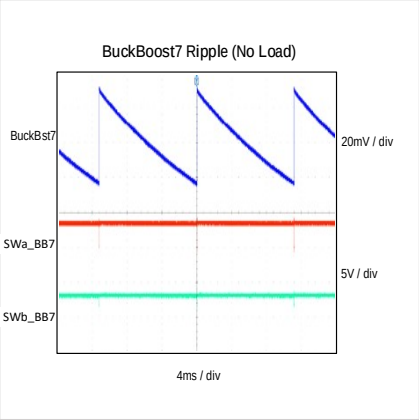


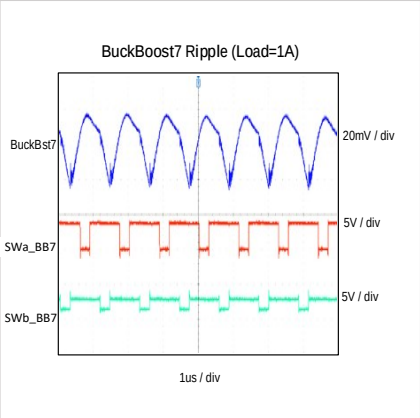
Buck5 Ripple (Load=1A)

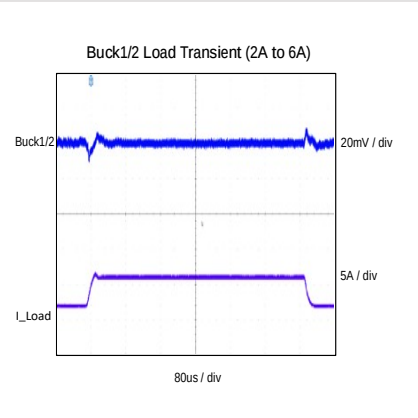


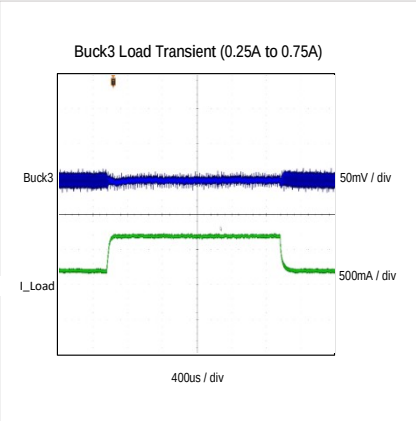


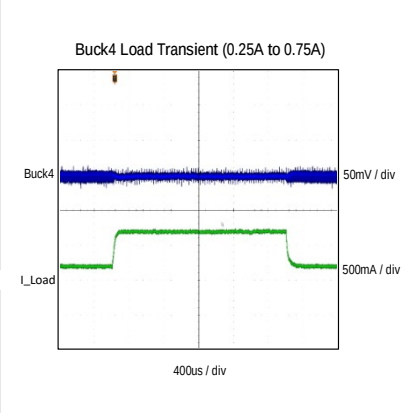


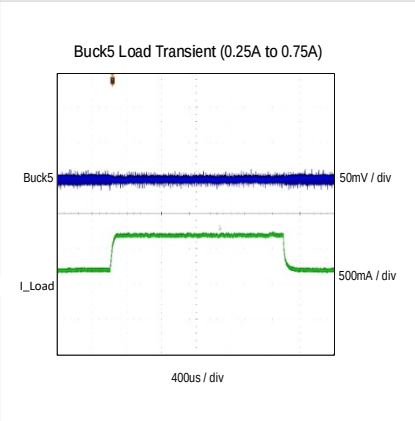


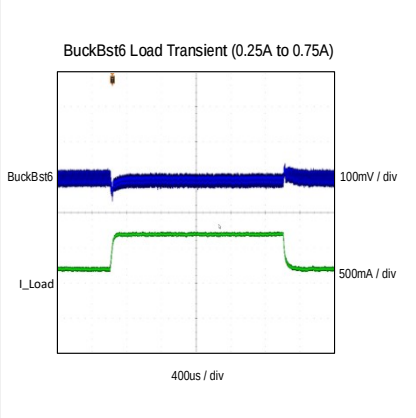


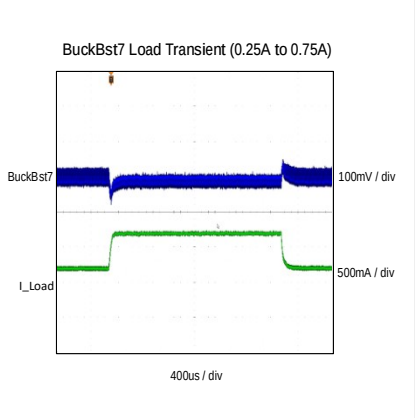


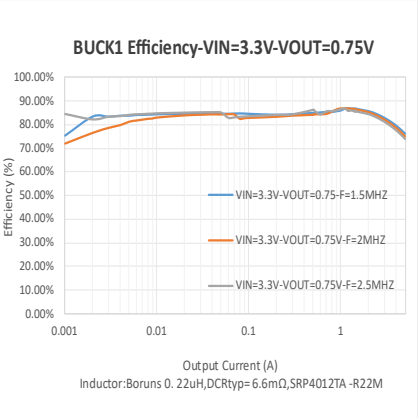


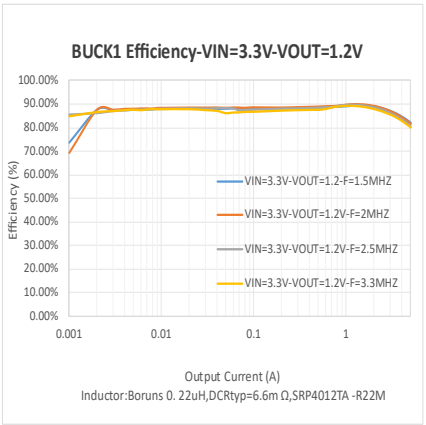


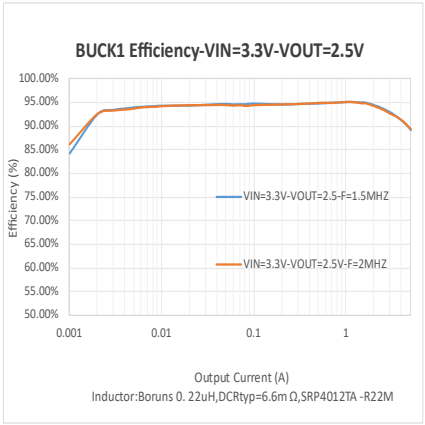


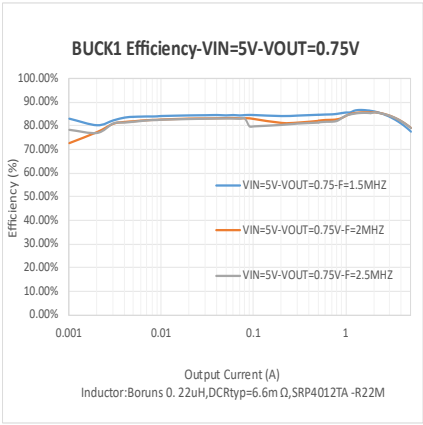


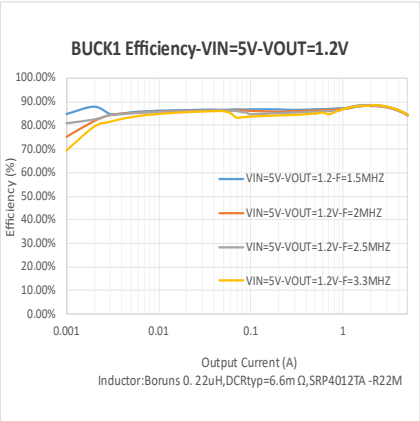


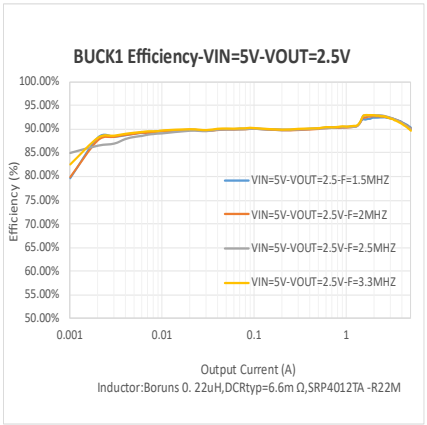


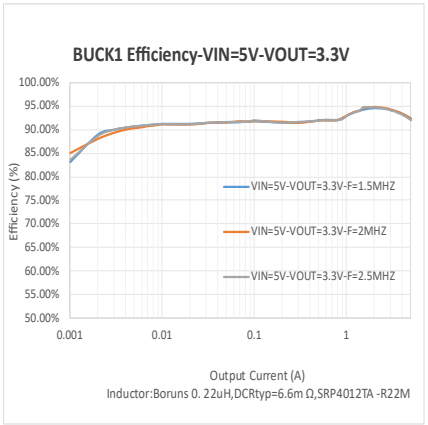


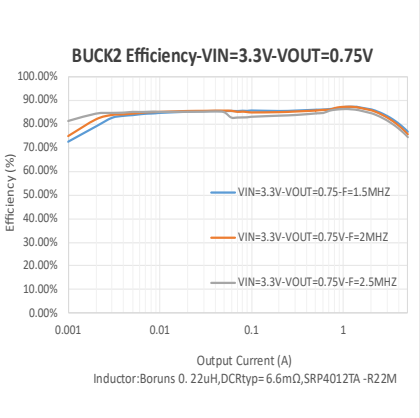


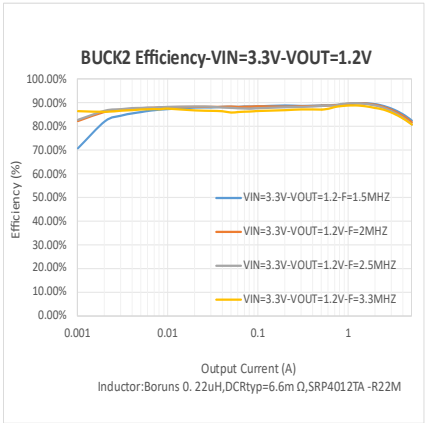


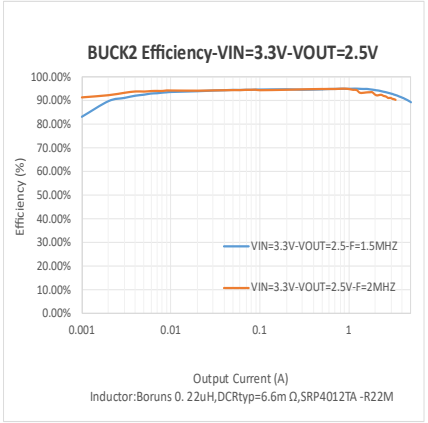


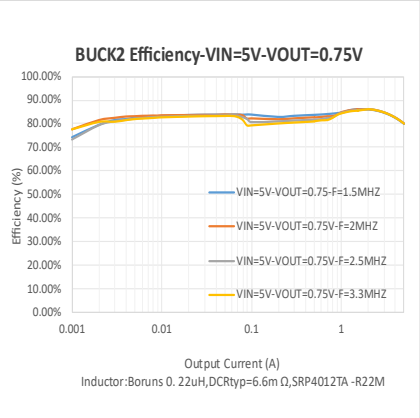


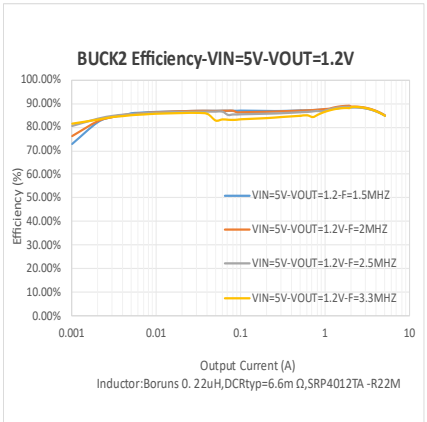


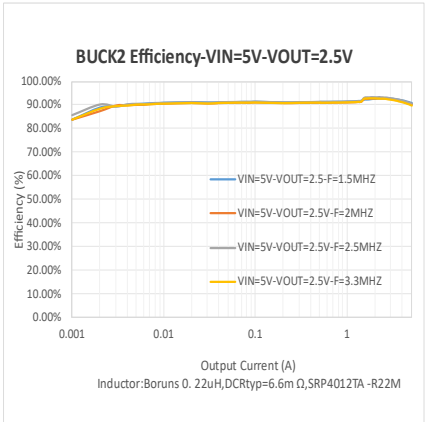


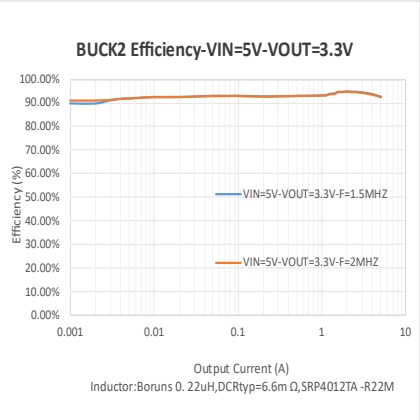


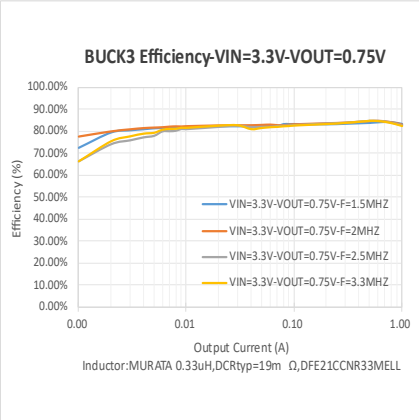


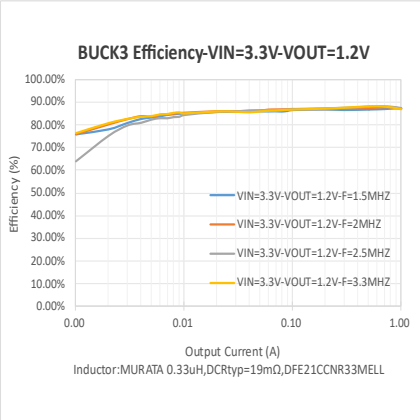


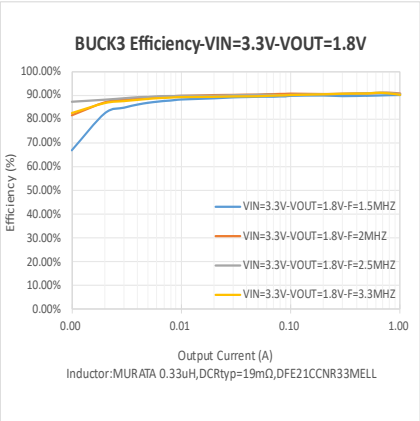


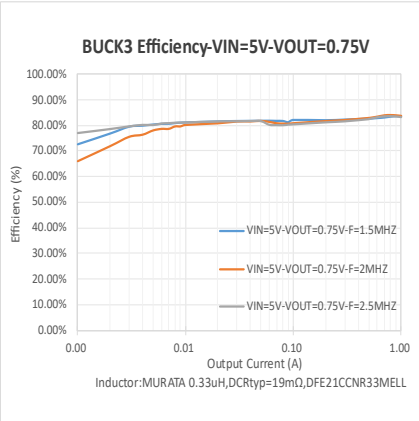


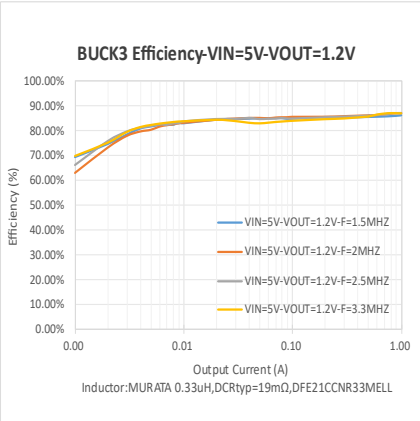


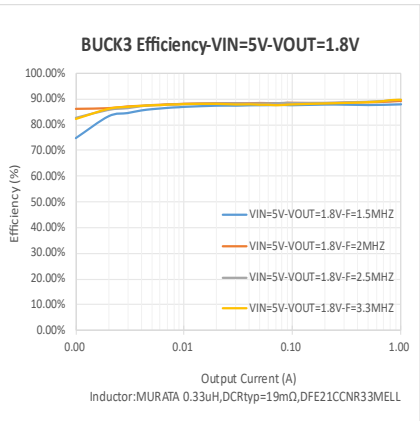


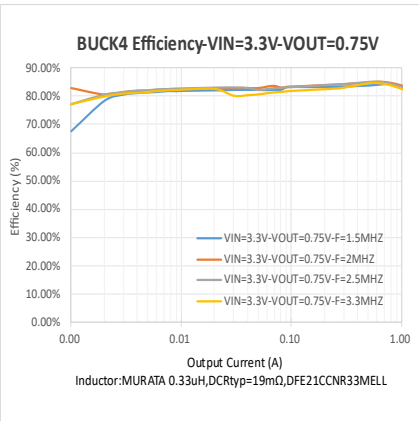


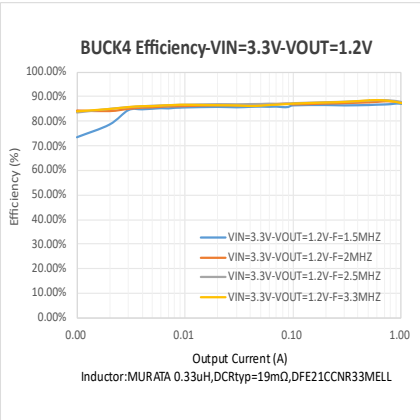


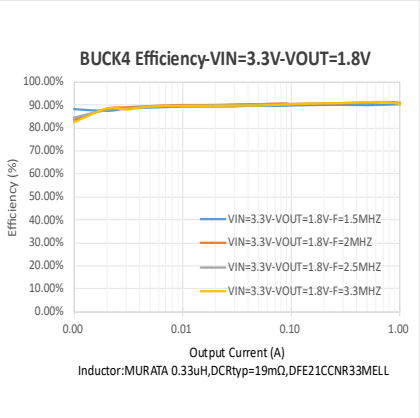


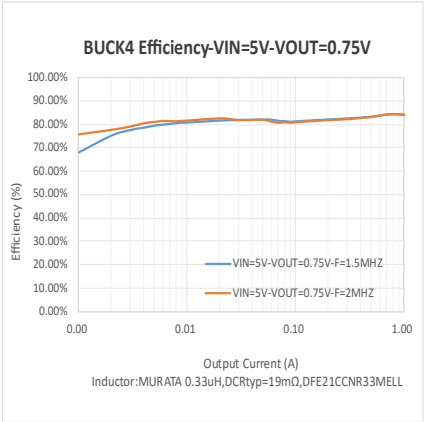


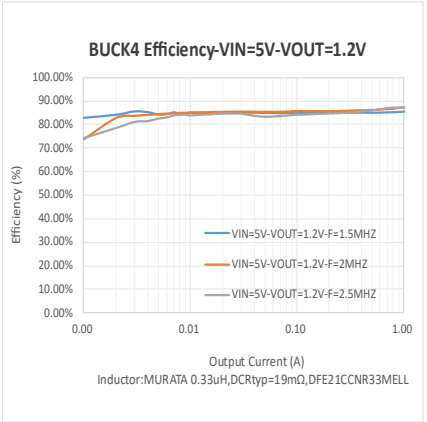


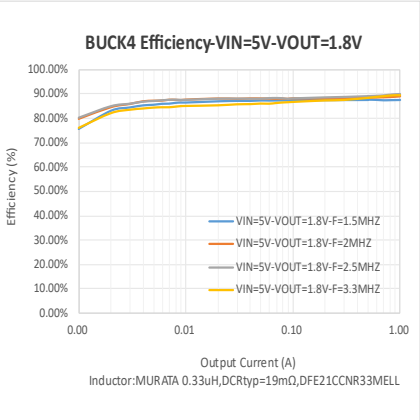


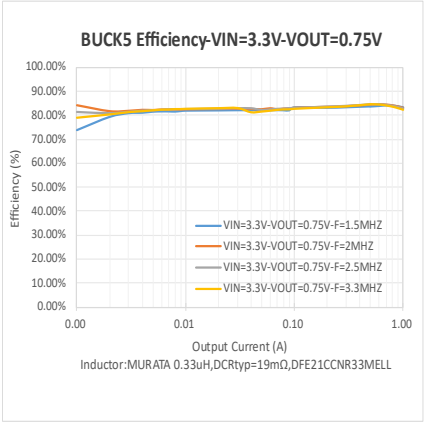


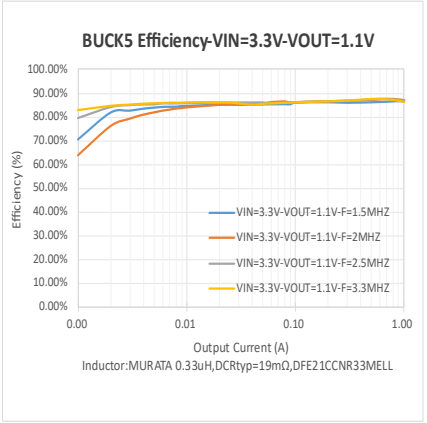


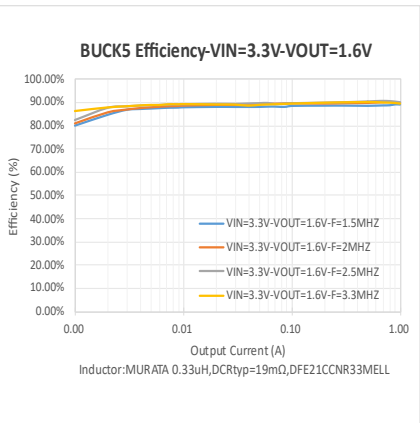


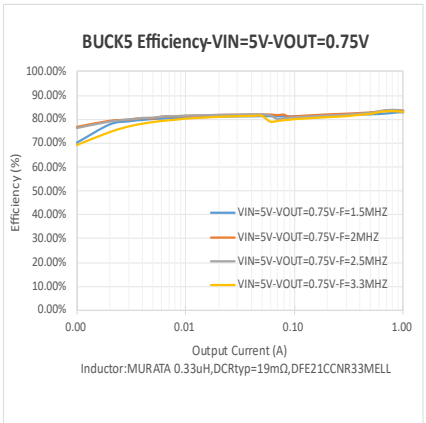


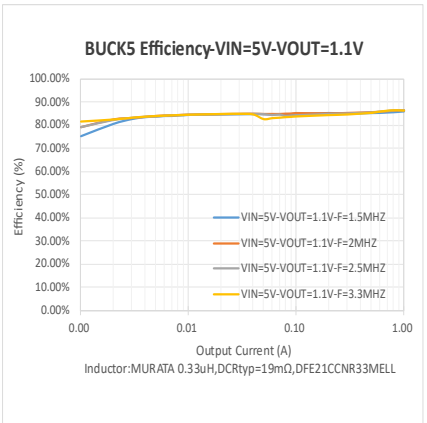


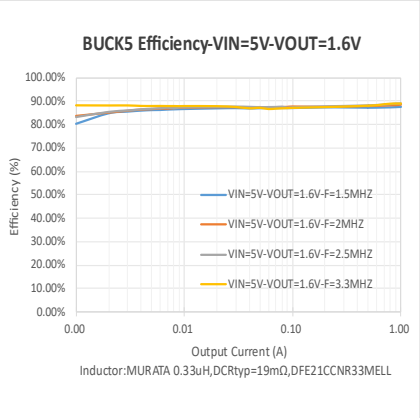


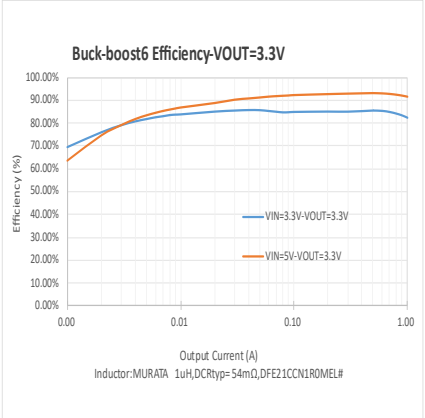


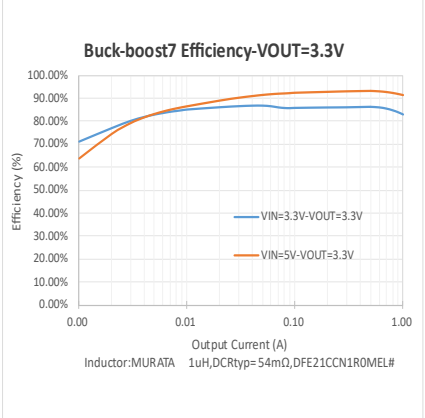


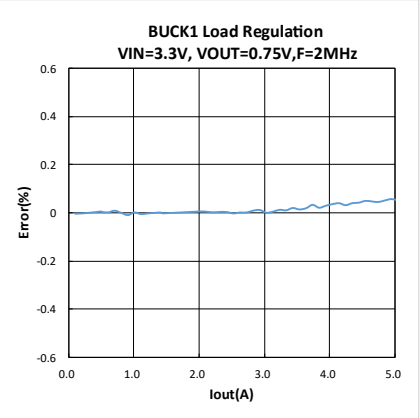


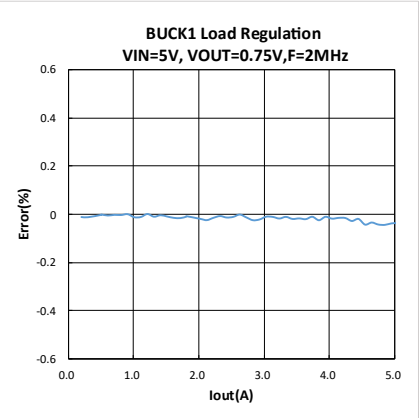


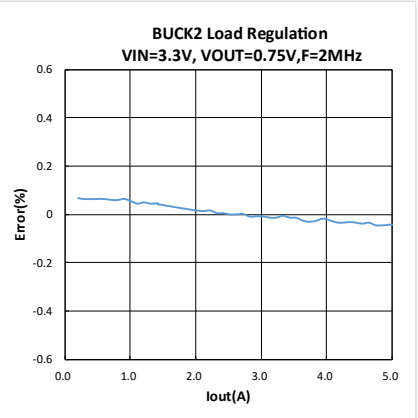


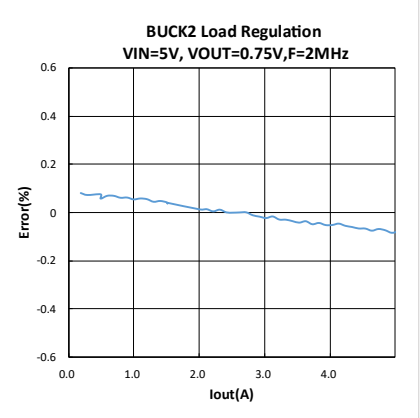


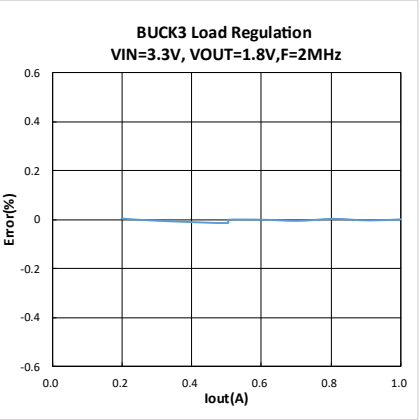


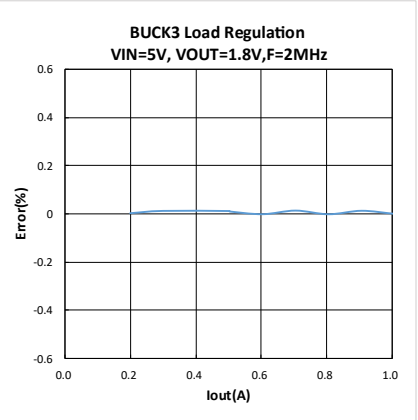


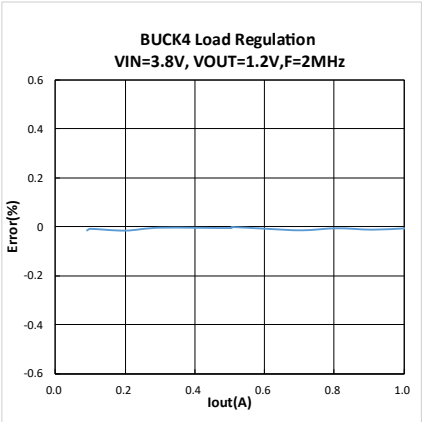


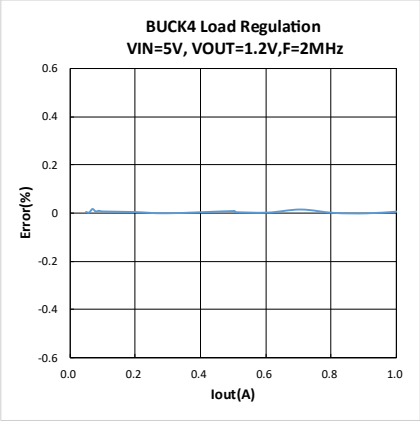


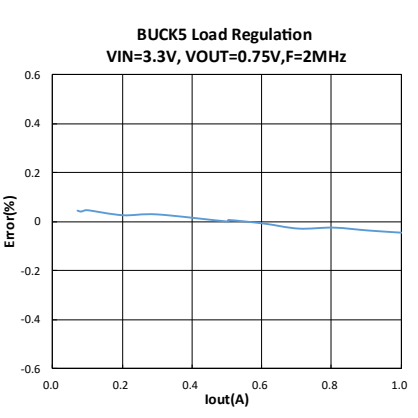


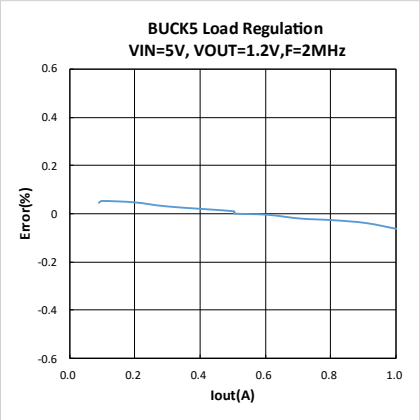


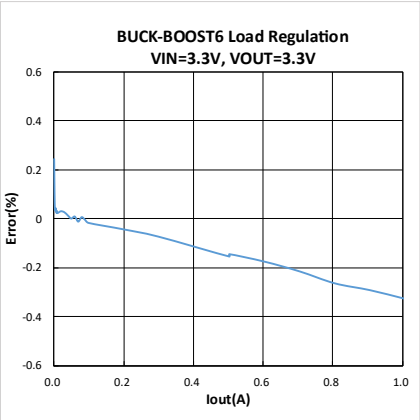


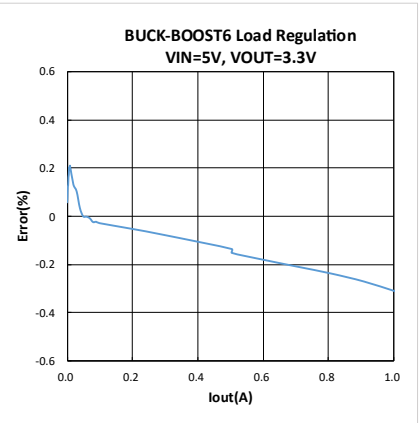


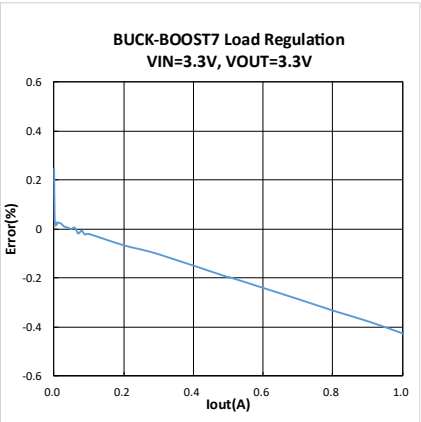


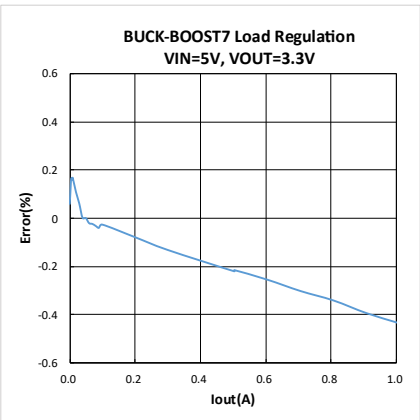


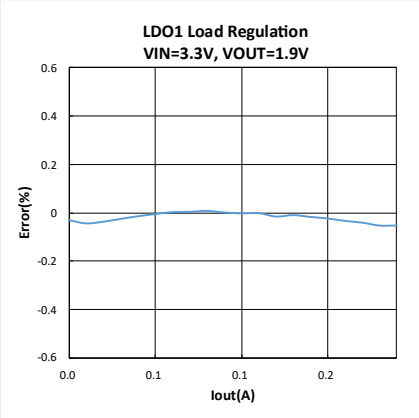


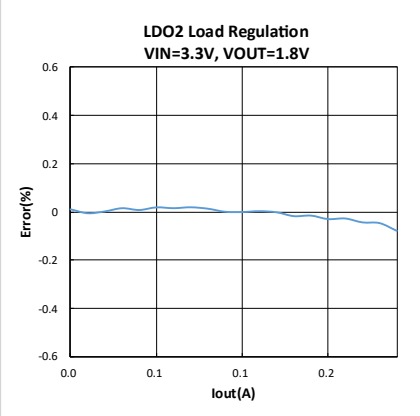


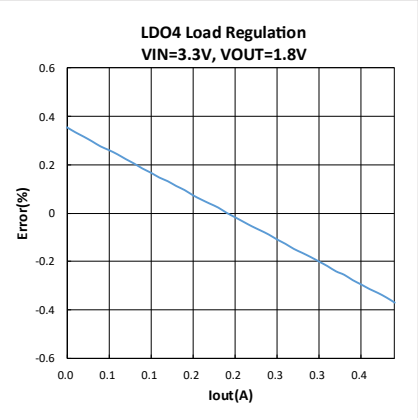


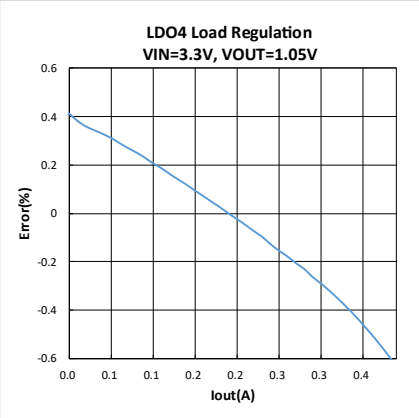












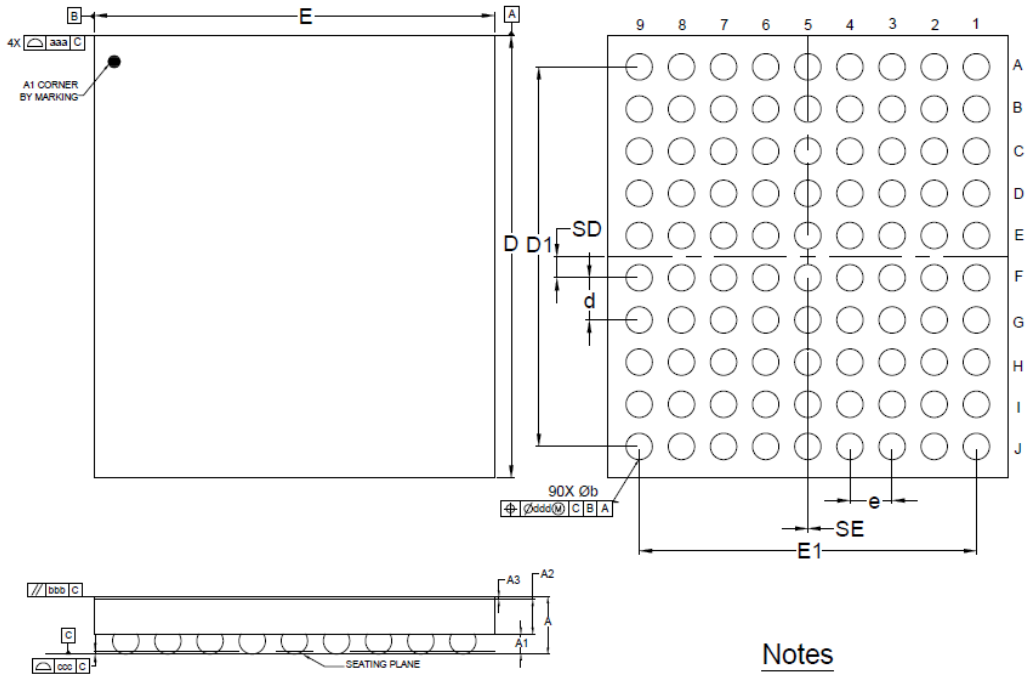
CMI OPTIONS

This section provides the basic default configuration settings for each available QP8817 CMI option. IC functionality in this section supersedes functionality in the main datasheet. Generating the desired functionality for a custom CMI sometimes requires reassigning internal resources, resulting in removal of base IC functionality. The following sections attempt to describe any removed functionality from the base IC functionality. The user is required to fully test all required functionality to ensure the CMI fully meets their requirements.

CMI A: QP8817A

CMI A is made for mass market. It is configured for a 3.8V input voltage. The output voltages and sequencing are programmable. Contact Qorvo for more details about this IC.

PACKAGE OUTLINE AND DIMENSIONS

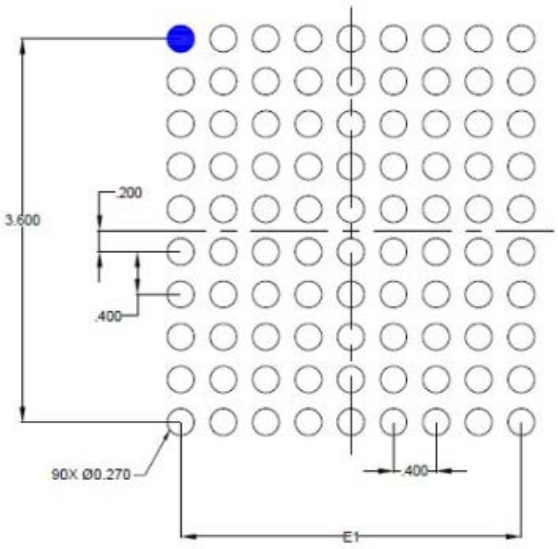


Dimensional Ref.			
REF.	Min.	Nom.	Max.
A	0.490	0.540	0.590
A1	0.145	0.165	0.185
A2	0.325	0.350	0.375
A3	0.022	0.025	0.028
D	4.155	4.170	4.185
E	3.755	3.770	3.785
D1	3.550	3.600	3.650
E1	3.150	3.200	3.250
b	0.210	0.240	0.270
d	0.400 BSC		
e	0.400 BSC		
SD	0.200 BSC		
SE	0.000 BSC		
Tol. of Form&Position			
aaa	0.10		
bbb	0.10		
ccc	0.05		
ddd	0.05		

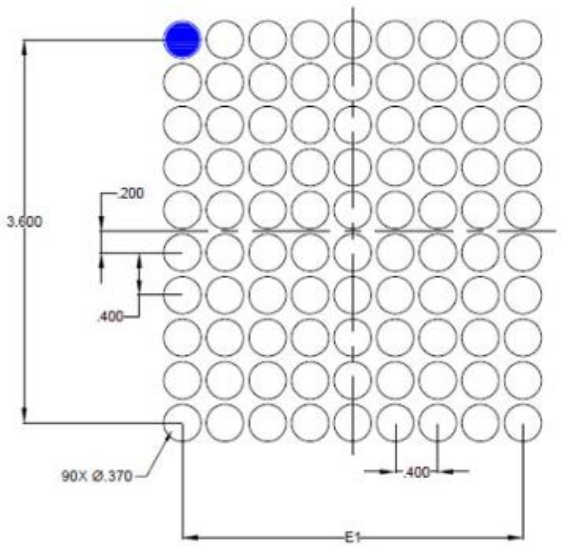
Notes

1. All DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
2. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M-1994.

1 EXAMPLE FOOTPRINT AND SOLDER MASK



Example PCB Footprint
Top View



Example PCB Solder Mask
Top View

Notes:
1. Shaded area represents Pin 1 location.

Product Compliance

This part complies with RoHS directive 2011/65/EU as amended by (EU) 2015/863.

This part also has the following attributes:

- Lead Free
- Halogen Free (Chlorine, Bromine)
- Antimony Free
- TBBP-A ($C_{15}H_{12}Br_4O_2$) Free
- PFOS Free
- SVHC Free

Contact Information

For the latest specifications, additional product information, worldwide sales and distribution locations:

Web: www.qorvo.com **Tel: 1-844-890-8163**

Email: customer.support@qorvo.com

For technical questions and application information:

Email: appsupport@qorvo.com

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