ACT82120 Datasheet Brief

Please refer to the ACT82120 Product Page for more information. Click here for a link to request the full datasheet.

BENEFITS and FEATURES

- JEITA Compliant 1.5 A, 1S, Active Power Path Switching Charger (APSC)
- On-the-Fly Adjustments to Charging Profile to Support Multi-step Battery Charging
- Dual Charging Input Support – USB or Wireless with Independent Input Current Limits
- 23 V Blocking Protection on Charger Inputs
- Max Operating Voltage of 13V on Wireless Charging Input
- Integrated Charger VBAT FET
- Integrated 1.8 V & 3.3 V Low I_Q LDOs Capable of 80 mA Output Currents
- Four 25 mA LED Drivers with 50 mV Drop Out & Programmable Drive Current, Duty Cycle, & PWM Period
- Integrated Volatile Memory for 3 LED Animation Sequences
- Push Button Input with Short, Medium, and Long Press Detection
- Support for Ultra-Low Power Shipping Mode
- 1MHz I2C Compliance with Programmable Address for PMIC Configuration & System Communication
- 2.86 x 2.90 mm 42 Balls 0.4 mm Pitch WLCSP

APPLICATIONS

- Earbud Charging Cases
- IoT Devices
- Portable Single Cell Battery-Powered Electronics

GENERAL DESCRIPTION

The ACT82120 provides a complete one cell charging ecosystem optimized for portable electronic devices in a single highly integrated PMIC. This IC combines a 1.5 A JEITA switching battery charger with integrated VBAT control MOSFET plus two low I_Q LDOs, push-button input, and four 25 mA LED drivers.

Design flexibility is offered through full programmability of the charging profile including pre-charge current, fast charge current, termination current, charge voltage, and battery temperature protection. Additionally, On-the-Fly adjustments to the charging profile allow for fine-tuned, multi-loop charge profiles through communication with an external MCU or processor. Support for both wireless charging and wired charging over USB-C, with smart selection between options, enhances the flexibility of the PMIC to accommodate the needs of many applications.

The ACT82120 provides two auxiliary rails from low I_Q LDOs for powering any peripheral loads in the system. Additionally, the switching charger allows the system voltage to be regulated at the battery voltage for operation even when the battery is completely discharged or removed. When extra power savings are required, the PMIC can be placed into a low I_Q Ship Mode with only two LDOs and basic Push Button and Charge source detection functionality.

A combination of push-button input and quad channel LED drivers allows for basic end user interaction without the need for microcontroller communication. The push-button input can detect short, medium, long, and quick presses with programmable time thresholds for each event. Onboard volatile storage of three flashing sequences for the LED drivers allows for standby, charging, or other status indication.

Communication through the I2C bus allows for configuration of the PMIC during the design process and on-the-fly communication to a microcontroller in end applications. Onboard NVM storage of all programable settings lets the system be fully operational upon start up with minimal external communication. A small form factor WLCSP and few required external components keep the overall solution size compact.

TYPICAL APPLICATION DIAGRAM

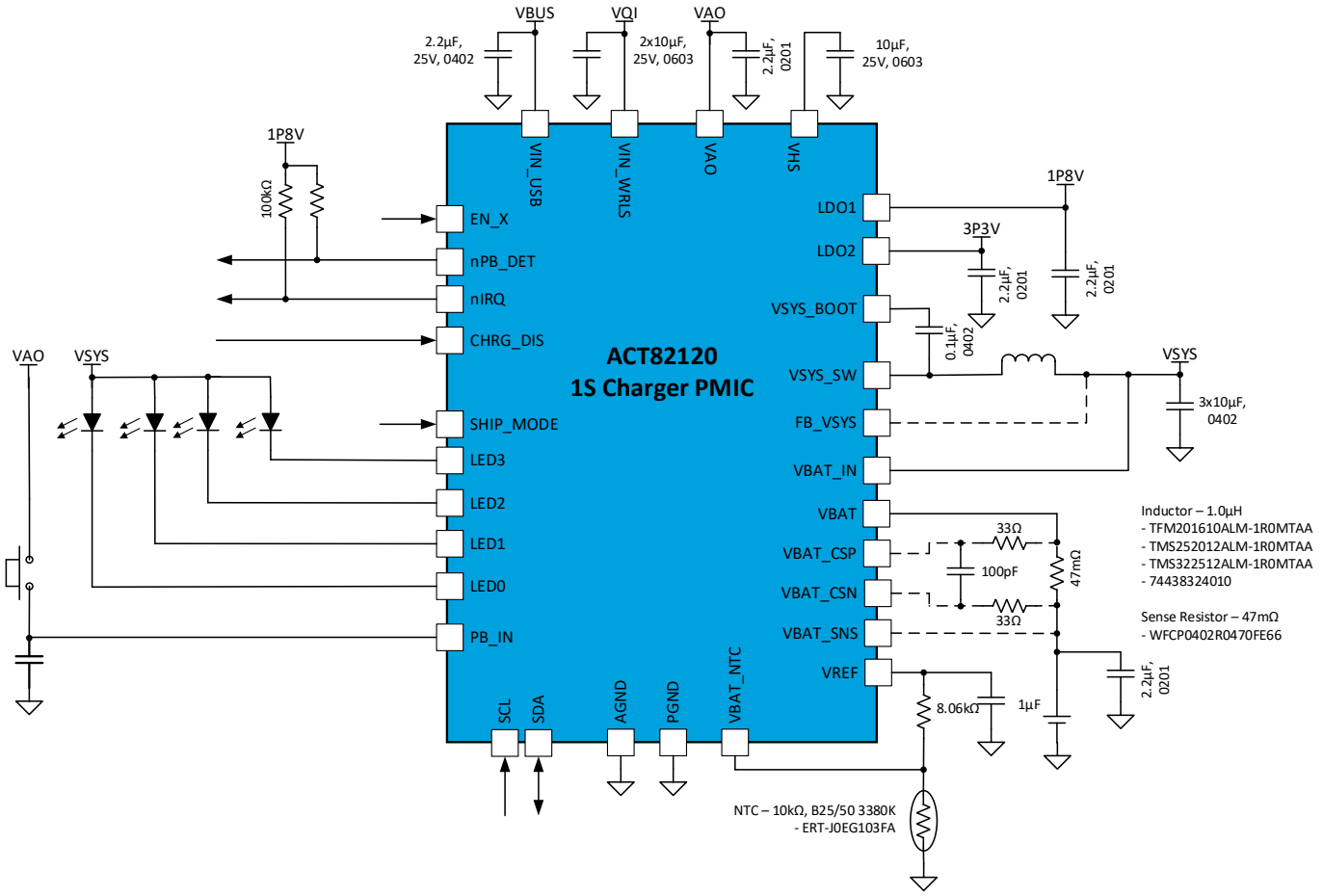


Figure 1: Simplified Applications Schematic

FUNCTIONAL BLOCK DIAGRAM

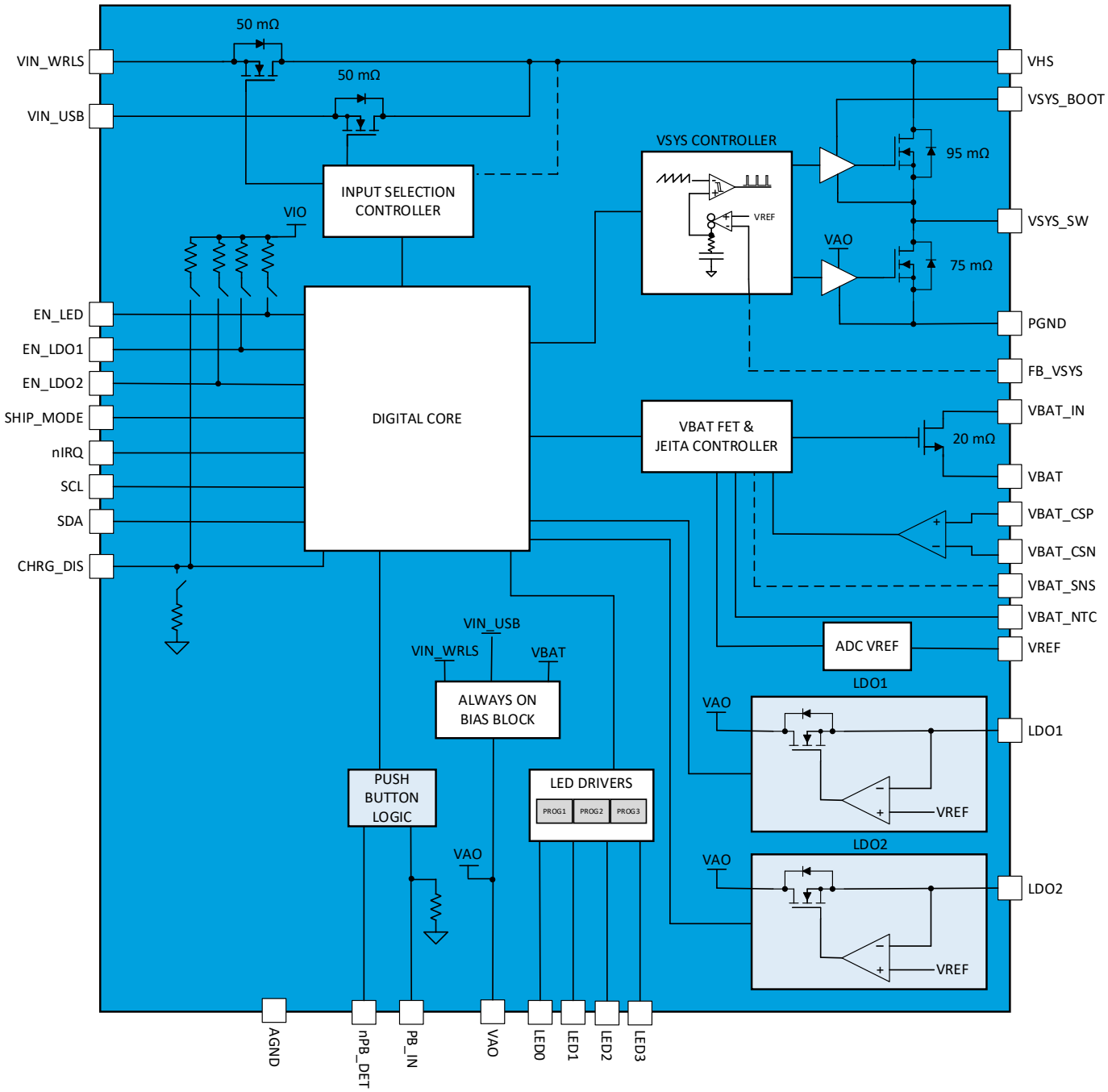
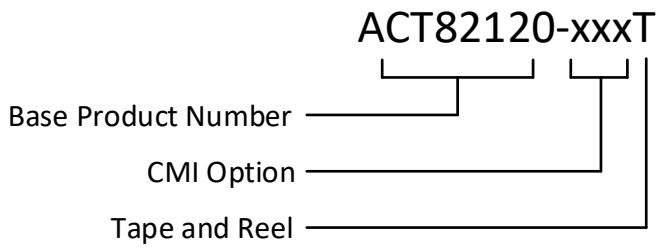


Figure 2: ACT82120 Block Diagram

ORDERING INFORMATION

PART NUMBER	DESCRIPTION
ACT82120-101T	Base PMIC Configuration



Note1: Standard product options are identified in this table. Contact factory for custom options, minimum order quantity required.
Note2: “xxx” represents the CMI (Code Matrix Index) option The CMI identifies the IC’s default register settings.

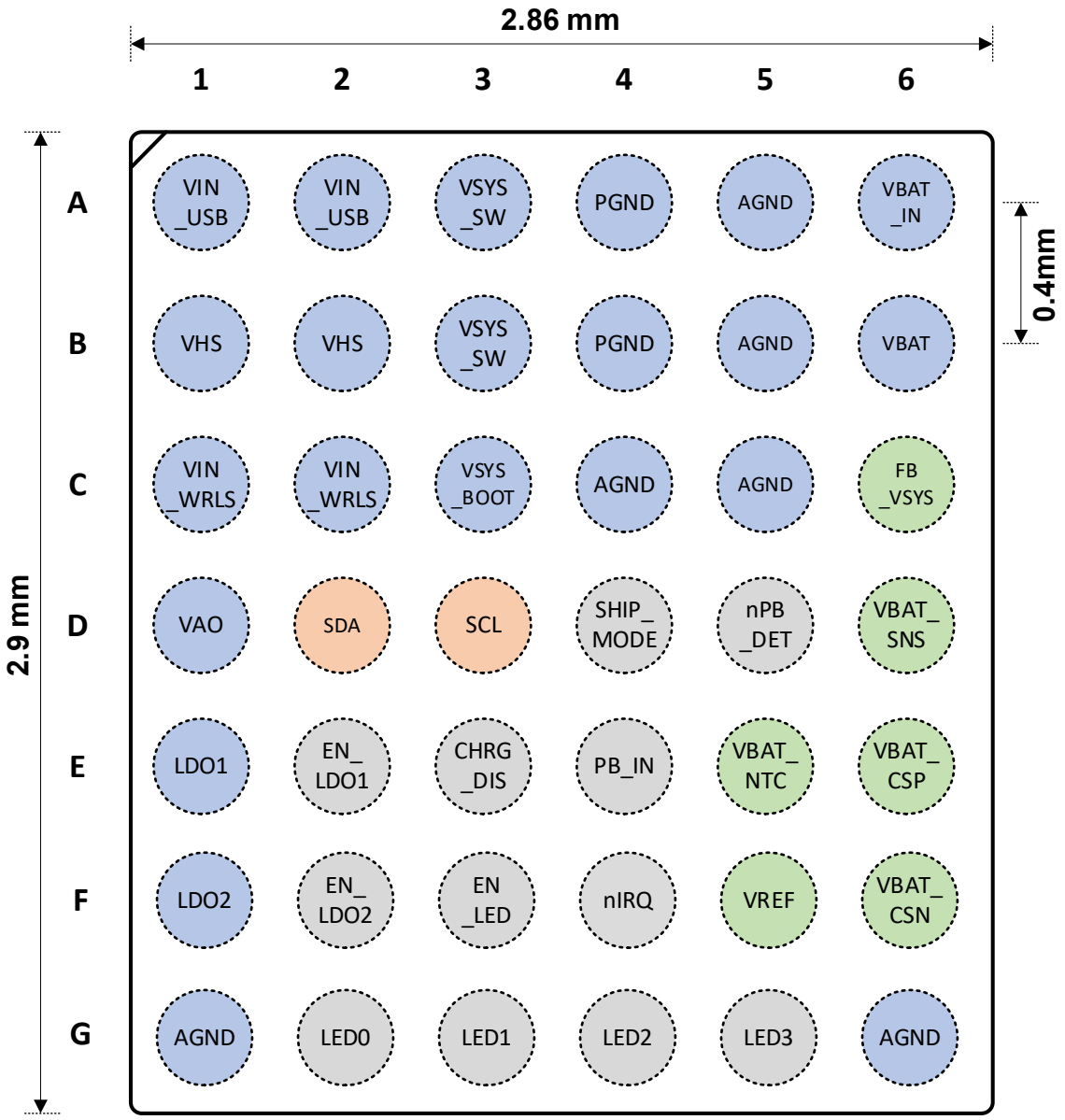


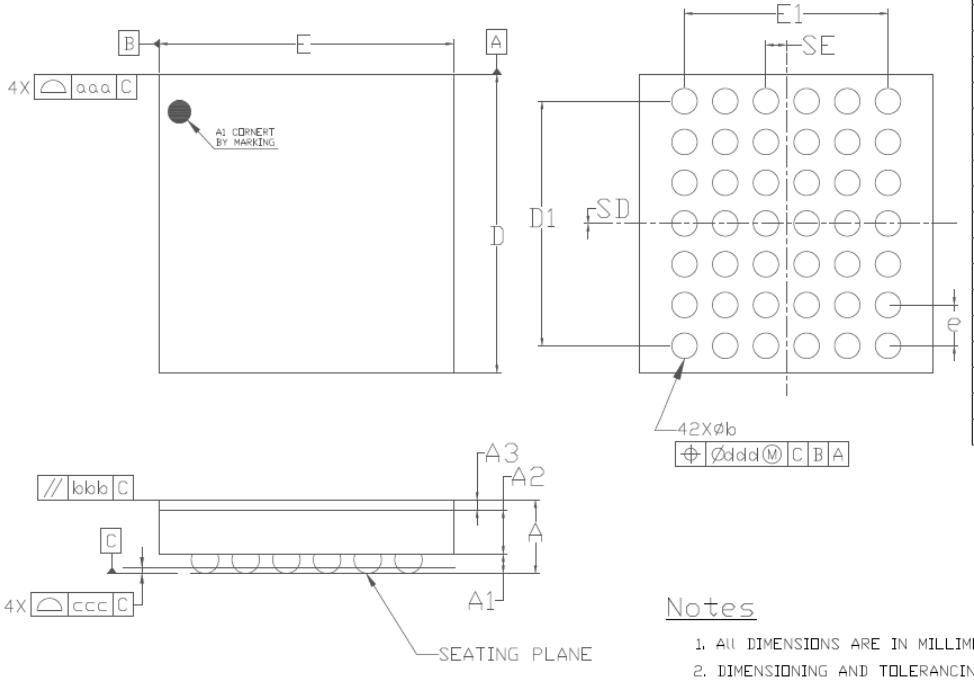
Figure 3: Pinout 42 Ball WLCSP, 0.4mm Pitch – Top View

PIN DESCRIPTIONS

PIN	NAME	DESCRIPTION
A1, A2	VIN_USB	5 V USB Input Supply to the PMIC. Decouple with appropriate capacitor.
A3, B3	VSYS_SW	Switch Node for the VSYS Regulator. Connect to inductor through short, wide copper pour.
A4, B4	PGND	Power Ground – Tie to larger PCB ground planes.
A5, B5, C4, C5, G1, G8	AGND	Analog Ground – Tie to larger PCB ground planes.
A6	VBAT_IN	Battery Charger Input Supply Connection. Connect to VSYS regulator output.
B1, B2	VHS	PMIC Power Supply from either the USB or Wireless Charger Supply Pins. Decouple with appropriate capacitor.
B6	VBAT	Battery Charger Output. Connect to positive terminal of battery current sense resistor.
C1, C2	VIN_WRLS	Wireless Charging Input Supply to the PMIC. Decouple with appropriate capacitor.
C3	VSYS_BOOT	VSYS Upper FET Bootstrap Connection. Connect bootstrap capacitor between BOOT_SYS and SW_SYS pins.
C6	FB_VSYS	VSYS Regulator Sense Line. Kelvin connect to VSYS Output Node.
D1	VAO	Always on regulator powering the internal IC blocks. Do not power external circuitry from this pin. Decouple with at least 1 µF of effective capacitance after DC bias derating is taken into account.
D2	SDA	I2C Data Pin. Connect to appropriate pull-up resistor.
D3	SCL	I2C Clock Pin. Connect to appropriate pull-up resistor.
D4	SHIP_MODE	Active High Input Pin to configure the PMIC into a low power state.
D5	nPB_DET	Active Low Signal generated from 3-tier Push Button Input.
D6	VBAT_SNS	VBAT Sense Pin to monitor battery voltage. Kelvin connect to positive terminal of battery.
E1	LDO1	LDO1 Output Pin. Decouple with appropriate capacitor.
E2	EN_LDO1	LDO1 Enable Pin. If pulled up to an off PMIC supply, ensure voltage is less than VAO for low leakage in Ship Mode & Deep Sleep.
E3	CHRG_DIS	Charge Disable Pin. Tie high to disable battery charging. Internal pulldown allows for either floating or tying pin low to enable charging.
E4	PB_IN	Push Button Input supporting 3 tier control.
E5	VBAT_NTC	Battery Temperature Monitor Pin. Connect to NTC resistor divider from VREF.
E6	VBAT_CSP	Battery Charger Current Sense Amplifier Positive Input Pin. Kelvin connect to positive side of battery current sense resistor.
F1	LDO2	LDO2 Output Pin. Decouple with appropriate capacitor.
F2	EN_LDO2	LDO2 Enable Pin. If pulled up to an off PMIC supply, ensure voltage is less than VAO for low leakage in Ship Mode & Deep Sleep.
F3	EN_LED	LED Driver Enable Pin. If pulled up to an off PMIC supply, ensure voltage is less than VAO for low leakage in Ship Mode & Deep Sleep.
F4	nIRQ	Open-Drain Interrupt Output. nIRQ goes low to indicate a fault condition and remains low

		until the appropriate Status Register is read to clear the interrupt flag.
F5	VREF	Reference voltage output for ADC temperature measurement circuit. Connect to top of Resistor-NTC voltage divider to VBAT_NTC pin. Do no power external circuitry from this pin. Decouple with appropriate capacitor.
F6	VBAT_CSN	Battery Charger Current Sense Amplifier Negative Input Pin. Kelvin connect to negative side of battery current sense resistor.
G2	LED0	Low-side LED Driver Pin
G3	LED1	Low-side LED Driver Pin
G4	LED2	Low-side LED Driver Pin
G5	LED3	Low-side LED Driver Pin

PACKAGE OUTLINE AND DIMENSIONS



Dimensional Ref.			
REF.	Min.	Nom.	Max.
A	0.515	0.540	0.565
A1	0.140	0.165	0.190
A2	0.335	0.350	0.365
A3	0.022	0.025	0.028
E	2.845	2.860	2.875
D	2.885	2.900	2.915
E1	1.950	2.000	2.050
D1	2.350	2.400	2.450
b	0.216	0.240	0.264
e	0.400 BSC		
SD	0.000 BSC		
SE	0.200 BSC		
Tol. of Form&Position			
aaa	0.10		
bbb	0.10		
ccc	0.05		
ddd	0.05		

Notes

1. ALL DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
2. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M-1994.

Product Compliance

This part complies with RoHS directive 2011/65/EU as amended by (EU) 2015/863.

This part also has the following attributes:

- Lead Free
- Halogen Free (Chlorine, Bromine)
- SVHC Free
- PFOS Free
- Antimony Free
- TBBP-A (C15H12Br402) Free

Contact Information

For the latest specifications, additional product information, worldwide sales and distribution locations:

Web: www.qorvo.com **Tel: 1-844-890-8163**

Email: customer.support@qorvo.com

For technical questions and application information:

Email: appsupport@qorvo.com

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