Introduction to Modulation of 3-Phase Inverters

Abstract

This application note introduces three widely used modulation techniques for hard-switched, two-level, three-phase voltage source inverters (2L-VSI): sinusoidal pulse width modulation (SPWM), space vector modulation (SVM), and discontinuous modulation. It explains their operating principles, implementation considerations, and performance tradeoffs in motor control and grid-connected applications. SPWM offers simplicity and phase independence but with limited DC link voltage utilization. SVM improves voltage utilization by approximately 15% and requires a floating neutral point, while discontinuous modulation significantly reduces switching losses without additional hardware. The discussion emphasizes modulation depth, harmonic performance, and efficiency implications for permanent magnet synchronous motor (PMSM) drives and similar systems.

1. Introduction

Modulation methods can be dizzyingly complex, especially when considering system-level interactions. There is also extensive literature about inverter modulation, so it can be difficult to know where to start. The intention here is to highlight three widely used modulation methods, with an emphasis on what happens in the inverter and its load. Sinusoidal pulse width modulation (SPWM) is presented first, followed by space vector modulation (SVM), and finally discontinuous modulation. The scope is limited to the hard-switched, 2-level, 3-phase voltage source inverter (2L-VSI) that can operate at any power factor. These modulation methods apply to various applications, from active front end rectification to electrical machine drive of any type except brushless DC (BLDC), which is a separate topic.

2. 2L-VSI

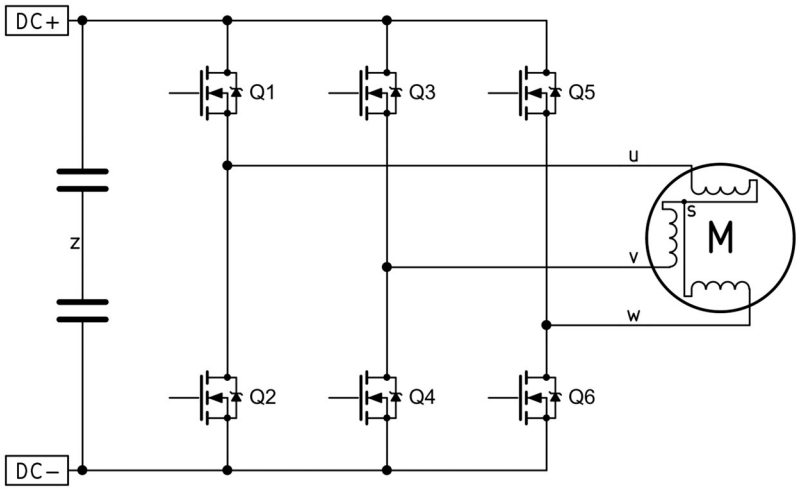


Fig. 2-1. 2l-VSI and permanent magnet synchronous motor

Fig. 2-1 shows a 2L-VSI connected to a permanent magnet synchronous motor, which could be some other load or a connection to an AC grid through a filter circuit. Some definitions are required before continuing with modulation methods. The inverter power source is the DC link, labelled DC+ and DC- in Fig. 2-1. To avoid confusion with other literature, the notation for the total DC link voltage from DC- to DC+ is V_{bus}. The DC link is “voltage stiff”, supported by a capacitor bank that supplies or absorbs high frequency ripple currents that are a normal aspect of inverter operation. The capacitor bank in Fig. 2-1 is drawn split with midpoint labeled ‘*z*’, however the capacitor bank of a 2-level inverter need not be split. In fact, the DC link voltage for a PM motor drive is generally not so high to require series-connecting capacitors. Therefore, point z is usually virtual, and reference and carrier voltages refer to it. The node labelled ‘*s*’ in the PM motor Fig. 2-1 is the star-connected neutral point of the three stator windings (the load).

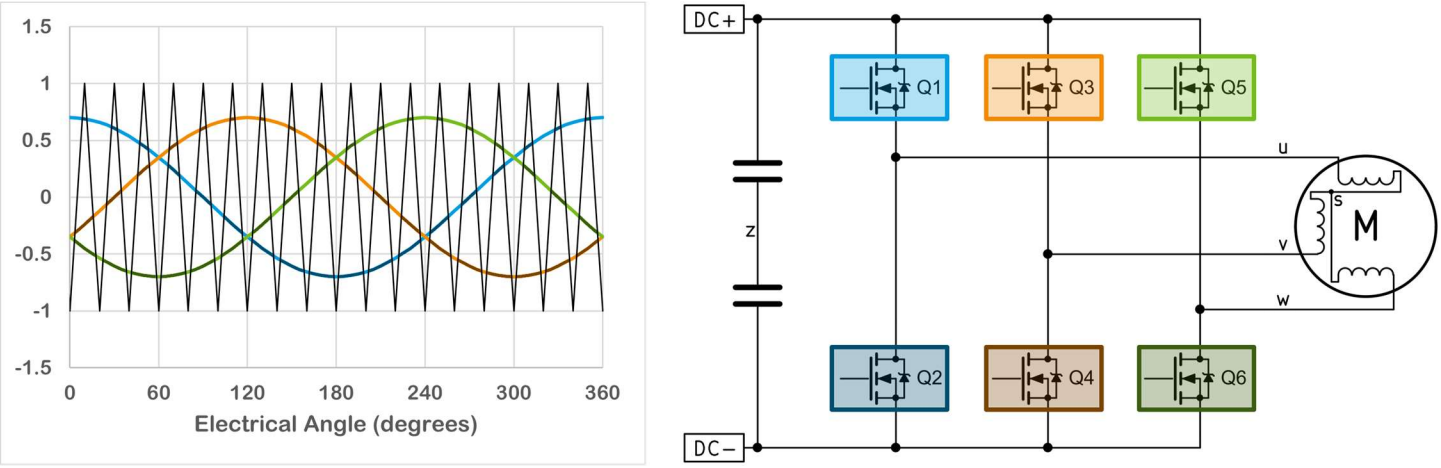
Safe operation of a 2L-VSI is governed by two simple rules:

1. The switches in each half-bridge must never conduct simultaneously.
2. Each switch must allow reverse current to flow regardless of whether the switch is on or off.

The first rule prevents shorting the DC link, which would cause catastrophic failure due to rapid overheating of the half-bridge switches. The second rule allows continuous current flow through an inductive load regardless of inverter switching. When one switch in a half-bridge switches off, there is a short deadtime when both half-bridge switches are off. Current can “freewheel” (flow in the reverse direction) through the other switch that subsequently turns on after the deadtime (synchronous rectification).

3. Sinusoidal Pulse Width Modulation

SPWM compares two waveforms to determine timing and pulse durations: modulation control and carrier. We call a modulation control waveform a reference voltage. It determines the fundamental AC frequency.



(a) (b)

Fig. 3-1. (a) Reference and carrier waveforms with M = 0.7, (b) 2L-VSI with colored switch positions corresponding to waveforms in (a)

The reference waveforms normalized to $V_{bus}/2$ in Fig. 3-1(a) are identical except for a 120-degree offset from each other. They are of the form

$$v_{uz}^{*} = M\cos(\omega_0 t) \tag{1}$$

$$v_{vz}^{*} = M\cos\left(\omega_0 t - \frac{2\pi}{3}\right) \tag{2}$$

$$v_{wz}^{*} = M\cos\left(\omega_0 t + \frac{2\pi}{3}\right) \tag{3}$$

Where $M = \frac{V_0}{V_{bus}/_2}$ is the modulation factor, also known as modulation index, and ω_0 is the fundamental angular frequency, and $\theta_0 = \omega_0 t$ is fundamental electrical angle. The * indicates reference voltage. V_0 is the peak amplitude of the fundamental output voltage, which is the voltage between the load neutral point *s* and the corresponding phase output. The reference and carrier voltages refer to the DC link midpoint *z*.

The carrier waveform determines the switching frequency. Note that the carrier frequency in Fig. 3-1(a) is artificially low for clarity. The carrier is either sequential ramps (shark tooth) or triangular. Sine-triangle modulation uses a triangular carrier as shown in Fig. 3-1(a). It is a popular SPWM variant for inverters due to lower output voltage harmonics. When a reference exceeds the carrier, the corresponding phase output is tied to DC+ by turning on its top switch; otherwise, it ties to DC-. Switch positions Fig. 3-1(b) are on when their color matches corresponding sections of reference waveforms in (a).

By inspecting the reference voltage equations, we see that the maximum amplitude for V_0 with SPWM is $V_{bus}/2$ when $M = 1$. What this means physically is the voltage between the load neutral point *s* and the DC link midpoint *z* is zero, or written as an equation, $v_{sz} = 0$. SPWM modulates each phase independently, so the load neutral point need not float. If accessible, it can connect to the DC link midpoint, which facilitates filtering electro-magnetic interference (EMI). Independent control of each phase is useful for testing inverters with an artificial load, which is a subject for a separate application note.

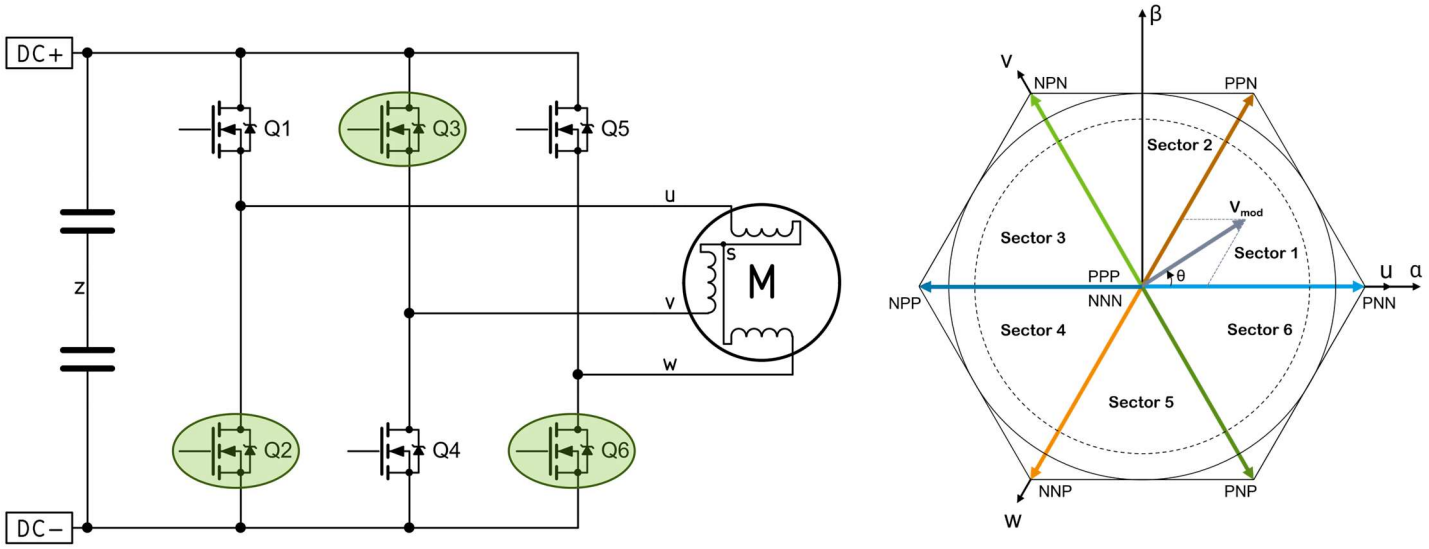
There is a widespread notion that 3-phase inverter systems require a carrier frequency that is an odd triplen multiple of the fundamental frequency for harmonic cancellation between phases, particularly for low carrier/fundamental frequency ratios. There is justification for an odd, integer carrier/fundamental frequency ratio for single-phase inverters with a very low frequency ratio, but this does not apply to 3-phase inverters. Furthermore, modern digital controllers have high performance and readily support high carrier/fundamental frequency ratios where low-frequency harmonic cancellation is not a concern. See [1] for details.

The following are additional observations about SPWM.

- SPWM works with any number of inverter phases.
- Overmodulation occurs when $M > 1$, which creates distortion in fundamental waveforms and should be avoided.
- What has been described so far is naturally sampled SPWM, the way an analog PWM controller would work. Most inverter controllers are digital, and they use regular sampling, typically at each trough or at each peak of the carrier waveform. The carrier is implemented as an up-down counter in a PWM peripheral, and the reference voltages are calculated and scaled to work with the carrier up-down counter.
- The simplicity and phase-independence of SPWM is at the expense of less utilization of the total DC link voltage compared to SVM, as we will soon see.

4. Space Vector PWM

The inverter is shown again in Fig. 4-1(a) with highlighted switch positions on and the others off, corresponding to one of eight allowed switch states. The NPN state is highlighted in (a), where the N or P notation corresponds to the bottom or top switch gated on, respectively. Each switch state is easier to track with the use of a switch state map as shown in **Error! Reference source not found.**(b). This map is aligned with the magnetic axes of a PMSM as load, with axis designators corresponding to inverter legs in (a).



(a) (b)

Fig. 4-1. 2L-VSI (a) inverter highlighting NPN switch state, and (b) switch state map

The map in **Error! Reference source not found.**(b) has six non-zero switch-state vectors, with each vector labelled with its corresponding switch state. Each of these vectors has a length of 2/3rds of the total DC link voltage, with the center of the state map representing the neutral point of the load *s*. Consider the NPN state for example. With Q2 and Q6 on, phase *u* and *w* windings are

parallel. By voltage division, the voltage across *u* and *w* windings is $\frac{1}{3} \cdot V_{bus}$, and the voltage across phase *v* winding is $\frac{2}{3} \cdot V_{bus}$, which is the length of the NPN state vector.

The non-zero state vectors form boundaries between six sextants, with each sextant occupying a 60-degree wedge of the state map. With the DC link as the energy source, the inverter alternately applies line-to-line voltages to the load. There is a rotating modulation control vector, called a reference vector, or reference voltage. Dashed lines show the projections of this vector onto the nearest state vectors. The inverter system approximates the reference vector at the load terminals by averaging time spent at nearby state vectors. For the reference vector shown in Fig. 4-1(b), the nearest vectors are PNN, PPN, PPP, and NNN. These last two vectors are redundant zero vectors that short the load terminals. The art of SVM is placing the two zero vectors among the voltage producing vectors.

The maximum reference vector length without overmodulating is indicated by the circle inscribed in the hexagonal border of the state map. The radius of this circle is $\frac{2}{3} \cdot V_{bus} \cdot \cos(30\,°) = \frac{\sqrt{3}}{3} \cdot V_{bus} = 0.577 \cdot V_{bus}$. By comparison, the dashed circle in Fig. 4-1(b) indicates the maximum SPWM reference vector length of $\frac{1}{2} \cdot V_{bus}$. SVM can apply 15% higher voltage to the load terminals compared to sine-triangle PWM, allowing higher current for the same DC link voltage.

There are two common characteristics of SVM:

1. For a wye-connected load as in a PMSM, the load neutral (common) point *must float* due to current interaction between phases. This is true for any modulation depth (reference vector length). We note that a floating load neutral point forces the sum of currents to be zero.
2. Full utilization of the DC link voltage is achieved by the variation in potential between the load neutral point and the DC link. Mathematically: $v_{sz} \neq 0$.

A typical vector sequence to approximate the reference vector in Fig. 4-1(b) is NNN → PNN → PPN → PPP → PPN → PNN → NNN. Notice in this sequence that only one phase leg switches at a time, or in other words, the vectors are adjacent. Dwell times can be calculated by projecting the reference vector onto the vector map using trigonometry.

An alternate approach is to add a common-mode voltage to each of the reference voltages in equations (1-3). The common-mode voltage is

$$v_{sz} = \frac{-\max(v_{uz}^*, v_{vz}^*, v_{wz}^*) - \min(v_{uz}^*, v_{vz}^*, v_{wz}^*)}{2} \tag{4}$$

This common-mode voltage is added to each desired (reference) phase output voltage to create a compare voltage for each phase to compare with the carrier voltage.

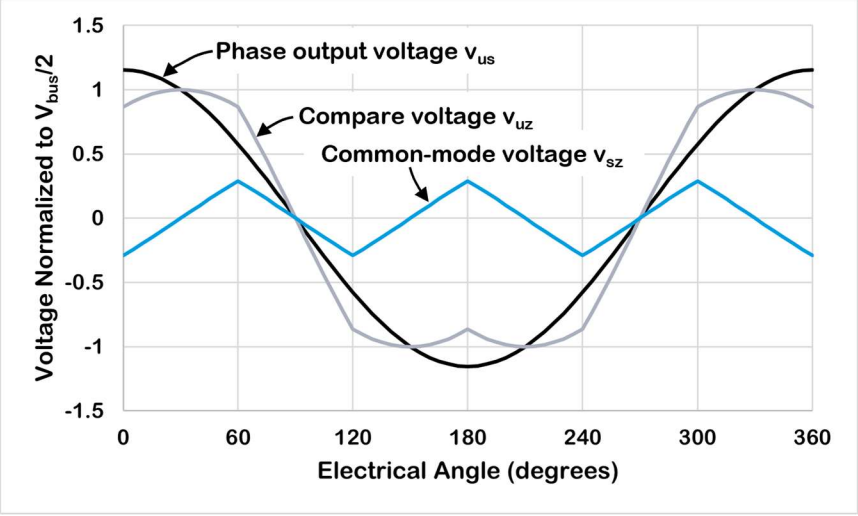


Fig. 4-2. Phase u compare voltage v_{uz} equal to v_{us} plus v_s , normalized to $V_{bus}/2$ with $M = {}^{2}/_{\sqrt{3}}$

Fig. 4-2 shows the desired phase *u* output voltage v_{us}, which when added to the common mode voltage v_{sz} results in the compare voltage v_{uz}. We note that v_{sz} is a repeating waveform with a frequency equal to 3 times the fundamental frequency. Each phase's compare voltage compares with a carrier as with SPWM, with each phase top switch on when its corresponding compare voltage exceeds the carrier voltage, otherwise off. This is easily implemented with analog circuitry, but it is also readily implemented in a digital SVM controller.

Note the reduced peak of the compare voltage compared to the desired phase output voltage. This allows the maximum modulation factor *M* to increase from 1 to $^2/_{\sqrt{3}} = 1.1547$ without overmodulating. As mentioned before, and by inspection of Fig. 4-1(b),

$$V_{0,max} = \frac{2}{3} \cdot V_{bus} \cdot \cos(30\,°) = \frac{\sqrt{3}}{3} \cdot V_{bus} = 0.577 \cdot V_{bus}$$

The maximum line-to-line voltage with SVM is V_{bus} versus $^{\sqrt{3}V_{bus}}/_2$ with SPWM. The maximum modulation factor and consequently the maximum output voltage increases by about 15%, and the line-to-line voltage is the maximum possible given the DC link voltage.

Some observations about SVM:

- Unlike SPWM, the inverter must have at least three phases for SVM to work. Current must be able to flow between the phase outputs. Each sinusoidal phase current results from summing non-sinusoidal component currents.
- The load neutral point must float so that its potential, with respect to the DC link midpoint, can fluctuate at 3x the fundamental frequency.
- Digital implementation of SVM is only slightly more complex than SPWM. First the common-mode voltage is calculated, then added to the reference voltages. The rest is the same as for SPWM.
- Power loss in the inverter is practically identical as with SPWM.

5. Discontinuous Modulation

Discontinuous modulation is often overlooked despite more than one-third reduction in switching power loss and a small change in conduction loss without adding components or altering circuitry. The efficiency advantage merits consideration of this more complex modulation method.

Discontinuous modulation eliminates the redundant zero vectors of SVM, replacing them with intervals when each phase stops switching and its output is switched either to the upper or lower DC rail. The most useful variant for synchronous motor drive and active front end rectifiers is 60° discontinuous modulation, termed DPWM1. Each phase leg stops switching during a 60° interval centered around the peak magnitude of the corresponding phase current. Other variants not covered here are useful for induction motor drive or other non-resistive type loads. Because of the discontinuous nature of the waveforms, it is most straightforward to use a lookup table for each compare voltage [2].

Table 5-1. Phase leg compare voltage waveforms normalized to V_{bus}/2 for 60° DPWM1

60° Sextant	Phase Leg *u*	Phase Leg *v*	Phase Leg *w*
$-\frac{\pi}{6} \le \theta_0 \le \frac{\pi}{6}$	1	$1 - \sqrt{3}M\cos\left(\theta_0 + \frac{\pi}{6}\right)$	$1 + \sqrt{3}M\cos\left(\theta_0 + \frac{5\pi}{6}\right)$
$\frac{\pi}{6} \le \theta_0 \le \frac{\pi}{2}$	$-1 - \sqrt{3}M\cos\left(\theta_0 + \frac{5\pi}{6}\right)$	$-1 + \sqrt{3}M\sin(\theta_0)$	-1
$\frac{\pi}{2} \le \theta_0 \le \frac{5\pi}{6}$	$1 + \sqrt{3}M\cos\left(\theta_0 + \frac{\pi}{6}\right)$	1	$1 - \sqrt{3}M\sin(\theta_0)$
$\frac{5\pi}{6} \le \theta_0 \le \frac{7\pi}{6}$	-1	$-1 - \sqrt{3}M\cos\left(\theta_0 + \frac{\pi}{6}\right)$	$-1 + \sqrt{3}M\cos\left(\theta_0 + \frac{5\pi}{6}\right)$
$-\frac{5\pi}{6} \le \theta_0 \le -\frac{\pi}{2}$	$1 - \sqrt{3}M\cos\left(\theta_0 + \frac{5\pi}{6}\right)$	$1 + \sqrt{3}M\sin(\theta_0)$	1
$-\frac{\pi}{2} \le \theta_0 \le -\frac{\pi}{6}$	$-1 + \sqrt{3}M\cos\left(\theta_0 + \frac{\pi}{6}\right)$	-1	$-1 - \sqrt{3}M\sin(\theta_0)$

There is a common-mode voltage ($v_{sz} \neq 0$) that allows full utilization of the DC link voltage, and $M = {}^{2}/_{\sqrt{3}}$ maximum, as with SVM.

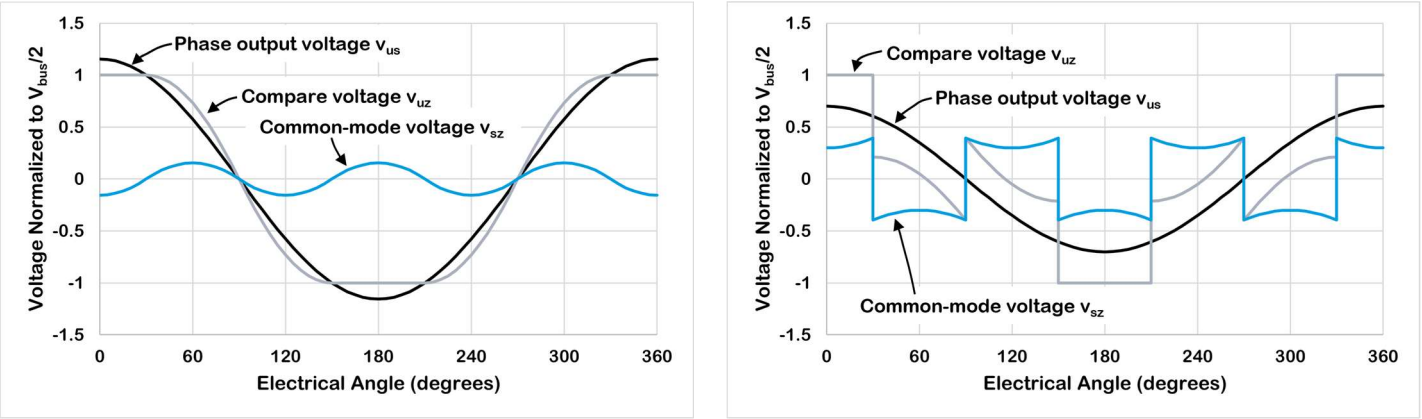


Fig. 5-1. DPWM1 for phase *u* compare voltage v_{uz} equal to v_{us} plus v_s , normalized to $V_{bus}/2$ (a) with $M = {}^{2}/_{\sqrt{3}}$, (b) with $M = 0.7$

Fig. 5-1 shows the desired phase *u* output voltage v_{us}, the common mode voltage v_{sz}, and the compare voltage v_{uz}. By way of comparison, (a) shows waveforms with maximum $M = {}^{2}/_{\sqrt{3}}$, and (b) with $M = 0.7$. Discontinuities in common-mode and compare voltages persist until *M* is at its maximum value. This is handled in Qorvo's Power Application Controller® with flexible latching options to synchronize changes to counters and compare registers. Again, we note that v_{sz} is a repeating waveform with a frequency equal to 3 times the fundamental frequency. As before, each phase's compare voltage compares with a carrier, with each phase top switch on when its corresponding compare voltage exceeds the carrier voltage, otherwise off.

For a PMSM drive or an active front end rectifier, current tracks the phase voltage because the power factor is 1 or -1 respectively. With switching stopped around the peak of the phase current, it is easy to see why DPWM1 reduces the switching loss by 45% or more.

Intuition dictates that reduced switching loss must be at the expense of higher conduction loss, but this is not necessarily the case. The change in conduction loss with discontinuous modulation is difficult to predict without a calculator or simulator that accounts for the changes in reference voltage and on-resistance with temperature. The substantial reduction in switching loss reduces total power loss in each switching device, which reduces its temperature and consequently its on-resistance. Total conduction loss can actually decrease slightly compared to SPWM or SVM. In any case, the change in conduction loss is slight and switching device dependent.

6. Summary

This application note introduces SPWM, SVM, and DPWM1 for 2L-VSI systems, highlighting their respective advantages and limitations, emphasizing interactions in the inverter and load. SPWM is straightforward, and it works with any number of inverter phases because each phase operates independently. It is useful for back-to-back inverter testing with an artificial, inductive load. The main drawback of SPWM is less utilization of the DC link voltage. SVM achieves higher output voltage with full DC link utilization through space vector principles, making it ideal for high-performance drives. Discontinuous modulation also fully utilizes the DC link voltage, and it reduces switching losses by well over 40%, improving efficiency with minimal change in conduction losses. These methods enable designers to balance simplicity, performance, and efficiency in inverter-based motor control and power conversion applications.

References

[1] D. Graham Holmes, Thomas A. Lipo; "Modulation of Three-Phase Voltage Source Inverters," in *Pulse Width Modulation for Power Converters, Principles and Practice*,Piscataway, NJ, USA: IEEE Press / Wiley InterScience, 2003, ch. 5, sec. 5.6, pp. 251-253.
[2] D. Graham Holmes, Thomas A. Lipo; "Zero Space Vector Placement Modulation Strategies," in *Pulse Width Modulation for Power Converters, Principles and Practice*,Piscataway, NJ, USA: IEEE Press / Wiley InterScience, 2003, ch. 6, sec. 6.7, pp. 302-310.

Revision History

Revision	Author	Date	Description
A	Jonathan Dodge, P.E.	19 Feb. 2026	Initial draft

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