Inverter Power Loss Calculation

Abstract

This application note derives closed-form equations for calculating semiconductor conduction and switching losses in a three-phase, two-level voltage-source inverter (2L-VSI) using sinusoidal pulse-width modulation (SPWM), space-vector modulation (SVM), and 60° discontinuous modulation (DPWM1). The analysis incorporates practical simplifications that enable fast, spreadsheet-based evaluation while retaining sufficient accuracy for design comparison and optimization. Methods are presented to estimate switching loss from polynomial curve-fitted energy data, calculate conduction loss for unipolar power devices, and solve simultaneously for device junction temperature and temperature-dependent on-resistance. The resulting loss equations apply to a wide range of inverter applications, including motor drives and active front end rectifiers, and provide a foundation for developing an intuitive and flexible inverter power loss calculator.

1. Introduction

Estimating power loss facilitates essential decision making early in the design process. Designers can quickly choose circuit topology, control methods, component selection, and configurations that are most likely to meet system requirements before committing substantial time and resources to build a prototype. For any calculator or simulator tool to be worthwhile, it must be intuitive and yield quick, meaningful results. This application note derives closed-form power loss equations for a 3-phase, 2-level voltage-source inverter (2L-VSI) using sinusoidal, conventional space vector, or discontinuous modulation, including reasonable simplifications. Calculations apply to various applications, from active front end rectification to electrical machine drive of any type except brushless DC (BLDC), which is a separate topic. Equations are easy to copy into a spreadsheet to make your own inverter power loss calculator. The methods explained here can apply to many other circuit topologies, such as single-phase inverters, DC-DC converters, Vienna rectifier, etc.

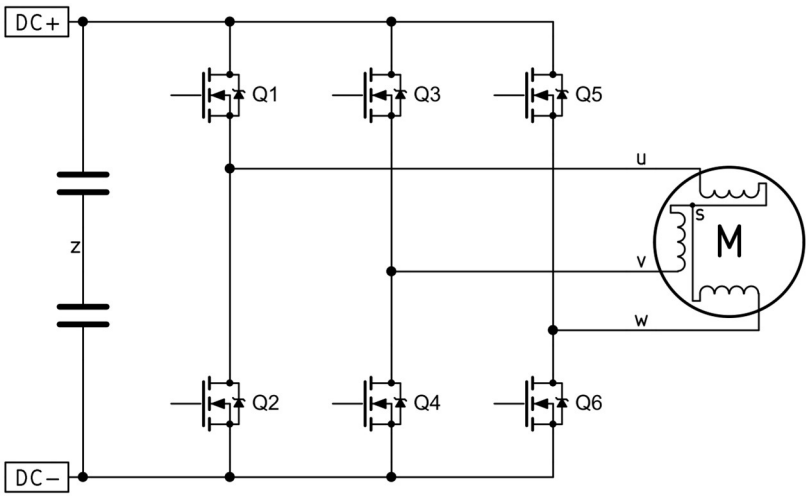


Fig. 1-1. Two-level voltage source inverter with permanent magnet synchronous machine as its load

Fig. 1-1 shows a 2L-VSI connected to a permanent magnet synchronous machine, which could be some other load or a connection to an AC grid through a filter circuit. The inverter power source is the DC link, labelled DC+ and DC- in Fig. 1-1. To avoid confusion with other literature, the notation for the total DC link voltage from DC- to DC+ is V_{bus}. The DC link is “voltage stiff”, supported by a capacitor bank that supplies or absorbs high frequency ripple currents that are a normal aspect of inverter operation. The capacitor bank in Fig. 1-1 is drawn split with midpoint labeled ‘z’, however the capacitor bank of a 2-level inverter need not be split. The node labelled ‘s’ in the PM machine in Fig. 1-1 is the star-connected neutral point of the three stator windings (the load). Phase voltage refers to this point.

2. Simplifications

To proceed with this analysis, we make the following simplifications:

- Loss is the average over the fundamental AC cycle, neglecting transient thermal changes.
- Transistor and diode switching times are negligible, which is valid since they are very short compared to the switching period.
- Include only unipolar power devices, referred to as FETs to comprise MOSFETs, JFETs, gallium-nitride devices, etc. IGBTs and other bipolar devices are excluded due to the number of varying parameters and significant change in switching power loss with temperature.
- Ignore deadtime, which is valid if very short compared to the switching period.
- Switching loss occurs only during forward conduction. Ignore forward and reverse recovery switching loss.
- Ignore switching frequency ripple current.
- Ignore quantization effects, which is valid if the switching frequency is much greater than the fundamental frequency.
- Exclude gate drive power loss. The focus is on losses in the power semiconductors.

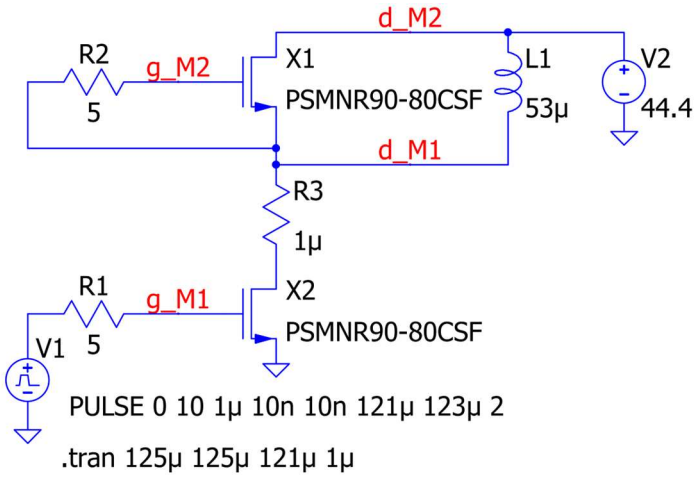
A power semiconductor chip saturates thermally after roughly 10 µs, and a discrete package after roughly 10 ms. After that, the capacity of the much slower responding heatsink becomes relevant. At 50 Hz, half a fundamental AC line cycle completes in 10 ms, so treating the heatsink temperature as constant is valid. Chip temperature variation is largely absorbed by the package, so chip temperature variation is small. At very low fundamental frequency and high operating power, the average power loss simplification is less justifiable and simulation is more applicable.

3. Sinusoidal Pulse Width Modulation and Space Vector Modulation

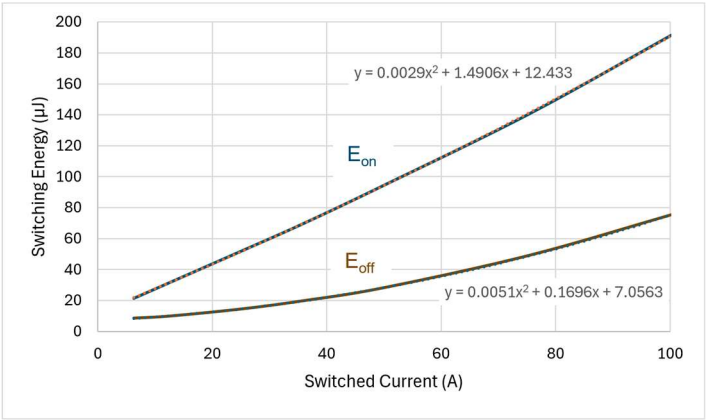
Modulation method strongly affects inverter power loss. Sinusoidal pulse width modulation (SPWM) and space vector modulation (SVM) have practically equal power loss, so the same power loss equations apply to both. Discontinuous modulation can significantly reduce inverter power loss, as will be seen. Both SVM and discontinuous modulation allow about 15% higher load voltage than SPWM, and unlike SPWM, both require three inverter phases. These modulation methods are introduced in [1].

3.1. SPWM and SVM Switching Loss

Data for turn-on and turn-off switching energy E_{on} and E_{off} are often unavailable for power FETs. A QSPICE simulation of a double-pulsed inductive load yields a reasonable estimate of switching energy versus switched current. Such a simulation schematic is shown in Fig. 3-1(a), with its switching energy versus current curves shown in (b). This simulation uses the PSMNR90-80CSF SPICE model from Nexperia. We see in (b) that switching energy increases more than linearly with current. This is almost always the case, regardless of device type. A second-order polynomial is generally an excellent fit for switching energy versus current curves.



(a)



(b)

Fig. 3-1. (a) QSPICE double-pulse simulation circuit, (b) switching energy versus current chart with polynomial fit equations

$$E_{sw} = a_{Ex} \cdot (\hat{\imath}\cos(\theta_0))^2 + b_{Ex} \cdot \hat{\imath}\cos(\theta_0) + c_{Ex} \quad (1)$$

In (1), the coefficients with subscript Ex are replaced by curve fit coefficients. For example, E_{on} in Fig. 3-1(b) has coefficients a_{Eon} = 0.0029, b_{Eon} = 1.4906, and c_{Eon} = 12.433. Similarly, for E_{off}, a_{Eoff} = 0.0051, b_{Eoff} = 0.1696, and c_{Eoff} = 7.0563.

We ignore switching loss with reverse current (synchronous rectification), so we calculate switching energy only with forward current. To calculate the average switching energy, we divide by the fundamental period but integrate over half of it, for example when there is positive current in the top switch position of phase *u*. Using the E_{on} and E_{off} versus current curve fit coefficients, we calculate the switching energy as:

$$E_{sw} = \left[\frac{1}{2\pi}\int_{-\pi/2}^{\pi/2} (a_{Ex} \cdot (\hat{\imath}\cos(\theta_0))^2 + b_{Ex} \cdot \hat{\imath}\cos(\theta_0) + c_{Ex})\, d\theta_0\right] \cdot \left(\frac{V_{bus}}{V_{ref}}\right)^x = \left(\frac{a_{Ex} \cdot \hat{\imath}^2}{4} + \frac{b_{Ex} \cdot \hat{\imath}}{\pi} + \frac{c_{Ex}}{2}\right) \cdot \left(\frac{V_{bus}}{V_{ref}}\right)^x \quad (2)$$

The designation for the peak amplitude of the fundamental phase current *divided by the number of parallel switching FETs* is $\hat{\imath}$, so the result of (2) is the forward switching loss *per FET*. Scaling is required to account for any difference between operating and switching energy characterization voltages. This is the purpose of the term $\left(\frac{V_{bus}}{V_{ref}}\right)^x$, where V_{bus} is the total DC link voltage, and $V_{ref}$is the characterization voltage. For turn-off switching energy E_{off}, the exponent $x = 1$. For E_{on}, *x* varies from 1.25 to 2 for 60 V to 600 V rated FETs, respectively, or better yet, based on double-pulse test characterization. The exponent x is greater than 1 because of the effect of voltage on reverse recovery of a freewheeling FET, and its subsequent effect on E_{on} of the other switch position in the phase leg.

Total switching energy is the sum of E_{on} and E_{off}, and finally, switching power loss is simply the switching energy multiplied by the switching frequency.

$$P_{sw,total} = f_{sw} \cdot (E_{on} + E_{off}) \quad (3)$$

3.2. SPWM and SVM Conduction Loss

Average forward conduction loss of a corresponding top switch position during the positive half of the voltage fundamental waveform is:

$$P_{cond,fwd} = \frac{1}{2\pi}\int_{-\pi/2}^{\pi/2} v_{DS} \cdot \hat{\imath}\cos(\theta_0) \cdot \tau_{fwd}(\theta_0)\, d\theta_0 = \frac{1}{2\pi}\int_{-\pi/2}^{\pi/2} r_{on}(\hat{\imath}\cos(\theta_0))^2 \cdot \tau_{fwd}(\theta_0)\, d\theta_0 \quad (4)$$

One switch position conducts in the forward (or reverse) direction on average half the time during a fundamental cycle. Therefore, equation (4) solves for the average loss over a full period, but the integration limits cover half a period. As a side note, the purpose of using $\cos(\theta_0)$ with integration limits $^{-\pi}/_2$ to $^{\pi}/_2$ is to align the peak of the phase fundamental voltage (and phase current with unity power factor) with the *u* axis of a motor (with *uvw* axes) or the *a* axis of a grid-connected inverter (with *abc* axes). Mathematically, $\sin(\theta_0)$ with integration limits 0 to π could replace $\cos(\theta_0)$ in (4) with the same results.

In (4), v_{DS} is the drain-source voltage of the FET. The angle $\theta_0 = \omega_0 t$ is the fundamental electrical angle, and ω_0 is the fundamental angular frequency. For unipolar devices (MOSFETs, JFETs, etc.), there is no offset voltage, so the voltage across a forward-conducting FET is simply on-resistance multiplied by drain current, or $r_{on}\hat{\imath}\cos(\theta_0)$. Again, $\hat{\imath}$ designates the peak amplitude of the fundamental current per FET, so the result of (4) is the forward conduction loss per FET.

A reference voltage function $v_{ref}(\theta_0, \varphi)$ compares with a triangular switching-frequency carrier waveform normalized to $^{V_{bus}}/_2$. The reference voltage depends on the fundamental electrical angle θ_0, and phase angle φ between fundamental voltage and current, and the modulation factor *M* (also known as modulation index or modulation depth). The modulation factor is

$$M = \frac{\sqrt{2} \cdot V_{LN,rms}}{^{V_{bus}}/_2} \quad (5)$$

In (5), $V_{LN,rms}$ is the line-to-neutral voltage root-mean-squared (RMS) voltage, meaning the voltage from a phase output to the load neutral point labelled *s* in Fig. 1-1. For sinusoidal modulation,

$$v_{ref} = M\cos(\theta_0 + \varphi) \tag{6}$$

Here we introduce the concept of a switching function $\tau(\theta_0)$, which is a function the reference voltage. The switching function describes the pulse pattern to control the switches in the inverter. When $\tau(\theta_0) = 1$, a corresponding switch is gated on, and the switch is gated off when $\tau(\theta_0) = 0$.

For a 2-level voltage source inverter (2L-VSI), the forward-conducting switching function is $\tau_{fwd}(\theta_0) = \frac{1}{2}\left(1 + v_{ref}\right) = \frac{1}{2}(1 + M\cos(\theta_0 + \varphi))$, where φ is the phase shift between the phase voltage and current. We recall that power factor $PF = \cos(\varphi)$, and $-\pi \le \varphi \le \pi$, inverting with $PF > 0$, and rectifying with $PF < 0$. Substituting $\tau_{fwd}(\theta_0)$ into (4) and solving the integral yields the average forward conduction loss per FET:

$$P_{cond,fwd} = \frac{1}{24\pi}\left(\hat{\imath}^2 \cdot r_{on}(3\pi + 8M\cos(\varphi))\right) \tag{7}$$

When one switch in a half-bridge turns off, the other turns on, after a short deadtime that we ignore. Freewheeling current flows in the reverse direction through the other switch. Forward and reverse on-resistances are practically equal for FETs. The freewheeling FET switching function in a 2L-VSI is $\tau_{rev}(\theta_0) = 1 - \tau_{fwd}(\theta_0) = \frac{1}{2}(1 - M\sin(\theta_0 + \varphi))$. The average reverse conduction loss per FET is:

$$P_{cond,rev} = \frac{1}{24\pi}\left(\hat{\imath}^2 \cdot r_{on}(3\pi - 8M\cos(\varphi))\right) \tag{8}$$

Total conduction loss per FET is:

$$P_{cond} = P_{cond,fwd} + P_{cond,rev} = \frac{\hat{\imath}^2 \cdot r_{on}}{4} = \frac{\left(i_{phase,rms}/N_{par}\right)^2 \cdot r_{on}}{2} \tag{9}$$

In (9), $i_{phase,rms}$ is the root-mean-squared phase current, N_{par} is the number of parallel FETs, and again, r_{on} is the on-resistance per FET. This result makes sense because the phase current always flows through one of two switch positions in each half-bridge, and each switch position is driven on during reverse (freewheeling) conduction as well as forward.

3.3. Simultaneously Calculate T_J and r_{on}

On-resistance changes with temperature, and the chip temperature is unknown. We solve for both after estimating the switching loss. A key to this is to ignore the small change in FET switching loss with respect to temperature. This is valid especially for FETs rated 200 V or less because the reverse recovery charge is small, and this slightly affects turn-on switching loss E_{on}. A second key is treating heatsink temperature as constant. There are two unknowns and two equations:

$$T_J = P_{diss} \cdot (R_{\theta JC} + R_{\theta CS}) + T_{sink} = (P_{cond} + P_{sw}) \cdot \left(R_{\theta JC} + R_{\theta CS}\right) + T_{sink} = \left(\frac{\hat{\imath}^2 \cdot r_{on}}{4} + P_{sw}\right) \cdot \left(R_{\theta JC} + R_{\theta CS}\right) + T_{sink} \tag{10}$$

$$r_{on} = R_{on,ref}\left(a_r \cdot T_J^2 + b_{Tr} \cdot T_J + c_r\right) \tag{11}$$

The coefficients in (11) are from a 2nd order polynomial curve fit of the normalized (to 25 °C) $R_{DS(on)}$ versus T_J, chart in the FET datasheet. Substituting (11) into (10) and solving for T_J:

$$T_J = \left(\frac{\hat{\imath}^2 \cdot R_{on,ref}\left(a_r \cdot T_J^2 + b_r \cdot T_J + c_r\right)}{4} + P_{sw}\right) \cdot \left(R_{\theta JC} + R_{\theta CS}\right) + T_{sink} \tag{12}$$

Equation (12) is a quadratic of the form:

$$T_J = \frac{-b_{TJ} - \sqrt{b_{TJ} - 4 \cdot a_{TJ} \cdot c_{TJ}}}{2a_{TJ}} \quad (13)$$

We compute the quadratic coefficients as follows and substitute them back into (11) to solve for T_J.

$$a_{TJ} = \frac{\hat{\imath}^2 \cdot R_{on,ref} \cdot a_r \cdot \left(R_{\theta JC} + R_{\theta CS}\right)}{4} \quad (14)$$

$$b_{TJ} = \frac{\hat{\imath}^2 \cdot R_{on,ref} \cdot b_r \cdot \left(R_{\theta JC} + R_{\theta CS}\right)}{4} - 1 \quad (15)$$

$$c_{TJ} = \left(\frac{\hat{\imath}^2 \cdot R_{on,ref} \cdot c_r}{4} + P_{sw}\right) \cdot \left(R_{\theta JC} + R_{\theta CS}\right) + T_{sink} \quad (16)$$

4. Assembling the Pieces

The following are inputs to an inverter loss calculator.

- Inverter apparent power rating
- Phase angle (0° = inverter, 180° = rectifier)
- Number of phases
- Load line-to-neutral RMS voltage
- Total DC link voltage
- Switching frequency
- Modulation method
- FET part number
- Number of parallel FETs
- Heatsink temperature
- $R_{\theta CS}$ (isolator pad thermal resistance)

The calculations work for any power factor (except with discontinuous modulation), and apparent input power in VA combined with the load line-to-neutral voltage yields the phase current. Inverter system efficiency depends on power semiconductor efficiency and other unknown factors (loss in inductors, transformer, filter damping, passive components, etc.). Furthermore, efficiency is typically high, so omitting efficiency from the loss calculations is valid. To estimate the effect of system efficiency, we simply enter an input power slightly higher than operating power.

Phase angle and hence power factor are absent in the power loss equations (3, 9) because total power loss is independent of power factor. Conduction loss equations (7, 8) include it to show how loss shifts between forward and reverse conduction loss as the phase angle (power factor) changes, but total conduction loss remains the same.

The calculator uses curve fit coefficients and other data from FET datasheets. A convenient way to compare FETs is to enter FET data in a spreadsheet, and then use indexing based on part number selection to load FET data into preselected fields for use in the equations. Losses are calculated per FET and then aggregated for each phase leg, and finally for the inverter.

Heatsink temperature is considered constant, and it is the starting point for FET junction temperature calculations. Common values are 50 to 65 °C for a circuit board (surface mount FETs) or a liquid-cooled heatsink, and 70 to 90 °C for an air-cooled heatsink. In addition to junction-to-case thermal resistance from the FET datasheet, the calculator must know the thermal resistance from case to heatsink. For discrete devices on a heatsink, typical value range is 0.2 to 1.8 °C/W, and about 6 °C/W for surface mount devices, but this varies greatly depending on circuit board and/or heatsink design.

Following are useful equations in the inverter calculator. First is a way to convert from line-to-neutral to line-to-line RMS voltage for any number of phases. This is not used in loss calculations, but it is useful to compare it with the line-to-neutral value. Again, arbitrary phase count applies only to SPWM.

$$V_{LL,rms} = V_{LN,rms} \cdot \sqrt{\left(1 - \cos\left(\frac{2\pi}{phase\_count}\right)\right)^2 + \left(\sin\left(\frac{2\pi}{phase\_count}\right)\right)^2} \quad (17)$$

Phase RMS current is input apparent power divided by phase count and again divided by line-to-neutral RMS voltage.

$$i_{phase,rms} = \frac{S_{in}/phase\_count}{V_{LN,rms}} \quad (18)$$

Peak FET current is:

$$\hat{\imath} = \frac{\sqrt{2} i_{phase,rms}}{N_{par}} \quad (19)$$

Switching losses are calculated as outlined in (2, 3). Now all the pieces are in place to complete the loss calculations. The next step is to calculate the junction temperature coefficients as in (14-16). Knowing T_J, we calculate the temperature-correlated r_{on} using (11), and finally we can calculate forward and reverse conduction losses using (7, 8). Total loss per FET is the sum of the switching and conduction losses, and total loss per phase is the total loss per FET multiplied by 2 and by parallel count. Finally, total inverter semiconductor loss is the total loss per phase multiplied by the phase count. Semiconductor efficiency is

$$\eta = 1 - \frac{P_{loss,total}}{S_{in}} \quad (20)$$

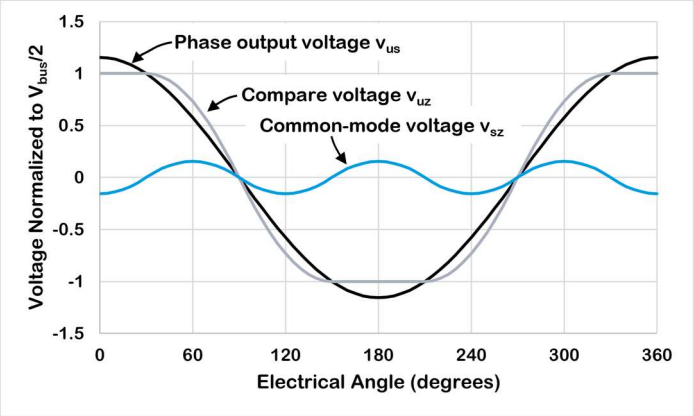
5. Discontinuous Modulation

This often-overlooked modulation method can substantially reduce power loss in the inverter without adding components or altering circuitry. The efficiency advantage merits consideration of this more complex modulation method. The scope here is limited to 60° discontinuous modulation, termed DPWM1, with PF = 1 or -1. It is possible to extend the equations to handle arbitrary PF, but most applications that would use an integrated motor controller & driver (MCD) such as Qorvo's Power Application Controller® (PAC) have PF = 1 or -1. Please refer to [1], [2] for more details.

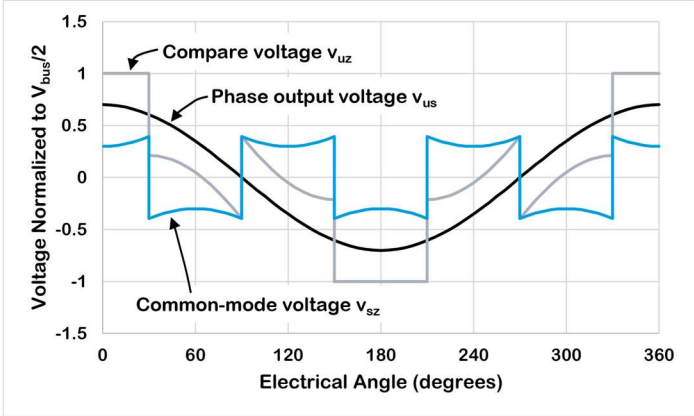
DPWM1 stops switching each phase during two 60° intervals centered around the peak magnitude of the corresponding phase current fundamental cycle, with the phase output tied either to the upper or lower DC rail. This reduces switching loss by more than one-third, at the expense of slightly increased forward conduction loss, countered by reduced reverse conduction loss (with PF = 1).

For convenience, Fig. 5-1 is duplicated here from [1]. It shows the desired phase *u* output voltage v_{us}, the common mode voltage v_{sz}, and the compare voltage v_{uz}. By way of comparison, (a) shows waveforms with maximum $M = 2/\sqrt{3}$, and (b) with $M = 0.7$.

Discontinuities in each compare voltage is handled by PAC MCDs with flexible latching options to synchronize changes to counters and compare registers. Each phase's compare voltage compares with a switching-frequency triangular carrier, with each phase top switch on when its corresponding compare voltage exceeds the carrier voltage, otherwise off.



(a)



(b)

Fig. 5-1. DPWM1 for phase *u* compare voltage v_{uz} equal to v_{us} plus v_s , normalized to $V_{bus}/2$ (a) with $M = {}^{2}/_{\sqrt{3}}$, (b) with $M = 0.7$

5.1. DPWM1 Switching Loss

Inspection of the waveforms in Fig. 5-1 is helpful to derive DPWM1 power loss equations. First, we divide the fundamental period into six 60° sextants, aligning boundaries with the step changes in the compare and common-mode voltages. Despite the step changes in these voltages, the phase currents are sinusoidal (ignoring switching noise and ripple). Therefore, the switching loss equations (2, 3) apply to DPWM1, with one key exception: The switching loss in one sextant is zero, namely in phase *u* when ${}^{-\pi}/_{6} \le \theta_0 \le {}^{\pi}/_{6}$, and similarly in phases *v* and *w*, offset from each other by 120°. By symmetry, the switching loss is equal in phase *u* when $\frac{\pi}{6} \le \theta_0 \le \frac{\pi}{2}$ and when $\frac{-\pi}{2} \le \theta_0 \le \frac{-\pi}{6}$. Therefore, we only need to calculate the switching loss in one of these sextants and then double it. Switching loss for sextant $\frac{\pi}{6} \le \theta_0 \le \frac{\pi}{2}$ is:

$$E_{sw} = \left[\frac{1}{2\pi}\int_{\pi/6}^{\pi/2} (a_{Ex}\cdot(\hat{\imath}\cos(\theta_0))^2 + b_{Ex}\cdot\hat{\imath}\cos(\theta_0) + c_{Ex})\, d\theta_0\right]\cdot\left(\frac{V_{bus}}{V_{ref}}\right)^x = \left(\frac{a_{Ex}\cdot\hat{\imath}^2(4\pi - 3\sqrt{3})}{48\pi} + \frac{b_{Ex}\cdot\hat{\imath}}{4\pi} + \frac{c_{Ex}}{6}\right)\cdot\left(\frac{V_{bus}}{V_{ref}}\right)^x \quad (21)$$

As before, the coefficients with subscript Ex are replaced by E_{on} and E_{off} curve fit coefficients. Multiplying equation (21) by 2 yields the total E_{on} or E_{off} switching energy per FET. Summing E_{on} and E_{off} and multiplying by the switching frequency as in equation (3) yields the total switching energy. Note again that switching loss is independent of phase angle φ.

5.2. DPWM1 Conduction Loss

Thanks to symmetry, we only need to calculate losses during one-third of the fundamental period. We focus on two sextants with positive output voltage v_{us} and hence positive phase current, assuming PF = 1. If PF = -1, we simply swap forward and reverse conduction losses; total conduction losses remain the same regardless of PF.

As before, we use switching functions $\tau_{fwd}(\theta_0) = \frac{1}{2}(1 + v_{ref})$ and $\tau_{rev}(\theta_0) = 1 - \tau_{fwd}(\theta_0) = \frac{1}{2}(1 - v_{ref})$. We simplify with $\varphi = 0$. We omit r_{on} from the equations for now, so the result is FET current squared. Since each FET conducts half the time, we divide by the fundamental period 2π but integrate over only half a period total by integrating over 60° for each of three sextants. Then we add the squared FET currents for the three sextants and finally multiply by r_{on}. This allows simultaneous calculation of junction temperature and r_{on} adjusted for temperature, as before. We use the solutions to the following integrals as we calculate the per-FET forward and reverse conduction losses, the results of which are shown in Table 5-1.

$$\int_{x_{start}}^{x_{end}} (\cos(x))^2\,dx = \frac{1}{2}\left(x + \frac{1}{2}\sin(2x)\right)\Big|_{x_{start}}^{x_{end}} \tag{22}$$

$$\int_{x_{start}}^{x_{end}} (\cos(x))^2 \cdot \cos(x+y)\,dx = \frac{1}{2}\left(\frac{1}{2}\cos(x+y)\sin(2x) + \sin(x+y) - \frac{1}{4}\sin(-x+y) - \frac{1}{12}\sin(3x+y)\right)\Big|_{x_{start}}^{x_{end}} \tag{23}$$

Table 5-1. Phase *u* conduction loss equations for two sextants that apply to other sextants by symmetry

Sextant	Equations	Equation Number
$\frac{-\pi}{6} \le \theta_0 \le \frac{\pi}{6}$	$i_{fwd1}^2 = \frac{1}{2\pi}\int_{-\pi/6}^{\pi/6} (\hat{\imath}\cos(\theta_0))^2 \cdot 1\,d\theta = \frac{\hat{\imath}^2}{2\pi}\cdot\frac{1}{2}\left(\theta_0 + \frac{1}{2}\sin(2\theta_0)\right)\Big|_{-\pi/6}^{\pi/6} = \frac{\hat{\imath}^2(2\pi + 3\sqrt{3})}{24\pi}$	(24)
$\frac{\pi}{6} \le \theta_0 \le \frac{\pi}{2}$	$i_{fwd2}^2 = \frac{\hat{\imath}^2}{2\pi}\int_{\pi/6}^{\pi/2} (\cos(\theta_0))^2 \cdot \frac{1}{2}\left(1 - 1 - \sqrt{3}M\cos\left(\theta_0 + \frac{5\pi}{6}\right)\right)d\theta_0 = \frac{M\hat{\imath}^2}{8\pi}$	(25)
$\frac{\pi}{6} \le \theta_0 \le \frac{\pi}{2}$	$i_{rev2}^2 = \frac{\hat{\imath}^2}{2\pi}\int_{\pi/6}^{\pi/2} (\cos(\theta_0))^2 \cdot \left[1 - \frac{1}{2}\left(1 - 1 - \sqrt{3}M\cos\left(\theta_0 + \frac{5\pi}{6}\right)\right)\right]d\theta = \frac{\hat{\imath}^2}{48\pi}(4\pi - 3\sqrt{3} - 6M)$	(26)

The first row in Table 5-1 corresponds to the 60° interval when the top switch position in phase *u* remains on and the bottom switch remains off, so there is only forward current and zero reverse current. The second row shows phase *u* forward current squared when $\frac{\pi}{6} \le \theta_0 \le \frac{\pi}{2}$, and by symmetry when $\frac{-\pi}{2} \le \theta_0 \le \frac{-\pi}{6}$. The third row shows phase *u* reverse current squared for the same intervals.

The junction temperature quadratic coefficients are:

$$a_{TJ} = a_r.R_{on,ref}\left(i_{fwd}^2 + i_{rev}^2\right)\cdot\left(R_{\theta JC} + R_{\theta CS}\right) \tag{27}$$

$$b_{TJ} = b_r R_{on,ref}\left(i_{fwd}^2 + i_{rev}^2\right)\cdot\left(R_{\theta JC} + R_{\theta CS}\right) - 1 \tag{28}$$

$$c_{TJ} = \left(c_r R_{on,ref}\left(i_{fwd}^2 + i_{rev}^2\right) + P_{sw}\right)\cdot\left(R_{\theta JC} + R_{\theta CS}\right) + T_{sink} \tag{29}$$

On-resistance r_{on} adjusted for temperature is calculated using equation (11). Sextants $\frac{\pi}{6} \le \theta_0 \le \frac{\pi}{2}$ and $\frac{-\pi}{2} \le \theta_0 \le \frac{-\pi}{6}$ have equal conduction losses. Therefore, to calculate forward conduction loss, add equation (24) (sextant $\frac{-\pi}{6} \le \theta_0 \le \frac{\pi}{6}$ when the top switch remains on) to 2 times equation (25), then multiply by r_{on}. Reverse conduction loss is 2 times equation (26) times r_{on}.

$$P_{cond,fwd} = r_{on}\left[\frac{\hat{\imath}^2(2\pi + 3\sqrt{3})}{24\pi} + 2\cdot\frac{M\hat{\imath}^2}{8\pi}\right] \tag{30}$$

$$P_{cond,rev} = r_{on}\left[2\cdot\frac{\hat{\imath}^2}{48\pi}(4\pi - 3\sqrt{3} - 6M)\right] \tag{31}$$

6. Summary

This application note presents a systematic, calculation-based approach to inverter semiconductor power loss estimation that is well suited for early-stage design tradeoff studies. Closed-form expressions are developed for switching and conduction losses in a three-phase, two-level inverter using SPWM, SVM, and DPWM1, with emphasis on unipolar power devices such as MOSFETs, JFETs,

and GaN FETs. SPWM and SVM yield nearly identical losses, while discontinuous modulation can significantly reduce switching loss with minimal change in conduction loss. A practical method is also provided to account for temperature-dependent on-resistance by solving junction temperature and device loss simultaneously. By combining modulation effects, device characteristics, and thermal considerations into a compact set of equations, the techniques described enable rapid comparison of device options, modulation strategies, and paralleling choices without requiring detailed time-domain simulation.

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Revision History

Revision	Author	Date	Description
A	Jonathan Dodge, P.E.	19 Feb. 2026	Initial draft

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