A 1-8GHz Gallium Nitride Distributed Power Amplifier MMIC Utilizing a Trifilar Transformer

Charles F. Campbell, Michael D. Roberg, Jonathan Fain and Sabyasachi Nayak
Infrastructure and Defense Products
Qorvo
Richardson, TX, USA

***Abstract*—This paper describes the design and measured performance of a 1-8GHz power amplifier MMIC fabricated with a 0.15um Gallium Nitride (GaN) process technology. The process features a 100um thick Silicon Carbide (SiC) substrate and compact transistor layouts with individual source grounding vias (ISV). The design utilizes a non-uniform distributed power amplifier (NDPA) topology with a novel trifilar connected output transformer. The 2-stage amplifier demonstrates 9.3-13.1W of output power over a 1-8GHz bandwidth with greater than 29% associated power added efficiency (PAE).**

Keywords— MMIC; distributed amplifier; power amplifier; Gallium Nitride; trifilar transformer

I. Introduction

Many modern microwave electronic systems specify amplifiers with high output power, wide bandwidth and high efficiency. Until recently most wideband high power amplifier solutions have relied on vacuum electronics based technologies. Recent publications however show steady progress in realizing high power, high frequency, wideband amplifiers utilizing Gallium Nitride (GaN) MMIC technology that operate from near DC up to 7GHz [1-3]. In [1] 1-6GHz 10W and 1-7GHz 20W fully monolithic amplifiers are reported. A 25W 0.02-6GHz power amplifier is advertised in [2]; the amplifier core is monolithic however off chip bias tees are required to operate the part. Another design requiring external biasing is described in [3] demonstrating 10W output power from 0.03-2.7GHz. In this paper a fully monolithic 2-stage 1-8GHz GaN power amplifier MMIC utilizing a novel trifilar output transformer is described.

II. Process Technology

The wideband power amplifier MMIC reported here was fabricated with a production released 0.15µm gate length process technology with a AlGaN/GaN epitaxial layer grown on a 100µm thick SiC wafer. Typical DC characteristics of these transistors are I_{max}=1.15A/mm, $g_{m,max}$=425mS/mm and -2.9V pinch-off voltage at 10V V_{ds}. Gate-drain breakdown voltage typically exceeds 75V at I_{gd}=1mA/mm allowing 28V operation. The process surface features and grounding include three metallization layers for element connection, thin film and epitaxial resistors, three different capacitance densities and through substrate vias for grounding to the back of the MMIC. The vias are small enough to support compact high performance transistor cell layouts with individual source grounds.

III. Circuit Design

Design goals for the power amplifier MMIC are as follows; 1-8GHz bandwidth, greater than 25dB small signal gain, 10W saturated output power and power added efficiency (PAE) exceeding 30%. A small signal gain goal in excess of 25dB will require at least 2 amplification stages. To meet the bandwidth requirement, the non-uniform distributed power amplifier (NDPA) topology was adopted [4,5]. The output power realized with the NDPA approach is proportional to V_d^2/R_L where V_d is the power supply voltage and R_L is the load impedance that the amplifier is driving. Output power may be increased by designing the amplifier to operate with a higher power supply voltage and/or a lower load impedance. Increasing the supply voltage can be problematic as the transistor technology may not be able to operate reliably at higher voltage and the drain transmission line impedances can become unrealizably high. Therefore to increase output power a novel monolithic trifilar coupled line transformer design (patent pending) was used to reduce the 50Ω load impedance to around 25Ω. An idealized schematic for the transformer connected in the "bootstrap" configuration is shown in Fig.1.

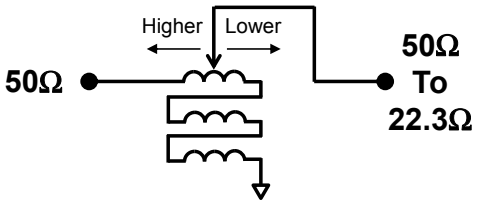

Fig. 1. Trifilar transformer for up to a 2.25:1 transformation ratio.

Theoretically transformation ratios up to 2.25:1 are possible depending on the location of the output tap [6]. Due to physical limitations regarding the location of the low impedance side tap, the microstrip implementation produced a ratio closer to 2:1. Electromagnetic simulations performed on the transformer design suggest that an 8:1 bandwidth can be supported with this approach. For the NDPA application the ground connection is replaced by a bypass capacitor providing a drain bias injection port. This mitigates the need for a wideband high current drain bias choke which can negatively

impact the performance and bandwidth of the amplifier. The layout and electromagnetic simulation results using the Axiem™ EM solver resident within AWR Microwave Office are shown in Fig. 2. The predicted loss varies between 0.28dB and 1.26dB over the 1-8GHz operating band.

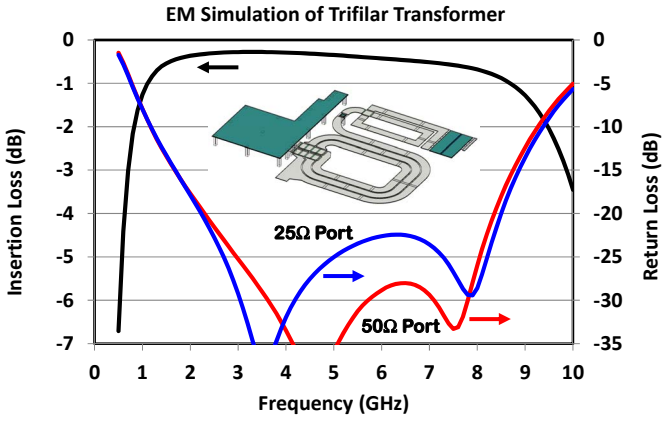

Fig. 2. EM simulation results for the Trifilar transformer.

Taking into consideration the frequency range, available transistor cells, transmission line current handling and realizable characteristic impedances; a 6-cell NDPA driving a 25Ω load was selected for the output stage of the amplifier. The output stage also utilizes non-uniform transistor cell sizes such that the optimum transmission line impedances are realizable on a 100µm thick SiC substrate [5]. The driver stage topology is a 3-cell NDPA driving a 50 Ω load. Both stages operate at equal V_d and current density such that the 1st and 2nd stage gate as well as 1st and 2nd stage drain bias taps can be connected together. Hence the circuit has single gate and drain bond pads. A photograph of the fabricated power amplifier MMIC is shown in Fig. 3, die dimensions are 3.25 x 3.50 mm^2.

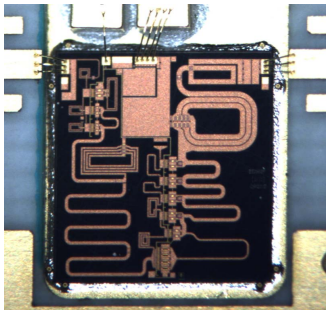

Fig. 3. Photograph of the manufactured MMIC mounted to a test fixture.

Thermal analysis was performed on the design as shown in Fig. 4. Channel temperature assessment is complex for a NDPA design as the power dissipation is transistor and frequency dependent making it difficult to identify a worst case condition. It was determined that the maximum channel temperature occurred in the large FET at the bottom of the layout shown in Fig. 3 when driven at 2.5GHz. The thermal analysis results are shown in Fig. 4 with the MMIC backside (AuSn solder included) held at +85°C. The maximum channel temperature under this worst case operating condition is estimated to be +211°C, well under the process limit for 10^6 hours MTTF.

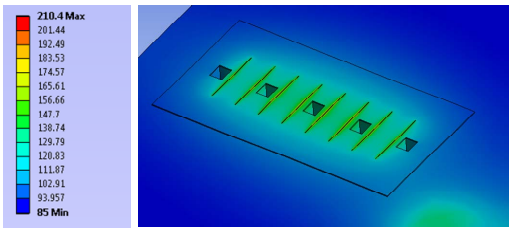

Fig. 4. Thermal analysis results under worst case conditions.

IV. Measured Results

Fabricated devices were 100% DC and RF tested on-wafer, pulsed on-wafer output power and PAE data is shown in Fig. 5. The sample size is 187 MMICs from a 5 wafer process lot. The amplifier was driven with +16dBm continuous wave (CW) and the 28V drain bias supply is pulsed at 100µs pulse width and 10% duty factor. The quiescent bias current was 600mA.

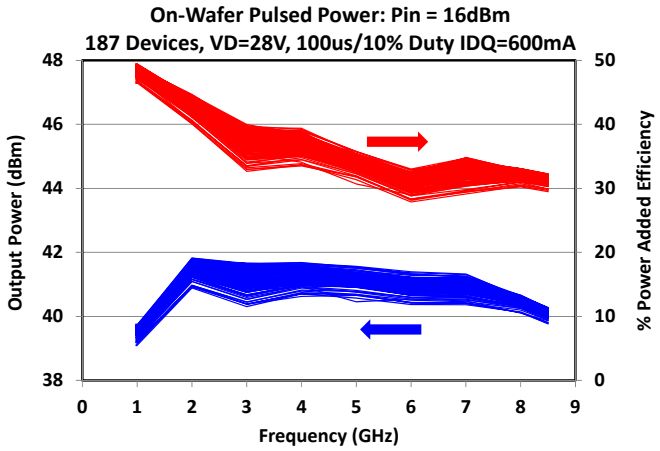

Fig. 5. Output power and PAE results measured on-wafer.

The measured output power is greater than 10W from 2-8GHz rolling off to about 9W at 1GHz. The measured PAE is typically above 30% for the test frequency range. A property of the trifilar transformer is increasing impedance at the lower band edge before eventually becoming a short circuit. This reduces the output power but boosts the efficiency at low frequency. The observed part to part variation in output power is less than 1dB for most of the frequency range

To facilitate testing with bond wires singulated die were soldered to 40mil thick CuMo carrier plates as shown in Fig. 3. The input and output bond pads are connected to 50Ω de-embedding lines with 3 bond wires. The reported results are de-embedded to the wire/trace interface. In-fixture S-parameter data was collected for a 28V drain bias condition with the back of the carrier maintained at approximately +25°C. Measured S-parameter results for 5 MMICs are plotted in Fig. 6.

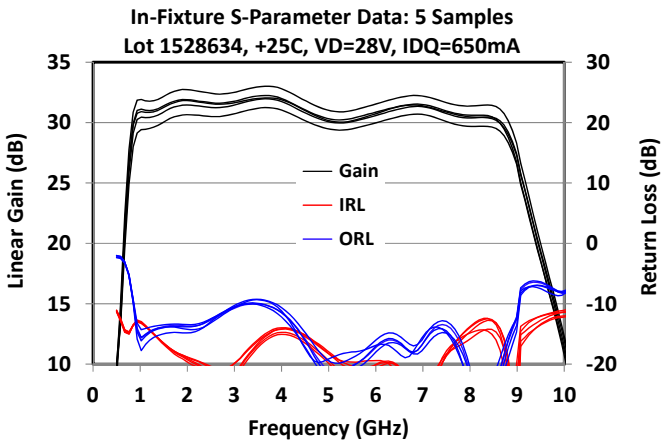

Fig. 6. S-parameter data measured in-fixture.

The small signal gain is typically greater than 30dB over the 1-8GHz frequency range with about 2dB of gain variation. Wideband data for a single unit over temperature is shown in Fig. 7. The amplifier is well behaved over temperature with no observable peaking or regeneration. The +25°C simulated results are also shown in Fig. 7 as the dashed traces.

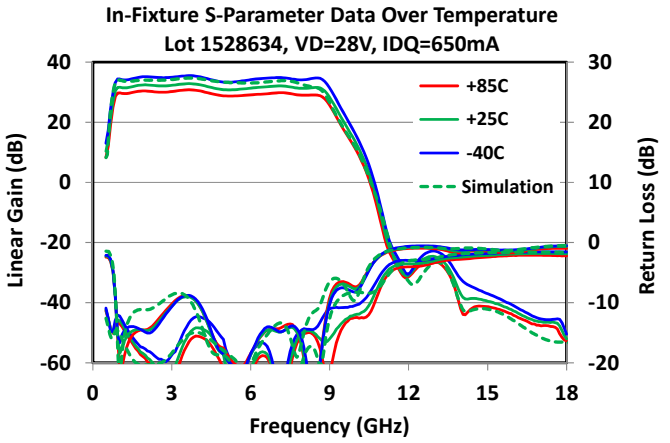

Fig. 7. S-parameter data over temperature measured in-fixture.

Large signal characterization of the amplifier was performed under the same conditions as the s-parameter testing. Measured output power and power added efficiency results under CW operating conditions are plotted in Fig. 8 and Fig. 9. For a 16dBm input drive the saturated output power for the amplifier was observed to vary between 9.3W and 13.1W over the 1-8GHz design frequency range. The measured PAE for 16dBm input power is greater than 29% peaking up to 46% at 1GHz. The power amplifier MMIC was also characterized over temperature to check for performance degradation due to drive margin or thermal issues. The results for power and efficiency at 7dB of gain compression are plotted in Fig. 10 and Fig. 11 respectively. Similar to the S-parameter results over temperature the output power and PAE are well behaved. The output power varies 0.2-0.4dB over the 125°C temperature range.

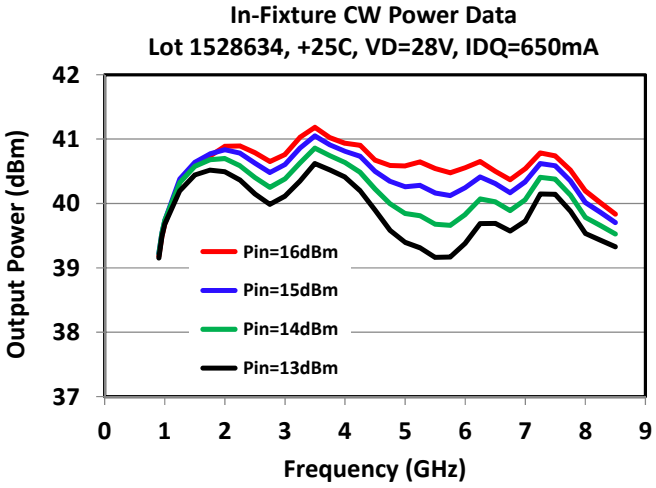

Fig. 8. CW power data measured in-fixture

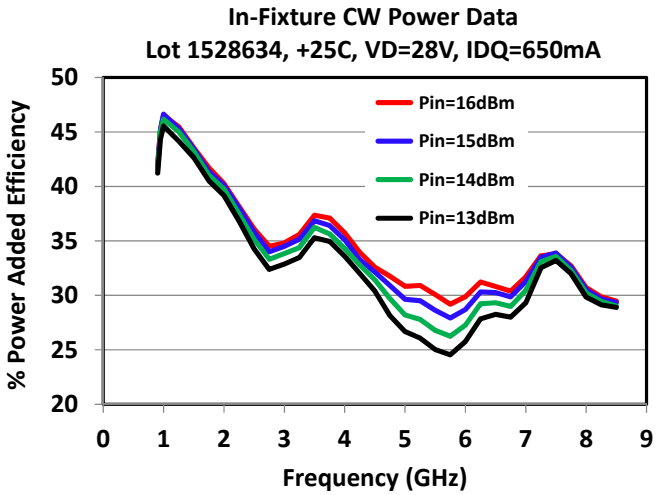

Fig. 9. CW power added efficiency data measured in-fixture

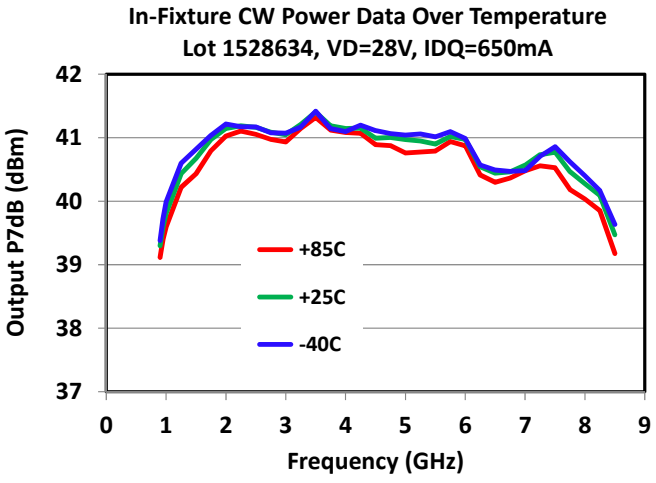

Fig. 10. CW output power data over temperature measured in-fixture

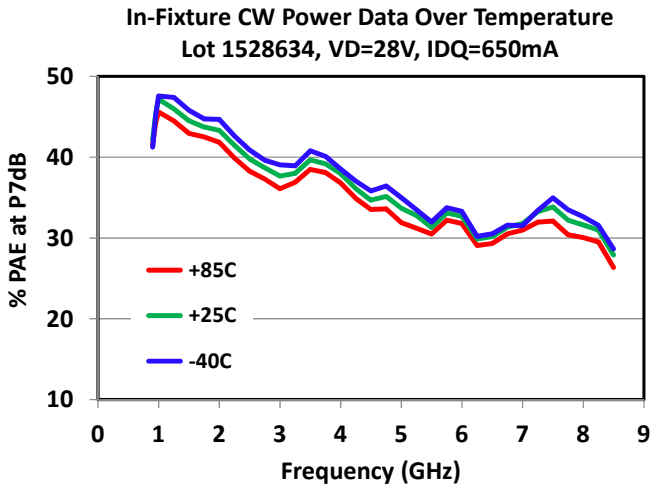

Fig. 11. CW efficiency data over temperature measured in-fixture

Power compression curves measured at -40°C are plotted in Fig. 12. Note that the compression characteristic is well behaved with no discontinuities or kinks that would otherwise suggest drive dependent and/or parameteric instability.

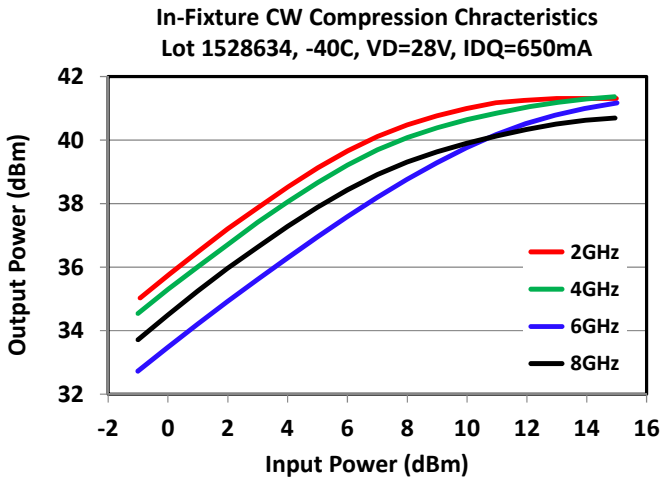

Fig. 12. CW power compression characteristics at -40°C measured in-fixture.

V. Comparison to Published Results

The performance of this power amplifier is compared to recently published GaN MMIC power amplifier benchmarks in Table I. References included operate over a similar frequency range, exhibit wide bandwidth and output power levels that exceed 10W at some point in the operating band. The circuits described here and in reference [1] are fully monolithic power amplifiers with bias chokes, bypasses and DC blocks all integrated on chip. To operate the amplifiers described in references [2] and [3] one has to supply bias chokes and DC blocks off chip at both the input and output ports of the MMIC. Comparing the output power, PAE and die size for parts that utilize off chip versus on chip bias circuitry, it becomes clear how significantly these components impact the performance and size of the amplifier. Monolithically integrating the bias choke on chip while maintaining a reasonable die size is clearly a significant challenge when designing wideband power amplifiers.

TABLE I

Ref #	Freq (GHz)	Gain Stages	SS Gain (dB)	Power (dBm)	PAE (%)	Area (mm^2)	Bias & Block
[1]	1.0-6.0	1	10-15	39.2-41.6	18-46	60.4	On Chip
[1]	1.0-7.0	2	8-16	41.4-44.3	18-44	47.4	On Chip
[2]	0.02-6.0	1	18-21	43.2-45.1	29-52	9.6	Off Chip
[3]	0.03-2.7	1	19-25	39.5-40.4	53-70	4.3	Off Chip
Here	1.0-8.0	2	30-32	39.7-41.2	29-46	11.4	On Chip

VI. Conclusion

The design and measured performance of a 1-8GHz power amplifier MMIC fabricated with a 0.15µm Gallium Nitride (GaN) process technology has been described. The design utilizes a non-uniform distributed power amplifier (NDPA) topology with a novel trifilar output transformer. The transformer provides a drain bias injection point mitigating the need for a high current wideband bias choke and all other bias circuitry is monolithically integrated on chip. The 2-stage amplifier demonstrates 31dB typical small signal gain, 9.3-13.1W of output power over a 1-8GHz bandwidth with greater than 29% associated power added efficiency (PAE). Large and small signal data collected over temperature for the MMIC demonstrates well behaved, stable operation. The measured performance of the amplifier MMIC described here compares favorably with recently published results for bandwidth, gain, die size and efficiency.

References

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