Design of a Broadband L-band 160 W GaN Power Amplifier using SMT Packaged Transistors

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Abstract

This paper details the design of a broadband power amplifier using a state-of-the-art Qorvo transistor in a cost-effective SMT plastic package. The realised amplifier has 160 W of output power between 1.2 and 1.8 GHz and is ideally suited to L-band radar and wideband communications applications. The QPD1013 transistor utilises Qorvo's 0.50 µm GaN-on-SiC technology which enables operation at 65 V, leading to improved efficiency and wide bandwidths.

The design of the PA is described, including load-pull measurements and EM simulation of input and output matching networks. Particular consideration is given to the thermal challenges involved in using high-power GaN transistors in SMT packages. Two approaches to optimizing the thermal performance of the PCB have been assessed, the first using an array of copper-filled vias beneath the ground paddle of the transistor and the second using a copper coin embedded into the PCB. The results of both approaches are compared. Small- and large-signal measurements demonstrate the broadband performance of the realised amplifier.

1 Introduction

Continuing advances in Gallium Nitride technology are leading to operation at higher powers, supply voltages and frequencies. Some recent examples of GaN-on-SiC power amplifiers are described in [1]. The QPD1013 transistor from Qorvo, shown in Figure 1, utilises 0.50 µm GaN-on-SiC technology. It is packaged in a cost-effective 6.6 x 7.2 mm DFN (Dual Flat No Leads) package that allows for simpler PCB assembly compared to traditional metal-ceramic packages.

Whilst Qorvo's GaN transistors are very efficient, the high RF power levels under consideration mean that even an efficient PA will have significant power dissipation in the transistor. As the transistor is an SMT component, careful design of the PCB is required in order to optimize the thermal performance. Two approaches have been evaluated and the results of both are reported. The first makes use of an array of copper-filled vias beneath the ground paddle of the transistor and the second uses copper coin technology. A copper coin is a solid piece of copper (often known as a slug) embedded into the PCB during fabrication to allow efficient heat transfer from the transistor to the carrier on which the PCB is mounted. Many PCB manufacturers have experience with copper-filled via technology, but copper-coin techniques at RF frequencies are less well established.

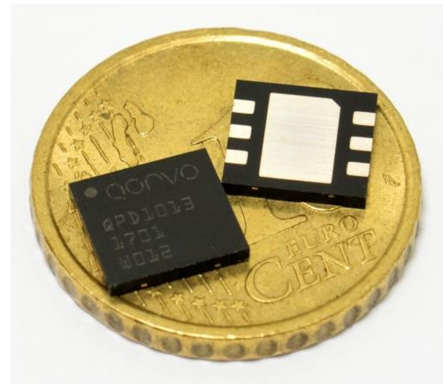

Figure 1: Photograph of the QPD1013 transistor

2 Transistor Measurements

The design uses large signal and small signal measurements of sample transistors assembled on Rogers RO4350 with a thickness of 20 mil. The transistor quiescent bias was 65 V, 240 mA.

Figure 2 shows the Maximum Available Gain (MAG) versus frequency for three different transistors, which clearly demonstrates very good unit-to-unit consistency. Whilst the QPD1013 exhibits gain beyond 6 GHz, for practical considerations its use is best-suited to operation up to around 3.5 GHz.

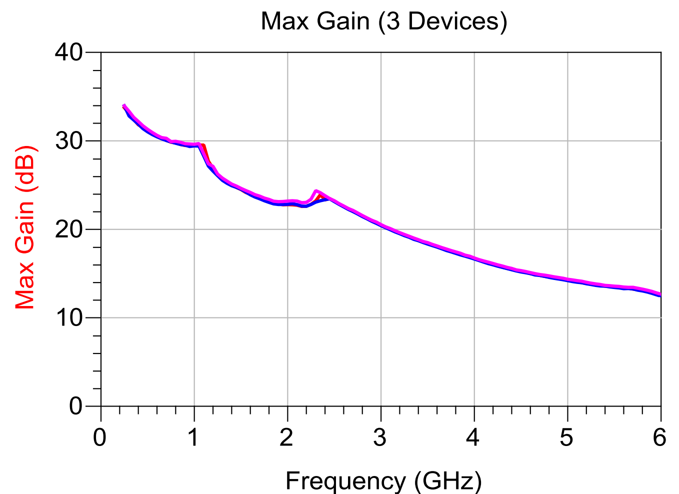

Figure 2: Transistor MAG versus frequency; 3 transistors

Load-pull measurements show that the transistor delivers over 52 dBm (160 W) of RF output power at efficiencies of around 70% when operated at 10% duty cycle and 100 µs pulse width. This load-pull data was used as the basis for the large signal design of the PA.

3 Power Amplifier Design

The starting point for the PA design was to make the transistor unconditionally stable across the operating band. In-band stability must be ensured at the outset and this was achieved by including an RC stability network at the RF input. The power dissipated in the series resistors is too high for conventional SMT components and so high-power Aluminium Nitride resistors from IMS [2] were used. The amplifier is required to be unconditionally stable at all frequencies down to temperatures of -40°C to allow the amplifier to operate across a broad range of temperatures. Low-frequency stability can be greatly improved with the addition of appropriate RC de-coupling at the bias feed points, which can be added later in the design process.

Initial load-pull data, provided by Qorvo, was used to determine the optimal load impedances for output power and drain efficiency between 1.2 GHz and 1.8 GHz. The QPD1013 delivers up to 200 W under certain load conditions but the operating efficiency also needed to be carefully considered to ensure the operating temperature of the transistor was acceptable. The load impedances that result in highest drain efficiency were selected as the target impedances to be presented by the output matching network. The corresponding RF output power level was still high and the higher efficiency ensured acceptable thermal performance.

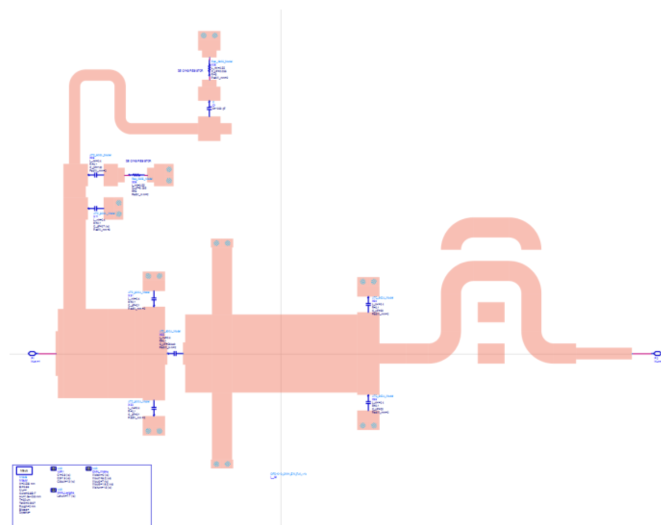

Figure 3: EM simulated output match

The output matching network utilised a band-pass topology to meet the target load impedances. The high operating voltages and high RF power levels present potential pitfalls to the unwary designer. It is vital to keep the RF tracks wide enough to avoid excessive temperature rise and potential destruction due to the very high RF power levels. Matching capacitors must be selected carefully to have adequate breakdown voltage to withstand the DC plus RF voltage swings with adequate Q to avoid excess power dissipation and reduced efficiency.

Planar EM simulations were performed on the metalwork of the output matching network, using Keysight Momentum, and the multi-port S-parameter block was simulated in conjunction with embedded high-frequency models of the 0805 SMT components. Figure 3 shows the hybrid EM/schematic of the output matching network circuit.

The simulated load impedance is plotted against the target on a Smith Chart normalised to 10 Ω in Figure 4. Overlaying the simulated load curve on the supplied load-pull contours (not pictured), suggests that the target power and efficiency values will be met.

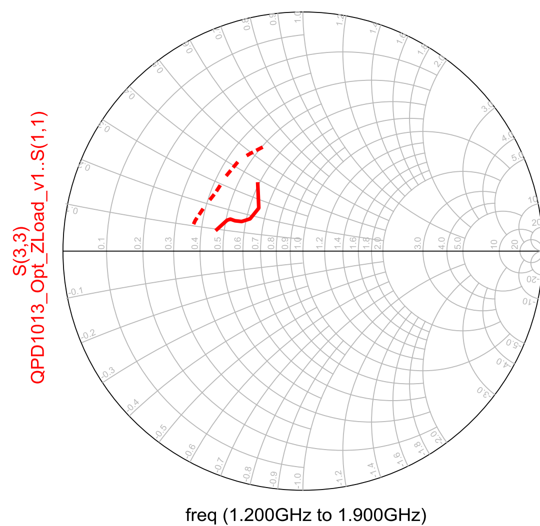

Figure 4: Target (dotted) to simulated (solid) load impedance, 10 Ω chart

The simulated insertion loss of the output network is shown in Figure 5. Output matching network loss results from transmission line losses in the PCB dielectric and from SMT component losses. Even a fraction of a dB loss at these output power levels will amount to several Watts of dissipated power, significantly reducing overall PA efficiency.

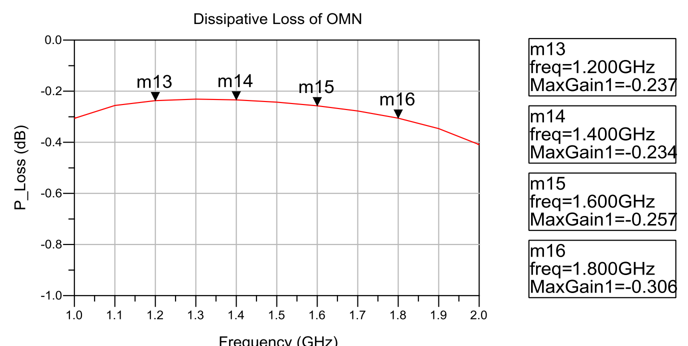

Figure 5: Simulated insertion loss of output network

The input matching network adopted a low-pass architecture. IMS Aluminium Nitride resistors were used in the gate stability

network. These can dissipate several Watts of power, which allows the PA to withstand the high input drive levels of 10 to 20 W required to operate the PA at P-3dB compression. Figure 6 shows the input matching network, which was simulated in the same manner as the output matching network.

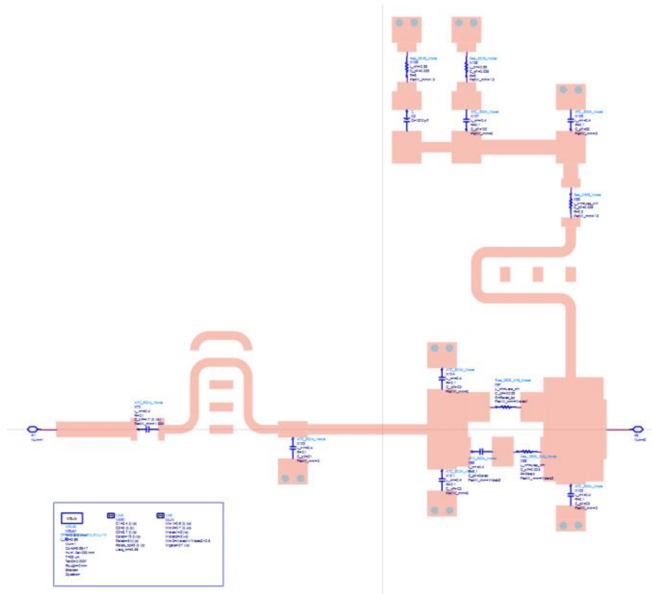

Figure 6: EM simulated input match

It can be seen that the layout of both the input and output matching networks included inductive loops and solder pads to allow tuning of the PA performance following fabrication. These were ultimately not required and the only post fabrication modifications were small changes to capacitor values.

The simulated small signal performance of the PA is shown in Figure 7. Wide bandwidth and flat gain versus frequency response is demonstrated.

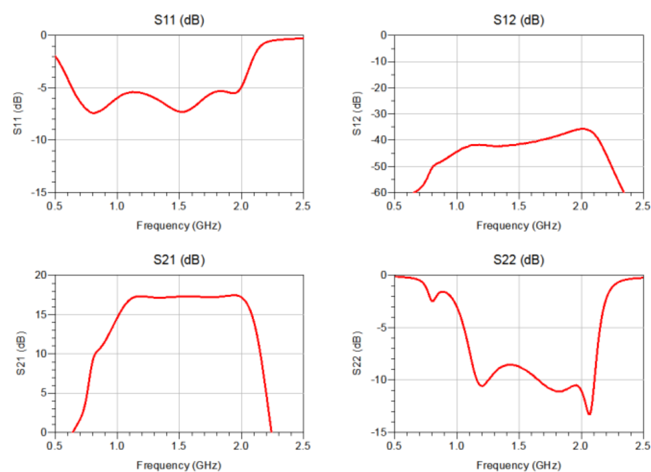

Figure 7: Simulated small signal performance

3.1 Thermal Considerations

Gallium Nitride is capable of higher power densities than either LDMOS or GaAs. A consequence of this is that dissipated power needs to be removed efficiently from the package in order to keep the junction temperature adequately low and ensure a long transistor lifetime.

The main heat transfer mechanism from the package is through the die attach paddle into the PCB. Careful design of the PCB is essential to ensure good heat transfer to ambient and so maintain the transistor temperature at a suitably low level. Two practical approaches were evaluated in the work, one using an array of Copper filled vias (shown on the RHS of Figure 8) and one using a Copper coin fitted into the PCB (shown in the LHS of Figure 8). In both cases the PCB is mounted on an aluminium carrier.

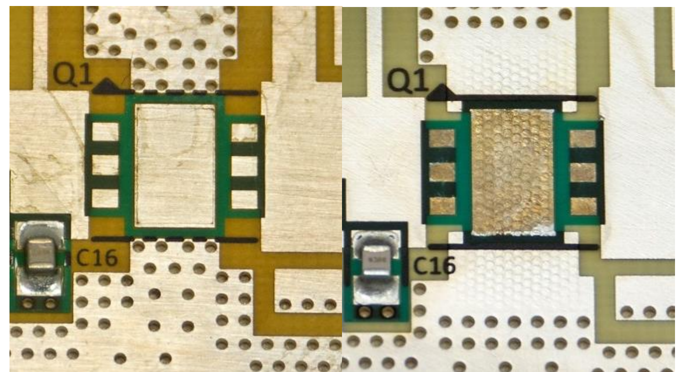

Figure 8: Copper coin (left) and copper-filled vias (right)

4 Realisation and Measured Performance

A photograph of one of the fully-assembled power amplifiers is shown in Figure 9. The hole in the front of the aluminium carrier allows a thermocouple to be placed directly below the QPD1013 transistor.

Figure 9: Photograph of the manufactured PA

PAs were fabricated using both copper-filled vias and copper coin technology. The measured RF performance was very similar in both cases; the copper coin did, however, offer improved thermal performance with the transistor operating 10°C cooler compared to the copper-filled via PCB. Unless otherwise stated the results presented below are for the copper-filled via version of the PCB.

4.1 Small-Signal Measurements

The small-signal S-parameters of 5 PAs at 25°C (transistor base temperature) are plotted in Figure 10. Of particular note is the gain flatness across the operating band and the good agreement between simulation and measurement. All four plots demonstrate consistency across the range of measured PCBs.

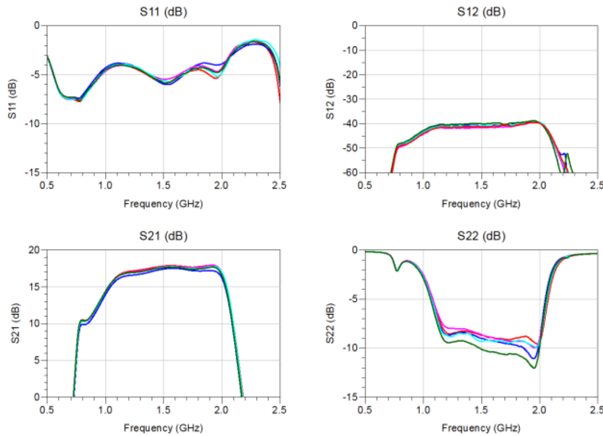

Figure 10: Measured S-parameters of 5 PAs at 25°C

The small-signal performance of one PA over temperature is plotted in Figure 11. The measured S_{21} is ~1 dB higher at -40°C and ~0.5 dB lower at 85°C, with respect to the 25°C measurements.

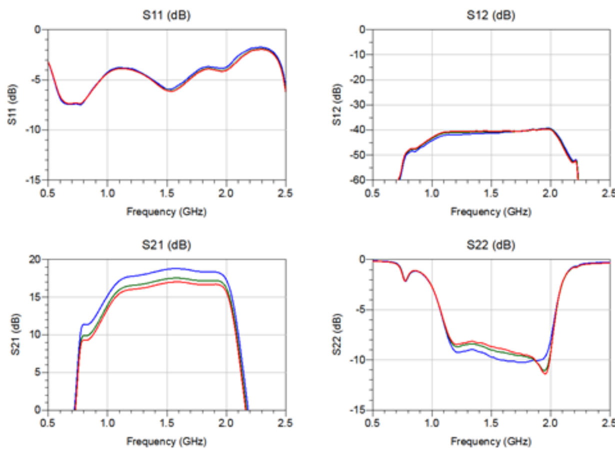

Figure 11: Measured s-parameters of one PA over temperature

A comparison of the small-signal performance of a PA using copper filled vias to a PA using the copper coin PCB technology is shown in Figure 12. It can be seen that the RF performance is very similar, and this was also observed in the large signal performance.

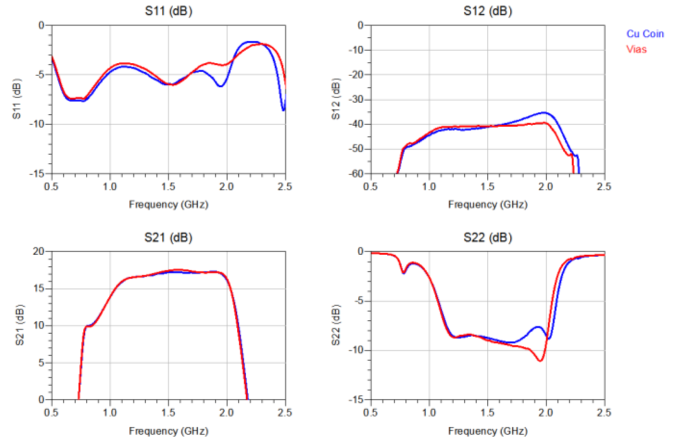

Figure 12: Comparison of S-parameters on copper-filled via PCB to copper coin PCB

4.2 Large-Signal Measurements

The power transfer characteristics were measured for multiple PAs over temperature. The unit-to-unit performance was very similar and the performance obtained for the copper-filled via PCB versions was similar to that obtained for the PAs using copper coin technology. The typical performance of one PA is plotted at three temperatures in Figure 13, where it can be seen that a minimum of 100 W is output at the high end of the band and 160 W is output at the low end. Figure 14 shows a typical efficiency at the output of the PA of 55%, which includes output matching network and connector losses. Whilst the efficiency of the PA is impressive, the dissipated power can still exceed 100 W, highlighting the need for an effective thermal solution.

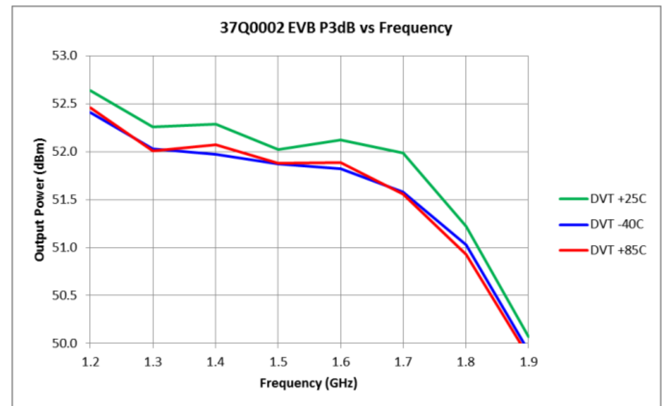

Figure 13: Measured RF out at P-3dB over temperature

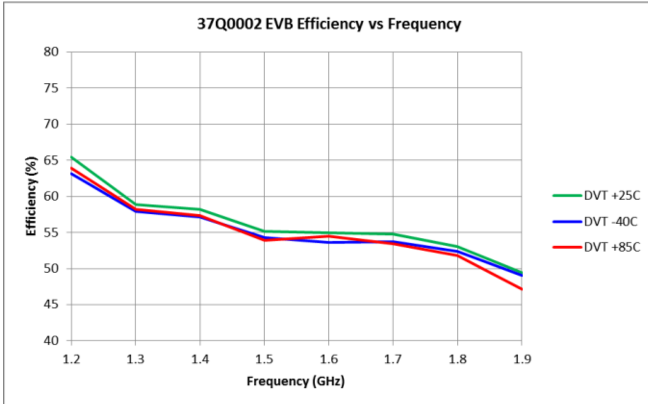

Figure 14: Measured efficiency at P-3dB over temperature

The two tone intermodulation performance of the PAs was also measured. Figure 15 plots the level of the 3rd order and 5th order products for a typical amplifier versus output power. The output IP3 is around +60 dBm for a total RF output power of 10 W (40 dBm).

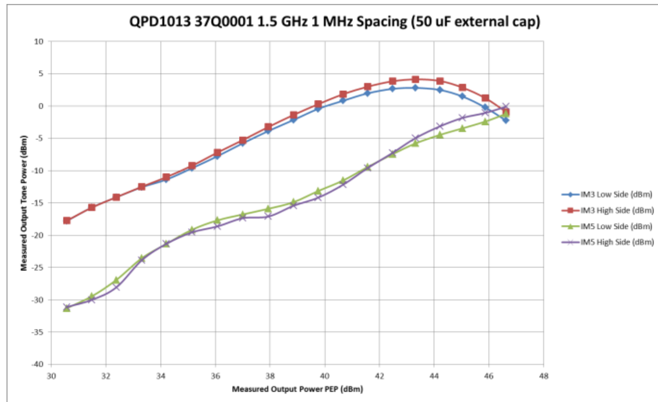

Figure 15: Two tone intermodulation products

5 Conclusions

This paper describes the design and realisation of a GaN PA using a commercially available SMT transistor (the QPD1013 from Qorvo). The amplifier covers 1.2 to 1.8 GHz band and delivers an RF output power of around 160 W with an efficiency of around 60%.

The key performance data for the amplifier versus frequency is tabulated in Table 1.

Freq (GHz)	*P-3dB (dBm)*	*P-3dB (W)*	*Gain at P-3dB (dB)*	*Efficiency (%)*
1.2	52.61	182.39	13.11	65.56
1.4	52.17	164.82	14.03	58.70
1.6	51.95	156.68	13.63	55.28
1.8	51.30	134.90	14.27	52.94

Table 1: Summary of measured performance

As with all power transistors, careful thermal design is key to reliable operation. Variants of the PA have been fabricated and evaluated using two different PCB approaches to ensure good thermal performance; an array of copper filled vias and an embedded copper coin. The RF performance was very similar in both cases. The use of the copper coin PCB led to a 10°C reduction in channel temperature.

Although the improved thermal impedance of the copper coin PCB is attractive, great care must be taken to ensure that the surface of the PCB remains planar and that good contact is made between the copper coin and the ground paddle of the DFN. Any air gaps or solder voids can mitigate the inherent advantages of the copper coin approach.

References

[1] R. M. H. Smith, A. W. Dearn, S. F. Glynn. "The Design of High Performance L-band GaN PAs Using Commercially Available Discrete Transistors", *ARMMS Conference Nov. 2016*, available from http://www.plextekrfi.com/wp-content/uploads/Lband-Qorvo-GaN-PA-125W-PlextekRFI.pdf

[2] IMS Resistors Product Website: https://www.ims-resistors.com/products/