

GaN Thermal Analysis for High-Performance Systems

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Abstract

This paper addresses Qorvo's integrated approach to thermal design that leverages modeling, empirical measurements (including micro-Raman thermography), and finite element analysis (FEA) for high performance microwave GaN HEMT devices and MMICs. This methodology is highly effective and has been empirically validated. By properly addressing FEA boundary condition assumptions and the limitations of infrared microscopy, resulting model calculations are more accurate at both the product and end application level than traditional methods based on lower power density technology.

Introduction

The need for higher and higher output power amplifiers from system requirements has resulted in successive solid state technology improvements. As the technology has moved toward higher capabilities, the applications that drive the technology have moved even further. Power requirements of 10's of Watts from just a few years ago have moved upward to 50 Watts and higher. Gallium Nitride on Silicon Carbide (GaN-on-SiC) has emerged as a superior device technology which boasts high power density, typically greater than 5W/mm gate periphery, high drain operating voltage, typically 20V to 48V, and comparable gain and drain efficiency when compared to traditional Gallium Arsenide (GaAs) pseudomorphic high electron mobility transistor (pHEMT) technology. The requirement to get more power into a smaller circuit area has resulted in the development of GaN power amplifier products that provide thermal challenges at both the product and system level.

In order to fully appreciate the thermal implications of GaN technology, a multi-prong approach involving die-level electrical modeling, empirical measurements, and finite element analysis has been developed. This paper will discuss this approach to GaN thermal analysis in four sections:

- Thermal modeling and empirical measurements, including micro-Raman measurements;
- Thermal analysis, including finite element analysis (FEA), the uses and limitations of infrared microscopy, and a secondary verification using RF testing;
- Die-attach methods, including accounting for contact resistance when comparing epoxy to solder, and die-attach performance as a factor in device operating temperature; and
- Improved packaging options from Qorvo, including GaN on Copper, and GaN in Plastic

I. THERMAL MODELING AND EMPIRICAL MEASUREMENTS

To construct the baseline thermal model for a given process, an electrical simulation of the GaN device using non-linear models for the field effect transistors is used to obtain estimates of heat generation which allow for an initial prediction of thermal performance. The device is then physically fabricated and tested.

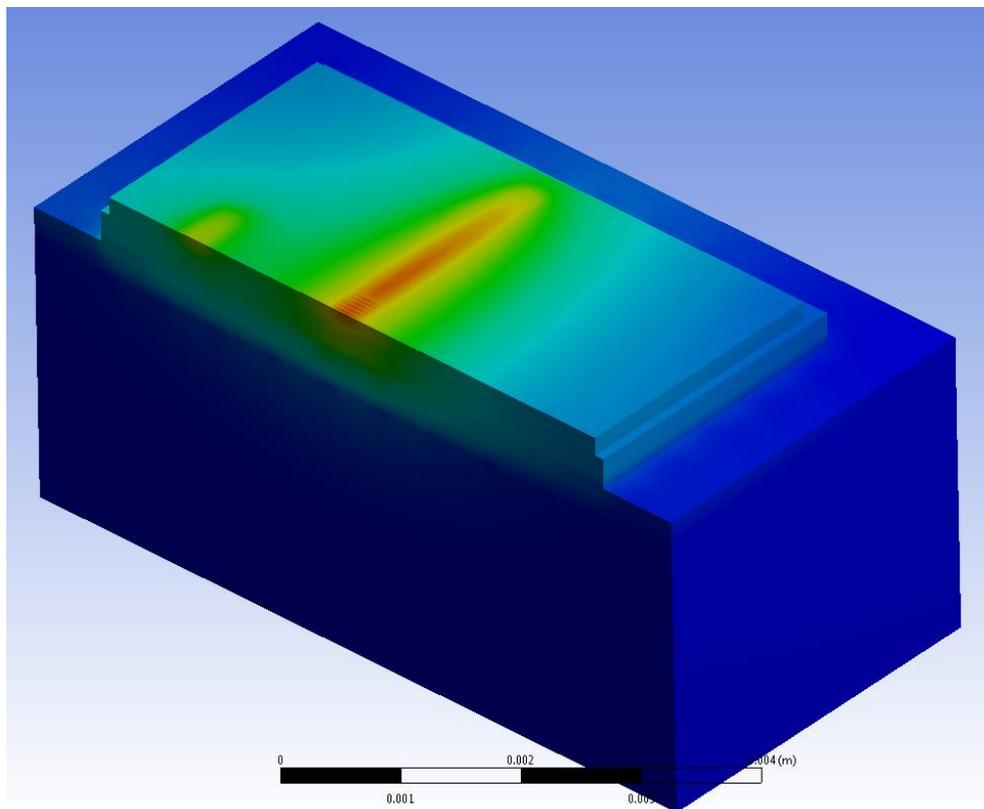


Figure 1: GaN thermal model



Empirical thermal data is collected with both electrical measurements and micro-Raman measurements. Raman thermography is a non-invasive optical technique, based on Raman scattering spectroscopy, that enables temperature measurements with sub-micron spatial and nanosecond time resolution.¹ It probes the temperature-induced phonon shift in a material, with respect to a reference phonon frequency measured at ambient temperature.² Additional details on experimental setups and applications of micro-Raman thermography are described in [1,2].

Raman thermography has been established as an important high fidelity regimen for physically small geometries. It offers proven, accurate and repeatable improvement in spatial resolution down to 0.5 μ m as well as micron scale depth resolution for true 3D thermography. As will be discussed below, Raman thermography improves upon the underestimation of device peak temperature due to lateral spatial averaging associated with conventional infrared (IR) thermography measurements.

A combination of measurement methods, including micro-Raman and electrical, should be used in conjunction with thermal simulations, in order to gain accurate information on the thermal properties of GaN devices.

Using the measured data as the empirical baseline, an FEA model is constructed, which then becomes the baseline for modeling and predicting thermal performance. There are typically multiple iterations between the micro-Raman measurements and the FEA in order to build models that provide good correlation over different geometries and materials stack-ups.

Finite element simulations are used to determine the power and environmental conditions required to run devices at specific elevated temperatures in order to properly accelerate and measure the life of the device. This measured life data is used for construction of a device reliability Arrhenius plot. Today's GaN transistors include gate lengths measuring down to 0.15 μ m in size and lower, meaning that there is still some area averaging that occurs with micro-Raman thermography. With this methodology

these averages are reflected in both the thermal model and device reliability Arrhenius plots. This process enables a tightly-coupled mean time to failure (MTTF) curve and product level thermal analysis that accurately predicts product life.

II. THERMAL ANALYSIS

Once the baseline thermal model development is complete, FEA is then employed to accurately predict channel temperature and thermal resistances at the product level. The FEA begins with a die-level simulation, proceeds to the package level, and continues all the way to system level, where it examines the packaged product within the next higher assembly.

When modeling and measuring heat generation and removal, it is critical to select proper boundary conditions and to understand the impact of those assumptions. Commonly, unrealistic or improper assumptions are made on temperature and heat removal boundary conditions. The unrealistic predictions and measurements that result often lead to product designs that appear to work well on a datasheet, but will fail in application.

Uses and limitations of infrared

Infrared microscopes are widely-used for determining fault location by searching for hot spots in semiconductor devices. However the application of IR for thermal characterization is limited due to spatial resolution incompatibility. IR microscopes cannot resolve a spot size as small as the active area of a GaN transistor. Therefore, IR measurement necessarily averages-in colder, non-active areas with the active area that needs to be measured. In other words, when an IR measurement is taken of an area that is only $0.25\mu\text{m}$ wide, for example, the resultant temperature reading can be $20\text{-}30^{\circ}\text{C}$ cooler than the peak temperature of the active area. An example IR image of a discrete GaN transistor is shown in Fig 2.

A typical IR microscope collects light in the Mid Wave Infrared (MWIR) spectrum. The theoretical spatial resolution limits of MWIR measurement can be calculated using Rayleigh's resolution criteria:

$$D = \frac{0.61\lambda}{\text{N.A.}}$$

D = distance between resolvable targets

λ = wavelength (3-5 μm for MWIR)

N.A. = numerical aperture (cannot exceed 1)

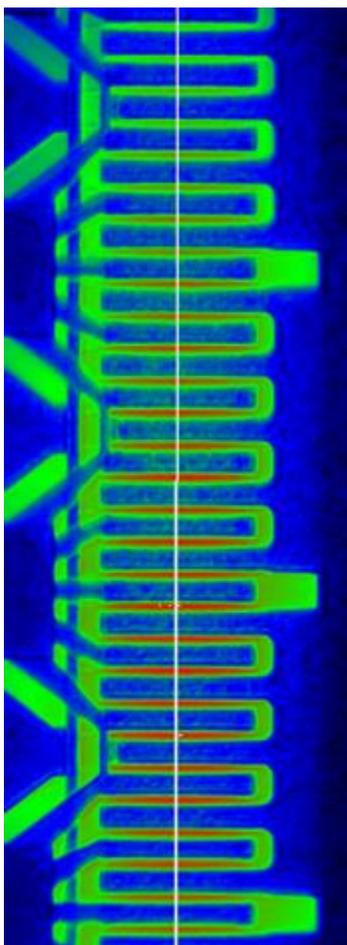


Figure 2: IR image of a typical GaN FET cell



To demonstrate the impact of IR resolution limits when measuring GaN devices, a half symmetry finite element model of a GaN device was constructed. The model assumes bilateral symmetry about the y-axis. This simulation places the device on a .040" thick copper-tungsten base with AuSn die-attach. A boundary condition of 85°C has been applied at the base of the CuW.

A volumetric heat load typical of GaN devices has been applied beneath the channel; the resulting 3D temperature field is shown in the contour plot of Figure 2(a) and the corresponding surface temperature is shown in Figure 2(b).

The peak temperature recorded in the simulation is 204°C at the midpoint of the GaN channel ($x = 0$ for this half-model). This condition occurs below the surface of the substrate and cannot be imaged by infrared thermography. Table 1 lists the maximum and average temperatures for the surface regions as would be recorded by IR measurement. These surface regions are identified in Figures 3(a) through 3(d).

Table 1: FEA Temperature Estimates

Measured Body or Area	Size ($\mu\text{m} \times \mu\text{m}$)	Pixel Alignment to Hot Spot	True Max Temp., °C	Surface Temp. as Measured with IR, °C
Simulated GaN Device	-	-	204.3	-
Surface region #1	2.5 x 2.5	centered	-	195.9
Surface region #2	2.5 x 2.5	offset	-	189.1
Surface region #3	5.0 x 5.0	centered	-	188.3
Surface region #4	5.0 x 5.0	offset	-	183.0

In this ideal example, the application of infrared thermography to image a $2.5\mu\text{m} \times 2.5\mu\text{m}$ area, a representative IR resolution limit, of the surface above the channel results in a measurement which underestimates the peak channel temperature by 8-15°C. The range of offset is caused by an inability to precisely align the center of one pixel on top of

the hottest section of a channel. Figures 3(b) and 3(d) show the impact of having the pixel alignment such that the channel lies at the boundary of the area imaged by the pixel. In this case, the average surface temperature of a $2.5\mu\text{m} \times 2.5\mu\text{m}$ area underestimates maximum channel temperature by more than 15°C . Using a $5\mu\text{m} \times 5\mu\text{m}$ area pushes the error to 21°C .

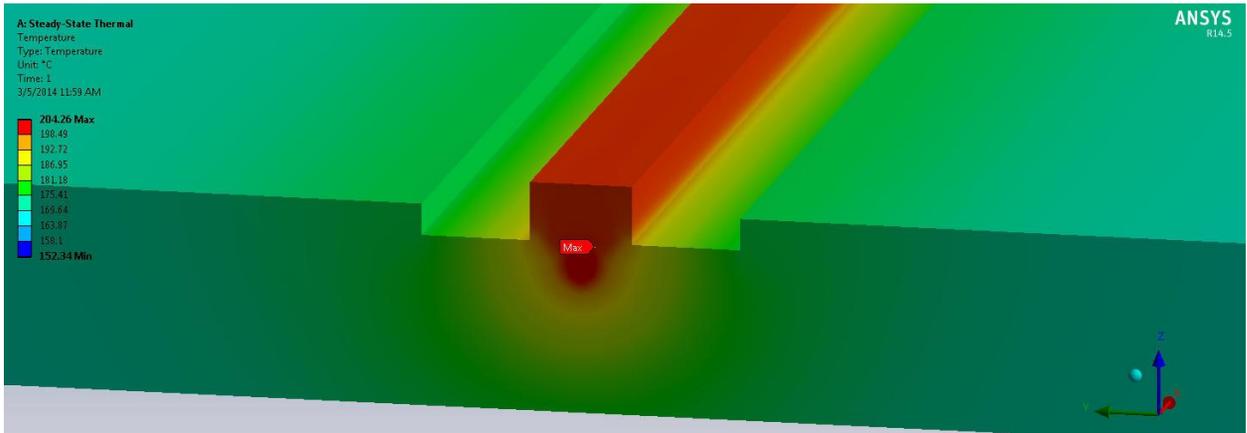


Figure 2(b): Temperature field in the ~2micron thick GaN layer above the SiC substrate

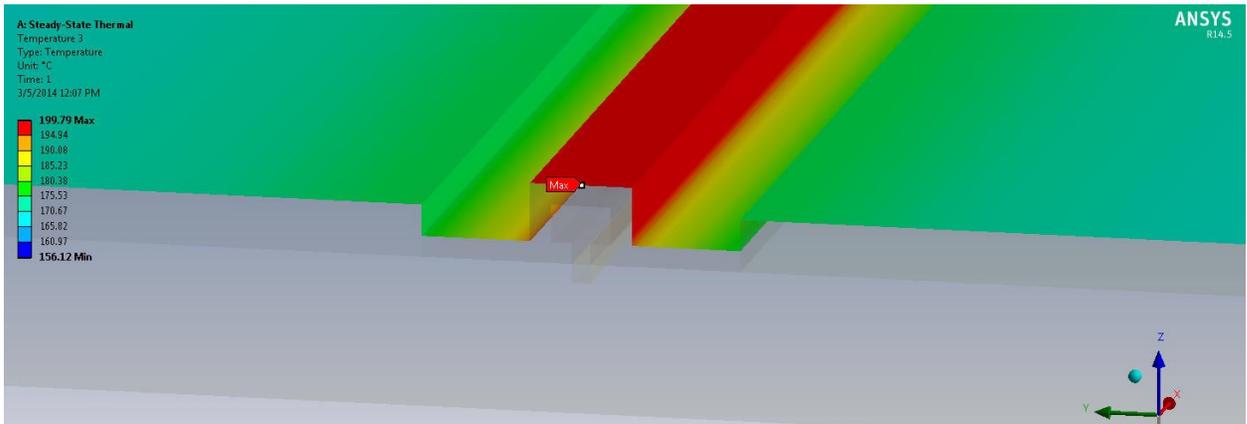


Figure 2(c): Surface temperature above the gate

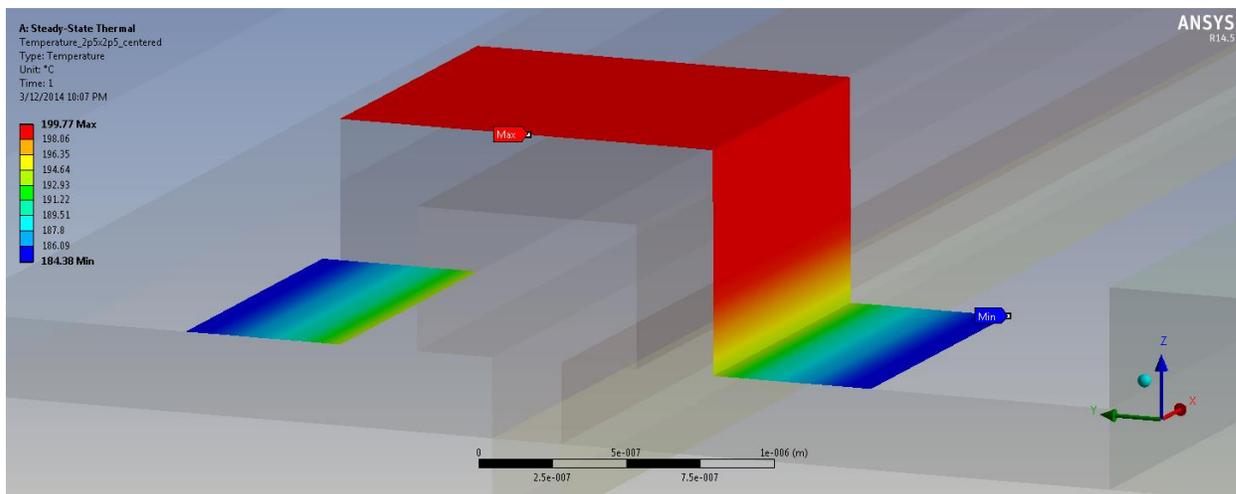


Fig 3(a) Surface Region #1: Width = 2.5 microns (centered over hottest part of channel)

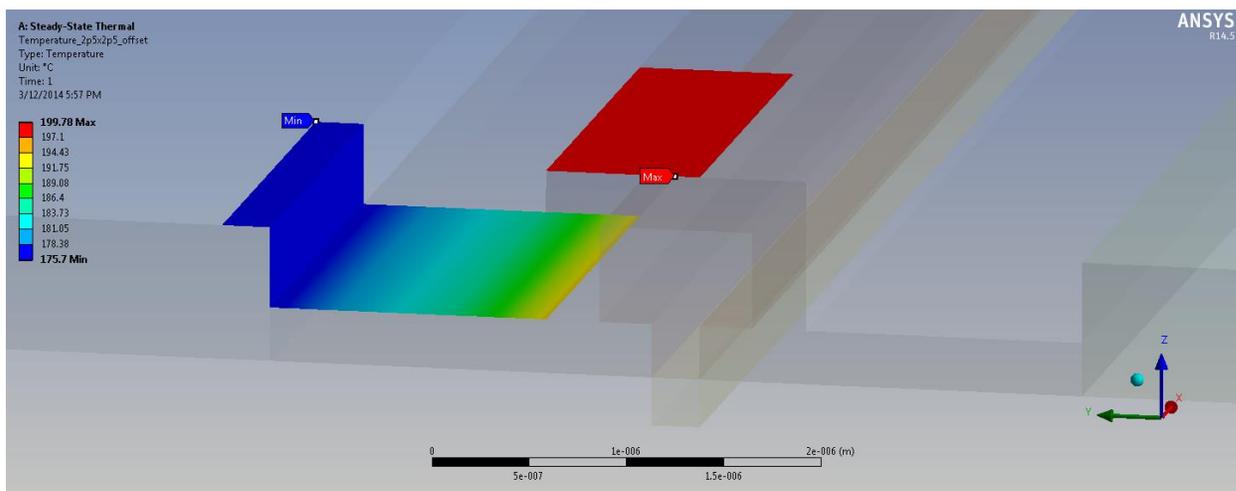


Fig 3(b) Surface Region #2: Width = 2.5 microns (offset in both x and y)

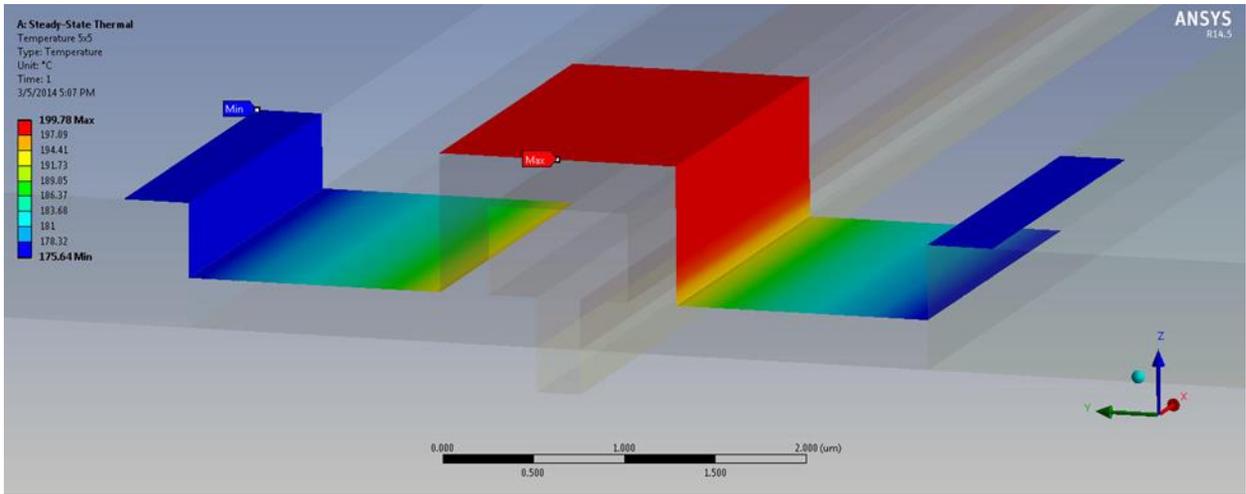


Fig 3(c) Surface Region #3: Width = 5 microns (centered over hottest part of channel)

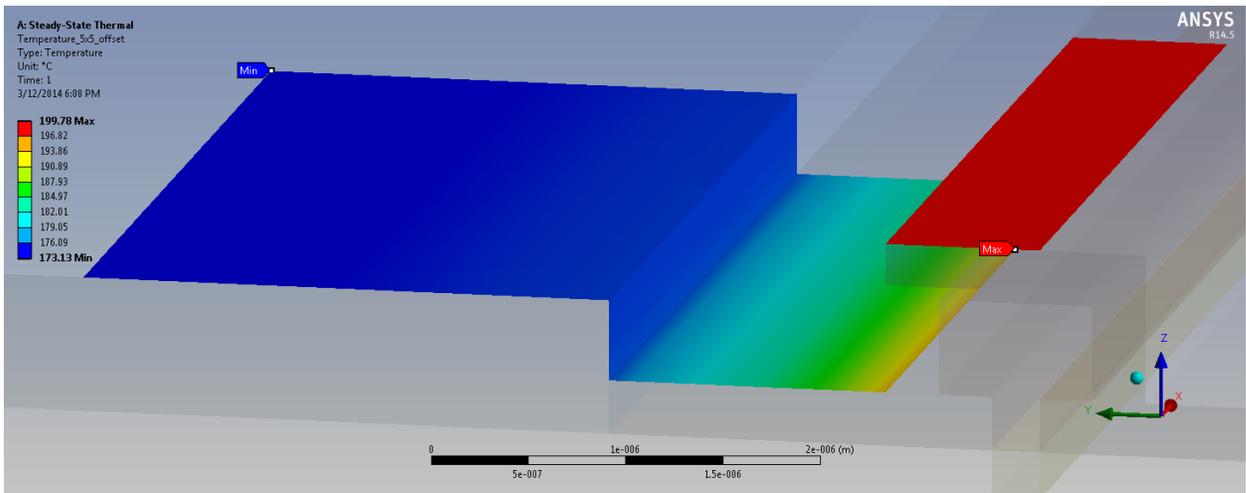


Fig 3(d) Surface Region #4: Width = 5 microns (offset in both x and y)

In the case of GaN thermal analysis, sub-micron processes are used to make the transistors, with hotspots that are significantly smaller than $0.5\mu\text{m}$, and IR microscopy is only capable of resolving—in complete detail—something that is on an order of magnitude larger.

Additionally, IR thermography only measures the surface temperature of the transistor, whereas the peak temperature actually occurs below the surface, in the gallium nitride epitaxy. This reduction in measured temperature is exaggerated during pulsed operation



where the thermal time constant of the semiconductor material above the heat source dampens the measured temperature range.

Finally, emissivity (ϵ) on the surface of a die varies significantly. The common solution is to paint the die matte black to achieve a near $\epsilon = 1$, but a true and consistent blackbody cannot be created.

Table 2: Effects of Emissivity Variation

Measured Body or Area	Size ($\mu\text{m} \times \mu\text{m}$)	Emissivity	True Max Temp., °C	Surface Temp. as Measured with IR, °C
Simulated GaN Device	-	-	204.3	-
Surface Area	2.5 x 2.5	1.0	-	189.1
Surface Area	2.5 x 2.5	0.9	-	170.2

The effects of emissivity are included in this extension of the previous example. Here it is seen that IR thermography underestimates peak GaN channel temperatures by as much as 34°C assuming an ideally small measurement area.

Another challenge this creates is that paint imparts a dielectric load on the die, which can be difficult to predict and is typically inconsistent. This changes RF performance and as a result, accuracy and repeatability suffer.

Secondary verification - RF testing

A secondary verification approach involves assembling a part and testing it in a condition where the channel temperature is expected to be 200°C, for example. If the RF performance has shifted, that can be correlated with temperature sensitivity to power output.

By taking multiple approaches to thermal analysis, and importantly, keeping in mind the importance of proper FEA boundary condition assumptions and limitations of infrared microscopy, model outputs are more accurate and reliable on datasheets, as well as in application.



III. DIE-ATTACH METHODS

Accounting for contact resistance when comparing epoxy to solder

When comparing conductive epoxy to solder, contact resistance is often neglected, and it is assumed that the thermal conductivity of an epoxy joint is equal to what is represented on the epoxy datasheet. A preferred approach is to empirically benchmark solder performance and then determine the actual epoxy performance relative to solder which allows for more accurate simulations and tradeoff studies. This exposes contact resistance as a significant contributor to epoxy joint thermal impedance. If, instead, a datasheet value is used in a model without contact resistance, it leads to an overly optimistic calculation of thermal resistance.

Die-attach performance as a factor in device operating temperature

One of the challenges of thermal modeling is finding an accurate estimate for die-attach thermal performance, which is a very important factor in device operating temperatures.

Vendors of die-attach solders/epoxies often only list the bulk thermal conductivity (k) of their product. This is only one component of the overall die-attach thermal impedance. Bondline thickness, interfacial resistances, voiding, and filler characteristics all contribute to the overall thermal resistance, and these are to a large extent dependent on dispensing and curing processes. In addition, die-attach integrity and performance are impacted by material properties and surface characteristics of the two items being bonded. Experimentation is usually required to know with reasonable certainty how a die-attach solution will perform.

The graphic below illustrates the relationship between bondline thickness, bulk thermal conductivity, and total die-attach thermal resistance.

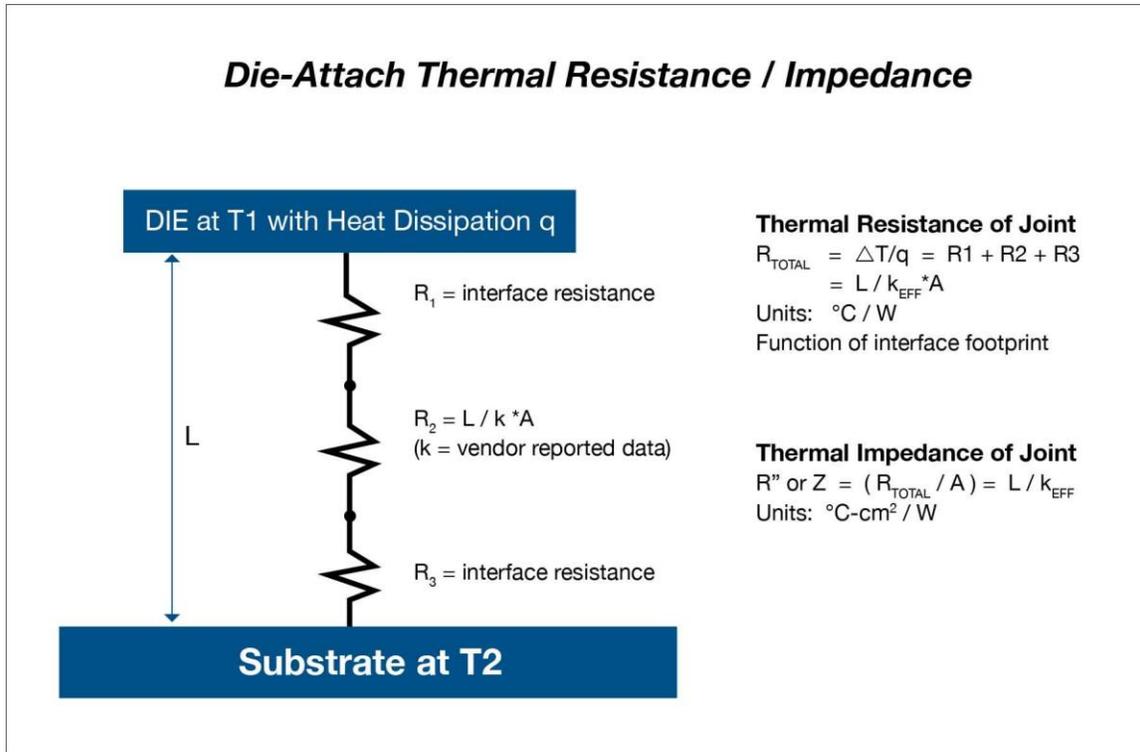


Figure 4: Illustration of die-attach thermal resistance / impedance

Below is a chart that illustrates the importance of accurate die-attach performance data. Here a GaN power amplifier die has been modeled in a typical QFN package. The maximum channel temperature has been plotted against the die-attach thermal impedance ($R_{D/A}''$).

As the $R_{D/A}''$ approaches zero (i.e., die-attach performance improves), the maximum channel temperature (T_{CH}) decreases, approaching a limit which is set by the conductive thermal resistance of the die and the QFN base. The left vertical dashed line denotes $R_{D/A}''$ as calculated solely from the measured bondline thickness (L) and the vendor-supplied value for bulk thermal conductivity (k). The right vertical dashed line is $R_{D/A}''$ as measured in the laboratory.

For this particular die/package combination, T_{CH} is underestimated by 40°C when interfacial resistances are not taken into account.

Operation for the die in this model is such that $P_{DISS} = 23$ Watts. If the total package thermal resistance R_{θ} is calculated, ignoring interfacial resistances yields an incorrect value of:

$$R_{\theta} = (T_{CH} - T_{BASE}) / P_{DISS} = (180^{\circ}\text{C} - 100^{\circ}\text{C}) / 23\text{W} = 3.5^{\circ}\text{C/W}$$

whereas the actual package thermal resistance is more accurately represented by:

$$R_{\theta} = (T_{CH} - T_{BASE}) / P_{DISS} = (220^{\circ}\text{C} - 100^{\circ}\text{C}) / 23\text{W} = 5.2^{\circ}\text{C/W}$$

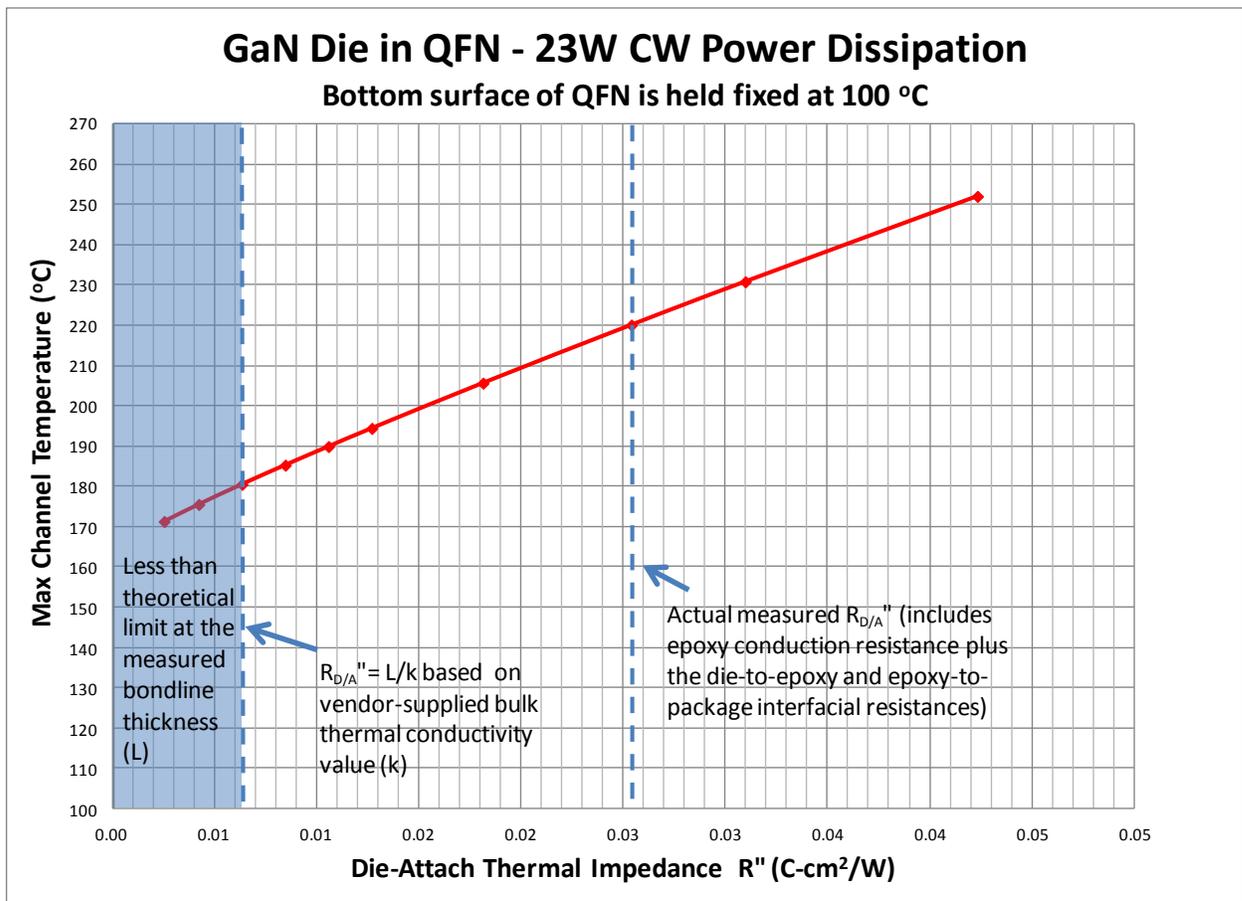


Figure 5: Illustration of the importance of accurate die-attach performance data

IV. IMPROVED PACKAGING OPTIONS FROM QORVO

Qorvo has been an industry-leader in meeting the demand for GaN technology worldwide, with extensive research and development programs and numerous GaN-based standard



product releases. As GaN technology has developed, and its power potential realized, existing semiconductor packaging technology has proven incapable of effectively supporting high power GaN products. In response, Qorvo has developed improved packaging options that provide a complete product solution for the ever-widening array of military and commercial GaN applications. Included in Qorvo's new GaN package options for high-performance systems are GaN on Copper and GaN in Plastic which are available through a number of products to be launched in 2014.

GaN on Copper

There is a growing demand for the ability to have a high-reliability, high-power, large chip size in a copper package. Qorvo has developed a copper flange-type package with leads (commonly called a module) that can handle very high power and also be scaled easily to accommodate small, large, or multiple die and components. The copper flange is thermally superior to low CTE industry standards such as CuW and CuMo, while simultaneously increasing system level reliability and allowing for solder attach to a high CTE heat sink.

GaN in Plastic

Qorvo also offers GaN in Plastic options—air cavity plastic or over-molded plastic. These packages are very small in size and low cost, but they still maintain good power handling capabilities. Plastic packages are CTE-matched to PCBs, so system level reliability is excellent. The small package sizes and excellent RF performance make them ideal replacements for costly flanged or metal-backed module components.

SUMMARY

In summary, a combination of thermal measurement methods, including micro-Raman and electrical is highly accurate and should be used in conjunction with thermal simulations, in order to gain accurate information on the thermal performance of GaN devices. Using this integrated approach enables a tightly-coupled MTTF plot and product level thermal simulation.



Additional important considerations include advanced package options for high-performance systems, accounting for contact resistance when comparing epoxy to solder, and die-attach performance as a factor in device operating temperature.

References

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