QPC6713

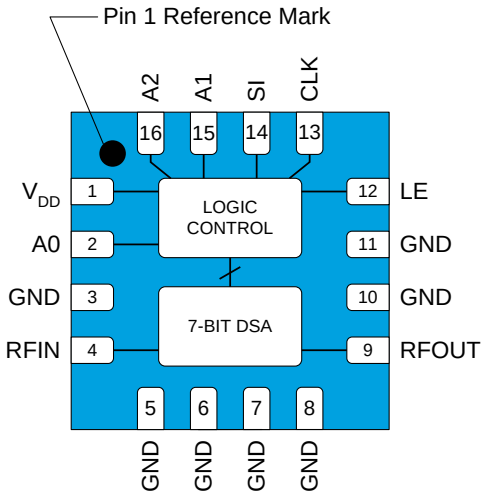
50 MHz to 6000 MHz Digital Step Attenuator

Product Description

The QPC6713 is a 7-bit digital step attenuator (DSA) that features high linearity over the entire 31.75 dB gain control range in 0.25 dB steps. The QPC6713 uses a serial control interface and has a low insertion loss of 1.7 dB at 2 GHz. The patented circuit architecture provides overshoot-free transient switching performance using a single +3 V to +5 V power supply. External address pins allow up to eight DSAs to be controlled on a single bus.

The QPC6713 is available in a standard lead-free, RoHS-compliant 16 pad 3 x3 mm QFN package.

Functional Block Diagram



Top View

16 Pad 3.0 mm x 3.0 mm x 0.85 mm QFN package

Product Features

- 7-Bit, 31.75 dB Range, 0.25 dB Step
- Patented Circuit Architecture
- Overshoot-free Transient Switching Performance
- Frequency Range 50 MHz to 6000 MHz
- High Linearity, IIP3 > +55 dBm
- Serial Control Interface
- Fast Switching Speed, 50 nsec Typical
- Devices Serial Addressable Up to Eight
- Single Supply +3 V to +5 V Operation
- RF Pins with Zero DC Voltage, No Issue with DC Grounded Externally
- Power-up Default Setting Is Maximum Attenuation

Applications

- 2G through 4G Base Stations
- Point-to-Point
- Wi-Fi
- Test Equipment

Ordering Information

Part No.	Description
QPC6713TR7	2500 pieces on a 7” reel
QPC6713PCK401	50 – 6000 MHz PCBA w/5-pc. sample bag

Absolute Maximum Ratings

Parameter	Rating
Storage Temperature	−40 to +150 °C
Supply Voltage (V_{DD})	−0.5 to +6.0 V
All Other DC and Logic Pins (Supply Voltage Must Be Applied Prior to Any Other Pin Voltages)	−0.5 to +6.0 V
Input Power (RFIN Pin, +85°C Case Temp.)	+30 dBm
Input Power (RFOUT Pin, +85°C Case Temp.)	+27 dBm

Exceeding any one or a combination of the Absolute Maximum Rating conditions may cause permanent damage to the device. Extended application of Absolute Maximum Rating conditions to the device may reduce device reliability.

Recommended Operating Conditions

Parameter	Min	Typ	Max	Units
Supply Voltage (V_{DD})	+2.7		+5.5	V
Case Temperature	−40		+105	°C
Operating Junction Temp.			+125	°C

Electrical specifications are measured at specified test conditions. Specifications are not guaranteed over all recommended operating conditions.

Electrical Specifications

Parameter	Conditions	Min	Typ	Max	Units
Frequency Range		50		6000	MHz
Insertion Loss	2000 MHz, 0 dB Attenuation Setting		1.7		dB
Attenuation Range	0.25 dB step size		31.75		dB
Attenuation Step			0.25		dB
Attenuation Accuracy		± (0.15 + 3% of Atten. Setting)			dB
Input IP3			+55		dBm
Input P0.1dB			+30		dBm
RF Input Power at RFIN Pin				+27	dBm
RF Input Power at RFOUT Pin				+20	dBm
Return Loss			15		dB
Switching Time	50% CTL to 10% / 90% RF		50		ns
Successive Step Phase Delta	2000 MHz		2		Deg.
Supply Current, I_{DD}	Steady state operation, current draw during attenuation state transitions is higher.		180		µA
Thermal Resistance			66		°C/W

Notes:
1. Test conditions unless otherwise noted: V_{DD}=+5 V, Temp= +25 °C, Freq.=2000 MHz, 50 Ω system,

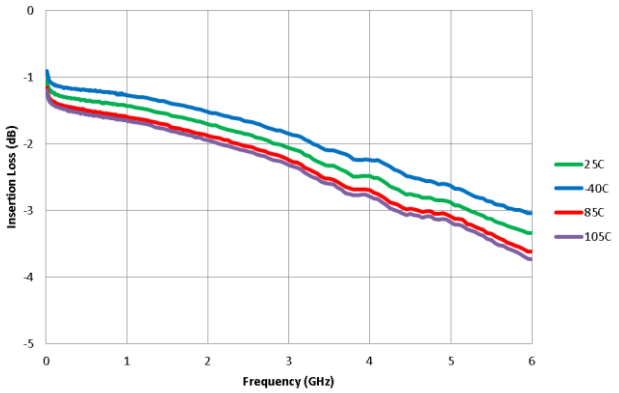
Control Logic Requirements

Parameter	Conditions	Min	Typ	Max	Units
Low State Input Voltage		0		+0.63	V
High State Input Voltage		+1.17		V_{DD}	V

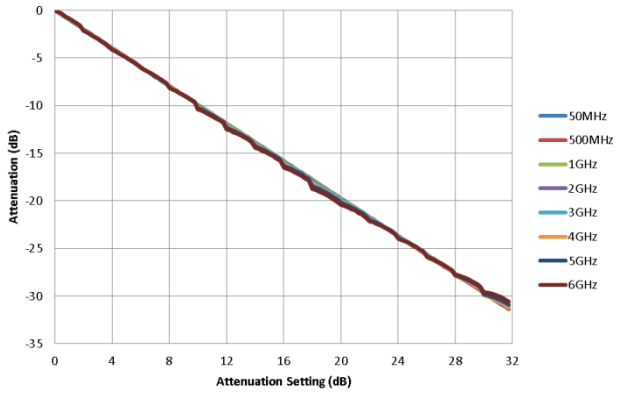
Notes:
1. Test conditions unless otherwise noted: V_{DD}=+5 V, Temp= +25 °C, Freq.=2000 MHz, 50 Ω system,

Typical Performance Plots

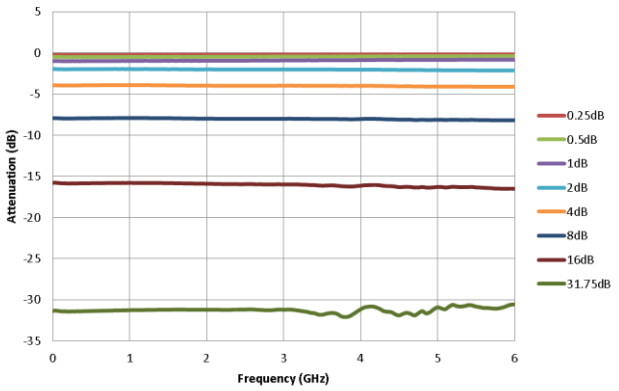
Minimum Insertion Loss vs Frequency
V_{DD} = 5V, Over Temp



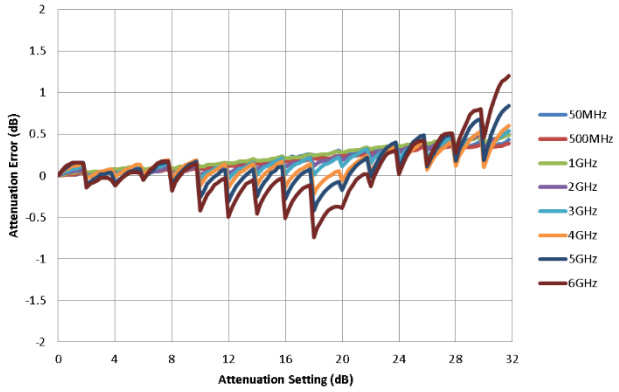
Normalized Attenuation vs Attenuation Setting
V_{DD} = 5V, Temp = +25°C



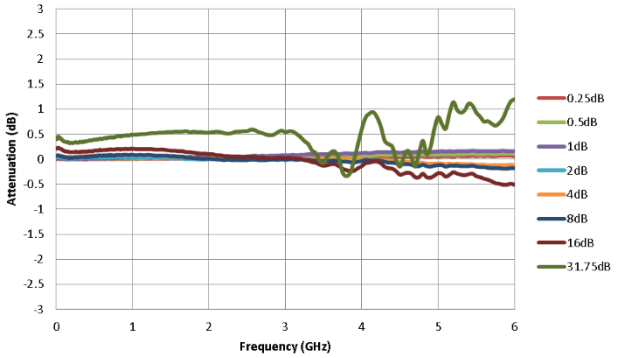
Normalized Attenuation vs Frequency
V_{DD} = 5V, Temp = +25°C



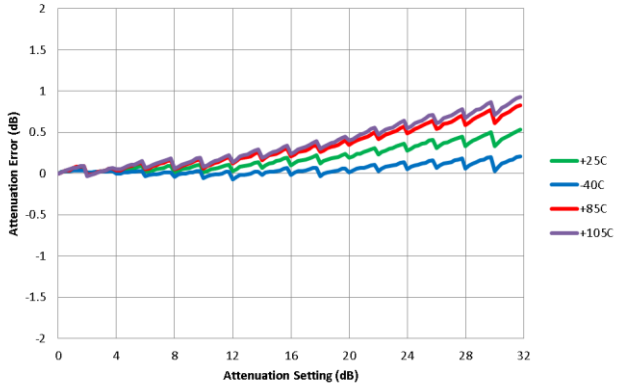
Absolute Attenuation Error vs Attenuation Setting
V_{DD} = 5V, Temp = +25°C



Major State Absolute Attenuation Error vs Frequency
V_{DD} = 5V, Temp = +25°C

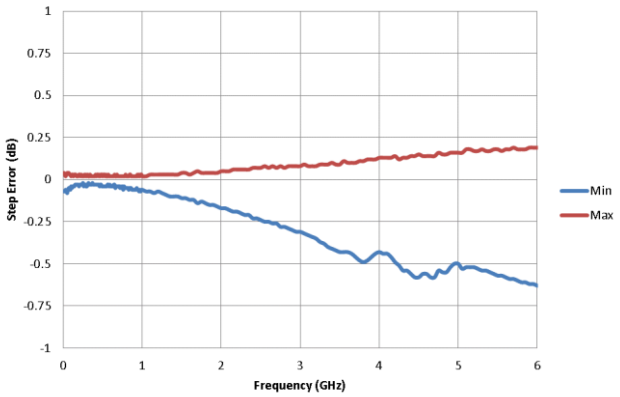


Absolute Attenuation Error vs Attenuation Setting
2GHz, V_{DD} = 5V, Over Temp

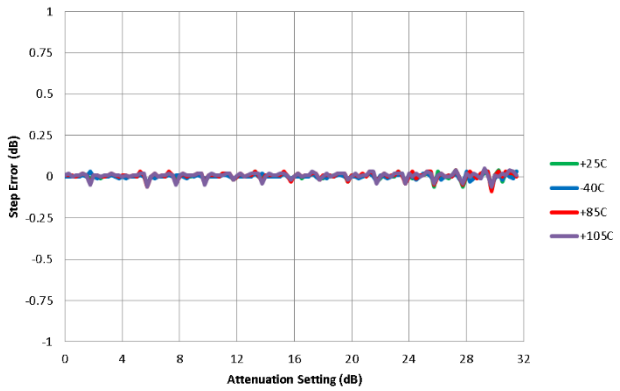


Typical Performance Plots

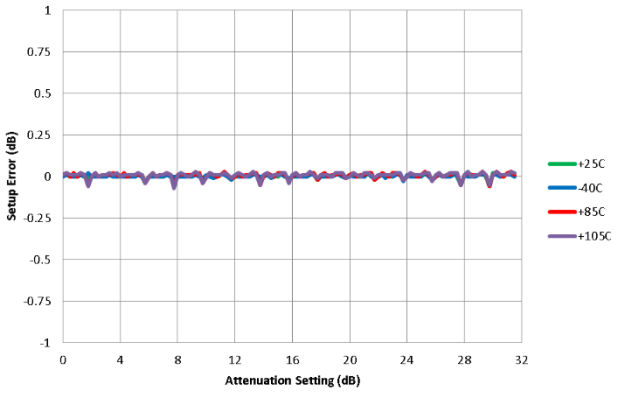
Worst Case Successive Step Error vs Frequency
0.25dB Steps, V_{DD} = 5V, Temp = +25°C



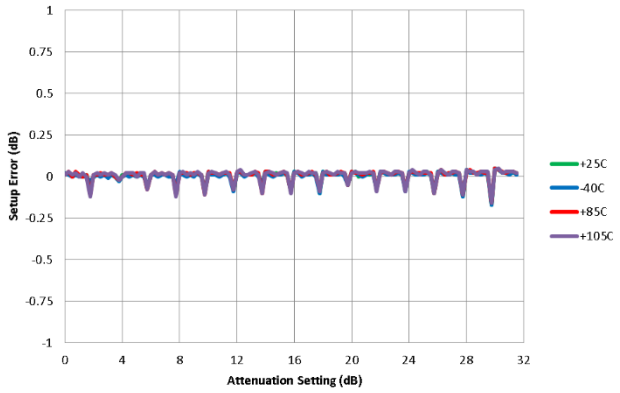
Successive Step Error vs Attenuation Setting
50 MHz, 0.25dB Steps, V_{DD} = 5V, over Temp



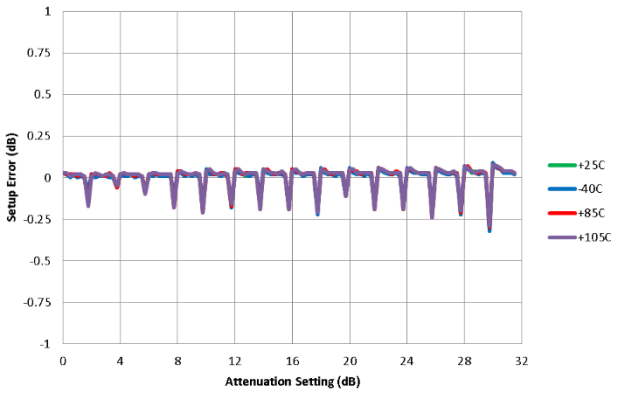
Successive Step Error vs Attenuation Setting
1 GHz, 0.25dB Steps, V_{DD} = 5V, over Temp



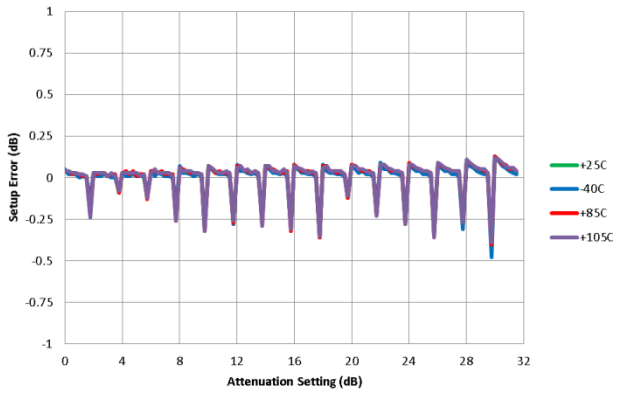
Successive Step Error vs Attenuation Setting
2 GHz, 0.25dB Steps, V_{DD} = 5V, over Temp



Successive Step Error vs Attenuation Setting
3 GHz, 0.25dB Steps, V_{DD} = 5V, over Temp

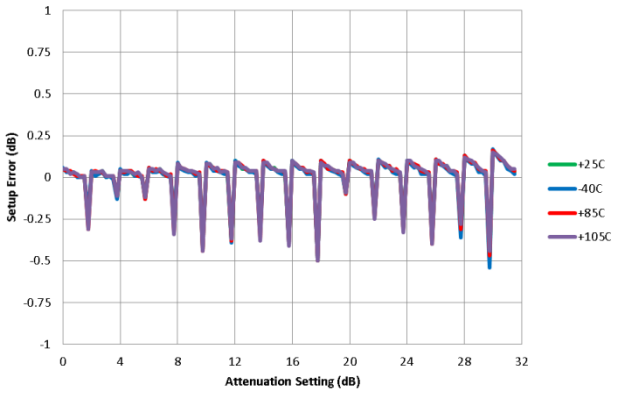


Successive Step Error vs Attenuation Setting
4 GHz, 0.25dB Steps, V_{DD} = 5V, over Temp

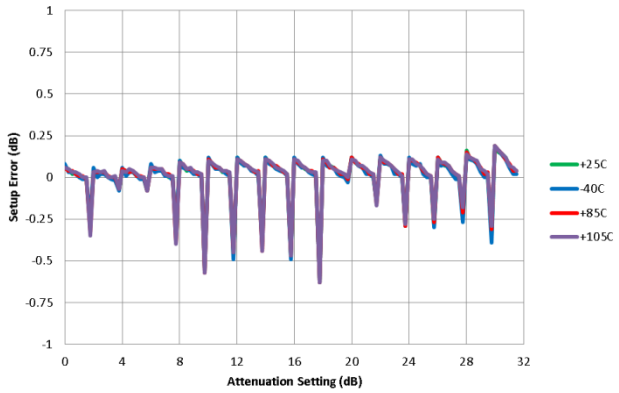


Typical Performance Plots

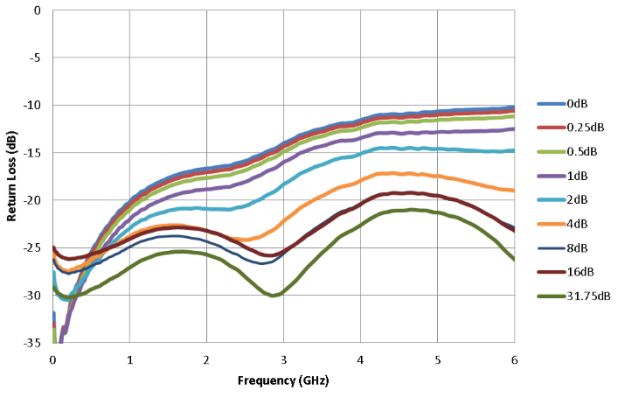
Successive Step Error vs Attenuation Setting
5 GHz, 0.25dB Steps, V_{DD} = 5V, over Temp



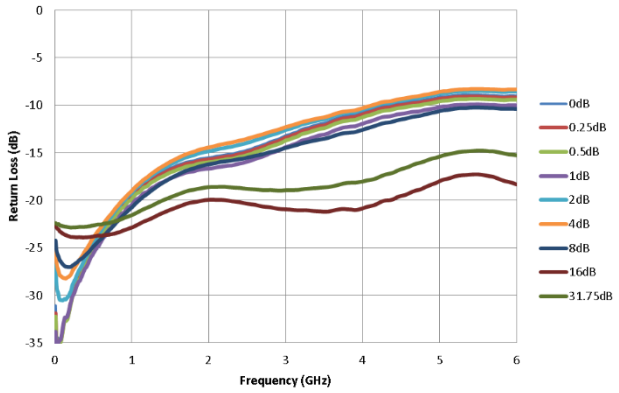
Successive Step Error vs Attenuation Setting
6 GHz, 0.25dB Steps, V_{DD} = 5V, over Temp



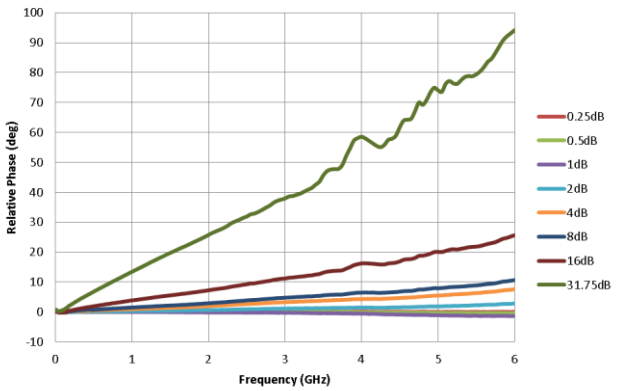
Input Return Loss vs Frequency
V_{DD} = 5V, Temp = +25°C



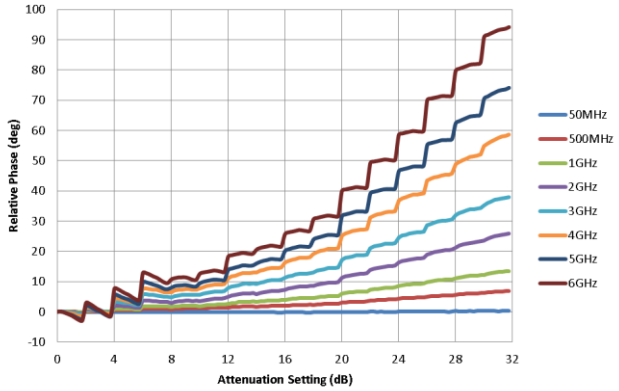
Output Return Loss vs Frequency
V_{DD} = 5V, Temp = +25°C



Relative Phase vs Frequency
V_{DD} = 5V, Temp = +25°C

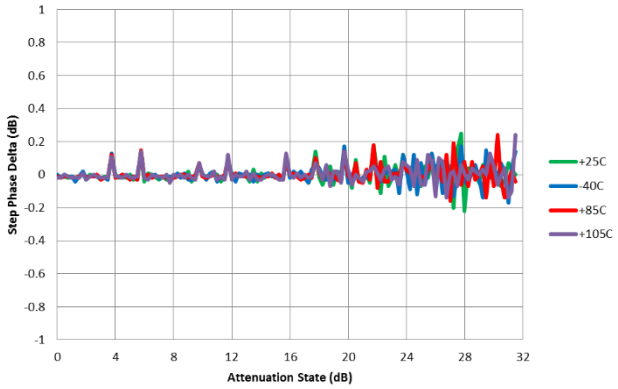


Relative Phase vs Attenuation Setting
V_{DD} = 5V, Temp = +25°C

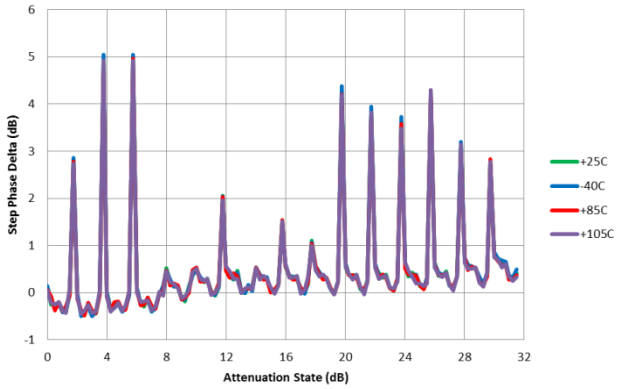


Typical Performance Plots

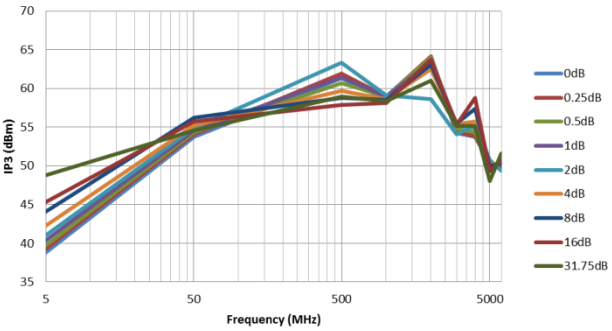
Successive Step Phase Delta versus State
50 MHz, 0.25dB Steps, V_{DD} = 5V



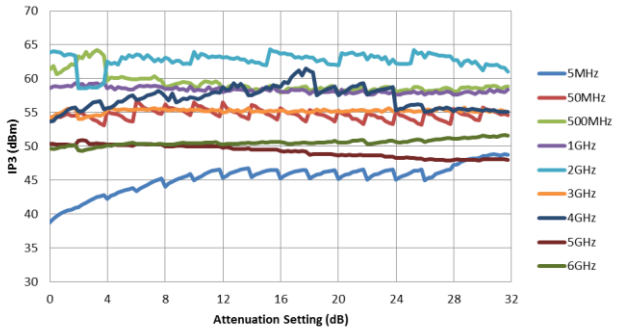
Successive Step Phase Delta versus State
4 GHz, 0.25dB Steps, V_{DD} = 5V



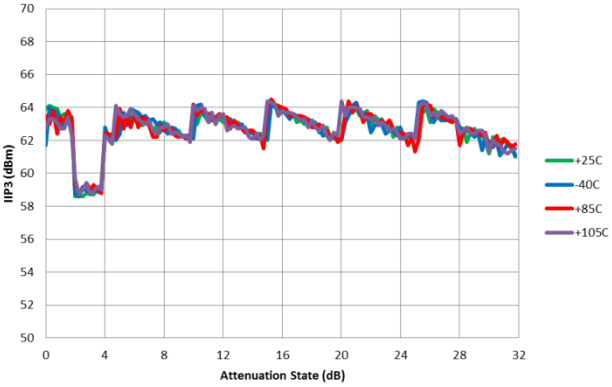
Input IP3 versus Frequency
V_{DD} = 5V, Temp = +25^{0}C
RF at 5MHz, Pin = +15dBm/Tone
RF at 50-6000MHz, Pin = +18dBm/Tone



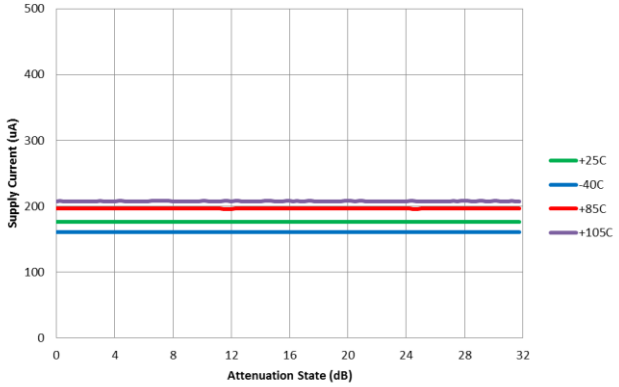
Input IP3 versus Attenuation Setting
V_{DD} = 5V, Temp = +25^{0}C
RF at 5MHz, Pin = +15dBm/Tone
RF at 50-6000MHz, Pin = +18dBm/Tone



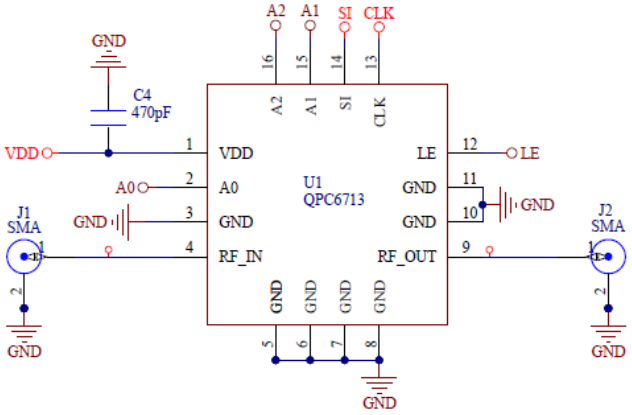
Input IP3 versus Attenuation State
RF = 2GHz, V_{DD} = 5V, Pin = +18dBm/Tone



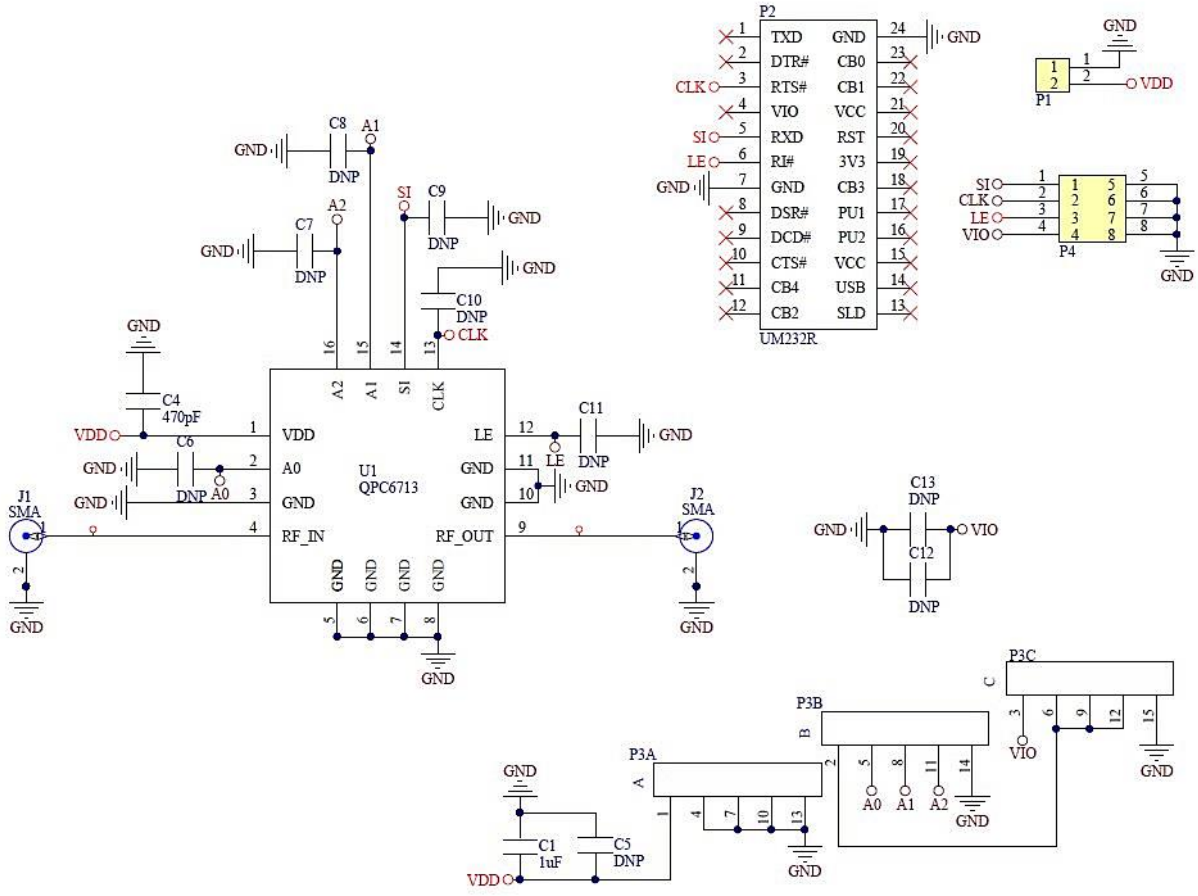
Supply Current versus Attenuation State
RF = 2GHz, V_{DD} = 5V



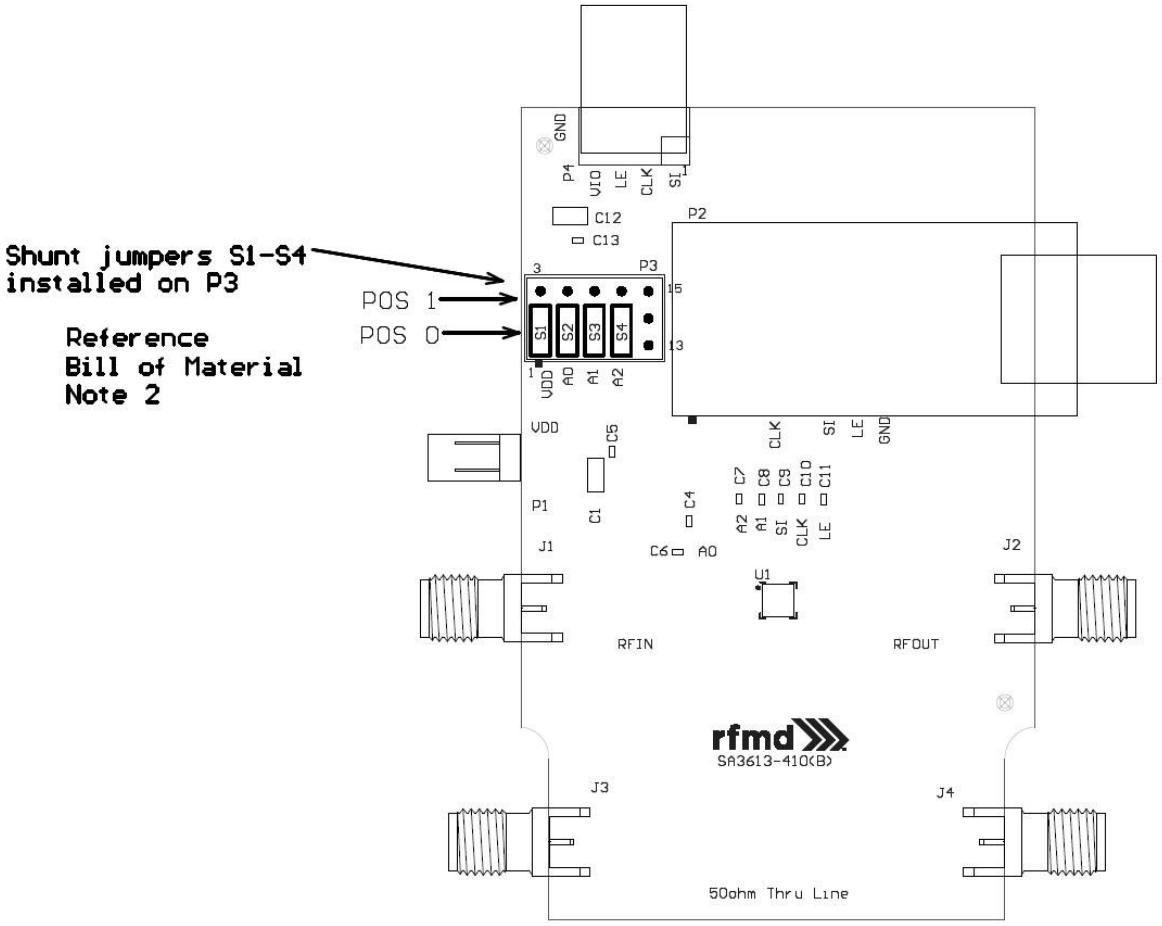
Typical Application Schematic – 50 MHz to 6000 MHz



Evaluation Board Schematic – 50 MHz to 6000 MHz



Evaluation Board Assembly Drawing



Bill of Material – Evaluation Board

Reference Des.	Value	Description	Manufacturer	Part Number
n/a	-	PCB	Qorvo	SA3613-410(B)
U1	-	Digital Step Attenuator, 50MHz to 6000MHz	Qorvo	QPC6713SB
C1	1 µF	CAP, 1µF, 10%, 25V, X7R, 1206	Taiyo Yuden	CE TMK316BJ105KL-T
J1-J4	-	CONN, SMA, END LNCH, UNIV, HYB MNT, FLT	Molex	SD-73251-4000
P1	-	CONN, HDR, ST, PLRZD, 2-PIN, 0.100”	ITW Pancon	MPSS100-2-C
P3	-	CONN, HDR, ST, 3 x 5, 0.100”, T/H	Samtec Inc.	TSW-105-07-L-T
P4	-	CONN, HDR, 2 x 4, RA, 0.100”, T/H	Samtec Inc.	TSW-104-08-G-D-RA
P2	-	CONN, SKT, 24-PIN DIP, 0.600”, T/H	Aries Electronics Inc.	24-6518-10
M1 (See Note)	-	MOD, USB TO SERIAL UART, SSOP-28	Future Technology	UM232R
C4	470 pF	CAP, 470pF, 5%, 50V, C0G, 0402	Murata Electronics	GRM1555C1H471JA01D
C5-C13	-	DNP	-	-

Notes:
1. M1 should be mounted into P2 with respect to the Pin 1 alignment of M1 and P2.
2. Install S1-S4 into P3 as indicated on the Evaluation Board Assembly Drawing.

Jumper Connections and Descriptions

Jumper	Connector	Signal	Position	U1 Connection	Comment
S1	P3	Logic Voltage	0*	V_{DD} (From P1)	
			1	V_{IO} (From P4)	
S2		A0	0*	GND	External Address
			1	U1_V_{DD}	
S3		A1	0*	GND	External Address
			1	U1_V_{DD}	
S4		A2	0*	GND	External Address
			1	U1_V_{DD}	

Asterisk (*) indicates default factory jumper position.

Evaluation Board Programming Using USB Interface

Serial Addressable Mode

All programming jumpers on the evaluation board are set to the default values indicated in the table. Refer to the Control Bit Generator (CBG) Software Reference Manual for detailed instructions on how to setup the software for use. Apply the supply voltage to P1. Select ‘QPC6713’ from the RFMD parts list of the CBG user interface. Set the attenuation value using the CBG user interface. The attenuator is set to the desired state and measurement can be taken. Note that the external address bits must all be set to ‘0’ when using the USB interface as the CGB software does not have the capability to set the external address in the serial data stream at this time.

Evaluation Board Programming Using External Bus

Serial Addressable Mode

The configuration allows the user to control the attenuator through the P4 connector using an external harness. Remove the USB interface board if it is currently installed on the evaluation board. Connect a user-supplied harness to the P4 connector. Note that the top row of P4 contains the serial bus signals and the bottom row is ground. Programming jumper S1 is set to ‘0’. External address jumpers S2 through S4 can be set to any value desired by the user. Apply the supply voltage P1. Send the appropriate signals onto the serial bus lines in accordance with the Serial Mode Timing Diagram. The attenuator is set to the desired state and measurements can be taken.

Default Power-up State

The default attenuation state is maximum (31.75 dB) when supply voltage is applied to the attenuator. The LE signal must be held to logic ‘0’ during power up.

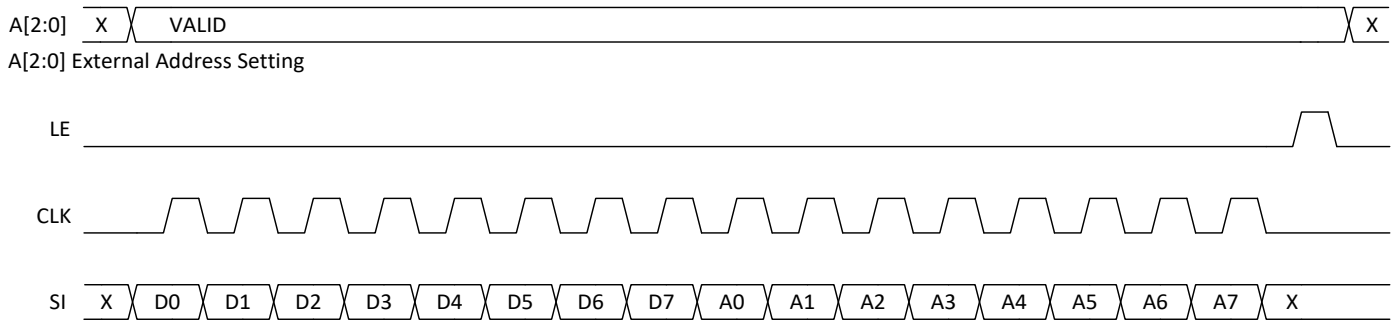
Serial Addressable Mode Attenuation Word Truth Table

Attenuation Word								
D7	D6	D5	D4	D3	D2	D1	D0 (LSB)	Attenuation State
X	L	L	L	L	L	L	L	0dB / Reference Insertion Loss
X	L	L	L	L	L	L	H	0.25dB
X	L	L	L	L	L	H	L	0.5dB
X	L	L	L	L	H	L	L	1dB
X	L	L	L	H	L	L	L	2dB
X	L	L	H	L	L	L	L	4dB
X	L	H	L	L	L	L	L	8dB
X	H	L	L	L	L	L	L	16dB
X	H	H	H	H	H	H	H	31.75dB

Serial Addressable Mode Address Word Truth Table

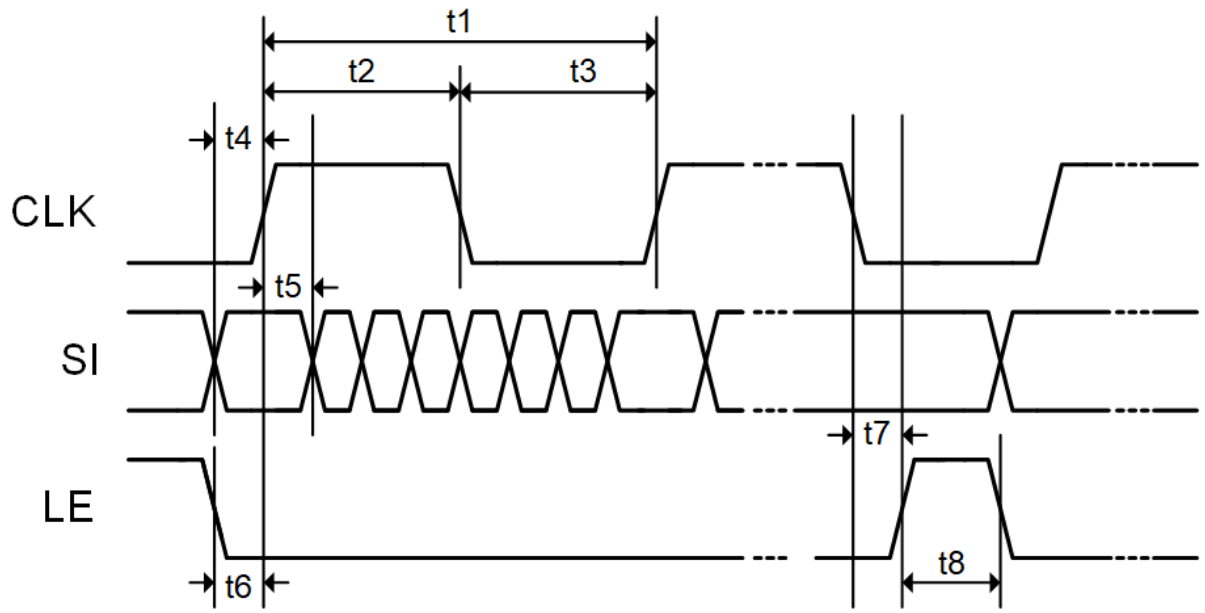
Address Word								
A7	A6	A5	A4	A3	A2 (MSB)	A1	A0	Address Setting
X	X	X	X	X	L	L	L	000
X	X	X	X	X	L	L	H	001
X	X	X	X	X	L	H	L	010
X	X	X	X	X	L	H	H	011
X	X	X	X	X	H	L	L	100
X	X	X	X	X	H	L	H	101
X	X	X	X	X	H	H	L	110
X	X	X	X	X	H	H	H	111

Serial Addressable Mode Timing Diagram



Note: Bits D7, A3-A7 are not used
and can be set to logic high or low

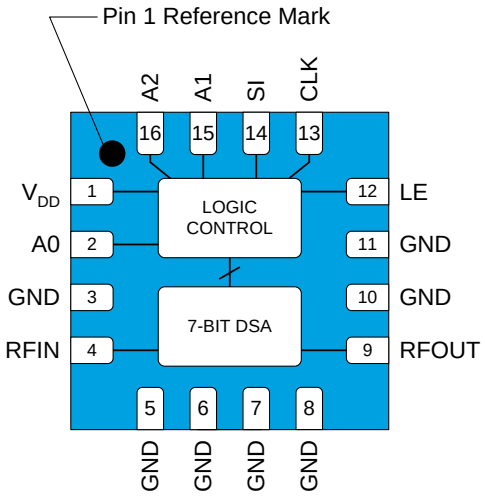
Serial Bus Timing Specifications



Parameter	Symbol	Min.	Max.	Unit
CLK Frequency	1/t1		25	MHz
CLK High Time	t2	20		ns
CLK Low Time	t3	20		ns
SI Setup Time	t4	5		ns
SI Hold Time	t5	5		ns
LE Low Setup Time	t6	5		ns
LE High Setup Time	t7	5		ns
LE High Time	t8	10		ns

Pad Configuration and Description

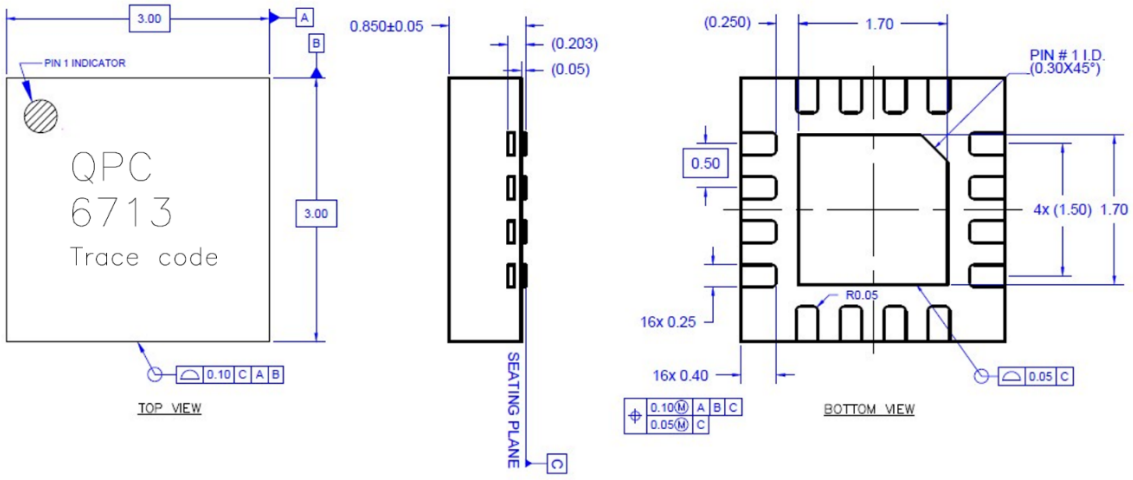
Top View



Pad No.	Label	Description
1	V_{DD}	Supply Voltage
2	A0	A0 External Address
3	GND	Ground
4	RFIN	RF Input. Incident RF power must enter this pin for rated thermal performance and reliability. DC blocking required while non-zero DC voltage present externally.
5	GND	Ground
6	GND	Ground
7	GND	Ground
8	GND	Ground
9	RFOUT	RF Output. DC blocking required while non-zero DC voltage present externally.
10	GND	Ground
11	GND	Ground
12	LE	Latch Enable. The leading edge of signal on LE causes the attenuator to change state
13	CLK	Serial Clock Input
14	SI	Serial data Input
15	A1	A1 External Address
16	A2	A2 External Address
Backside Pad	GND	RF/DC ground. Use recommended via hole pattern to minimize inductance and thermal resistance. See PCB Mounting Pattern for suggested footprint.

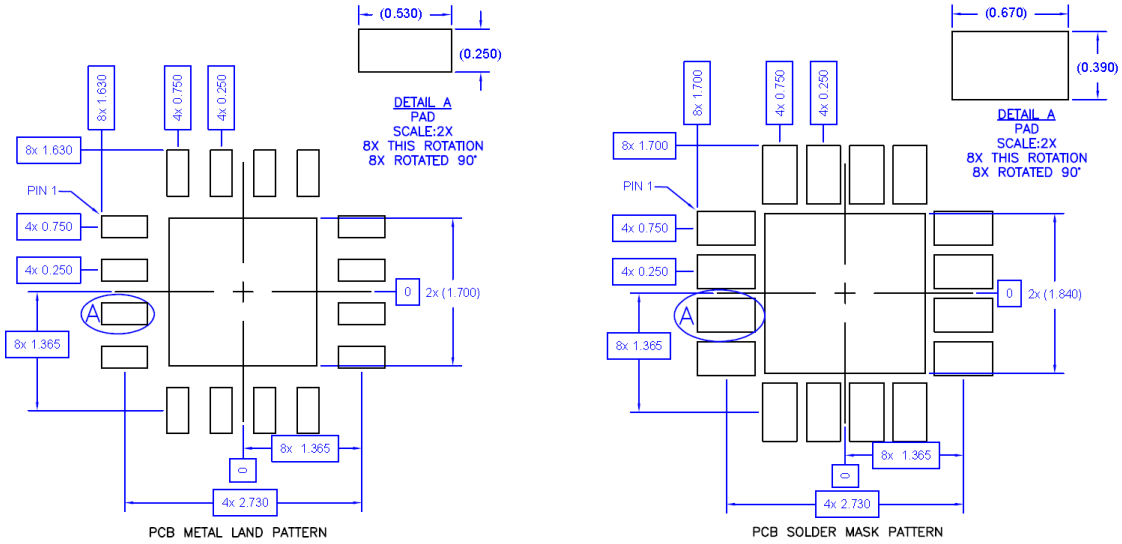
Package Marking and Dimensions

Marking: ● – Pin 1 Indicator
QPC6713 – Part Number
Trace code – Assigned by Contract Manufacture



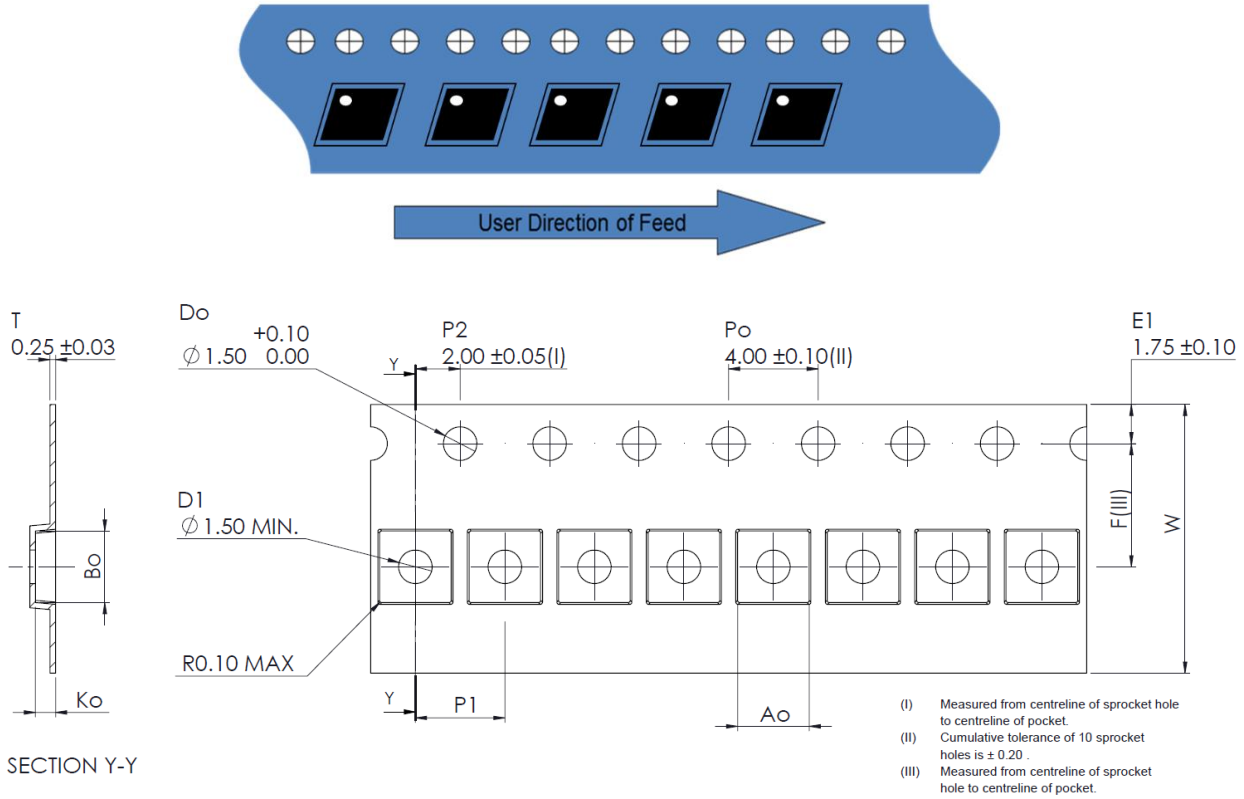
Notes:
1. All Dimensions in millimeters

PCB Mounting Pattern



Notes:
1. All dimensions are in mm. Angles are in degrees.
2. A heat sink underneath the area of the PCB for the mounted device is recommended for proper thermal operation.
3. Ground / thermal via holes are critical for the proper performance of this device. Via holes should use a .35mm (#80 / .0135") diameter drill and have a final plated through diameter of .25 mm (.010").
4. Add as much copper as possible to inner and outer layers near the part to ensure optimal thermal performance.

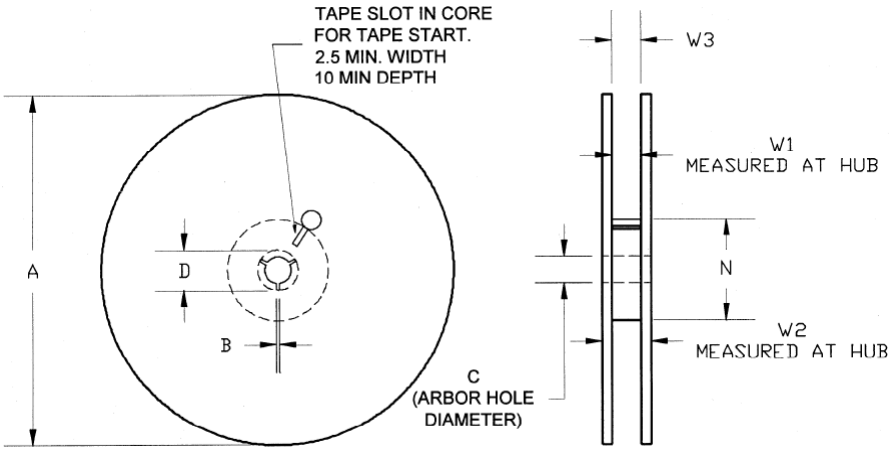
Tape and Reel Information – Carrier and Cover Tape Dimensions



Feature	Measure	Symbol	Size (in)	Size (mm)
Cavity	Length	A0	0.125	3.20
	Width	B0	0.125	3.20
	Depth	K0	0.040	1.00
	Pitch	P1	0.157	4.00
Centerline Distance	Cavity to Perforation - Length Direction	P2	0.079	2.00
	Cavity to Perforation - Width Direction	F	0.217	5.50
Cover Tape	Width (Reference Only)	C	0.362	9.20
Carrier Tape	Width	W	0.472	12.0

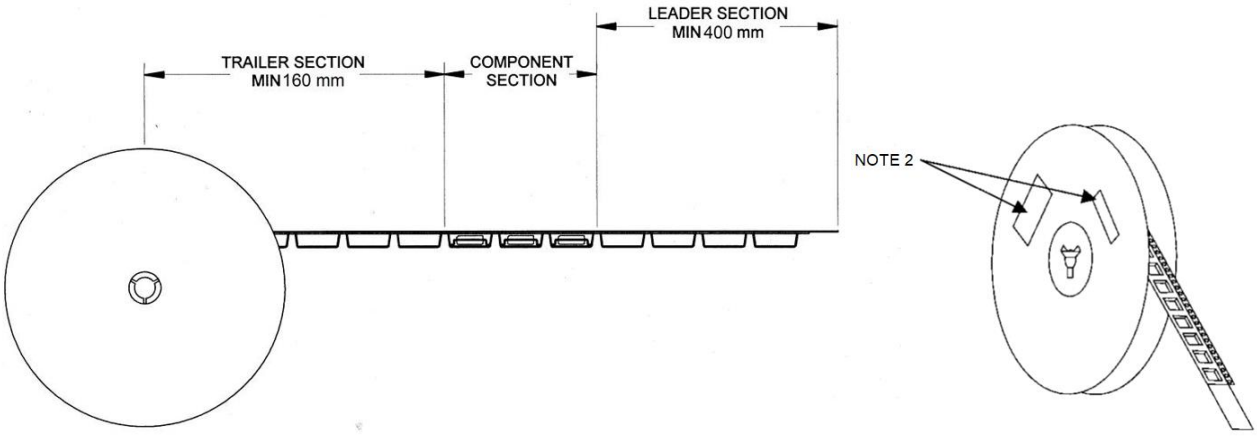
Tape and Reel Information – Reel Dimensions

Standard T/R size = 2,500 pieces on a 7” reel.



Feature	Measure	Symbol	Size (in)	Size (mm)
Flange	Diameter	A	6.969	177.0
	Thickness	W2	0.717	18.2
	Space Between Flange	W1	0.504	12.8
Hub	Outer Diameter	N	2.283	58.0
	Arbor Hole Diameter	C	0.512	13.0
	Key Slit Width	B	0.079	2.0
	Key Slit Diameter	D	0.787	20.0

Tape and Reel Information – Tape Length and Label Placement



Notes:
1. Empty part cavities at the trailing and leading ends are sealed with cover tape. See EIA 481-1-A.
2. Labels are placed on the flange opposite the sprockets in the carrier tape.

Handling Precautions

Parameter	Rating	Standard
ESD – Human Body Model (HBM)	Class 1C	ESDA / JEDEC JS-001-2012
ESD – Charged Device Model (CDM)	Class C3	JEDEC JESD22-C101F
MSL – Moisture Sensitivity Level	Level 1	IPC/JEDEC J-STD-020

Caution!
ESD-Sensitive Device

Solderability

Compatible with both lead-free (260°C max. reflow temp.) and tin/lead (245°C max. reflow temp.) soldering processes.
Solder profiles available upon request.

Contact plating: Matte Tin

RoHS Compliance

This part is compliant with 2011/65/EU RoHS directive (Restrictions on the Use of Certain Hazardous Substances in Electrical and Electronic Equipment) as amended by Directive 2015/863/EU.

This product also has the following attributes:

- Lead Free
- Halogen Free (Chlorine, Bromine)
- Antimony Free
- TBBP-A ($C_{15}H_{12}Br_4O_2$) Free
- PFOS Free
- SVHC Free

Contact Information

For the latest specifications, additional product information, worldwide sales and distribution locations:

Web: www.qorvo.com
Tel: 1-844-890-8163
Email: customer.support@qorvo.com

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