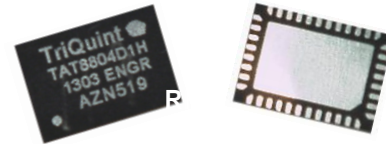


Product Overview

The TAT8804 is an ultra-linear, QFN GaAs amplifier MMIC intended for output stage amplification in CATV infrastructure applications. The device features a push-pull cascode design which provides flat gain along with ultra-low distortion, making it ideal for use in CATV distribution systems requiring high output power capability. ESD protection is also provided at the output of the device.

The TAT8804 draws approximately 650 mA from a single +12 V supply providing 21dB gain with excellent linearity. Users may adjust the bias current with external voltage enabling the TAT8804 to be used in applications such as doublers or for lower power system applications.

The TAT8804 is packaged in an industry standard 40 pin 5 x 7 mm QFN package with exposed paddle (EP) beneath the device for thermal and electrical grounding. For applications requiring demanding VSWR tolerance at high input overdrive conditions, an EVB with level protection is available (TAT8804D1H-EBP).

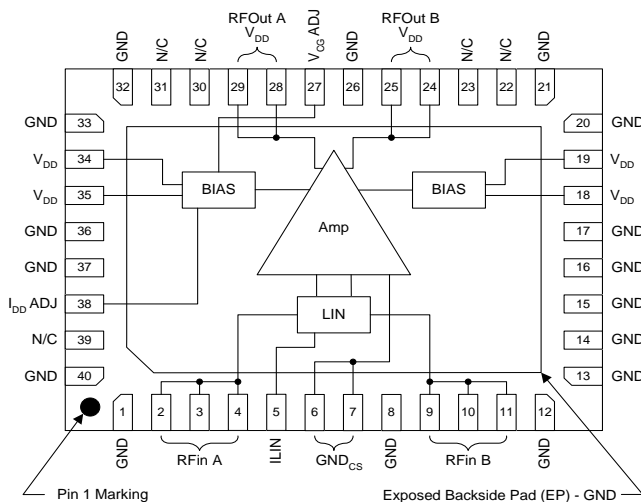


Package: QFN, 40-pin, 5 x 7mm

Key Features

- 50 to 1000 MHz Bandwidth
- Excellent High Output Linearity at Reduced Supply Voltages
- Ultra-Low CSO / CTB / XMOD
- Low Noise through 1.2 GHz
- Excellent Input/Output Return Loss
- High Gain: 21 dB typical at 1.2 GHz
- Variable Bias Control
- Compact 5 X 7 mm QFN Package
- High Reliability with RF ESD protection
- +12 V Supply Voltage
- 650 mA Operating Current

Functional Block Diagram



Top View

Applications

- HFC Nodes
- CATV Line Amplifiers
- Head End Equipment
- 50 – 1000 MHz 75Ω Amplifier

Ordering Information

Part Number	Description
TAT8804D1H	GaAs Power Doubler MMIC
TAT8804D1H-EB	50 – 1200 MHz Evaluation Board
TAT8804D1H-EBP	50 – 1200 MHz EVB + Protection

Absolute Maximum Ratings

Parameter	Rating
Storage Temperature	-40 to +100 °C
Operating Temperature	-40 to +85 °C
Device Voltage (V _{DD})	+18 V
Device Current (I _{DD})	750 mA

Exceeding any one or a combination of the Absolute Maximum Rating conditions may cause permanent damage to the device. Extended application of Absolute Maximum Rating conditions to the device may reduce device reliability.

Recommended Operating Conditions

Parameter	Min	Typ	Max	Units
Device Voltage (V _{DD})		+12		V
Tj for >10 ⁶ hours MTTF			+165	°C

Electrical specifications are measured at specified test conditions. Specifications are not guaranteed over all recommended operating conditions.

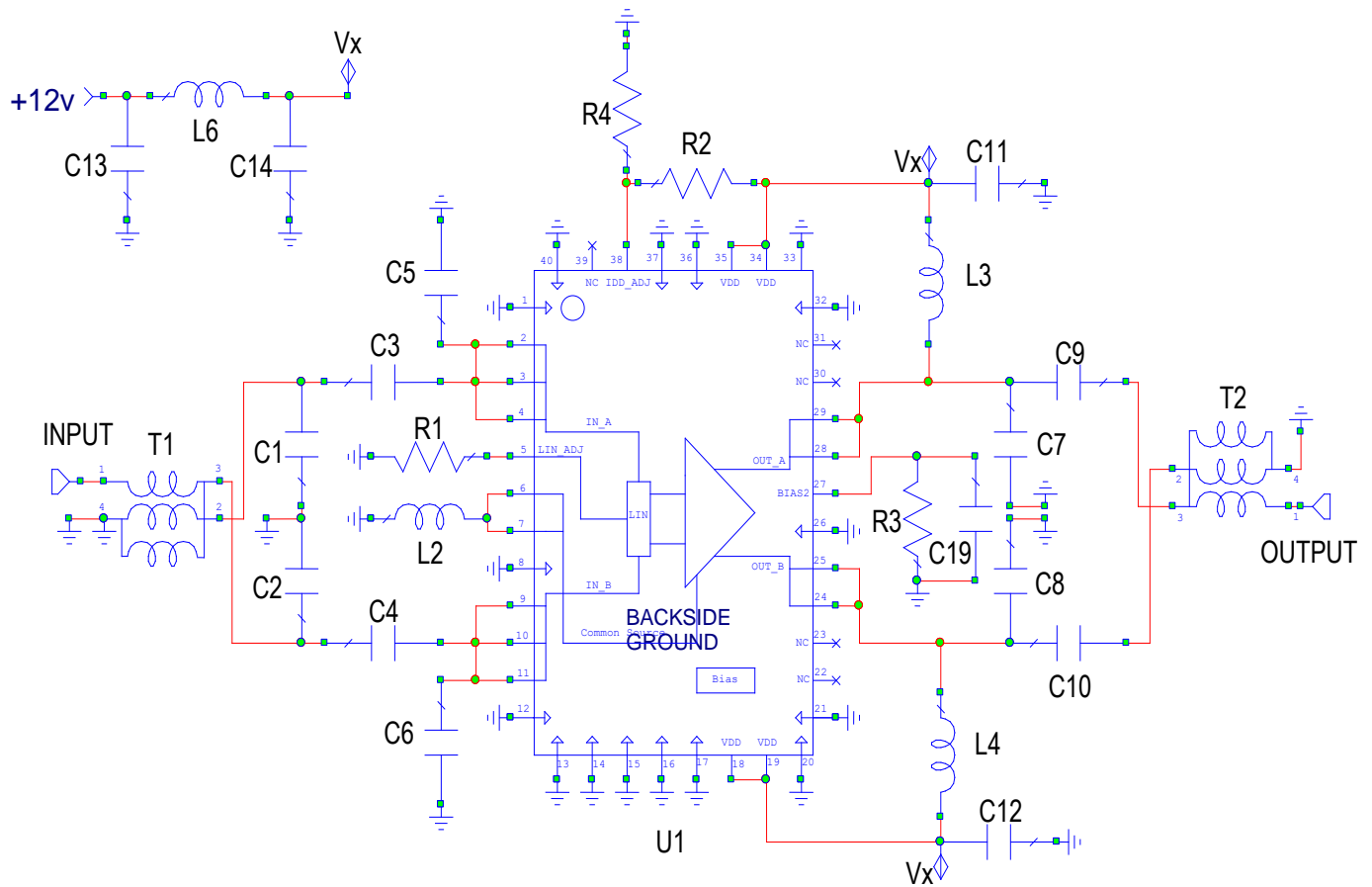
Electrical Specifications

Parameter	Conditions	Min	Typ	Max	Units
Operational Frequency Range		50		1200 ⁽¹⁾	MHz
Current (I _{DD})		550	650	720	mA
Gain	f _o = 50 & 1003 MHz	EVB: EB	21		dB
		EVB: EBP ⁵	19.5		
Gain Flatness	50 to 1003 MHz ⁽²⁾	-0.5		+0.5	
Gain Tilt	50 to 1003 MHz ⁽³⁾		+0.6		
Input Return Loss	f _o = 55 MHz		20		dB
	f _o = 1003 MHz		17		
	f _o = 1200 MHz		16		
Output Return Loss	f _o = 55 MHz		20		dB
	f _o = 1003 MHz		17		
	f _o = 1200 MHz		12		
Overdrive VSWR Mismatch Tolerance	79 Ch. NTSC + 75 Ch. QAM, -6 dB offset, Vin = +44 dBmV per channel	EVB: EB		1.37:1 (16)	VSWR (dB)
		EVB: EBP ⁵		5.85:1 (3)	
CSO	79 Ch. NTSC + 75 Ch. QAM, -6 dB offset EQ Vout = +57dBmV with 15.6 dB tilt	Note 4	-73	-68	dBc
CTB			-79	-70	dBc
XMOD			-62		dBc
CCN			60	64	dB
OIP2	f ₁ - f ₂ = 50 MHz, +17 dBm / tone	Note 4	85		dBm
OIP3			49		dBm
P1dB	f _o = 50 & 1003 MHz		34		dBm
Noise Figure			4.5		dB
Thermal Resistance, θ _{jb}	Junction to base		5.5		°C / W

Notes:

1. S21 Bandwidth can extend to 1200 MHz with some S11 & S22 degradation
2. Using least squares fit across the band 50 to 1003 MHz
3. Gain of S21_{1003 MHz} – S21_{50 MHz}
4. Standard EB configuration (EVB without protection), R1 = 4.3 KΩ
5. EBP – Evaluation board with protection

Evaluation Board Schematic





TAT8804D1H

21dB CATV 12V Power Doubler

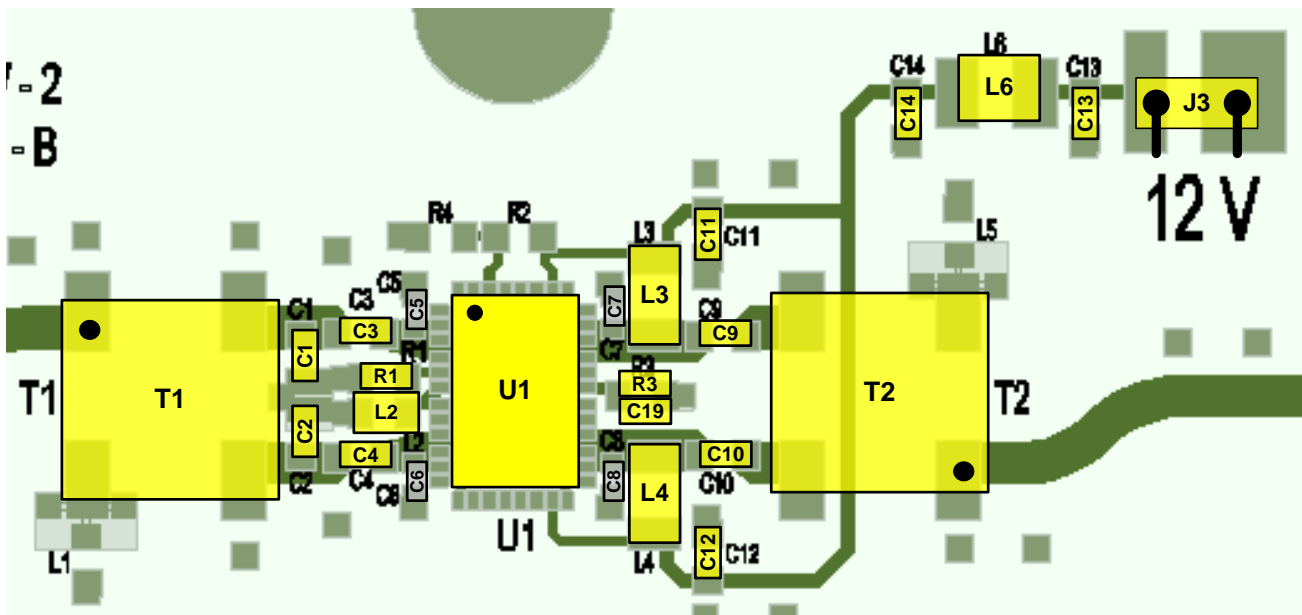
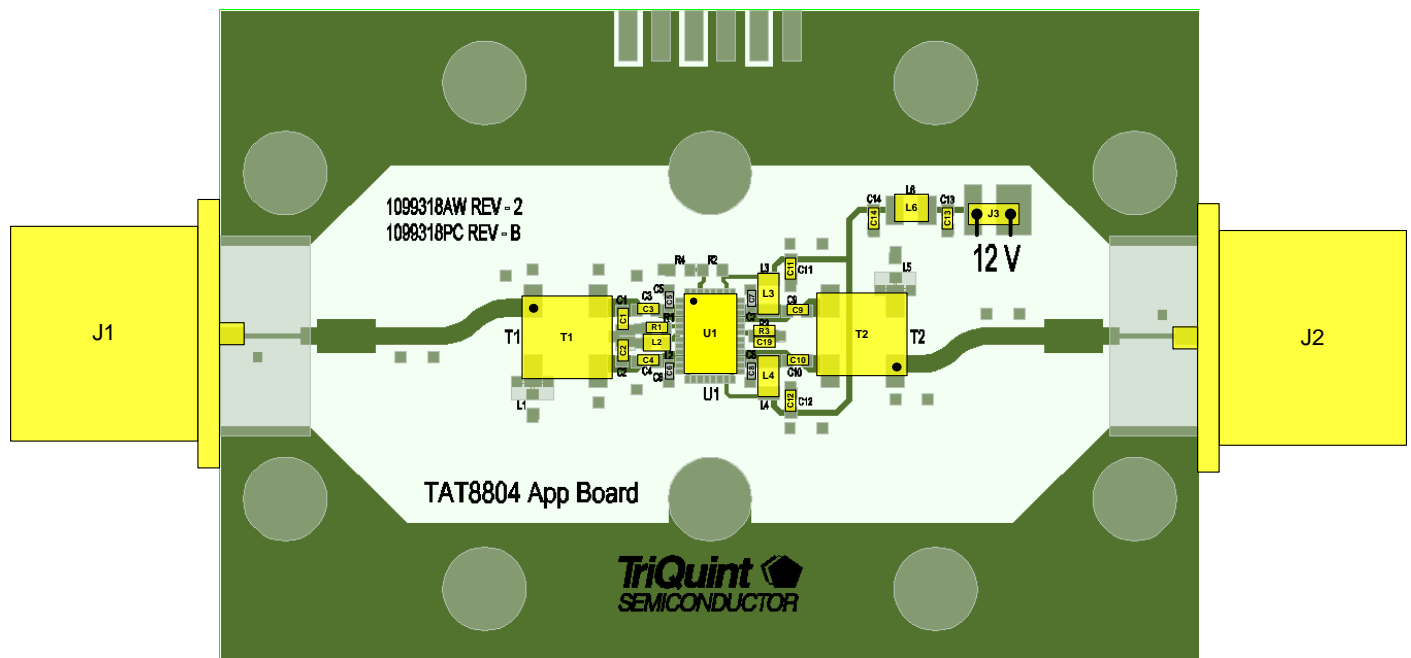
Bill of Material – TAT8804D1H – EB

Reference Designator	Value	Description	Manufacturer
PCB	Rev B	PCB TAT8804 – EVB	Qorvo
U1	n/a	TAT8804D1H Sample	Qorvo
T1, T2	1:1 BALUN, 75Ω	MABA – 009210 – CT1760	MACOM
C11, C12	0.01 uF	CAP, 0603, 10%, 50 V, X7R	TDK
C3, C4	270 pF	CAP, 0603, 5%, 50 V, NPO	TDK
C9, C10	330 pF	CAP, 0603, 5%, 50 V, NPO	TDK
C13, C14	0.1 uF	CAP, 0603, 10%, 50 V, X7R	TDK
C19	4.7 uF	CAP, 0603, 10%, 10 V, Y5V	Murata
L2 ¹ , L3, L4	680 nH	IND, 0805, 5%, 355 MHz SRF, 660 mA	Coilcraft
R1	4.3 KΩ	RES, 0603, 1%, 1/10W	Panasonic
R3	680 Ω	RES, 0603, 1%, 1/10W	Panasonic
L6	900 nH	IND, 1008, 10%, 1008AF – 901X	Coilcraft
J1, J2	75 Ω	N-TYPE MALE, PANEL MOUNT	Pasternack
J3	2 pin 0.1" RA	Molex SMT connector	Molex
R2, R4, R5, C1, C2, C5, C6, C7, C8 ² , L1, L5	n/a	Do Not Populate	N/A
PH 4-40	4-40, 0.25",	Pan Head Screw w/ lock washer	various
SH 4-40	4-40, 0.25",	Socket Head Screw	various
	Cut to 0.25" x 0.4"	Indium foil 1" x 1" x 0.004"	Indium Corp
Heatsink	Aluminum	Heatsink for 62 mil board	Qorvo

Notes:

1. Output source degeneration inductor must be rated for 650mA for I_{DD} flowing through RF output devices.
2. CSO may be improved by correcting Balun phase asymmetry by adding a 0.3 pF to C8.

Evaluation Board – TAT8804D1H – EB



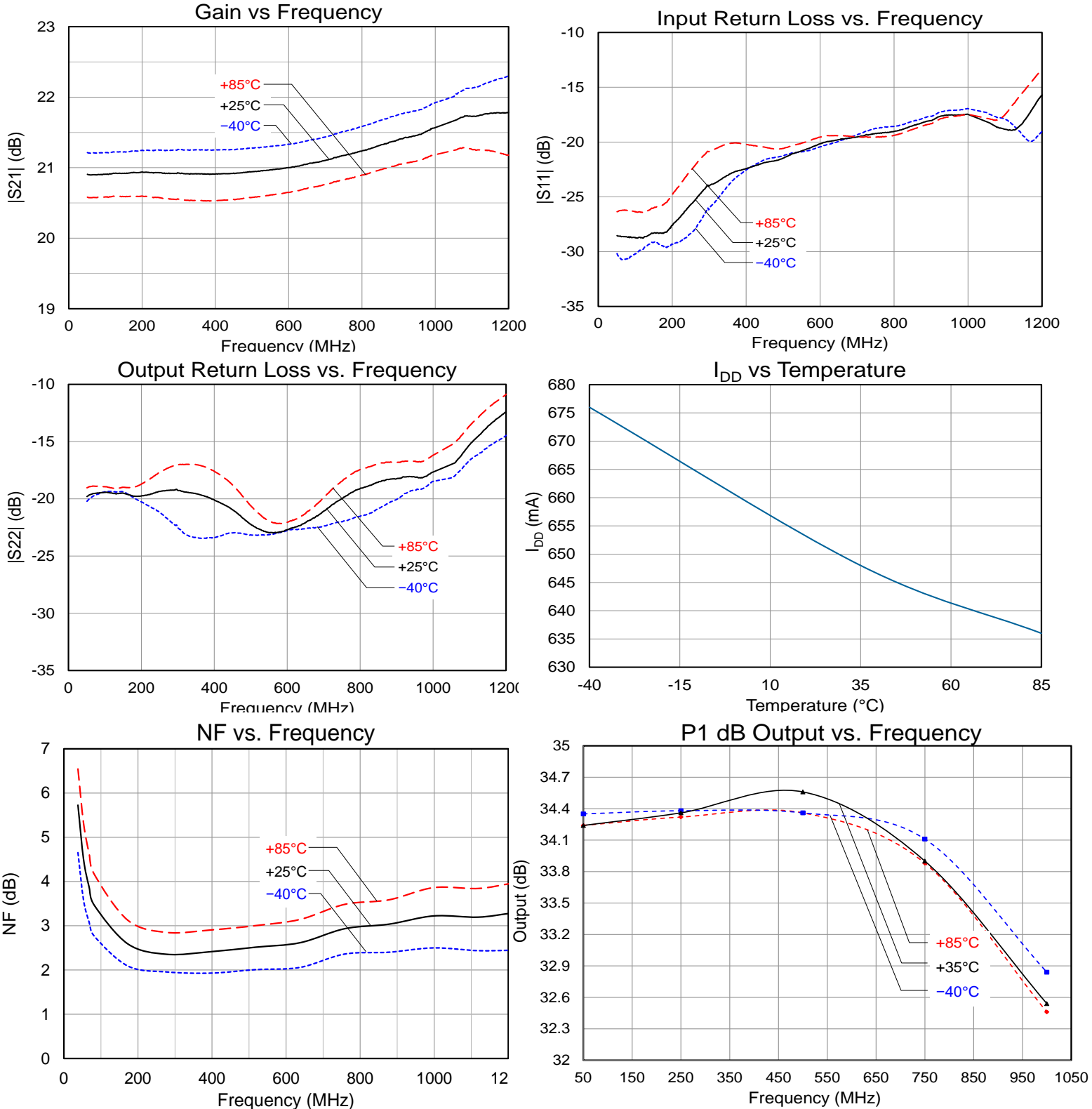
Typical Performance – TAT8804D1H – EB

Parameter	Conditions	Typical Value				Units
Frequency		50	550	1003	1200	MHz
Gain	Ptest = -20 dBm	21.2	21.1	21.3	21.5	dB
Input Return Loss		20	20	17	16	dB
Output Return Loss		20	19	17	12	dB
CSO	79 Ch. NTSC + 75 Ch. QAM, -6 dB offset, EQ Vout = +57 dBmV with 15.6 dB tilt	-73	-78			dBc
CTB		-79	-82			dBc
XMOD		-65	-62			dBc
CCN		64	66			dB
CIN		64	66			dB
Output P1dB		+34.2	+35.2	+35	+31.4	dBm
Output IP3	Pout = +17 dBm / tone, $\Delta f = 50$ MHz		+55	+50	+45.5	dBm
Noise Figure		5.8	2.5	3	3.3	dB
Current (IDD)		650				mA

Notes: Test conditions unless otherwise noted: $V_{DD} = +12V$, Heatsink Temp = +35 °C, $Z_{IN} / Z_{OUT} = 75\Omega$ using evaluation board EB. Includes input and output balun / transformer losses of tuned application circuit.

Performance Plots – TAT8804D1H – EB

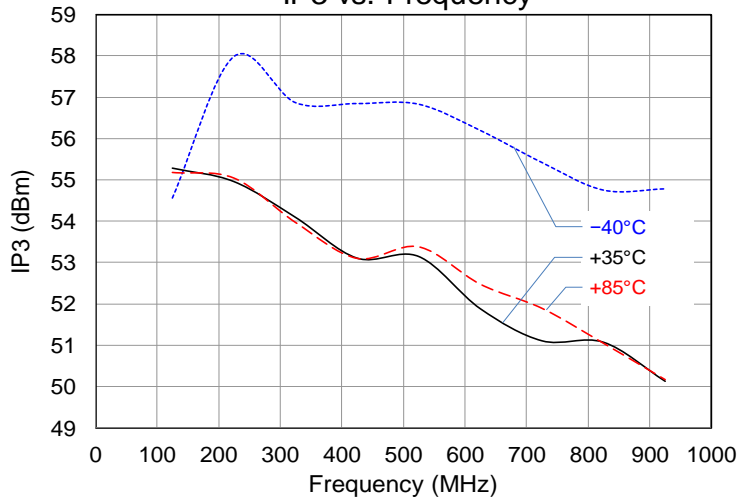
Test conditions unless otherwise stated: Heatsink Temp. = +35 °C, $V_{DD} = +12V$, $Z_0 = 75\Omega$



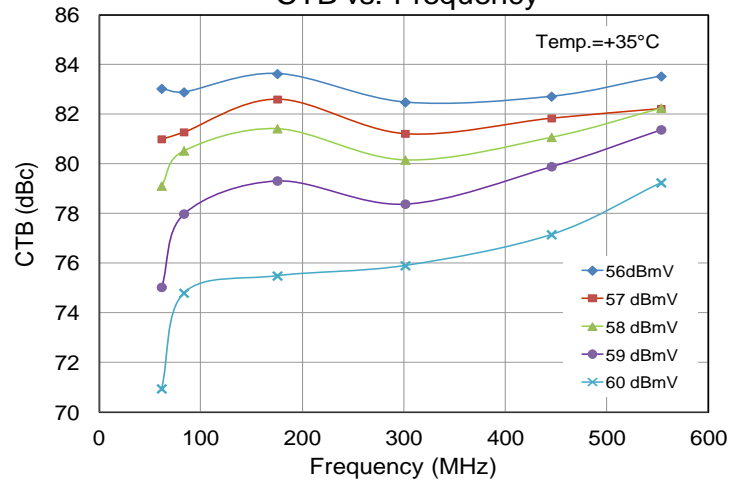
Performance Plots – TAT8804D1H – EB (cont'd)

Test conditions unless otherwise stated: Heatsink Temp. = +35 °C, $V_{DD} = +12V$, $Z_0 = 75\Omega$

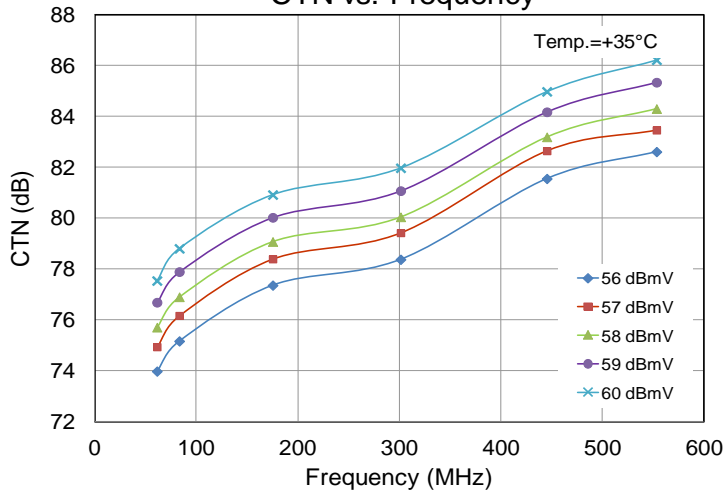
IP3 vs. Frequency



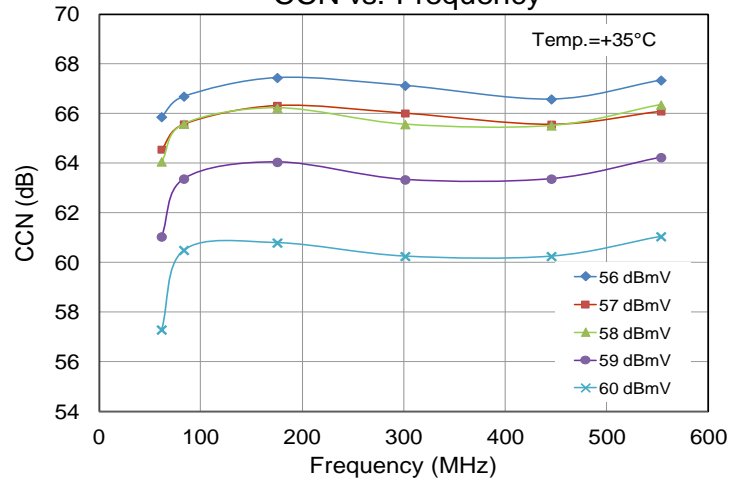
CTB vs. Frequency



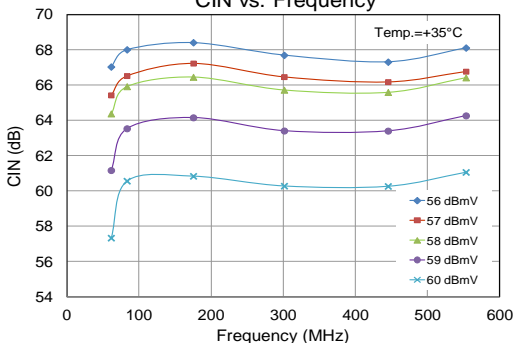
CTN vs. Frequency



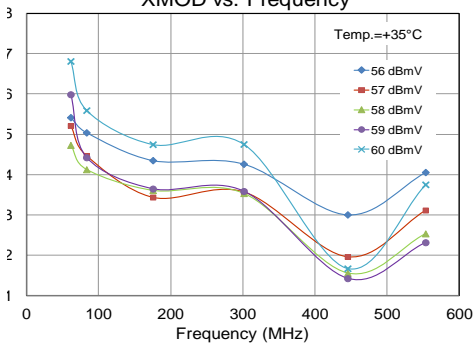
CCN vs. Frequency



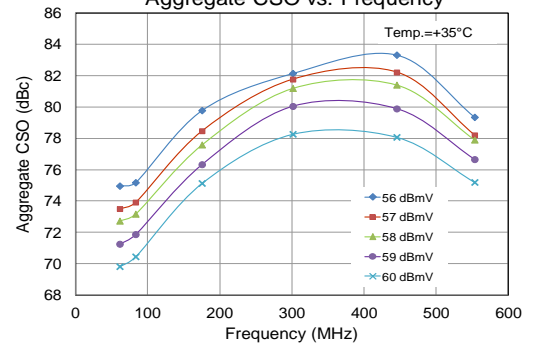
CIN vs. Frequency



XMOD vs. Frequency

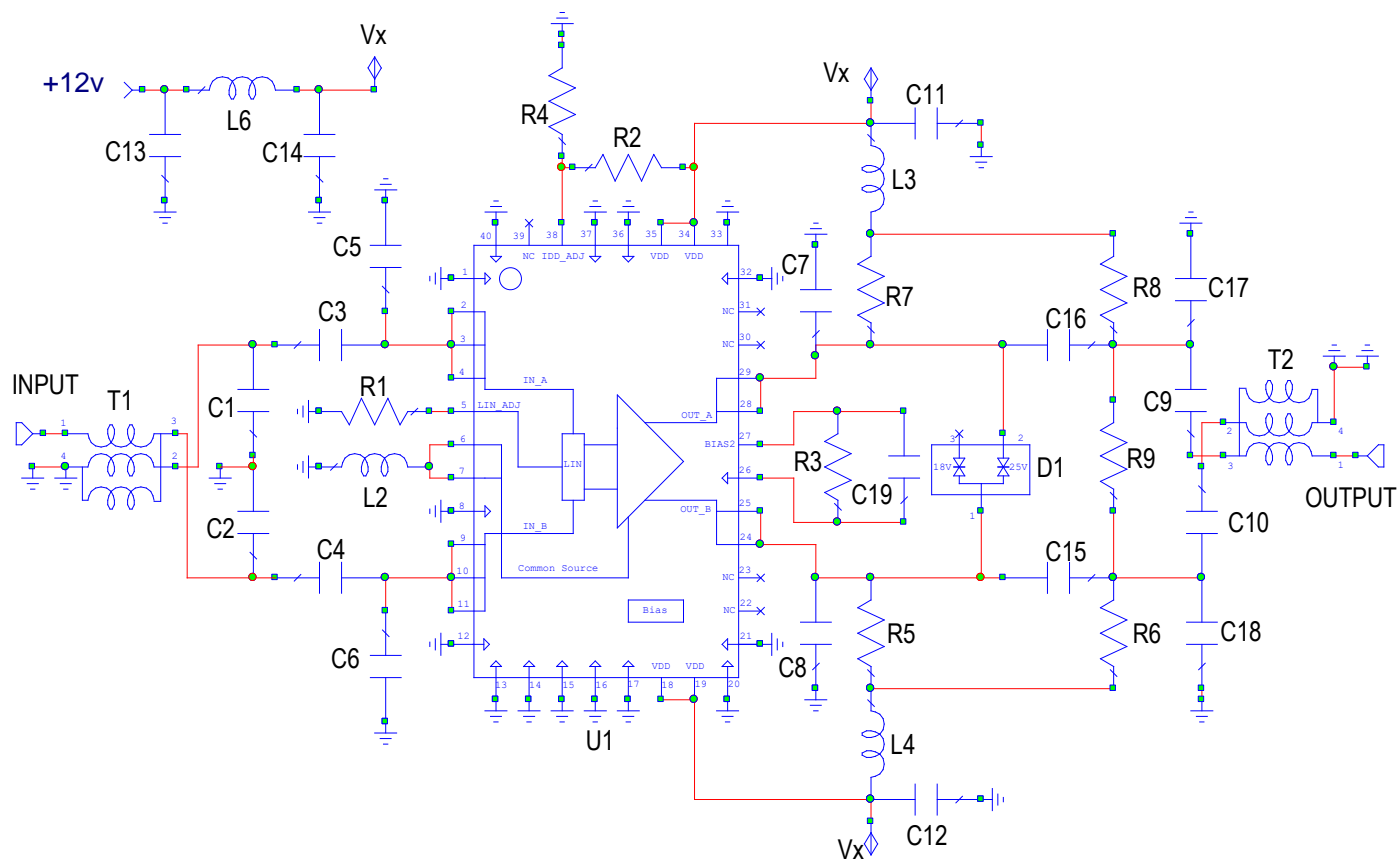


Aggregate CSO vs. Frequency



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TAT8804 D1H – EBP Schematic (w VSWR & Overdrive Protection)



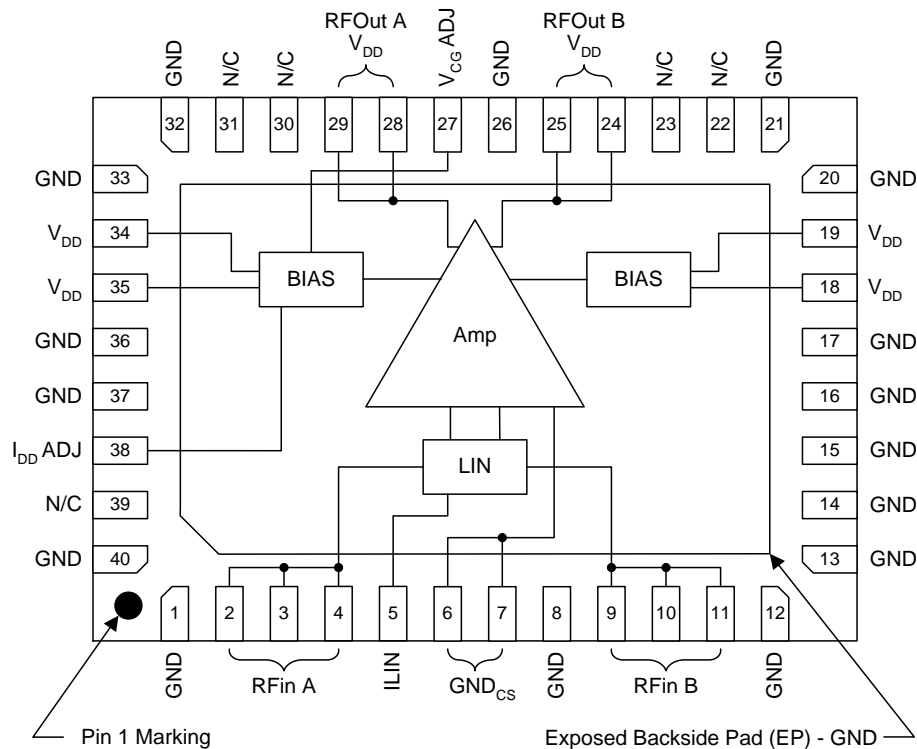
Bill of Material – TAT8804D1H – EBP (w VSWR & Overdrive Protection)

Reference Designator	Value	Description	Manufacturer	Part Number
PCB	Rev A	PCB TAT8804 – EVB Protected	Qorvo	1109707
U1	n/a	TAT8804D1H Sample	Qorvo	TAT8804D1H
D1	25V	ESD Clamp diode	Qorvo	TQP200002
T1,T2	1:1 BALUN, 75 Ω	MABA – 009210 – CT1760	MACOM	MABA-009210-CT1760
C3, C4	270 pF	CAP, 0603, 5%, 50 V, NPO	TDK	C1608C0G1H271J080AA
C9, C10	330 pF	CAP, 0603, 5%, 50 V, NPO	TDK	CGJ3E2C0G1H331J080AA
C11, C12	0.01 μ F	CAP, 0603, 10%, 50 V, X7R	TDK	C1608X7R1H103J
C13, C14	0.1 μ F	CAP, 0603, 10%, 50 V, X7R	TDK	C1608X7R1H104K
C15, C16	56 pF	CAP, 0603, 10%, 50 V, NPO	TDK	CGJ3E2C0G1H560J080AA
C19	4.7 μ F	CAP, 0603, 10%, 10 V, Y5V	Murata	GRM188F51A475ZE20D
R1	4.3K Ω	RES, 0603, 1%, 1 / 10W	Panasonic	ERJ3EKF4301V
R3	680 Ω	RES, 0603, 1%, 1 / 10W	Panasonic	ERJ3EKF6800V
R5, R7	2.2 ohm	RES, 0603, 1%, 1 / 16W	Panasonic	ERJ3GSYJ2R2H
R6, R8	5.1 ohm	RES, 0603, 1%, 1 / 10W	Panasonic	ERJ-3GSYJ5R1V
R9	475 Ω	RES, 0603, 1%, 1 / 10W	Panasonic	ERJ3EKF4750H
L2 ¹ , L3, L4	680 nH	IND, 0805, 5%, 355 MHz SRF, 660mA	Coilcraft	0805AF-681XJR
L6	900 nH	IND, 1008, 10%, 1008AF-901X	Coilcraft	1008AF-901X
R2, R4, C1, C2, C5, C6, C7, C8 ² , C17-C18, L1, L5	n/a	Do Not Populate	N/A	N/A
J1, J2	75 Ω	N-TYPE MALE, PANEL MOUNT	Pasternack	PE4504
J3	2 pin 0.1" RA	Molex SMT connector	Molex	022-28-8021
PH 4-40	4-40, 0.25",	Pan Head Screw w/ lock washer	various	
SH 4-40	4-40, 0.25",	Socket Head Screw	various	
	Cut to 0.25" x 0.4"	Indium foil 1" x 1" x 0.004"	Indium Corp	IND4HSD004
Heatsink	Aluminum	Heatsink for 62 mil board	Qorvo	1094050

Notes:

1. Output source degeneration inductor must be rated for 650 mA min for I_{DD} flowing through RF output devices
2. CSO may be improved by correcting Balun phase asymmetry by adding a 0.3 pF to C8.

Pin Configuration and Description



Pin Number	Label	Description
2-4	RFIn A	RF in A, requires external Balun. External DC Block required.
9-11	RFIn B	RF in B, requires external Balun. External DC Block required.
5	ILIN	Current adjust pin to optimize Linearity
28-29	RFout A/V _{DD}	RF Out A and supply voltage, external DC block & Balun required.
24-25	RFout B/V _{DD}	RF Out B and supply voltage, external DC block & Balun required.
18-19, 34-35	V _{DD}	Bias controller supply voltage
27	V _{CG} ADJ	Common Gate adjustment to optimize common gate amplifier bias voltage (normally open)
38	I _{DD} ADJ	I _{DD} current control (normally open), pulling to gnd lowers I _{DD} current
1,8,12-17, 20-21, 26, 32-33, 36-37, 39-40	GND	RF / DC Ground Connection
6-7	GND _{CS}	Common Source ground degeneration, grounded with inductor. Full DC current flows through this pin, inductor must handle total I _{DD} current.
Backside Paddle	GND	RF/DC ground. Use recommended via pattern to minimize inductance and thermal resistance. See PCB Mounting Pattern for suggested footprint.
22-23, 30-31, 39	N/C	No connection

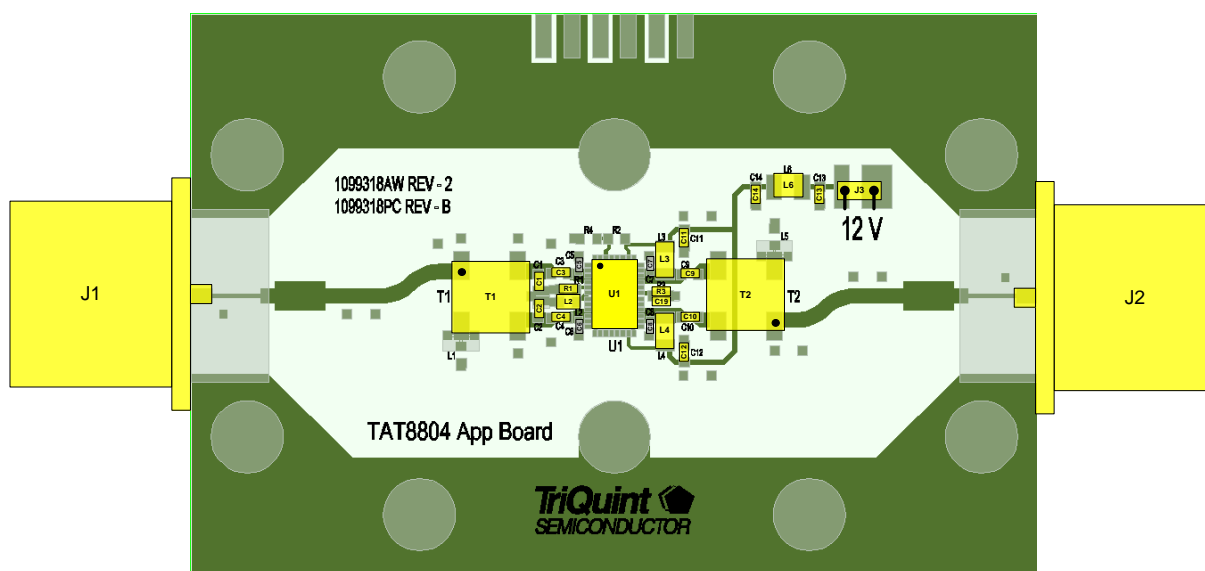
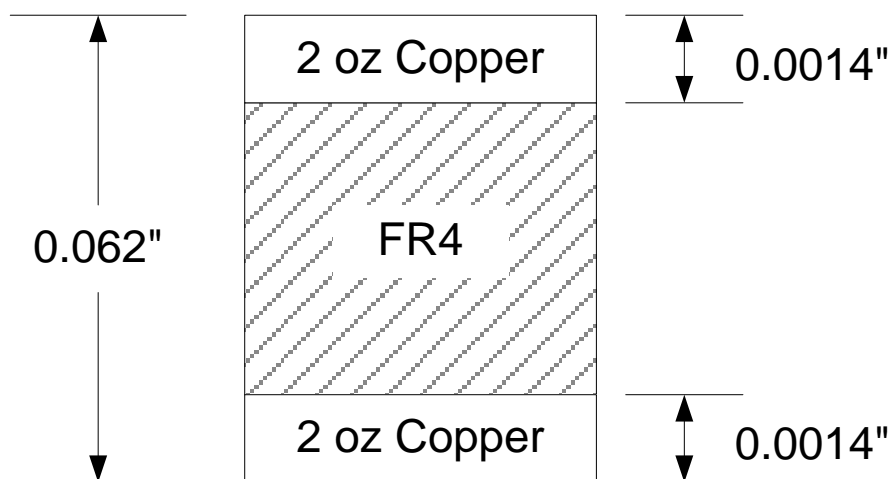
Evaluation Board PCB Information

EB and EBP PCB Material and Stack-up:

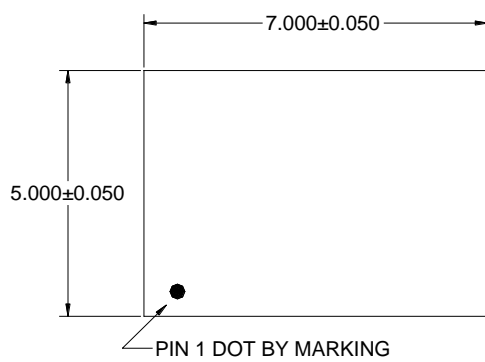
Board Material: 0.062" FR4, $\epsilon_r = 4.25$

Plating: 2 oz copper

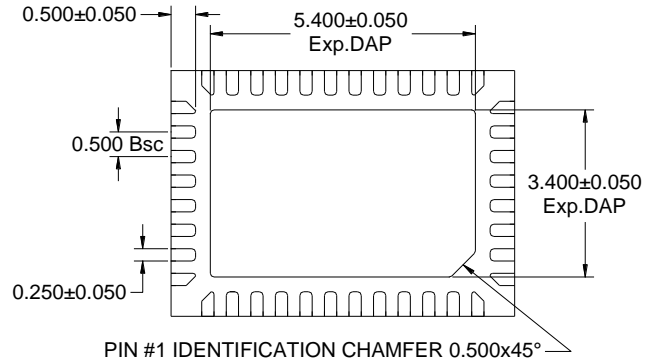
Board Dimensions: 3" x 2"



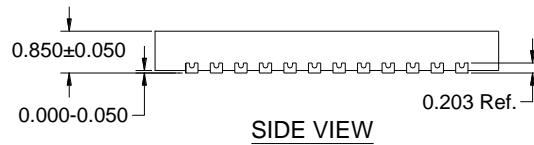
Package Dimensions



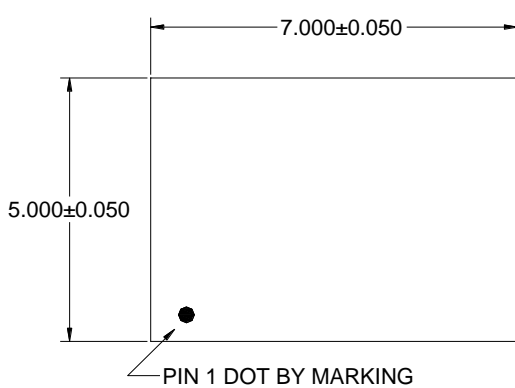
TOP VIEW



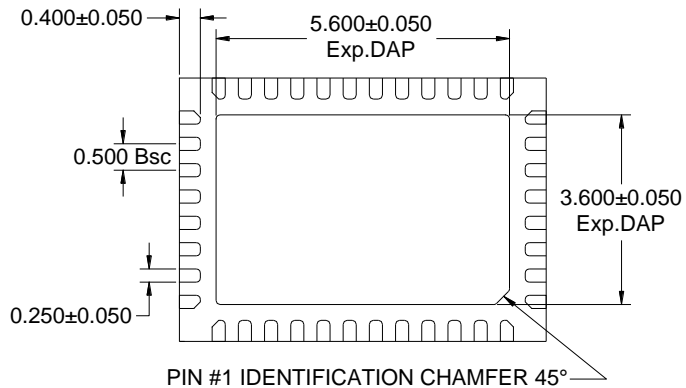
BOTTOM VIEW



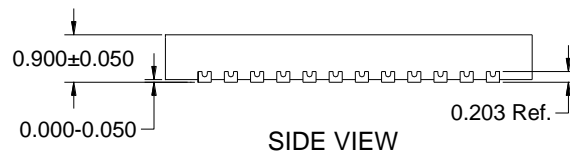
SIDE VIEW



TOP VIEW

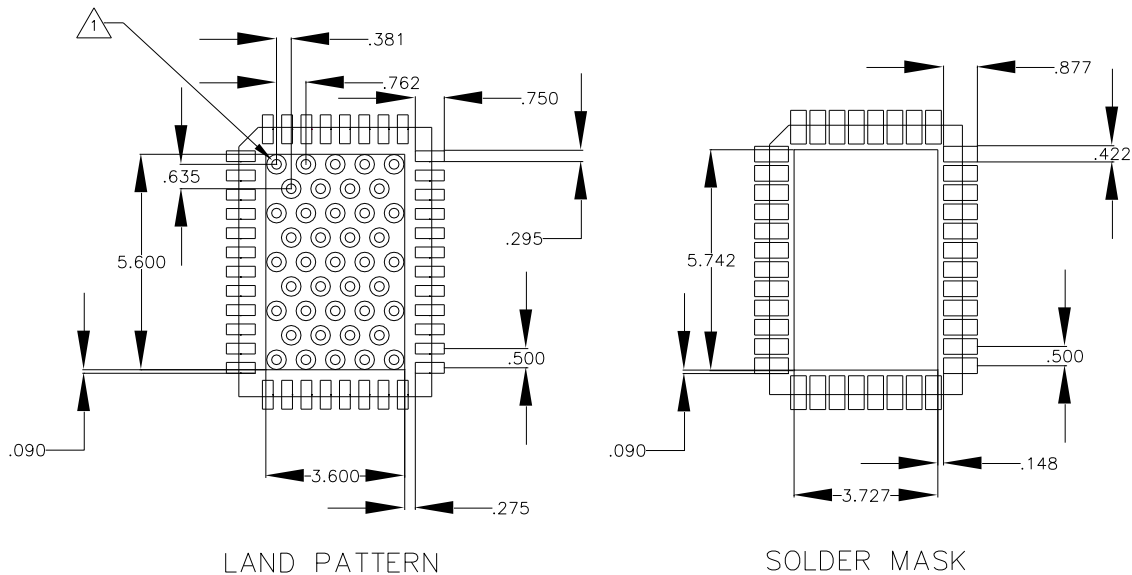


BOTTOM VIEW



SIDE VIEW

PCB Mounting Pattern



Notes:

1. All dimensions are in millimeters. Angles are in degrees.
2. Use 2 oz. copper minimum for top and bottom layer metal.
3. Vias are required under the backside paddle of this device for proper RF / DC grounding and thermal dissipation. We recommend a 0.35 mm (#80 / .0135") diameter bit for drilling via holes and a final plated thru diameter of 0.25 mm (0.10").
4. Ensure good package backside paddle solder attach for reliable operation and best electrical performance.
5. Place mounting screws near the part to fasten a backside heat sink.
6. Do not apply solder mask to the back side of the PC board in the heat sink contact region.
7. Ensure that the backside via region makes good physical contact with the heat sink.

Handling Precautions

Parameter	Rating	Standard
ESD – Human Body Model (HBM)	Class 1A	ESDA / JEDEC JS-001-2012
ESD – Charged Device Model (CDM)	Class C3	JEDEC JESD22-C101F
MSL – Moisture Sensitivity Level	Level 3	IPC/JEDEC J-STD-020



Caution!
ESD-Sensitive Device

Solderability

Compatible with both lead-free (260°C max. reflow temp.) and tin/lead (245°C max. reflow temp.) soldering processes. Solder profiles available upon request.

Contact plating: NiPdAu

RoHS Compliance

This part is compliant with 2011/65/EU RoHS directive (Restrictions on the Use of Certain Hazardous Substances in Electrical and Electronic Equipment) as amended by Directive.

This product also has the following attributes:

- Lead Free
- Halogen Free (Chlorine, Bromine)
- Antimony Free
- TBBP-A (C₁₅H₁₂Br₄O₂) Free
- PFOS Free
- SVHC Free



Contact Information

For the latest specifications, additional product information, worldwide sales and distribution locations:

Web: www.qorvo.com

Tel: 1-844-890-8163

Email: customer.support@qorvo.com

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