



TGA2752-SM

7.1 – 8.5 GHz Power Amplifier

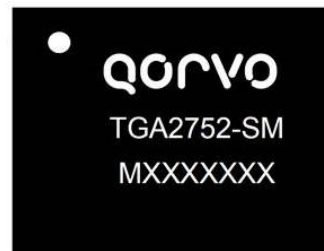
Product Overview

The Qorvo TGA2752-SM is a C-Band Power Amplifier with integrated power detector. The TGA2752-SM operates from 7.1 – 8.5 GHz and is designed using Qorvo's power GaAs pHEMT and GaN HEMT production processes.

The TGA2752-SM typically provides 40 dBm of saturated output power with small signal gain of 28 dB. Third Order Intercept is 48 dBm at 30 dBm SCL.

The TGA2752-SM is available in a low-cost, surface mount 42 lead 7 x 9 mm QFN package and is ideally suited for Point-to-Point Radio.

Lead-free and RoHS compliant.

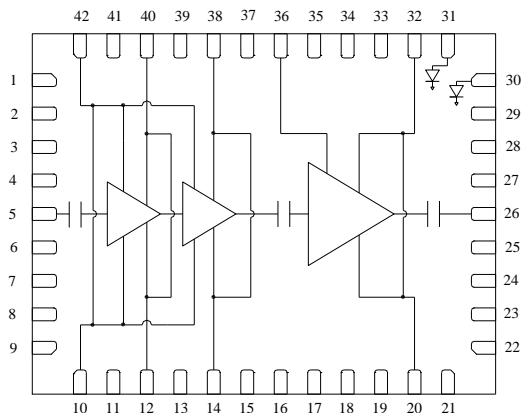


42-Lead 7.0 x 9.0 x 0.9 mm Package

Key Features

- Frequency Range: 7.1 – 8.5 GHz
- Power: +40 dBm Psat
- Gain: 28 dB
- TOI: 48 dBm at 30 dBm/tone
- Integrated Power Detector
- Bias: $V_{D1} = V_{D2} = +6$ V, $I_{D1} + I_{D2} = 1000$ mA, $V_{D3} = +28$ V, $I_{D3} = 190$ mA
- Package Dimensions: 7.0 x 9.0 x 0.9 mm

Functional Block Diagram



Top View

Applications

- Point-to-Point Radio
- Linear C-band Sat-Com

Ordering Information

| Part No. | Description |
|-----------------------|------------------------------------|
| TGA2752-SM T/R | 500 pieces on a 7" reel (standard) |
| TGA2752-SM Eval Board | Evaluation Board |
| TGA2752-SM, Sample | Waffle Tray with 4 pcs |

Absolute Maximum Ratings

| Parameter | Rating |
|--|-----------------|
| Drain Voltage, V_{D1} , V_{D2} | +9 V |
| Drain Voltage, V_{D3} | +32 V |
| Drain Current, $I_{D1} + I_{D2}$ | 2443 mA |
| Drain Current, I_{D3} | 825 mA |
| Gate Voltage, V_{G12} | -1.2 V / +0.5 V |
| Gate Voltage, V_{G3} | -8 V / 0 V |
| Power Dissipation, Driver Stages, P_{DISS} | 7.2 W |
| Power Dissipation, Final Stage, P_{DISS} | 17 W |
| RF Input Power, CW, 50 Ω , T = 25 °C | +29 dBm |
| Mounting Temperature (30 Seconds) | 260 °C |
| Storage Temperature | -40 to 150 °C |

Exceeding any one or a combination of the Absolute Maximum Rating conditions may cause permanent damage to the device. Extended application of Absolute Maximum Rating conditions to the device may reduce device reliability.

Recommended Operating Conditions

| Parameter | Min | Typ | Max | Units |
|--|-----|-------|-----|-------|
| Operating Temp. Range | -40 | +25 | +85 | °C |
| V_{D1} , V_{D2} | | +6 | | V |
| V_{D3} | | +28 | | V |
| $I_{D1} + I_{D2}$ | | 1000 | | mA |
| I_{D3} | | 190 | | mA |
| V_{G12} | | -0.65 | | V |
| V_{G3} | | -2.6 | | V |
| $I_{D1} + I_{D2}$ drive (at +34 dBm Pout) | | 1050 | | mA |
| I_{D3} drive (at +34 dBm Pout) | | 400 | | mA |

Electrical specifications are measured at specified test conditions. Specifications are not guaranteed over all recommended operating conditions.

Electrical Specifications

| Parameter | Conditions ⁽¹⁾ | Min | Typ | Max | Units |
|---|--------------------------------------|------|--------|-----|----------|
| RF Frequency Range | | 7.1 | | 8.5 | GHz |
| Small Signal Gain | | 24 | 28 | | dB |
| Input Return Loss, IRL | | | 12 | | dB |
| Output Return Loss, ORL | | | 15 | | dB |
| Output Power at Saturation, Psat | | +38 | +40 | | dBm |
| Output Power at 1 dB Gain Compression, P1dB | | | +30 | | dBm |
| Output Third Order Intercept, TOI @ 30 dBm/Tone | | | +48 | | dBm |
| GaN Gate Leakage | $V_{D3} = 10$ V $V_{G3} = -3.7$ V | -4.2 | | | mA |
| Gain Temperature Coefficient | | | -0.035 | | dB / °C |
| Power Temperature Coefficient | | | -0.012 | | dBm / °C |

Notes:

- Test conditions unless otherwise noted: $V_{D1} = V_{D2} = +6$ V, $I_{D1} + I_{D2} = 1000$ mA, $V_{G1} = V_{G2} = -0.7$ V, $V_{D3} = +28$ V, $I_{D3} = 190$ mA, $V_{G3} = -2.6$ V, Temp = +25 °C, $Z_0 = 50$ Ω

Thermal and Reliability Information (GaAs Driver Stages)

| Parameter | Test Conditions | Value | Units |
|---|--|-------|-------|
| Thermal Resistance (θ_{JC}) ⁽¹⁾ | CW | 6.17 | °C/W |
| Channel Temperature, T_{CH} | $T_{baseplate} = +85\text{ °C}$, $V_{D\ Driver} = +6\text{ V}$, $I_{DQ} = 1000\text{ mA}$, $P_{DISS} = 6.0\text{ W}$ | 139 | °C |
| Thermal Resistance (θ_{JC}) ⁽¹⁾ | CW | 6.19 | °C/W |
| Channel Temperature, T_{CH} (Under RF) | $T_{baseplate} = +85\text{ °C}$, $V_{D\ Driver} = +6\text{ V}$, $I_{D\ Driver} = 1050\text{ mA}$, $P_{OUT} = +34\text{ dBm}$, $P_{DISS} = 6.3\text{ W}$ | 142 | °C |

Notes:

1. Thermal resistance measured at back of package.



Thermal and Reliability Information (GaN Final Stage)

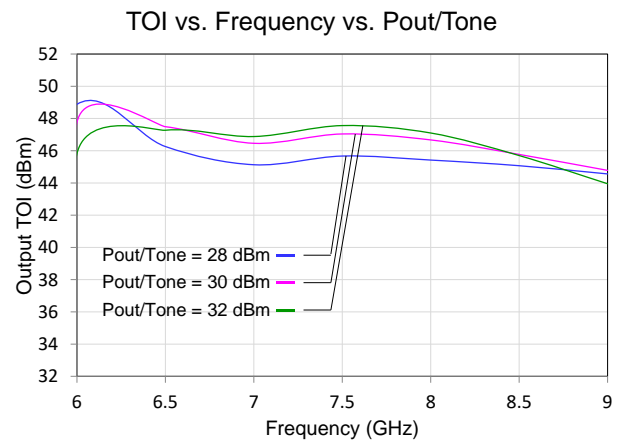
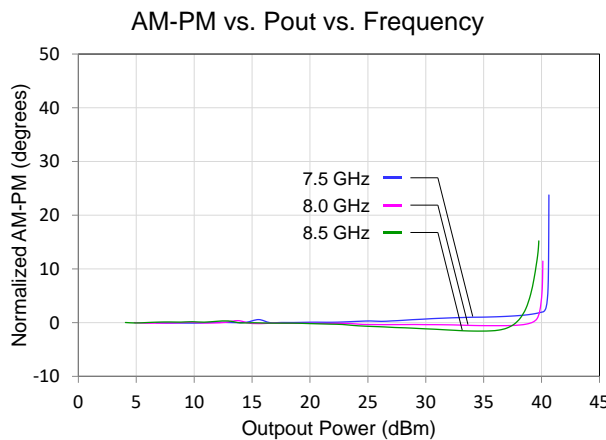
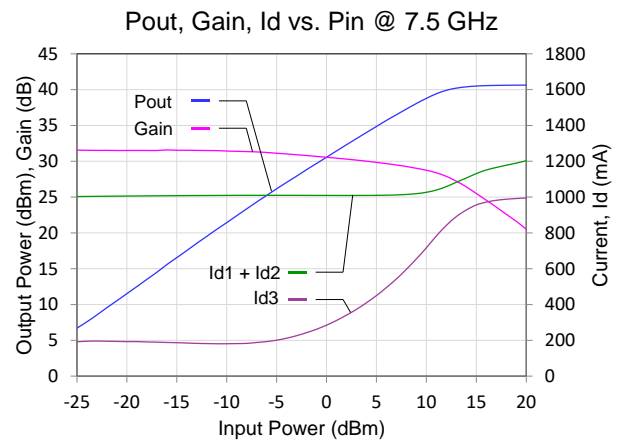
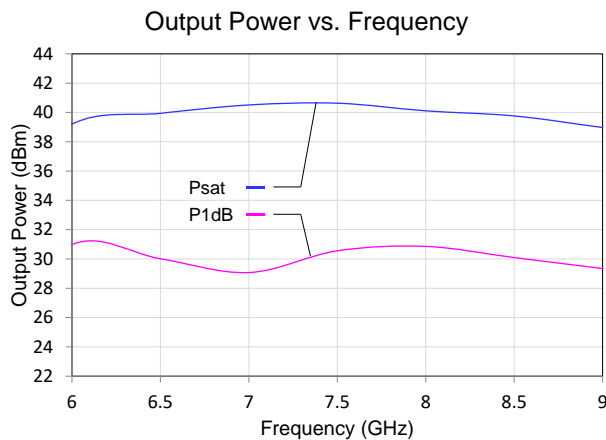
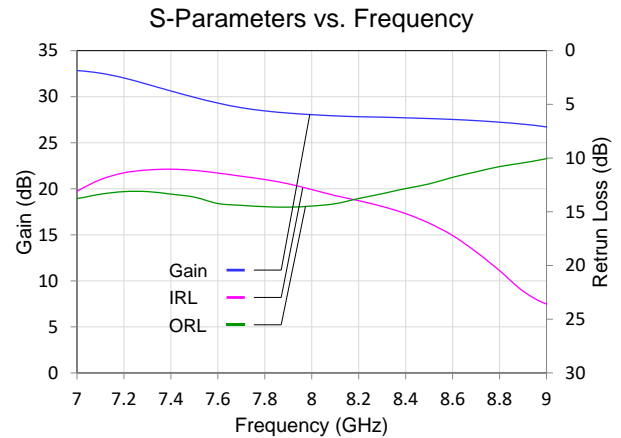
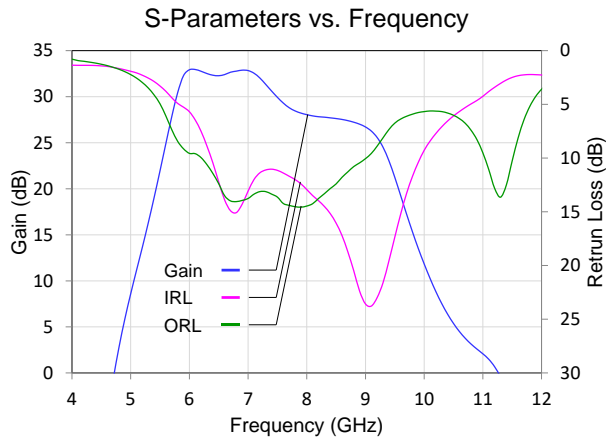
| Parameter | Test Conditions | Value | Units |
|---|---|-------|-------|
| Thermal Resistance (θ_{JC}) ⁽¹⁾ | CW | 5.66 | °C/W |
| Channel Temperature, T_{CH} ⁽²⁾ | $T_{baseplate} = +85\text{ °C}$, $V_{D\ Driver} = +28\text{ V}$, $I_{DQ} = 190\text{ mA}$, $P_{DISS} = 5.3\text{ W}$ | 115 | °C |
| Thermal Resistance (θ_{JC}) ⁽¹⁾ | CW | 5.52 | °C/W |
| Channel Temperature, T_{CH} (Under RF) ⁽²⁾ | $T_{baseplate} = +85\text{ °C}$, $V_{D\ Driver} = +28\text{ V}$, $I_{D\ Final} = 400\text{ mA}$, $P_{OUT} = +34\text{ dBm}$, $P_{DISS} = 8.7\text{ W}$ | 133 | °C |

Notes:

1. Thermal resistance measured at back of package.
2. IR scan equivalent. Refer to the following document: [GaN Device Channel Temperature, Thermal Resistance, and Reliability Estimates](#)

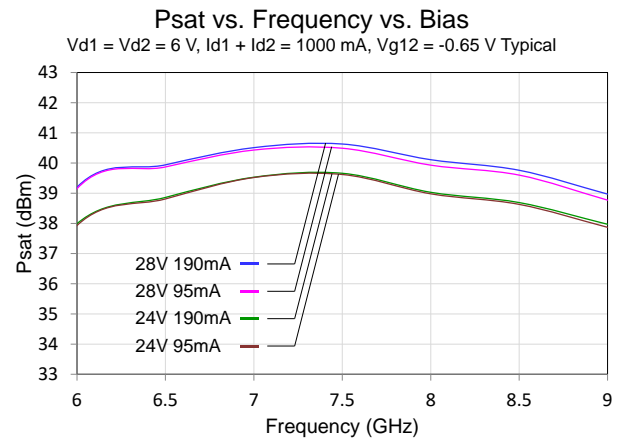
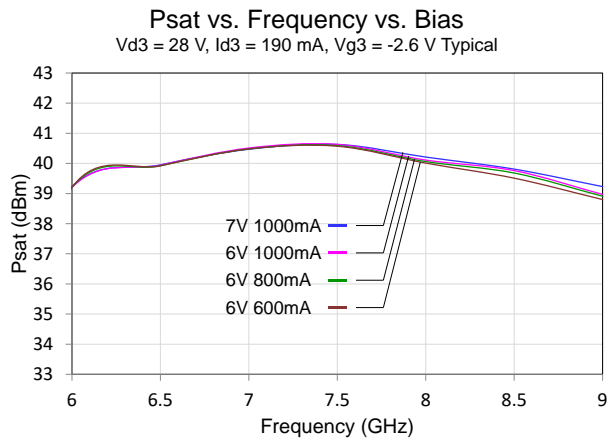
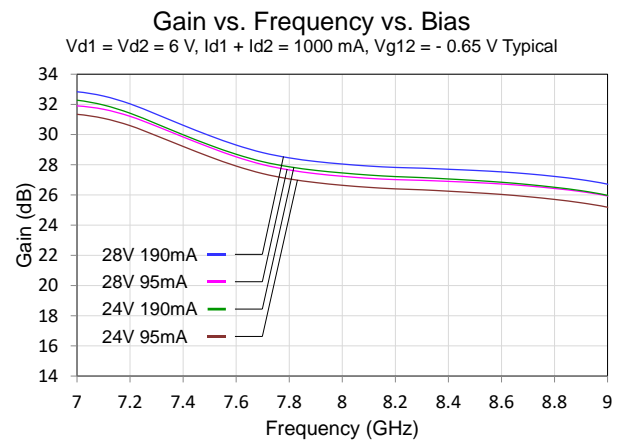
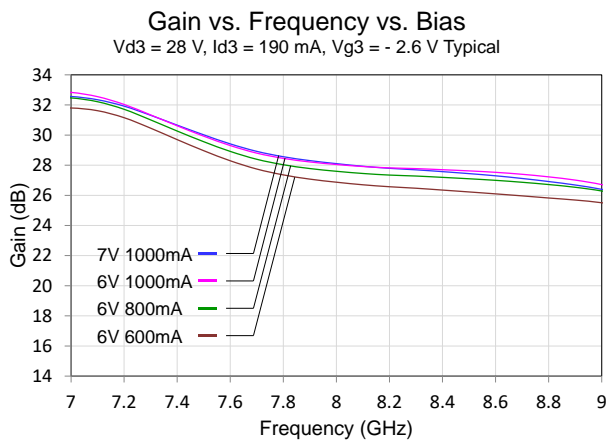
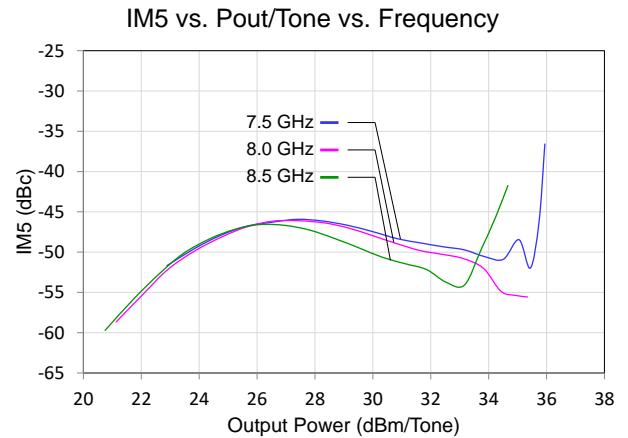
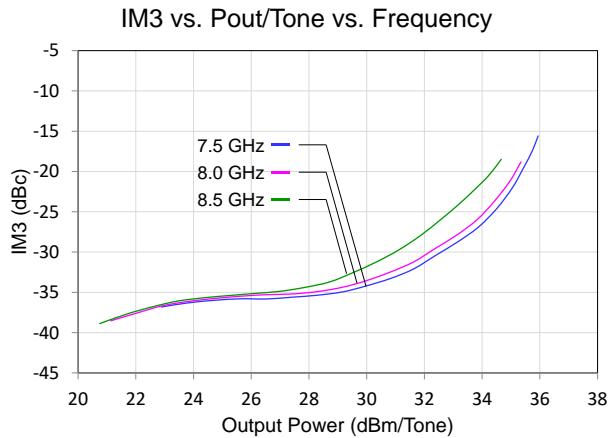
Performance Plots

Test conditions unless otherwise noted: $V_{D1} = V_{D2} = +6\text{ V}$, $I_{D1} + I_{D2} = 1000\text{ mA}$, $V_{G1} = V_{G2} = -0.65\text{ V}$, $V_{D3} = +28\text{ V}$, $I_{D3} = 190\text{ mA}$, $V_{G3} = -2.6\text{ V}$, Temp = $+25\text{ }^{\circ}\text{C}$, $Z_0 = 50\text{ }\Omega$



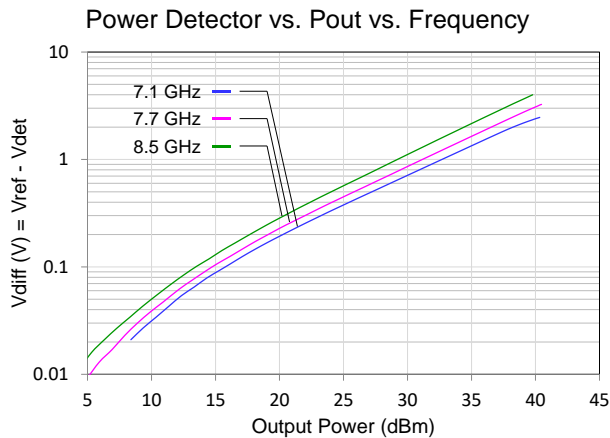
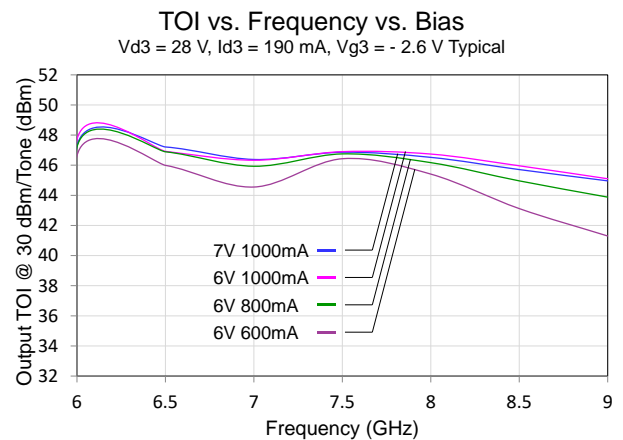
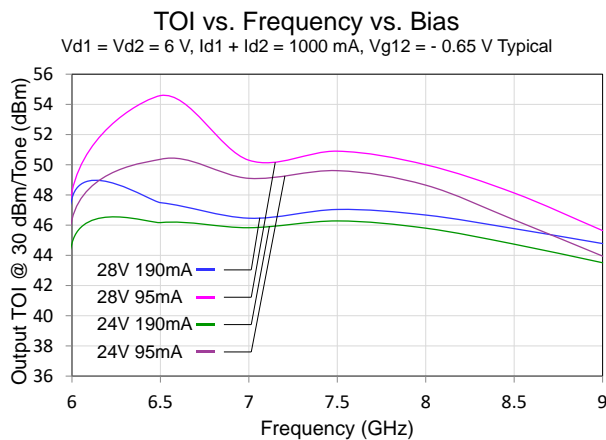
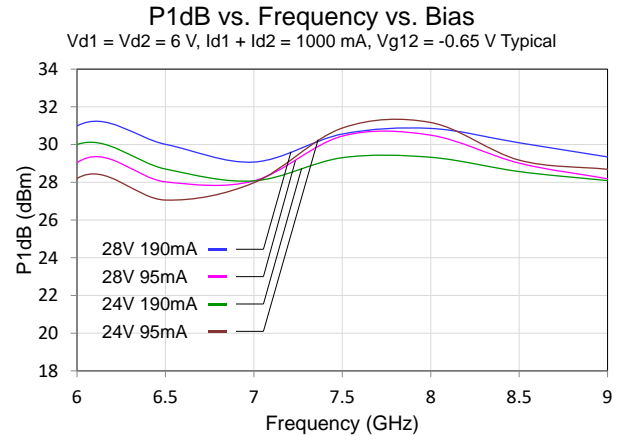
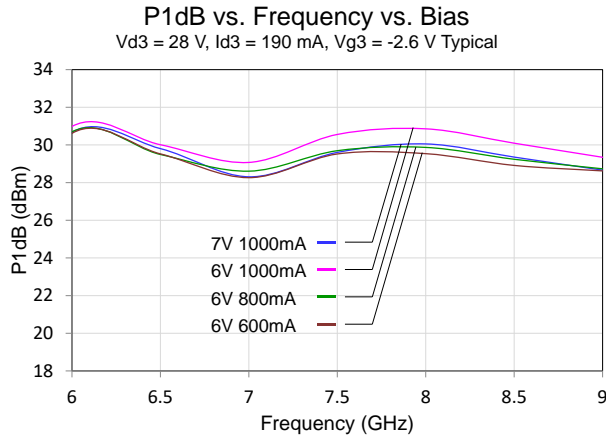
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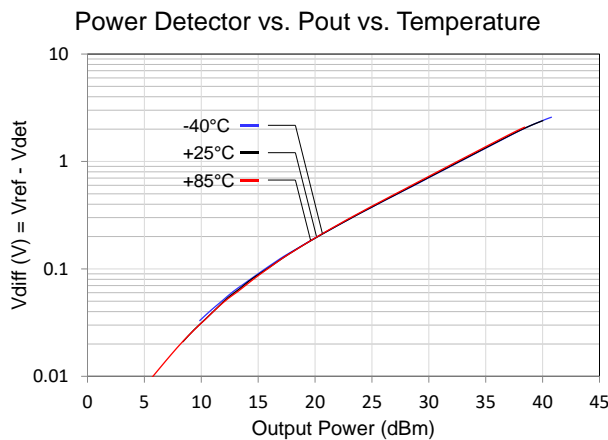
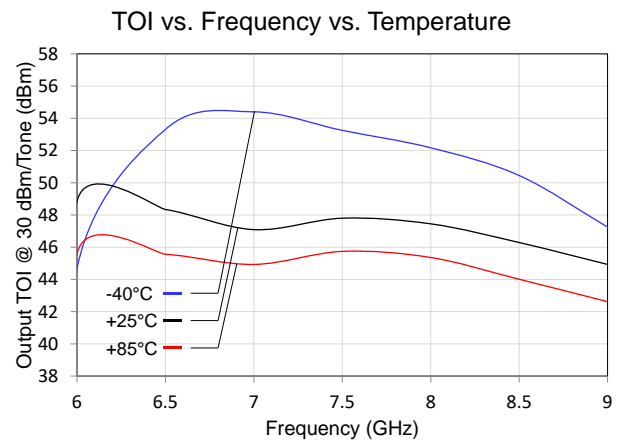
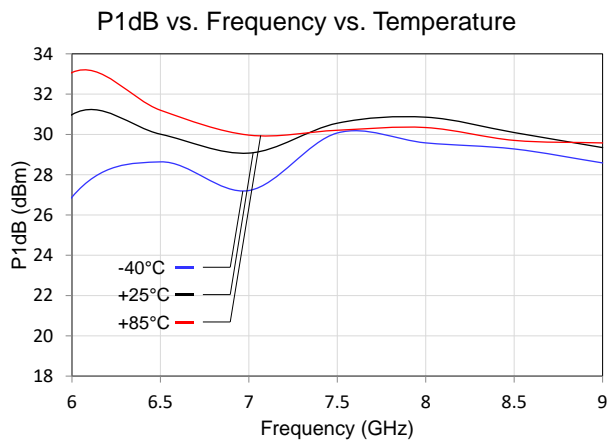
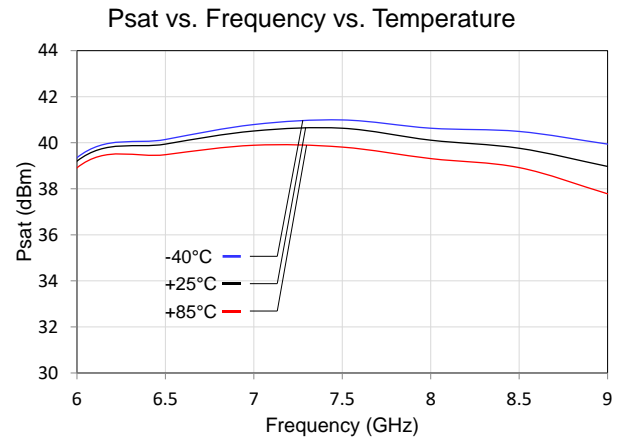
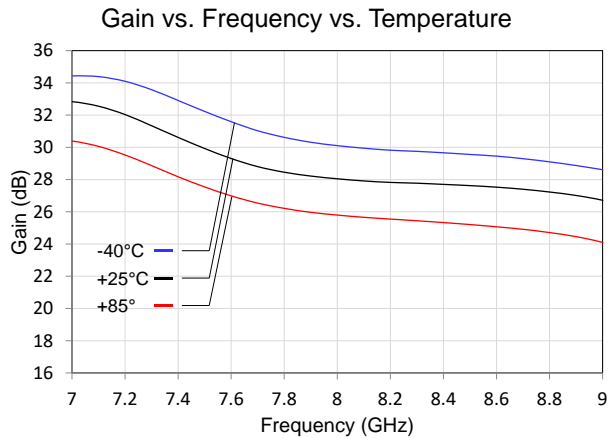
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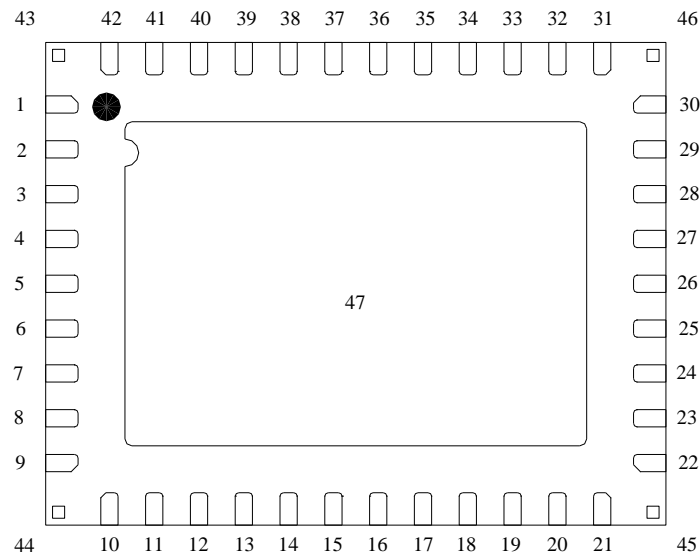


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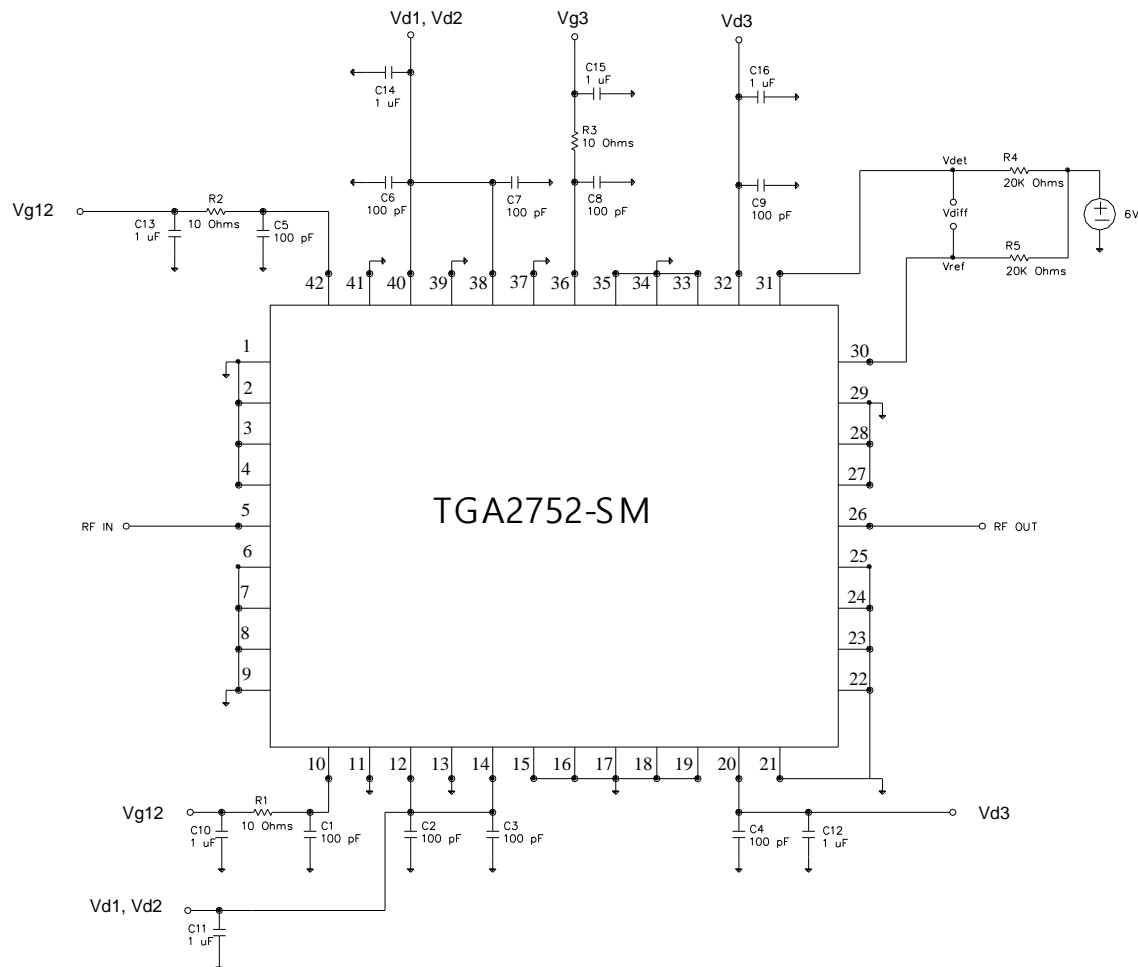
Pin Configuration and Description



Top View

| Pad No. | Label | Description |
|--|------------------|---|
| 1, 2, 3, 4, 6, 7, 8, 9, 11, 13, 15, 16, 17, 18, 19, 21, 22, 23, 24, 25, 27, 28, 29, 33, 34, 35, 37, 39, 41 | NC | No internal connection; can be grounded on PCB. |
| 5 | RF IN | RF Input, matched to 50 Ω , AC Coupled. |
| 10, 42 | V _{G12} | Gate voltage. Bias network is required; can be biased from either pin, and non-biased pin can be left open; see Application Circuit on page 11 as an example. |
| 12, 40 | V _{D1} | Drain voltage; must be biased from both sides. Bias network is required; see Application Circuit on page 11 as an example. |
| 14, 38 | V _{D2} | Drain voltage; must be biased from both sides. Bias network is required; see Application Circuit on page 11 as an example. |
| 20, 32 | V _{D3} | Drain voltage; must be biased from both sides. Bias network is required; see Application Circuit on page 11 as an example. |
| 26 | RF OUT | RF Output, matched to 50 ohms, AC Coupled. |
| 30 | V _{REF} | Reference diode output voltage. |
| 31 | V _{DET} | Detector diode output voltage. Varies with RF output power. |
| 36 | V _{G3} | Gate voltage. Bias network is required; see Application Circuit on page 11 as an example. |
| 43, 44, 45, 46, 47 | GND | Backside Paddle. Multiple vias should be employed to minimize inductance and thermal resistance; see Mounting Configuration on page 14 for suggested footprint. |

Application Circuit



V_{G12} can be biased from either side, and the non-biased side can be left open.
 V_{D1} , V_{D2} , V_{D3} , must be biased from both sides.

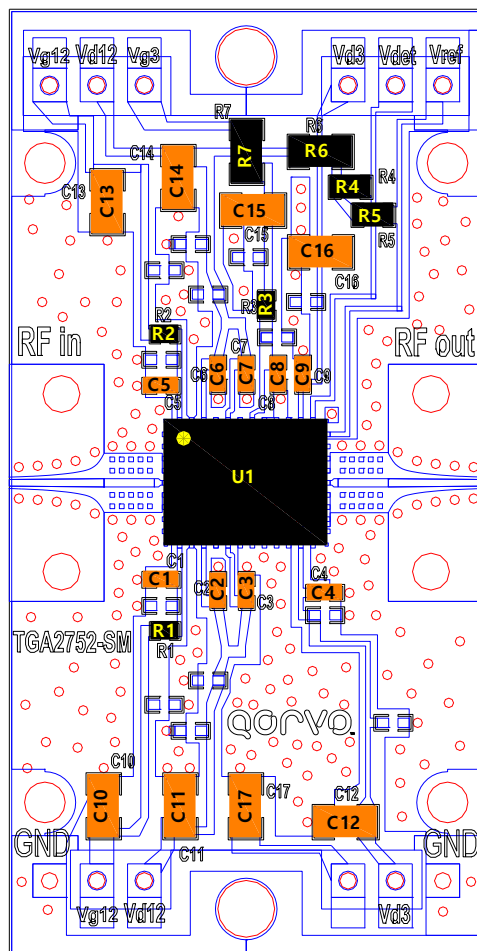
Bias-up Procedure

- V_{G12} set to -1.2 V
- V_{G3} set to -3.5 V
- V_{D1} , V_{D2} set to $+6$ V
- V_{D3} sets to $+28$ V
- Adjust V_{G12} more positive until quiescent I_D is 1000 mA
- Adjust V_{G3} more positive until quiescent I_D is 190 mA
- Apply RF signal

Bias-down Procedure

- Turn off RF signal
- Reduce V_{G12} to -1.2 V. Ensure $I_D \sim 0$ mA
- Reduce V_{G3} to -3.5 V. Ensure $I_D \sim 0$ mA
- Turn V_{D1} , V_{D2} , V_{D3} to 0 V
- Turn V_{G12} , V_{G3} to 0 V

Application Evaluation Board

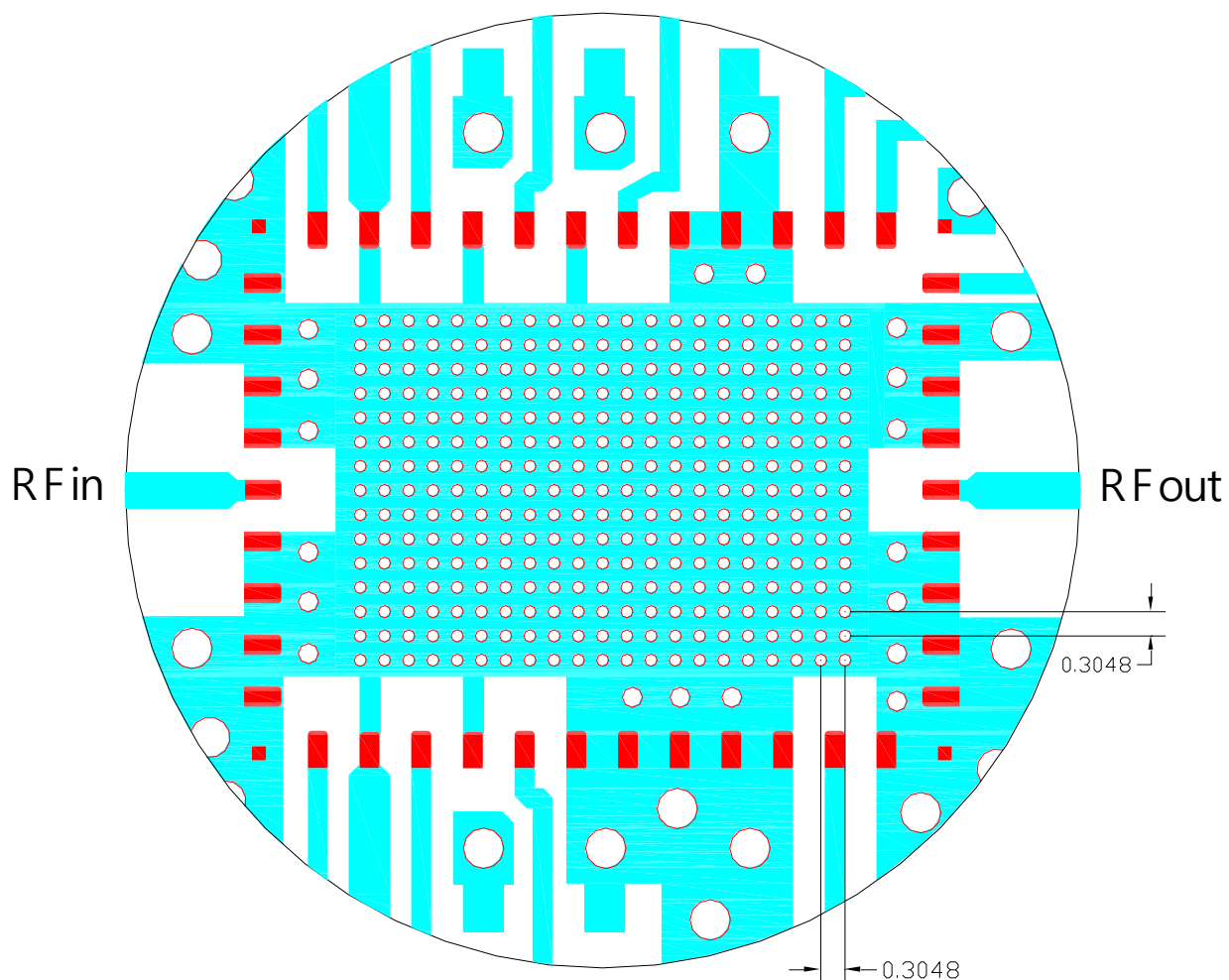


1. Board Material is RO4003 0.008" thickness with ½ oz. copper cladding

Bill of Material

| Reference Des. | Value | Description | Manuf. | Part Number |
|----------------|--------|-------------------------------|---------|-------------|
| n/a | n/a | Printed Circuit Board | Qorvo | |
| C1 – C9 | 100 pF | Cap, 0402, +50 V, 5%, COG | various | |
| C10 – C17 | 1 µF | Cap, 0603, +50 V, 5%, X5R | various | |
| R1 – R3 | 10 Ω | Res, 0402, 1/16W, 5%, SMD | various | |
| R4, R5 | 20 KΩ | Res, 0603, 1/16W, 5%, SMD | various | |
| R6, R7 | 0 Ω | Res, 0805, 1/16W, 5%, SMD | various | |
| U1 | | 7.1 – 8.5 GHz Power Amplifier | Qorvo | TGA2752-SM |

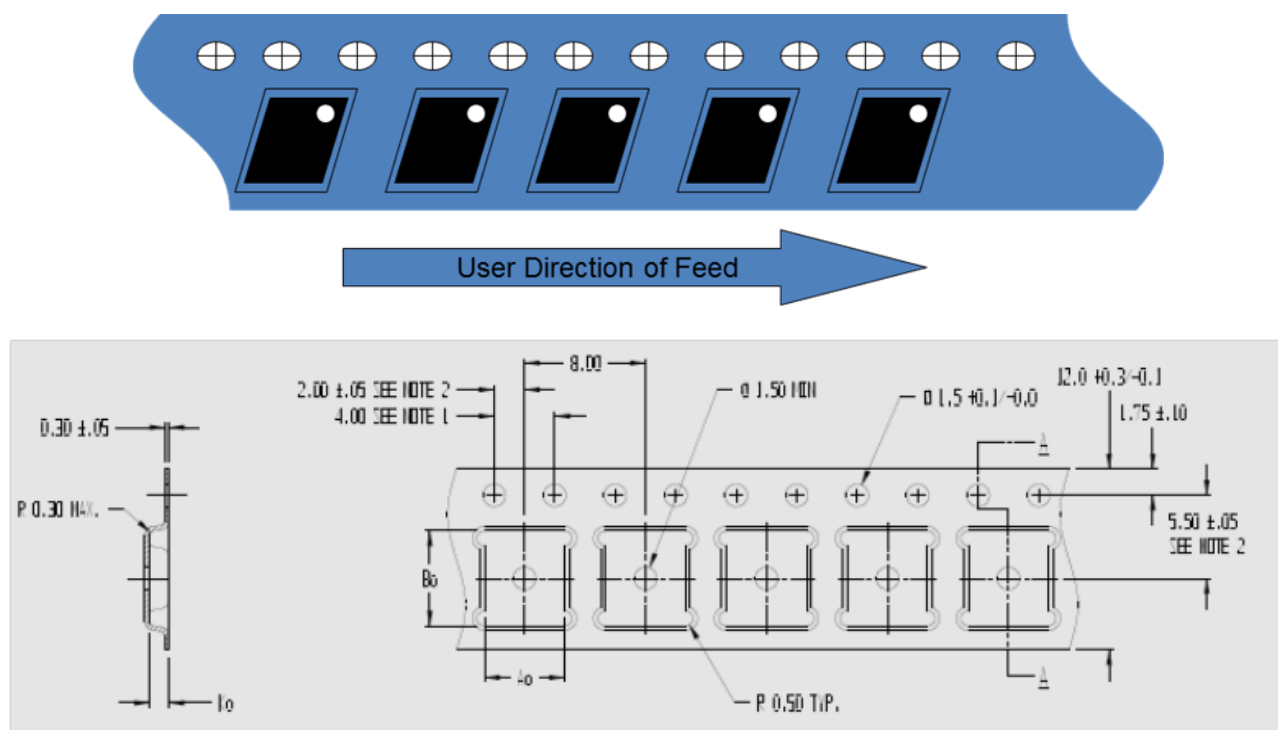
PCB Mounting Pattern



Notes:

1. The pad pattern shown has been developed and tested for optimized assembly at Qorvo. The PCB land pattern has been developed to accommodate lead and package tolerances. Since surface mount processes vary from company to company, careful process development is recommended.
2. Ground vias are critical for the proper performance of this device. Vias should have a final plated thru diameter of .1524 mm (.006").
3. For best thermal performance, vias under the ground paddle should be copper filled.

Tape and Reel Information



| Feature | Measure | Symbol | Size (in) | Size (mm) |
|---------------------|--|--------|-----------|-----------|
| Cavity | Length | A0 | 0.366 | 9.3 |
| | Width | B0 | 0.287 | 7.3 |
| | Depth | K0 | 0.047 | 1.2 |
| | Pitch | P1 | 0.472 | 12.0 |
| Centerline Distance | Cavity to Perforation - Length Direction | P2 | 0.079 | 2.0 |
| | Cavity to Perforation - Width Direction | F | 0.217 | 5.50 |
| Cover Tape | Width | C | 0.362 | 9.20 |
| Carrier Tape | Width | W | 0.630 | 16.0 |

Notes:

1. Empty part cavities at the trailing and leading ends are sealed with cover tape. See EIA 481-1-A.
2. Labels are placed on the flange opposite the sprockets in the carrier tape.

Handling Precautions

| Parameter | Rating | Standard |
|----------------------------------|----------|---------------------|
| ESD – Human Body Model (HBM) | Class 1A | ESDA / JEDEC JS-001 |
| ESD – Charged Device Model (CDM) | Class C1 | JEDEC JESD22-C10 |
| MSL – Moisture Sensitivity Level | Level 3 | IPC/JEDEC J-STD-020 |



Caution!
ESD-Sensitive Device

Solderability

Compatible with both lead-free (260°C max. reflow temp.) and tin/lead (245°C max. reflow temp.) soldering processes.

RoHS Compliance

This part is compliant with 2011/65/EU RoHS directive (Restrictions on the Use of Certain Hazardous Substances in Electrical and Electronic Equipment) as amended by Directive 2015/863/EU.

This product also has the following attributes:

- Lead Free
- Halogen Free (Chlorine, Bromine)
- Antimony Free
- TBBP-A (C₁₅H₁₂Br₄O₂) Free
- PFOS Free
- SVHC Free

Contact Information

For the latest specifications, additional product information, worldwide sales and distribution locations:

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Email: customer.support@qorvo.com

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