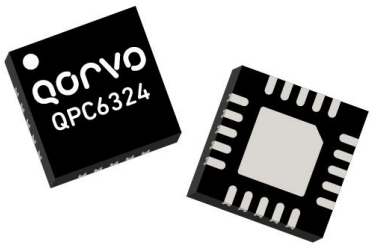
QPC6324

Absorptive, High Isolation SPDT Switch

Product Overview

The QPC6324 is a Silicon on Insulator (SOI) single-pole, double-throw (SPDT) switch, designed for use in 4G/5G wireless infrastructure applications and other high-performance communications systems. It offers high isolation with excellent linearity and power handling capability. No blocking capacitors are necessary on the RF ports. The design is non-reflective such that the RFX ports are terminated into 50 Ω in the off state. The QPC6324 is +1.8V logic compatible.

The QPC6324 is packaged in a RoHS-compliant, compact QFN 4x4 mm surface-mount leadless package.

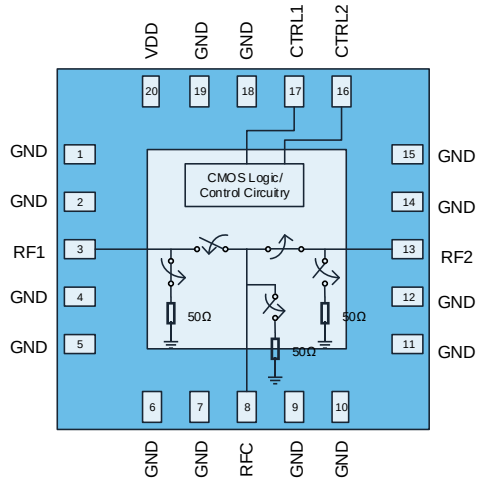


QFN 20 Pin 4 mm x 4 mm leadless SMT Package

Key Features

- 5 MHz to 6000 MHz Operation
- Non-Reflective (RFX ports)
- Terminated All-Off State mode
- No Blocking Caps needed unless voltage is on RF Line
- High Isolation: RFC-RFX: 63 dB at 2 GHz
  RFX-RFX: 63 dB at 2 GHz
- +1.8 V Logic Compatible

Functional Block Diagram



Top View

Applications

- Wireless Infrastructure
- Macro or picocell base stations
- TDD-based architectures

Ordering Information

Part No.	Description
QPC6324TR13	2500 pcs on a 13” reel
QPC6324EVB-01	Evaluation board

Absolute Maximum Ratings

Parameter		Rating
Storage Temperature		-50 to 150 °C
VDD		+6 V
$V_{CTRL1/2}$	High	+6 V
	Low	−0.2 V
Pin max (RFC-RFX), CW, 50 Ω		37 dBm
Pin max (RFX-TERM), CW, 50 Ω		31 dBm

Operation of this device outside the parameter ranges given above may cause permanent damage.

Recommended Operating Conditions

Parameter	Min	Typ	Max	Units
V_{DD}	+2.7	+5	+5.5	V
T_{CASE}	−40		+110	°C
Tj at MTTF>10^6 hrs			125	°C

Electrical specifications are measured at specified test conditions. Specifications are not guaranteed over all recommended operating conditions.

Electrical Specifications

Test conditions, unless otherwise noted: Temp = 25°C, VDD = +5V.

Parameter	Conditions	Min	Typ	Max	Units
Operational Frequency Range		5		6000	MHz
Insertion Loss (1)	100 – 2000 MHz		0.9	1.15	dB
	2000 – 4000 MHz		1.0	1.25	dB
	4000 – 5000 MHz		1.05	1.3	dB
	5000 - 6000 MHz		1.1	1.35	dB
Insertion Loss Ripple	In any 400 MHz band		0.03		dB
Isolation, RFC-RFX (1)	100 - 2000 MHz	55	61.5		dB
	2000 – 4000 MHz	50	57		dB
	4000 – 5000 MHz	48	54		dB
	5000 - 6000 MHz	44	50		dB
Isolation, RFX-RFX (1)	100 - 2000 MHz	57	63		dB
	2000 – 4000 MHz	50	57		dB
	4000 – 5000 MHz	48	54		dB
	5000 - 6000 MHz	44	50		dB
Return Loss, RFC (2)	100 - 4000 MHz	14	17		dB
	4000 – 5000 MHz	13	16		dB
	5000 - 6000 MHz	14	17		dB
Return Loss, RFX (2)	100 - 4000 MHz	13	16		dB
	4000 – 5000 MHz	12	15		dB
	5000 - 6000 MHz	15	18		dB
Return Loss	RFC Terminated, 2000 MHz		22		dB
	RFC Terminated, 6000 MHz		15		dB
Return Loss	RFX Terminated, 2000 MHz		20		dB
	RFX Terminated, 6000 MHz		13		dB

Note:
1. Production screen of product is done only at 2GHz and 6GHz.
2. Guaranteed by design only. Not tested in production.

Electrical Specifications Contd.

Test conditions, unless otherwise noted: Temp = 25°C, VDD = +5V.

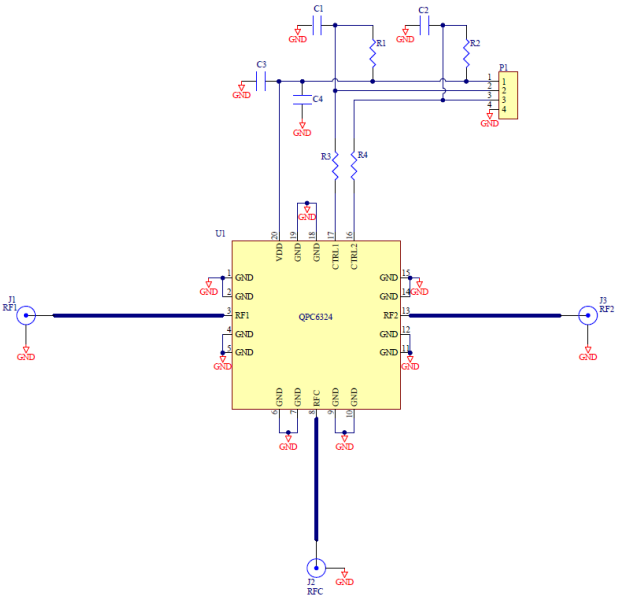
Parameter	Conditions	Min	Typ	Max	Units
Input P1dB	RFC-RFX, 2600 MHz	34	37		dBm
Input IP3	RFC-RFX, 2600 MHz, 13dBm/tone, 1MHz Δf	55	60		dBm
Switching Time	Turn-on, (50% Ctrl to 90% RF)		180		ns
	Turn-off, (50% Ctrl to 10% RF)		150		ns
	Turn-on, (50% Ctrl to 99% RF)		417		ns
	Turn-off, (50% Ctrl to 1% RF)		210		ns
Supply Current, IDD	VDD = +5V		90	200	µA
Control Voltage, $V_{CTRL1/2}$	VIH	1.2		VDD	V
	VIL	0		0.63	V
Control Current, $I_{CTRL1/2}$			1		µA
Spur Level	Any RF ports, >100MHz		< −125		dBm
Thermal Resistance			60		°C/W

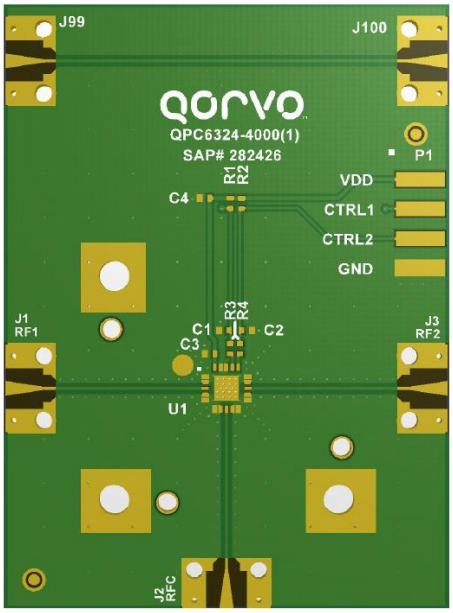
Power Handling Specification (MTTF≥10^6 Hours)

Input Port	Port State	Power(dBm)	T_{CASE}
RFC, RF1 or RF2[1,3]	ON	34.2	85°C
		31.6	105°C
		30.5	110°C
		29.0	115°C
		26.0	120°C
RFC, RF1 or RF2	OFF	28.4	85°C
		25.0	105°C
		23.8	110°C
		22.0	115°C
		19.5	120°C
RFC, RF1 and RF2 simultaneous[2]	All OFF	27.6	85°C
		24.2	105°C
		23.0	110°C
		21.5	115°C
		18.5	120°C

Note
1. For high VSWR loads, this power reduces by 4dB
2. Power is on each input, not total
3. For < 20MHz, max power reduces by 6dB

Application Circuit Schematic and Layout





Bill of Material

Ref Des	Value	Description	Manuf.	Part Number
n/a	n/a	Printed Circuit Board	Qorvo	
U1	n/a	High Isolation SPDT Switch	Qorvo	QPC6324
C1, C2	200 pF	CAP, 0402, 50V, 5%, C0G	Various	
C4	0.1 µF	CAP, 0402, 50V, 10%, X7R	Various	
R3, R4	0 Ω	RES, 0402	Various	
R1, R2, C3	DNP			

Logic Table

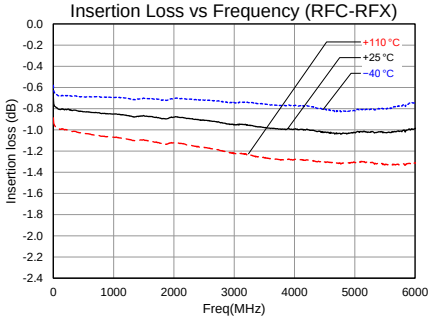
CTRL1	CTRL2	RFC-RF1	RFC-RF2
0	0	OFF	OFF
0	1	OFF	ON
1	0	ON	OFF
1	1	OFF (1)	OFF (1)

Notes:

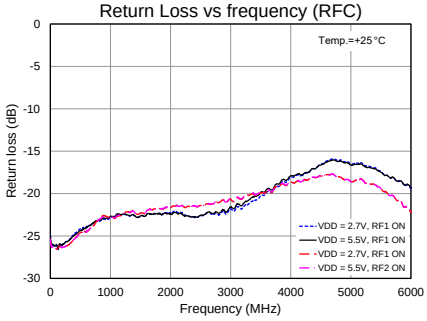
1. This is not a supported ‘switch’ mode. RFC is not terminated.

Performance Plots

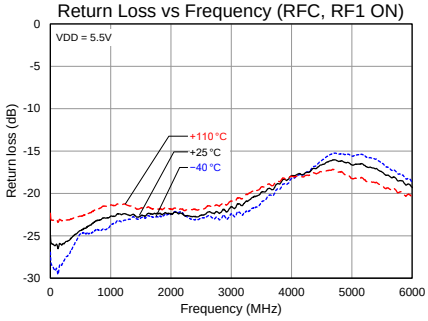
Insertion Loss vs Frequency (RFC-RFX)



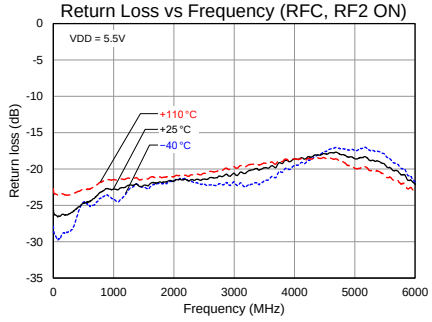
Return Loss vs frequency (RFC)



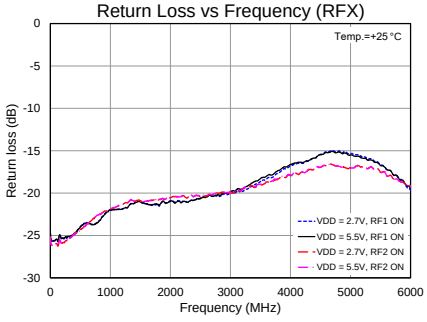
Return Loss vs Frequency (RFC, RF1 ON)



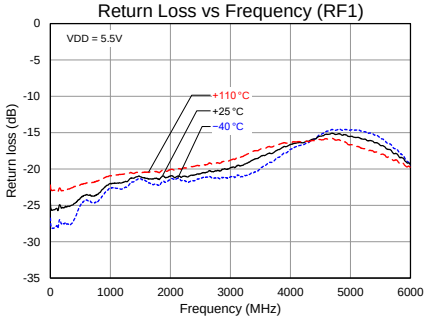
Return Loss vs Frequency (RFC, RF2 ON)



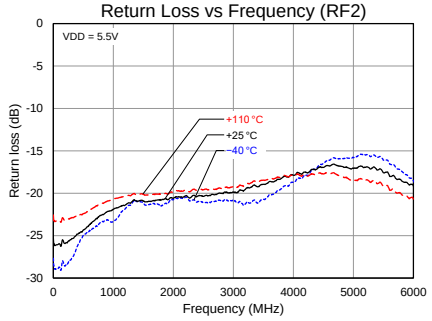
Return Loss vs Frequency (RFX)



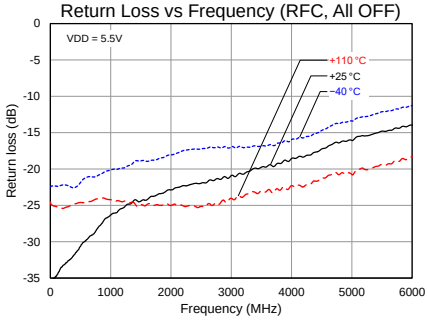
Return Loss vs Frequency (RF1)



Return Loss vs Frequency (RF2)



Return Loss vs Frequency (RFC, All OFF)



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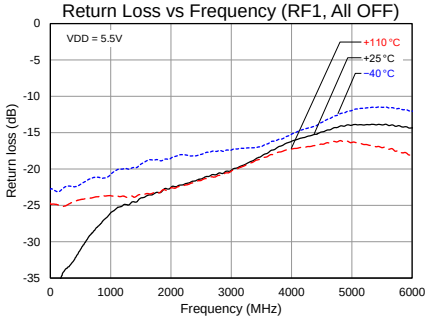

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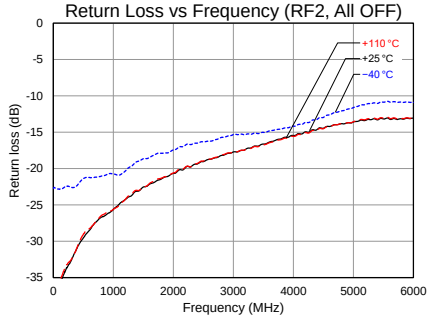
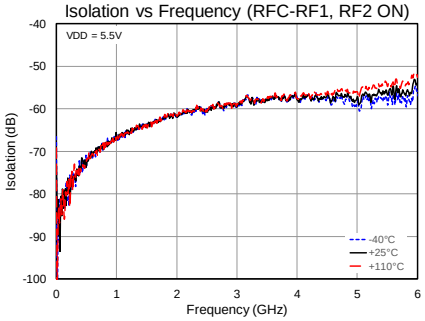
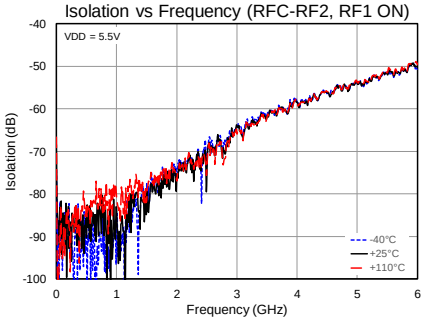


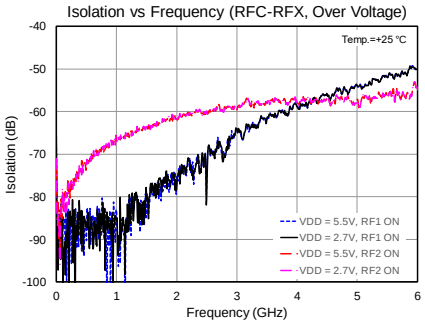
Isolation vs Frequency (RFC-RF1, RF2 ON)

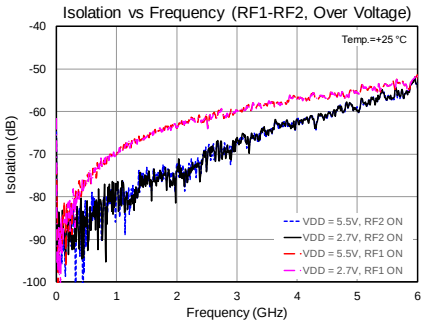


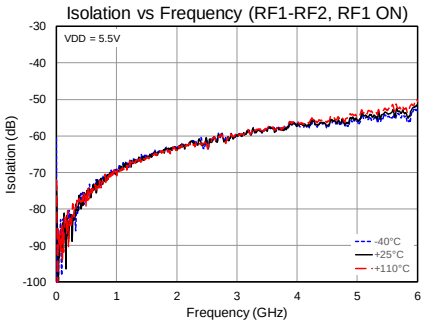
Isolation vs Frequency (RFC-RF2, RF1 ON)

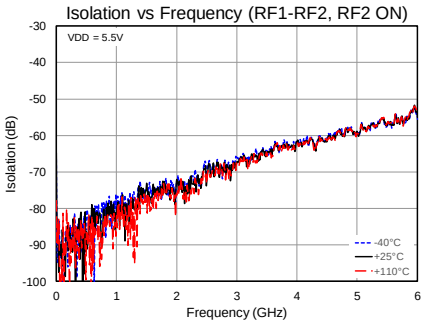


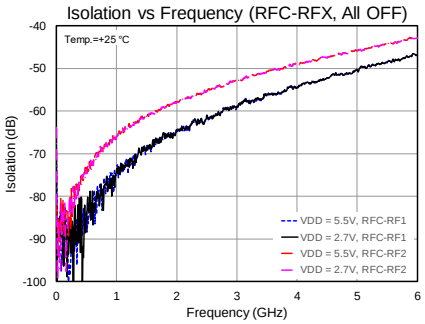
Performance Plots Contd.

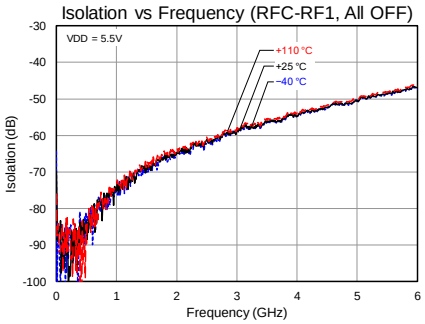


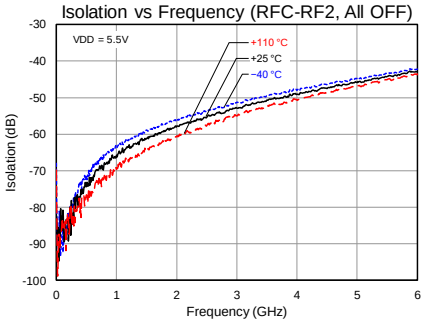


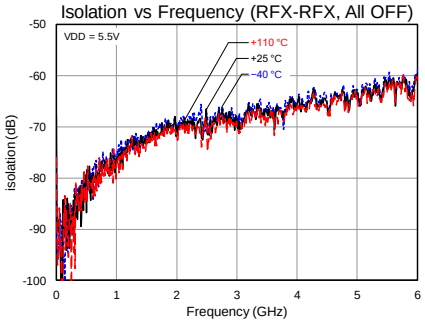


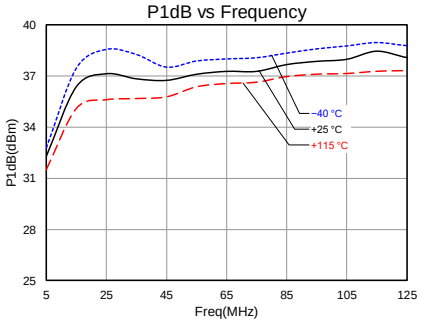




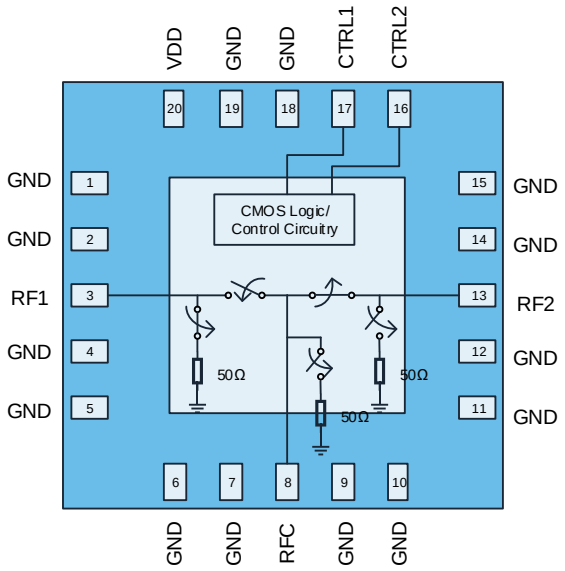








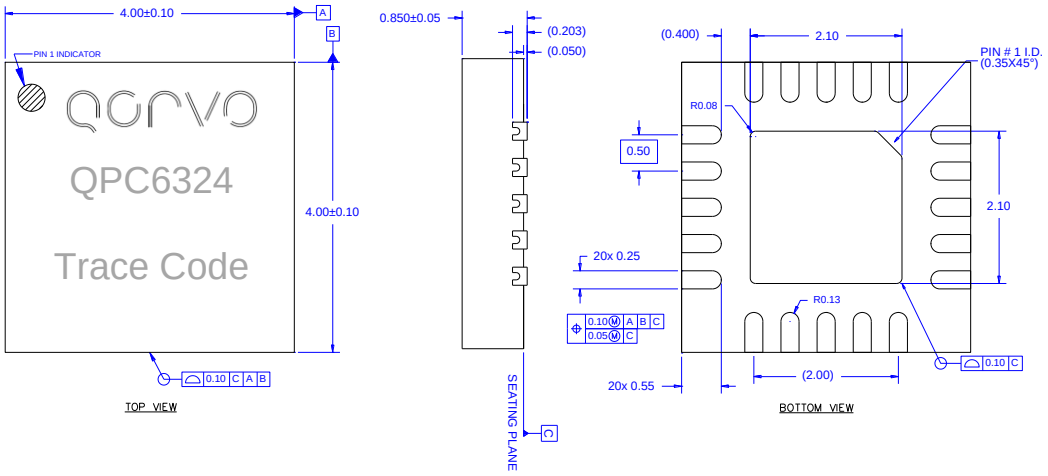
Pin Configuration and Description



Top View

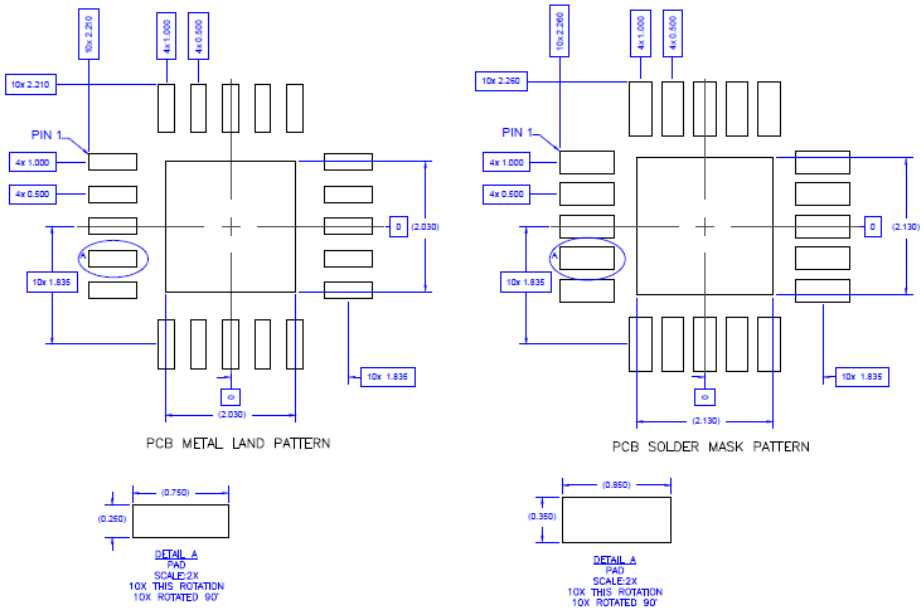
Pin No.	Label	Description	
1,2,5,6,9,10,11,12, 14,15	GND	No internal connection, recommend grounding on PCB board for proper mounting integrity.	
4, 7, 18, 19	GND	Internally connected and must be grounded on PCB board.	
3	RF1	Switch output port 1. Internally pulled to 0V (GND).	
8	RFC	Switch common port. Internally pulled to 0V (GND).	
13	RF2	Switch output port 2. Internally pulled to 0V (GND).	
16	CTRL2	Switch control input 2	Apply logic high after VDD ON and logic low before VDD OFF are recommended.
17	CTRL1	Switch control input 1	
20	VDD	Supply voltage. Bypassing capacitor(s) recommended.	
Backside Pad	GND	Ground connection. The back side of the package should be connected to the ground plane though as short of a connection as possible. PCB via holes under the device are required.	

Package Marking and Dimensions



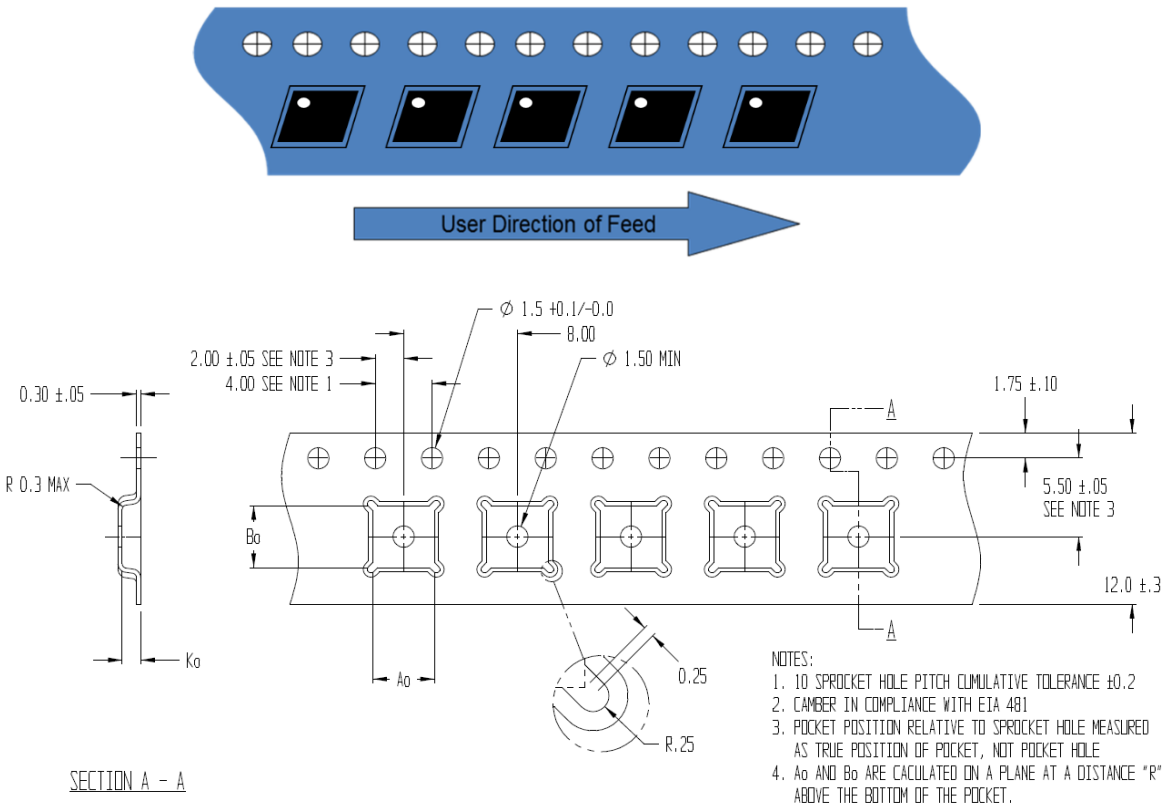
Notes:
1. All dimensions are in millimeters. Angles are in degrees.
2. Dimension and tolerance formats conform to ASME Y14.4M-1994.
3. The terminal #1 identifier and terminal numbering conform to JESD 95-1 SPP-012.

PCB Mounting Pattern



Notes:
1. All dimensions are in millimeters. Angles are in degrees.
2. Use 1 oz. copper minimum for top and bottom layer metal.
3. Via holes are required under the backside paddle of this device for proper RF/DC grounding and thermal dissipation.
4. Do not remove or minimize via hole structure in the PCB. Thermal and RF grounding is critical.
5. We recommend a 0.35mm (#80/.0135") diameter bit for drilling via holes and a final plated thru diameter of 0.25 mm (0.01”).
6. Ensure good package backside paddle solder attach for reliable operation and best electrical performance.

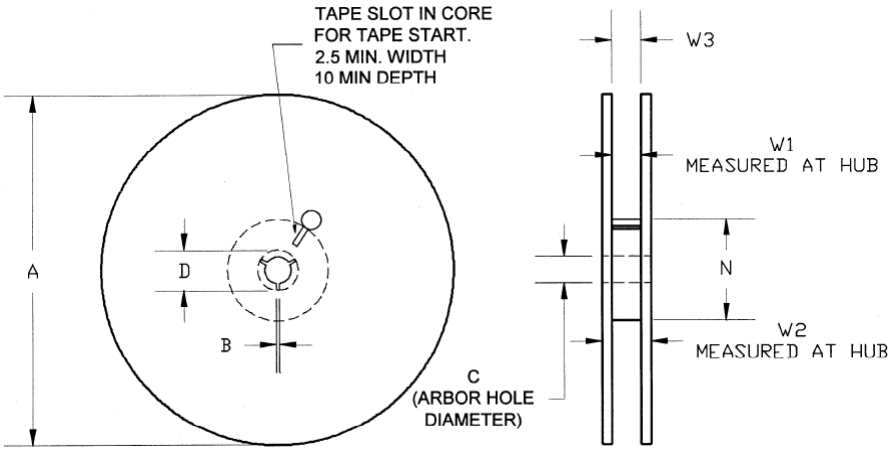
Tape and Reel Information – Carrier and Cover Tape Dimensions



Feature	Measure	Symbol	Size (in)	Size (mm)
Cavity	Length	A0	0.171	4.35
	Width	B0	0.171	4.35
	Depth	K0	0.051	1.10
	Pitch	P1	0.315	8.00
Centerline Distance	Cavity to Perforation - Length Direction	P2	0.079	2.00
	Cavity to Perforation - Width Direction	F	0.217	5.50
Cover Tape	Width	C	0.362	9.20
Carrier Tape	Width	W	0.472	12.0

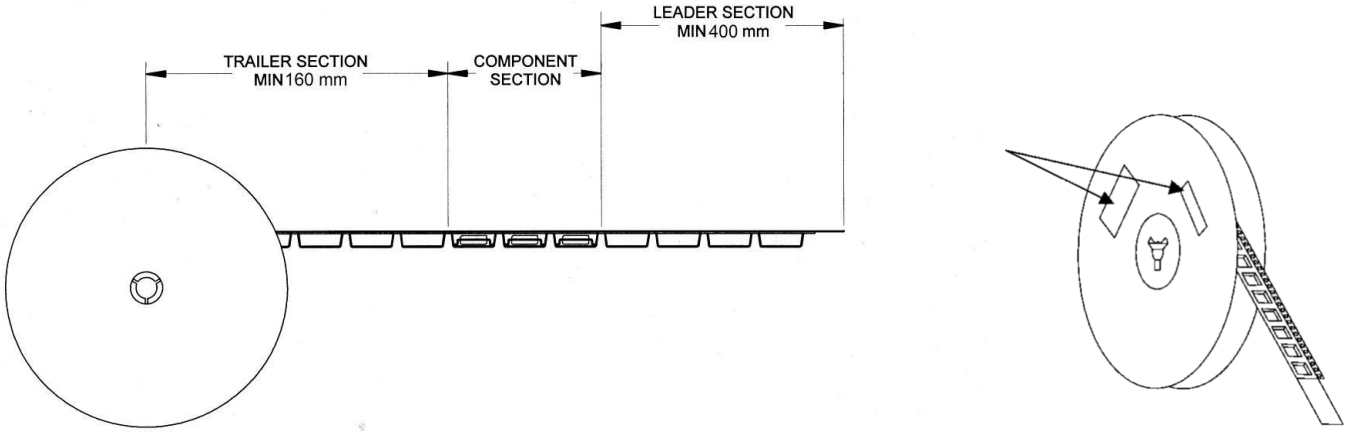
Tape and Reel Information – Reel Dimensions (13”)

Standard T/R size = 2,500 pieces on a 13” reel.



Feature	Measure	Symbol	Size (in)	Size (mm)
Flange	Diameter	A	12.992	330.0
	Thickness	W2	0.717	18.2
	Space Between Flange	W1	0.504	12.8
Hub	Outer Diameter	N	4.016	102.0
	Arbor Hole Diameter	C	0.512	13.0
	Key Slit Width	B	0.079	2.0
	Key Slit Diameter	D	0.787	20.0

Tape and Reel Information – Tape Length and Label Placement



Notes:
1. Empty part cavities at the trailing and leading ends are sealed with cover tape. See EIA 481-1-A.
2. Labels are placed on the flange opposite the sprockets in the carrier tape.

Handling Precautions

Parameter	Rating	Standard
ESD – Human Body Model (HBM)	Class 2	ESDA / JEDEC JS-001-2012
ESD – Charged Device Model (CDM)	Class C3	JEDEC JESD22-C101F
MSL – Moisture Sensitivity Level	Level 1	IPC/JEDEC J-STD-020

Caution!
ESD-Sensitive Device

Solderability

Compatible with both lead-free (260°C max. reflow temp.) and tin/lead (245°C max. reflow temp.) soldering processes.
Solder profiles available upon request.

Contact plating: NiPdAu *(Plating thickness: Ni 0.5000~2.0066 µm; Pd 0.01999~0.15011 µm; Au 0.00254~0.01501 µm)*

RoHS Compliance

This part is compliant with 2011/65/EU RoHS directive (Restrictions on the Use of Certain Hazardous Substances in Electrical and Electronic Equipment) as amended by Directive 2015/863/EU.

This product also has the following attributes:

- Lead Free
- Halogen Free (Chlorine, Bromine)
- Antimony Free
- TBBP-A ($C_{15}H_{12}Br_4O_2$) Free
- SVHC Free

Contact Information

For the latest specifications, additional product information, worldwide sales and distribution locations:

Web: www.qorvo.com

Tel: 1-844-890-8163

Email: customer.support@qorvo.com

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