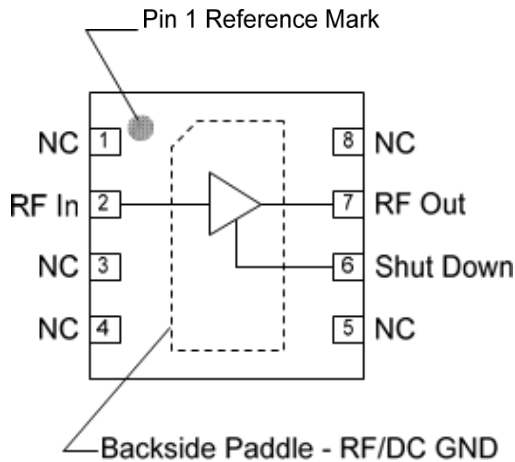


Product Description

The QPL6208Q is a high linearity, ultra-low noise gain block amplifier in a small 2x2 mm surface-mount package. At 2332 MHz, the amplifier typically provides +37dBm OIP3. The amplifier does not require any negative supplies for operation and can be biased from positive supply rails from 3 to 5 V. The device is housed in a lead-free/green/RoHS-compliant industry-standard 2x2 mm package.

The QPL6208Q uses a high performance E-pHEMT process. The low noise amplifier contains an internal active bias to maintain high performance over temperature.

Functional Block Diagram



Package: DFN, 8-pin
2.0mm x 2.0mm x 0.85mm

Feature Overview

- Tested in accordance with AEC-Q100 Grade 2
- Ultra-low noise figure, 0.48 dB NF at 2330 MHz
- High linearity, +37 dBm Output IP3
- High input power ruggedness, >22 dBm PIN, MAX
- Unconditionally stable
- Integrated on-chip matching, 50 ohm in/out
- Integrated active bias
- Integrated shutdown control pin
- 3-5 V positive supply voltage: -V_{gg} not required

Applications

- SDARS Active Antenna

Ordering Information

PART NUMBER	DESCRIPTION
QPL6208QSB	Standard 5-piece bag
QPL6208QSQ	Standard 25-piece bag
QPL6208QSR	Standard 100-piece reel
QPL6208QTR7	Standard 2.5K -piece Reel
QPL6208QPCK401	Evaluation Board + 5-piece bag

Standard T/R Size = 2500 pieces on a reel

Absolute Maximum Ratings

PARAMETER	RATING	UNITS
Storage Temperature	-65 to 150°	C
Supply Voltage (V _{DD})	+7	V
RF Input Power, CW, 50Ω, T = 25°C	+22	dBm

Recommended Operating Conditions

PARAMETER	MIN	TYP	MAX	UNITS
Supply Voltage (V _{DD})	+2.0	+3.6	+4.0	V
TCASE	-40		+105	°C
T _J (for >10 ⁶ hours MTTF)			+200	°C

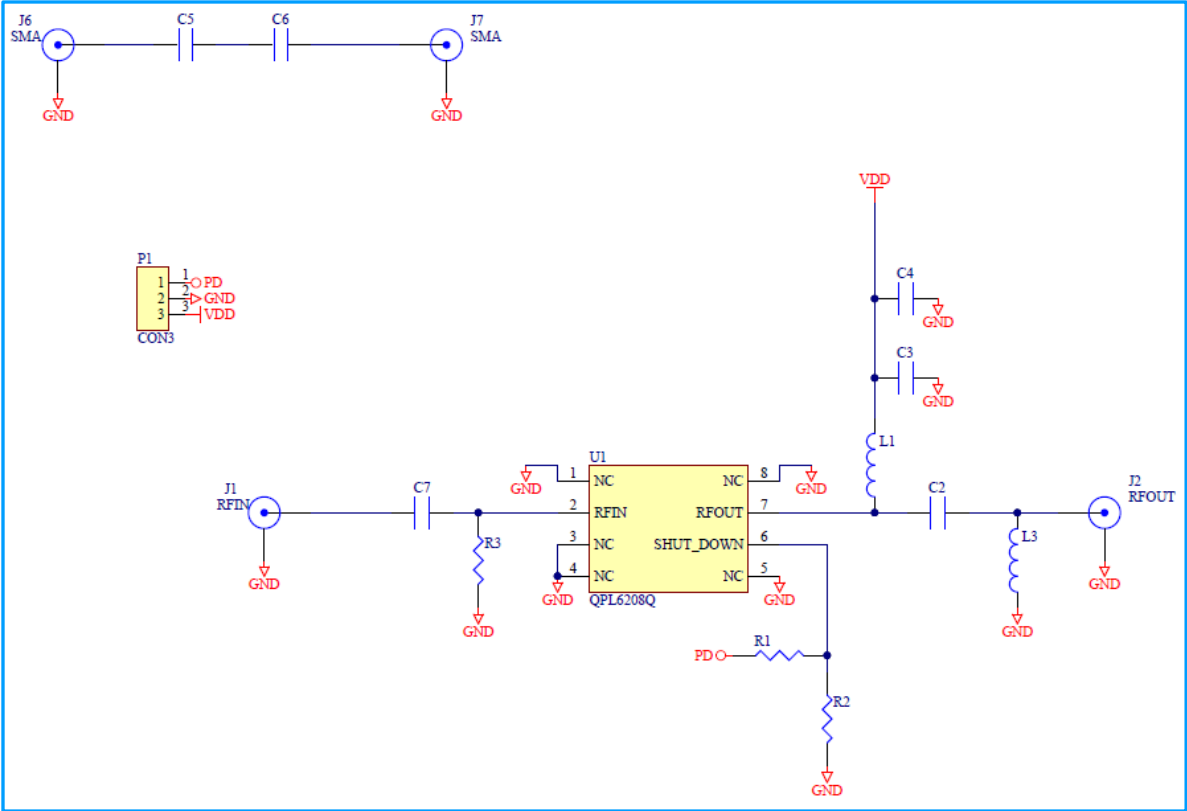
Electrical Specifications

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Operational Bandwidth		100		3000	MHz
Test Frequency			2330		MHz
Gain		13.3	13.7	14.5	dB
Input Return Loss			13		dB
Output Return Loss			18		dB
Output P _{1dB}		+19	+19.6		dBm
Output IP ₃	P _{out} =+5 dBm/tone, Δf=1 MHz	+32	+37		dBm
Noise Figure ¹			0.48	0.75	dB
Power Shutdown Control (Pin 6)	On state	0		0.4	V
	Off state (Power down)	2.5	3.3	V _{DD}	V
Current, I _{DD}	On state	40	53	60	mA
	Off state (Power down)		1.3		mA
Shutdown pin current, I _{SD}	VPD ≥ 3 V		75		μA
Thermal Resistance, θ _{JC}	V _{DD} = 5.0V		92		°C/W

Test conditions unless otherwise noted: V_{DD} = +3.6V, Temp=+25°C, 50 Ω system.

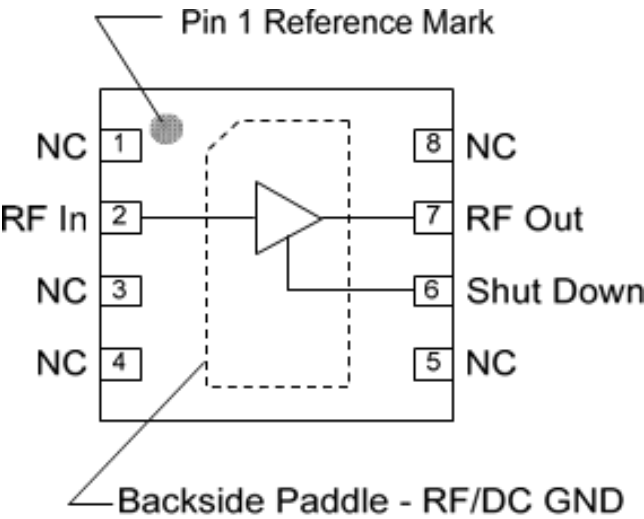
Note: 1) Noise Figure data has input trace loss de-embedded.

Applications Schematic



Qty	Ref Des	Description	UOM
1		LNA	EA
1		PCB, QPL6208Q	EA
1	C4	CAP, 1uF, 10%, 6.3V, X5R, 0603	EA
2	C2,C6	CAP, 8.2pF, +/-0.5pF, 50V, C0G, 0603	EA
3	C3,C5,C7	CAP, 100pF, 5%, 50V, C0G, 0603	EA
1	R2	RES, 10K, 1%, 1/16W, 0603	EA
1	R1	RES, 33K, 5%, 1/16W, 0603	EA
1	L3	IND, 6.8nH, 5%, W/W, 0402	EA
1	L1	IND, 68nH, 5%, W/W, 0603	EA
1	P1	CONN, HDR, ST, PLRZD, 3-PIN, 0.100"	EA
4	J1,J2,J6,J7	CONN, SMA, EL, FLT, 0.037" SPE-000317	EA
4	J1,J2,J6,J7	CONN, SMA, END LNCH, FLT, 0.037"	EA
1	R3	NOT POPULATED ITEM-1	EA

Pin Configuration and Description

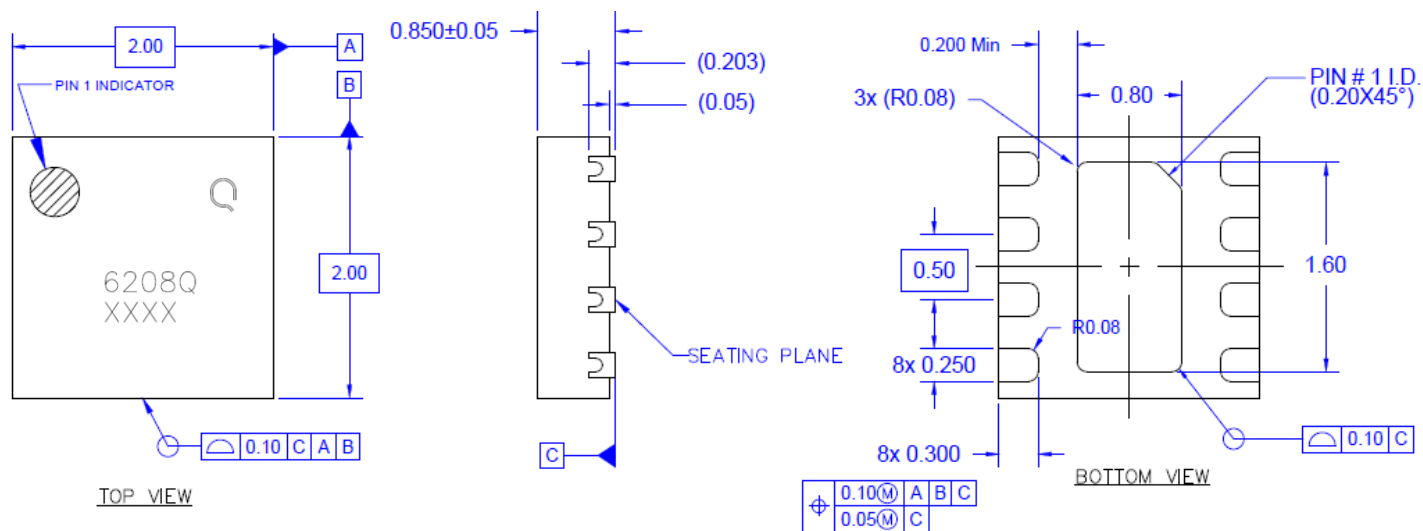


PIN NO.	LABEL	DESCRIPTION
2	RF In	RF Input pin. A DC Block is required.
6	Shut Down	A high voltage turns off the device. If the pin is not connected or is less than 0.4V, then the device will operate under its normal operating condition. Tie pin to ground if not being used.
7	RF Out / DCBias	RF Output pin. DC bias will also need to be injected through a RF bias choke/inductor for operation.
1, 3, 4, 5, 8	NC	No electrical connection. Provide grounded land pads for PCB mounting integrity.
Backside Paddle	RF/DC GND	RF/DC ground. Use recommended via pattern to minimize inductance and thermal resistance; see PCB Mounting Pattern for suggested footprint.

Mechanical Information

Marking: Part number – 6208Q

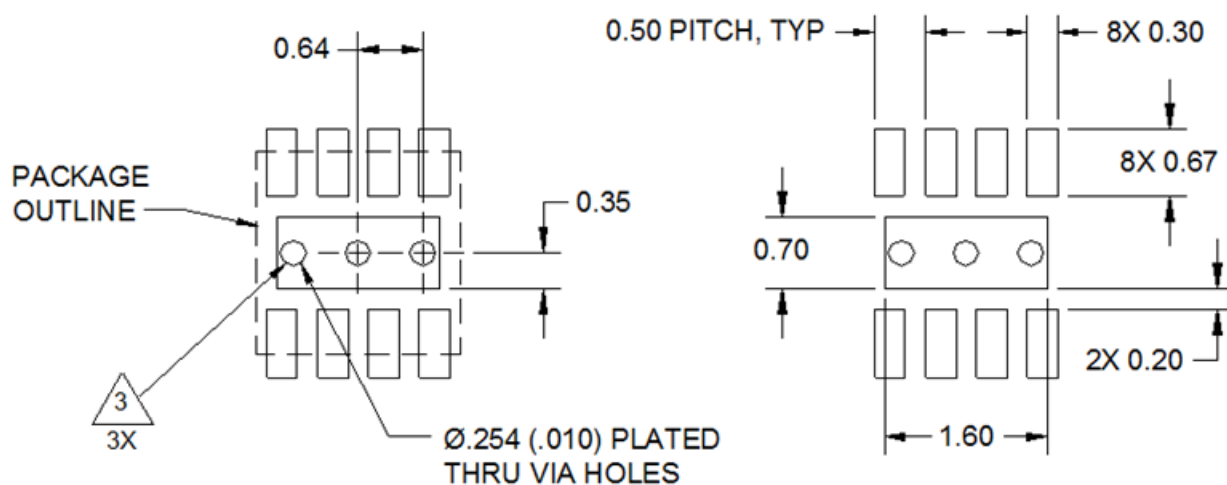
Trace Code – XXXX



NOTES:

1. All dimensions are in millimeters. Angles are in degrees.
2. Except where noted, this part outline conforms to JEDEC standard MO-220, Issue E (Variation VGGC) for thermally enhanced plastic very thin fine pitch quad flat no lead package (QFN).
3. Dimension and tolerance formats conform to ASME Y14.4M-1994.
4. The terminal #1 identifier and terminal numbering conform to JESD 95-1 SPP-012.

PCB Mounting Pattern



NOTES:

1. All dimensions are in millimeters. Angles are in degrees.
2. Use 1 oz. copper minimum for top and bottom layer metal.
3. Vias are required under the backside paddle of this device for proper RF/DC grounding and thermal dissipation. We recommend a 0.35mm (#80/.0135") diameter bit for drilling via holes and a final plated thru diameter of 0.25 mm (0.10").
4. Ensure good package backside paddle solder attach for reliable operation and best electrical performance.

Product Compliance Information

ESD Sensitivity Ratings



Caution! ESD-Sensitive Device

ESD Rating: Class 1B
Value: Passes ≥ 500 V to < 1000 V
Test: Human Body Model (HBM)
Standard: JEDEC Standard JESD22-A114

ESD Rating: Class C3
Value: Passes ≥ 1000 V to < 2000 V
Test: Charged Device Model (CDM)
Standard: JEDEC Standard JESD22-C101

MSL Rating

MSL Rating: Level 1
Test: 260°C convection reflow
Standard: JEDEC Standard IPC/JEDEC J-STD-020

Solderability

Compatible with both lead-free (260°C max. reflow temperature) and tin/lead (245°C max. reflow temperature) soldering processes.

Package contact plating: NiPdAu

This part is compliant with EU 2002/95/EC RoHS directive (Restrictions on the Use of Certain Hazardous Substances in Electrical and Electronic Equipment).

RoHS Compliance

This product also has the following attributes:

- Lead Free
- Halogen Free (Chlorine, Bromine)
- Antimony Free
- TBBP-A ($\text{C}_{15}\text{H}_{12}\text{Br}_4\text{O}_2$) Free
- PFOS Free
- SVHC Free

Contact Information

For the latest specifications, additional product information, worldwide sales and distribution locations:

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Tel: 1-844-890-8163

Email: customer.support@qorvo.com

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