APPLICATION NOTE

QPQ1907

2.4 GHz WLAN/BT LTE Co-Existence BAW Filter

High-performance, high power Bulk Acoustic Wave (BAW) band-pass filter, high rejection in the band-edge and adjacent LTE/TD-LTE bands.

Introduction

This purpose of this application note is to help customers translate the layout and design guidelines for the QPQ1907 Bulk Acoustic Wave (BAW) band-pass filter. The QPQ1907 is a high-performance, high power Bulk Acoustic Wave (BAW) band-pass filter with extremely steep skirts, simultaneously exhibiting low in-band insertion loss in the Wi-Fi band and high near-in rejection in the 2.6GHz bands. It is specifically designed to enable coexistence of WiFi and LTE signals within the same wireless communications module or in close proximity to one another. This BAW filter is housed a 1.4 x 1.2 x 0.915 mm CLP package. The filter exhibits excellent power handling capabilities meeting FCC max limits of 1Watt average power.

Product Details

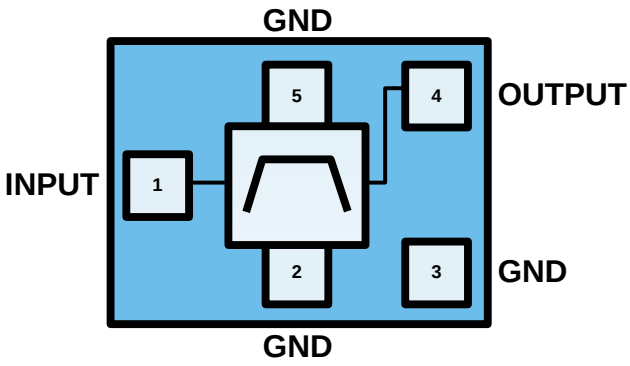

Figure 1. Functional Block Diagram & Pin-out Detail

Table 1. QPQ1907 Pin Description

PIN NUMBER	LABEL	DESCRIPTION
1	INPUT	Transmit Port (Large Signal Input Pin)
4	OUTPUT	Antenna Port
2, 3, 5	GND	Ground

Notes:

1. Pin 1 is the unidirectional large signal input port and pin 4 is the unidirectional large signal output port.
2. The Transmit (Pin 1) and Antenna (Pin 4) port are both bidirectional for small signals only.

Evaluation Board Information

The Qorvo QPQ1907 EVB is designed to provide performance representative of that obtainable in an actual application. The EVB is designed to operate with 50 Ω load impedances at all RF ports, which are provided with SMA connector interfaces.

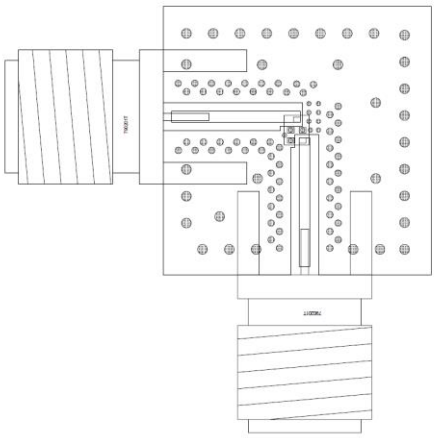

Figure 2a. QPQ1907 Evaluation Board Image

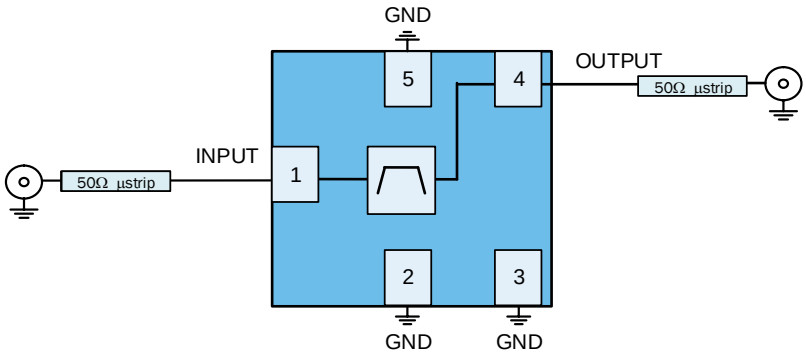

Figure 2b. QPQ1907 Evaluation Board Schematic

Table 2. QPQ1907-PCB Stack-up

Evaluation Board Layer Description/Stackup	
Top Layer:	1/2 oz. plated up to 1 mil holes
Dielectric 1:	7.5 mils total dielectric thickness using Taconic TYL-5A
Mid Layer 1:	1/2 oz. Copper
Dielectric 2:	x mils total dielectric thickness using FR4 material
Bottom Layer:	1/2 oz. copper plated up to 1 mil holes
Overall Thickness:	62 mils

Table 3. QPQ1907 Evaluation Board Bill of Materials

REFERENCE DESIGNATOR	VALUE	DESCRIPTION	MANUFACTURE	PART NUMBER
U1	-	QPQ1907 BAW Filter	Qorvo	QPQ1907
PCB	-	3 Layer	Multiple	QPQ1907-EVB

System Architecture Application Circuit Recommendations

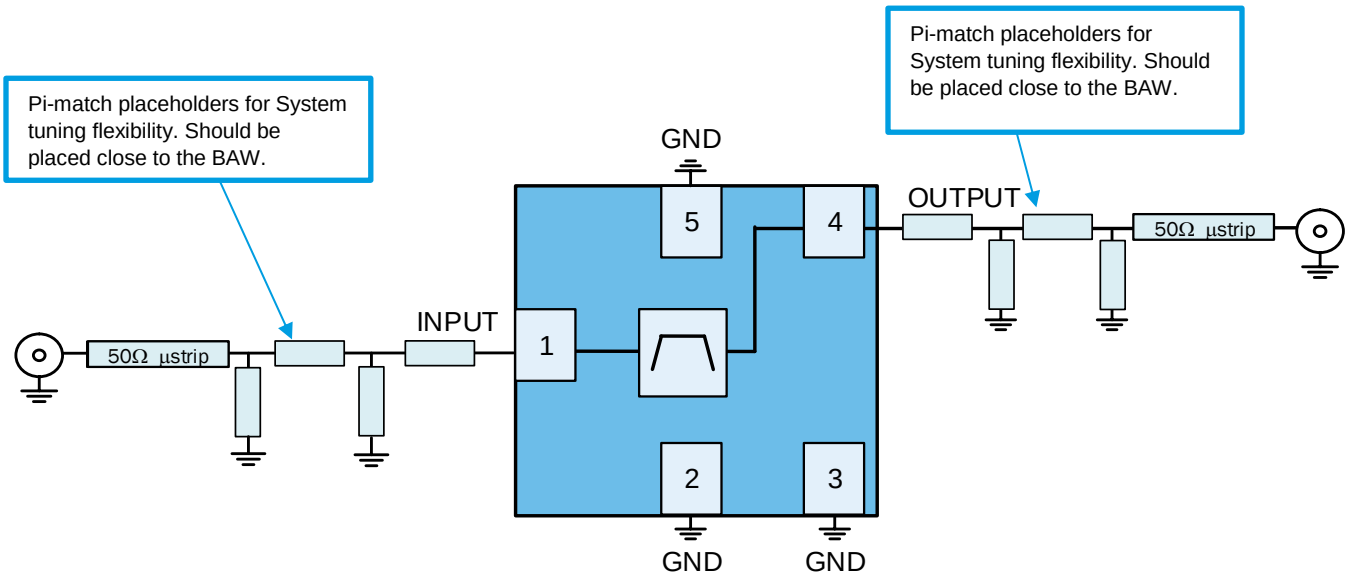

Figure 3. Recommended Application Circuit in a System.

1. The above schematic shows recommended Pi-network match placeholders for system tuning flexibility based on the QPQ1907 EVB. The customer should ensure that sufficient Pi-matching is provided based on their PCB layout.

2. It is recommended to place a ground via next to each GND pin of the BAW and to add ground vias around RF traces. For example, each ground pin should have their own ground via.

3. We recommend following Qorvo evaluation board layout guidelines as close as possible. The QPQ1907 evaluation board uses 8 mil GND vias with 18 mil pads under the BAW. Gerber files are available upon request.

4. We do not recommended connecting ground pins 2 and 5 with a common plane or trace between them due to some manufacturing limitations. **Figure 4a** illustrates the recommended configuration.

PCB Layout Considerations

Board layout must be carefully considered to achieve optimal performance from any BAW filter, including the QPQ1907. In addition to providing connectivity between the BAW and external components, the PCB layout is a part of the overall circuit. The RF parasitics of the traces, along with coupling between traces, must be evaluated. The QPQ1907 Evaluation Board PCB layout guidelines provide a good starting point for designing the layout in the actual application.

RF Traces

All PCB traces between the RF pins and matching networks (where applicable) should be 50 Ω controlled impedance lines, as should the traces between the matching networks and the next component in the chain. The RF traces should be routed on the top layer to minimize coupling with other RF, control input, and DC traces present on the PCB. If it is not possible for some reason to route RF traces on the top layer, we suggest that you make sure there is proper isolation between traces on the layout to avoid any coupling issues. RF lines should be isolated from other RF and DC signals from other components by adding solid ground planes (with vias) between them to minimize coupling and cross-talking. In addition, we also recommend reducing RF trace lengths, wherever possible.

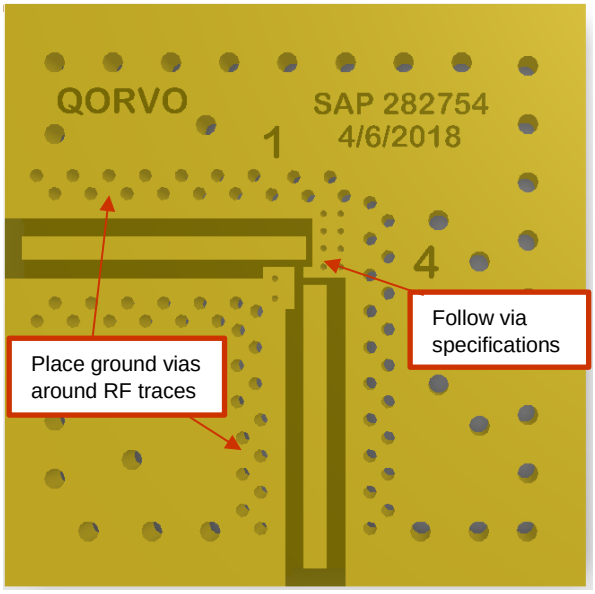

Figure 4a. Recommended PCB layout Considerations.

Grounding Considerations

Grounding of BAW GND pins - The ground pins serve as the primary RF ground reference for the entire BAW. Connect the BAW filter ground pins directly to the main ground plane layer of the PCB. The PCB ground layer should be close to the component layer, preferably the next layer down to minimize the lengths of via connections between the component and ground layers. Ground paths (under device) should be made as short as possible. This ground layer also provides the reference layer for microstrip lines.

Reference Plane - A larger number of via holes should be distributed over the entire area below/around the BAW to provide good RF ground reference ground plane, as shown in **Figure 4b** below. Alternately, it is recommended to place a ground via close and next to each GND pin of the BAW to avoid a ground loop. Each ground pin should have their own ground via The QPQ1907 EVB uses GND vias with an 18mil diameter and 8mil hole size under the BAW.

GND Vias for Thermal Considerations – The BAW GND pins serve as the primary path for heat removal, additionally, the PCB ground vias will serve as a low resistance thermal path between the BAW and the PCB. Vias passing through multiple copper layers provide the best overall RF and thermal performance. The QPQ1907 ground pins have special electrical and thermal grounding requirements. This pad is the main RF ground and main thermal conduct path for heat dissipation. The GND pad and vias pattern and size used on the Qorvo evaluation board should be replicated. The Qorvo layout files in Gerber format can be provided upon request.

DC Layout Considerations

All DC traces routed near the BAW must be isolated with a GND inbetween the BAW and the DC trace. The GND should have vias on them which route from the top layer through to the bottom GND layer. It is recommended to avoid routing traces underneath the BAW.

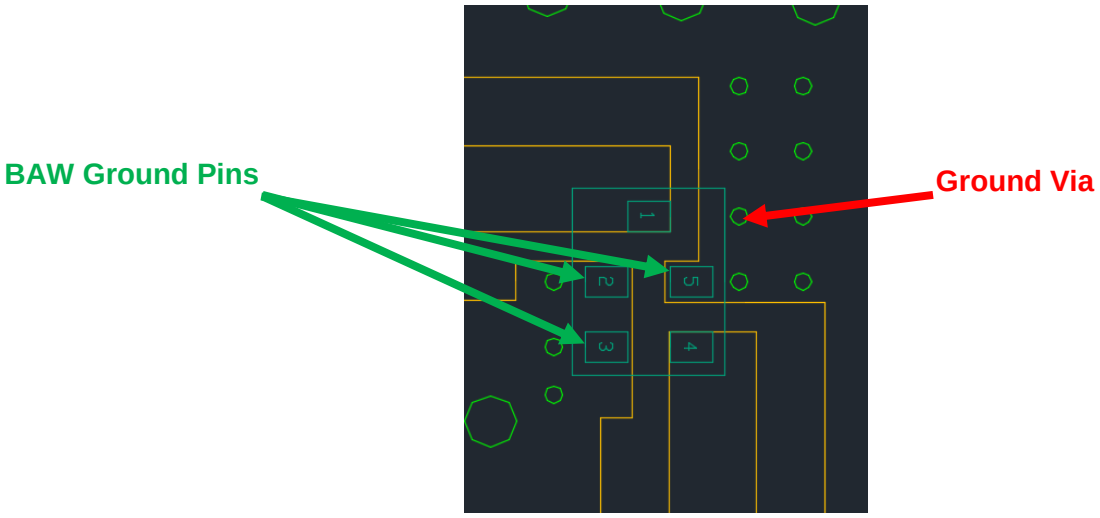

Figure 4b. Recommended Ground Via Placement.

PCB Footprint Recommendations

See **Figures 5a and 5b** below for the recommended package outline drawing and solder mask patterns.

PCB Layout Considerations

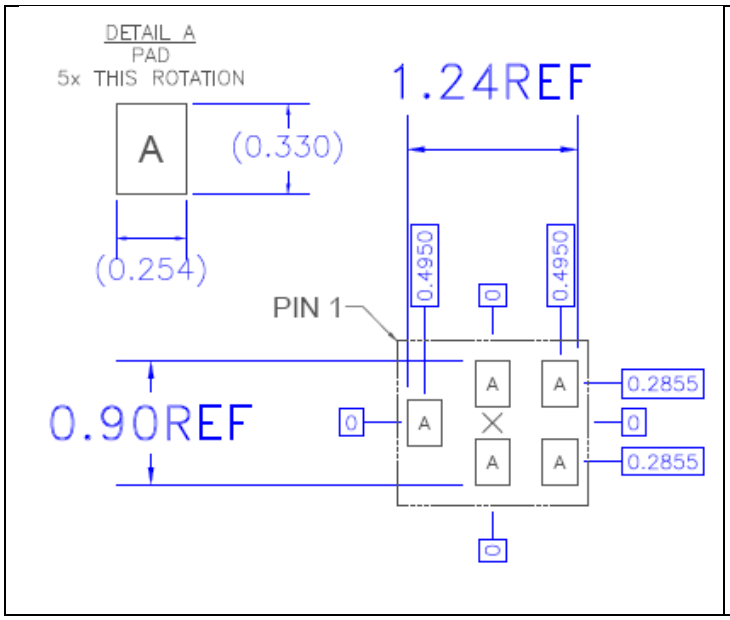

Figure 5a. PCB Footprint Recommended Landing Pattern

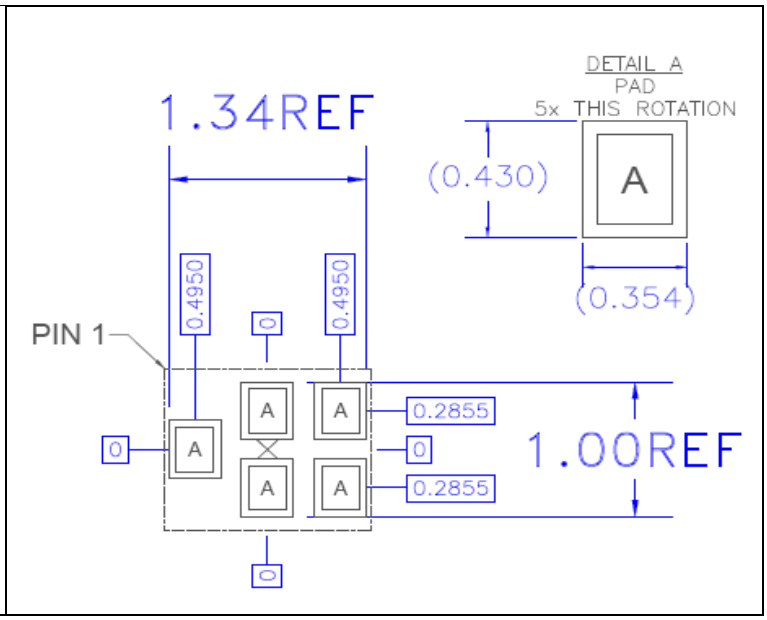

Figure 5b. PCB Footprint Recommended Solder Mask Pattern

Package Information

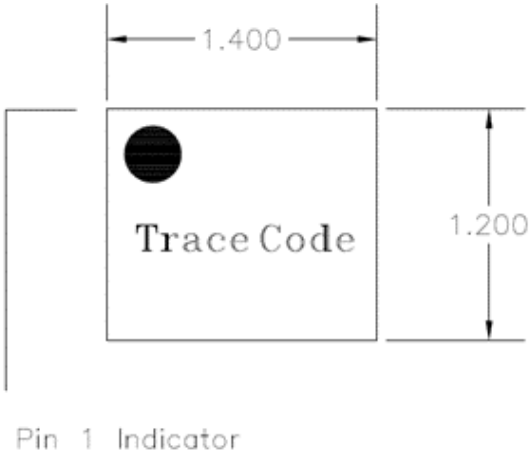

Figure 5c. Marking Diagram

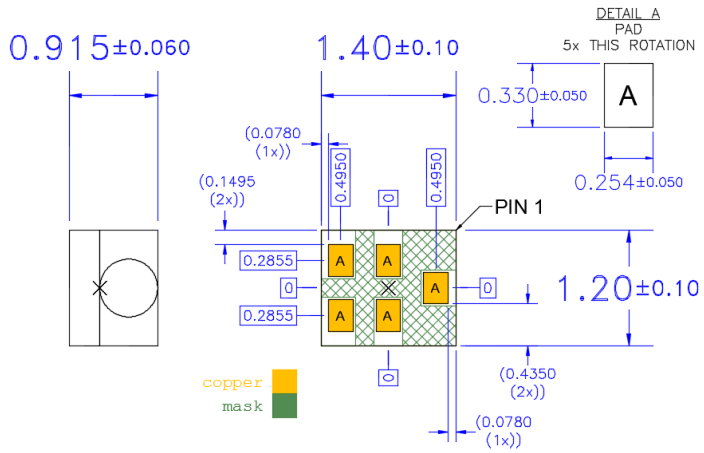

Figure 5d. QPQ1907 Package Outline Drawing

Package Style: Laminate
Dimensions: 1.4 x 1.2 x 0.915 mm

Package for Surface Mount Technology
Terminations: Au plating 0.5 - 1.0µm, over a 2- 6µm Ni Plating
Approximate weight 1.546 mg

Notes:

1. All dimensions shown are typical in millimeters. Angles are in degrees.
2. This drawing specifies the mounting pattern used on the Qorvo evaluation board for this product. Some modifications may be necessary to suit end user assembly materials and processes.

Reflow Profile & Solder Paste

Figure 6a illustrates the recommended reflow profile for the QPQ1907.

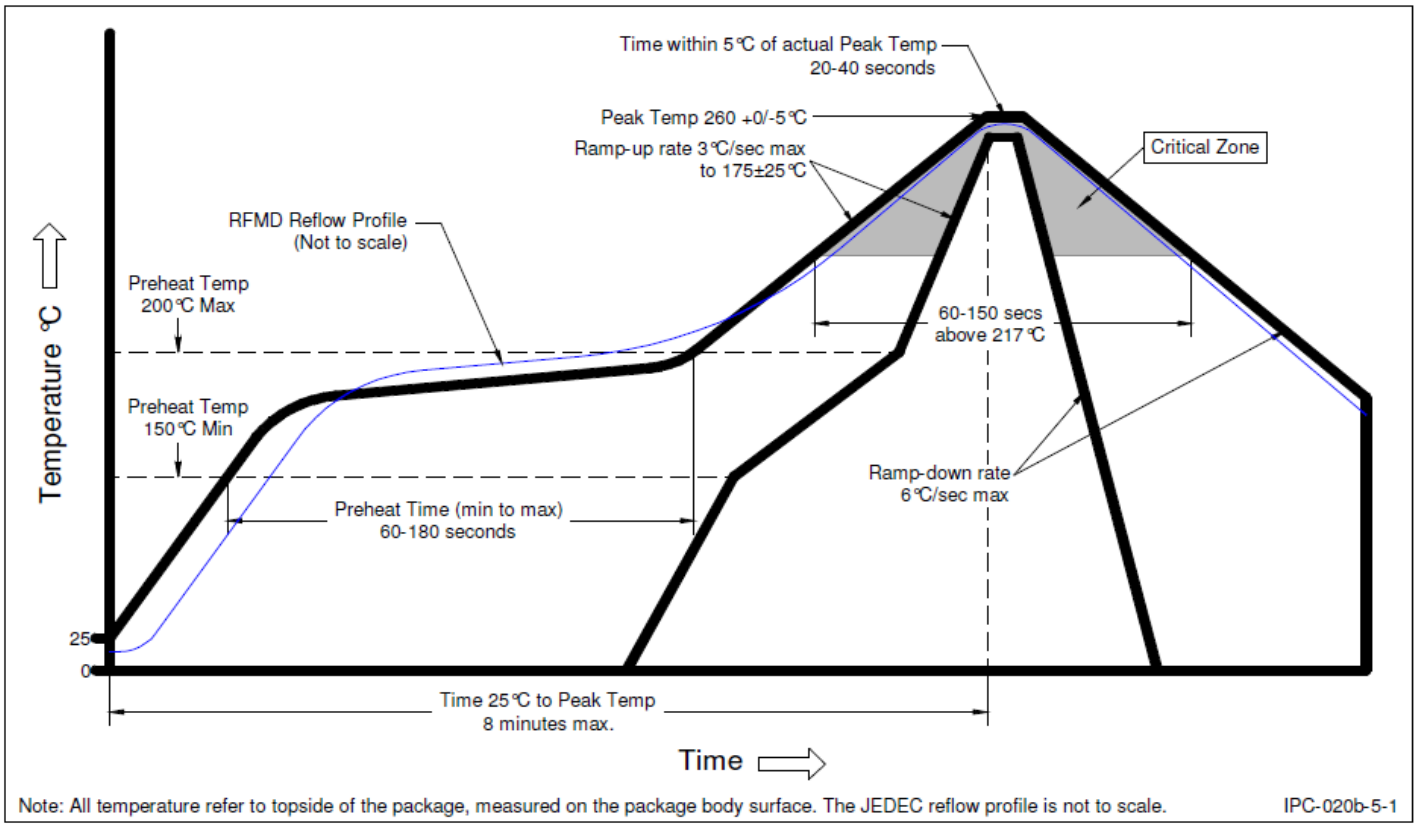

Table 4. Recommended Reflow Profile & Conditions

CONDITIONS	
Ramp-up rate	3 ºC/second max.
Preheat temperature 175 (±25) ºC	180 seconds max.
Temperature maintained above 217 ºC	60 seconds to 150 seconds
Time within 5 ºC of actual peak temperature	20 seconds to 40 seconds
Peak temperature range	260+0/-5 ºC
Ramp-down rate	6 ºC/second max.
Time 25 ºC to peak temperature	8 minutes max.
Maximum number of reflow cycles	≤ 3
Pre-baking requirements	Refer to JEDEC J-STD-033 if original device package is unsealed
Maximum reflow temperature	260 ºC

Maximum reflow temperature is 260°C. The temperature used to classify the MSL level appears on the MSL label on each shipping bag. Qorvo uses reflow profiles in accordance with IPC/JEDEC J-STD-020 for qualification except for the maximum reflow temperature of 260 °C.

Solder paste used for the Qorvo high temperature reflow qualification.

Table 5. Solder Paste Specifications.

SPECIFICATIONS	
Solder paste	Multicore 96SCAGS89 (CR39)
Alloy type	Sn95.5/Ag3.8/Cu0.7
Metal content	88.5%
Solder particle size	45 µm to 20 µm

Support Data

For any further data on the QPQ1907, please request Qorvo point of contact such as marketing, sales or a representative in your region.

Additional Information

For information on ESD, Soldering Profiles, Packaging Standards, Handling and Assembly, please contact Qorvo for general guidelines.

Contact Information

For the latest specifications, additional product information, worldwide sales and distribution locations:
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Email: customer.support@qorvo.com

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