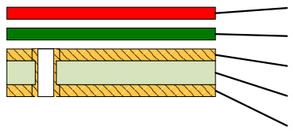
LAYER STACK LEGEND_SEE NOTE 3 FOR MATERIAL (COPPER THICKNESS IS @ FINISHED THICKNESS)

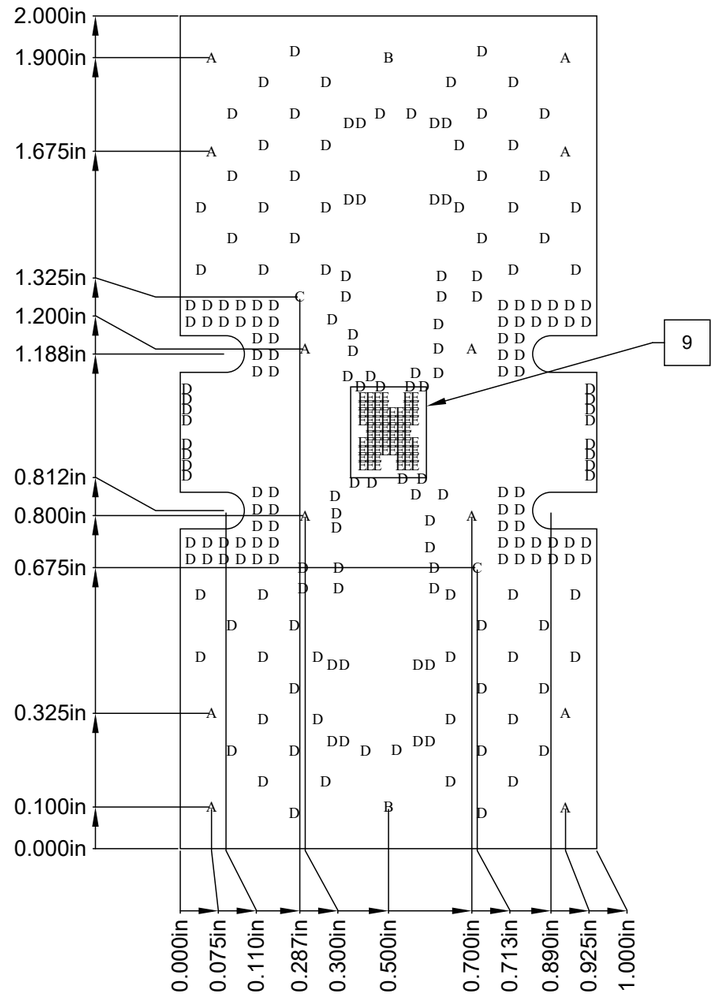


Material	Layer	Thickness	Dielectric Material	Type	Gerber
	SILKSCREEN TOP			Legend	GTO
Surface Material	SOLDERMASK TOP	0.0004in	SOLDER RESIST	Solder Mask	GTS
Copper	**METAL 1 TOP**	**0.0018in**		**Signal**	**GTL**
Core		*0.0080in*	*R4003C*	*Dielectric*	
Copper	**METAL 2 BOT**	**0.0018in**		**Signal**	**GBL**

Total thickness: 0.0120in

SUPPLIER MUST SEND EMAIL TO EVBHOLD@QORVO.COM IF JOB IS PLACED ON HOLD

SUPPLIER SHALL SEND A COPY OF FINAL WORKING GERBERS TO CEADS@QORVO.COM



NOTES: (UNLESS OTHERWISE SPECIFIED)

1. BOARD FABRICATION METHODS MUST COMPLY WITH:
   FABRICATE IN ACCORDANCE WITH IPC-6018B, per IPC-6011, CLASS 2.
2. ARTWORK FORMAT: GERBER 274X
   GERBER DATA SUPPLIED WITH DESIRED FINAL TRACE WIDTHS. PROCESS COMPENSATION TRACE WIDTH ADJUSTMENTS TO BE DONE BY PCB FABRICATOR
3. NUMBER OF LAYERS: 2 LAYERS
   METAL 1 0.5oz. (Plus Plating)
   CORE 1: ROGERS 4003C, .008in. THICK
   METAL 2 0.5oz. (Plus Plating)
   SOLDERMASK TOP: LPI (LIQUID PHOTO-IMAGEABLE), GREEN OR LDI (LASER DIRECT IMAGEABLE), GREEN. MAX FINISH THICKNESS OF SOLDERMASK TO BE 0.001in.
   SILKSCREEN TOP: HIGH TEMPERATURE, NON-CONDUCTIVE, WHITE EPOXY BASED INK.
4. FINISH PLATING:
   METAL 1 (TOP) AND METAL 2 (BOTTOM):
   ENIG (ELECTROLESS NICKEL/IMMERSION GOLD):
5. FINISHED BOARD THICKNESS: (0.012in) ±.003IN.
6. COPPER IS PULLED BACK PER GERBER DATA FROM EDGE OF BOARD ON METAL 1 (TOP) AND METAL 2 (BOTTOM) EXCEPT AROUND CONNECTOR AREA.
7. TOLERANCE: PC BOARD OUTLINE: ±0.002in.
8. BURRS SHALL NOT EXCEED 0.002in.

[9] VIA PLATING/FILLING:
A. ALL 8 MIL (A) VIAS UNDER THE DUT ARE TO BE COPPER-FILLED, OVER-PLATED AND PLANARIZED. FINISHED COPPER THICKNESS TO BE 0.0018 ±0.0004in.
B. ALL OTHER PLATED THRU HOLES TO BE PLATED TO 0.0007in. MIN. THICKNESS.

10. METAL 1(TOP) AND METAL2(BOTTOM) AFTER OVERPLATING AND PLANARIZATION SHALL HAVE A MAX ALLOWABLE NEGATIVE FEATURE OF 0.0008in. AND A MAX ALLOWABLE POSITIVE FEATURE OF 0.0003in.
11. CONDUCTOR WIDTHS AND SPACING TO BE WITHIN 0.001in. OF CAD DATABASE.
12. SOLDERMASK IN PLATED-THRU HOLES IS ACCEPTABLE AS LONG AS IT DOES NOT EXIST ON BACKSIDE OF BOARD.
13. ALL HOLES TO BE LOCATED WITHIN ±0.001 OF CAD DATABASE.
14. NO VENDOR MARKING OR SERIALIZATION ALLOWED.
15. DELIVER BOARDS BAGGED AS: SINGLES
16. NO ELECTRICAL TEST NEEDED.

Drill Table (HOLE SIZES ARE DRILLED SIZE)

Symbol	Count	Hole Size	Plated	Drill Layer Pair
E	68	8.00(0.20)	Plated	METAL 1 TOP - METAL 2 BOT
D	209	15.00(0.38)	Plated	METAL 1 TOP - METAL 2 BOT
C	2	63.00(1.60)	Non-Plated	METAL 1 TOP - METAL 2 BOT
A	12	100.00(2.54)	Plated	METAL 1 TOP - METAL 2 BOT
B	2	120.00(3.05)	Plated	METAL 1 TOP - METAL 2 BOT
	293 Total			

REFERENCE NOTE: Uses QPA2598_CAL-4000[1] CAL SAP No. 291855

* FOR MULTIPLE DRILL PROCESS JOBS SEE: *.DRL, *.DR1, *.DR2, etc.

UNLESS OTHERWISE SPECIFIED: DIMENSIONS ARE IN INCHES

INTERPRET DRAWING PER ANSI/ASME Y14.5 - 2009

THIRD ANGLE PROJECTION

DO NOT SCALE DRAWING

SAP MATERIAL NUMBER: 291847

APPROVAL AND RELEASE RECORDS MAINTAINED IN PDE		DATE
DESIGNER	OMARRUFO	06/20/2019
ENGR.	B.ZHAO	

PDE CONTROLLED

qorvo™

TITLE:
QPA2598 EVALUATION PCB DESIGN PACKAGE

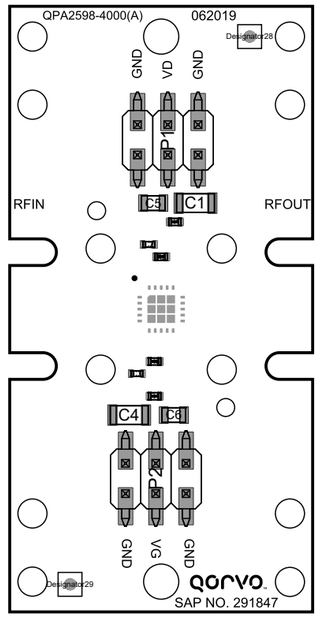
SIZE	DOCUMENT NUMBER:	PROTOTYPE INSTANCE:	REV.
B	QPA2598-4000	N/A	A

SHEET 1 OF 7 | CAD: ALTIUM DESIGNER | SCALE: 2:1

Current Date & Time: 7/24/2019 3:04 PM

SUPPLIER MUST SEND EMAIL TO EVBHOLD@QORVO.COM IF JOB IS PLACED ON HOLD
SUPPLIER SHALL SEND A COPY OF FINAL WORKING GERBERS TO CEADS@QORVO.COM

A STENCIL IS TO BE USED TO ENSURE PROPER COVERAGE OF SOLDER PASTE.



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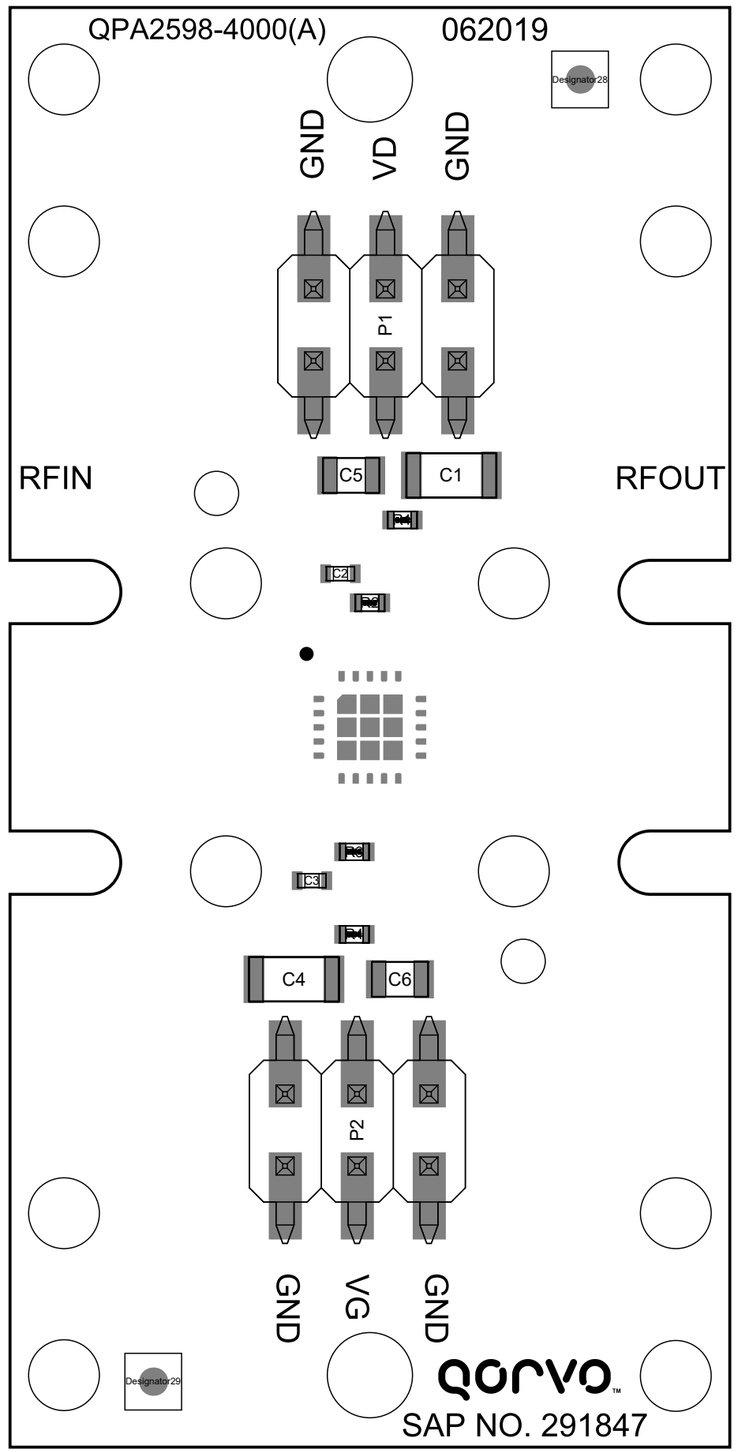
UNLESS OTHERWISE SPECIFIED: DIMENSIONS ARE IN INCHES	SAP MATERIAL NUMBER: 291847		qorvo™
	APPROVAL AND RELEASE RECORDS MAINTAINED IN PDE	DATE	TITLE: QPA2598 EVALUATION PCB DESIGN PACKAGE
	DESIGNER: OMARRUFO	06/20/2019	
	ENGR.: B.ZHAO		
INTERPRET DRAWING PER ANSI/ASME Y14.5 - 2009	PDE CONTROLLED		SIZE: B; DOCUMENT NUMBER: QPA2598-4000; PROTOTYPE INSTANCE: N/A; REV.: A
THIRD ANGLE PROJECTION			SHEET 2 OF 7; CAD: ALTIUM DESIGNER; SCALE: 2:1
DO NOT SCALE DRAWING			

Current Date & Time: 7/24/2019 3:04 PM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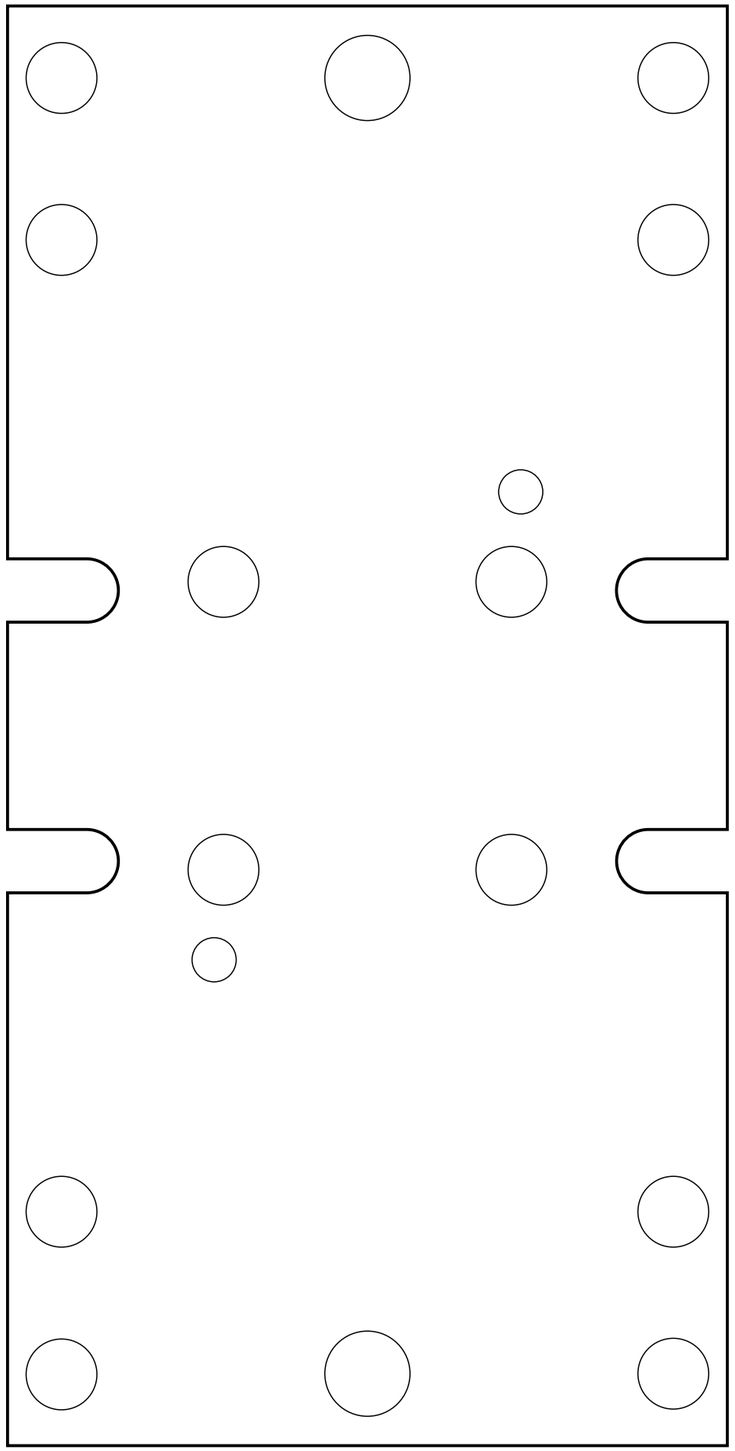
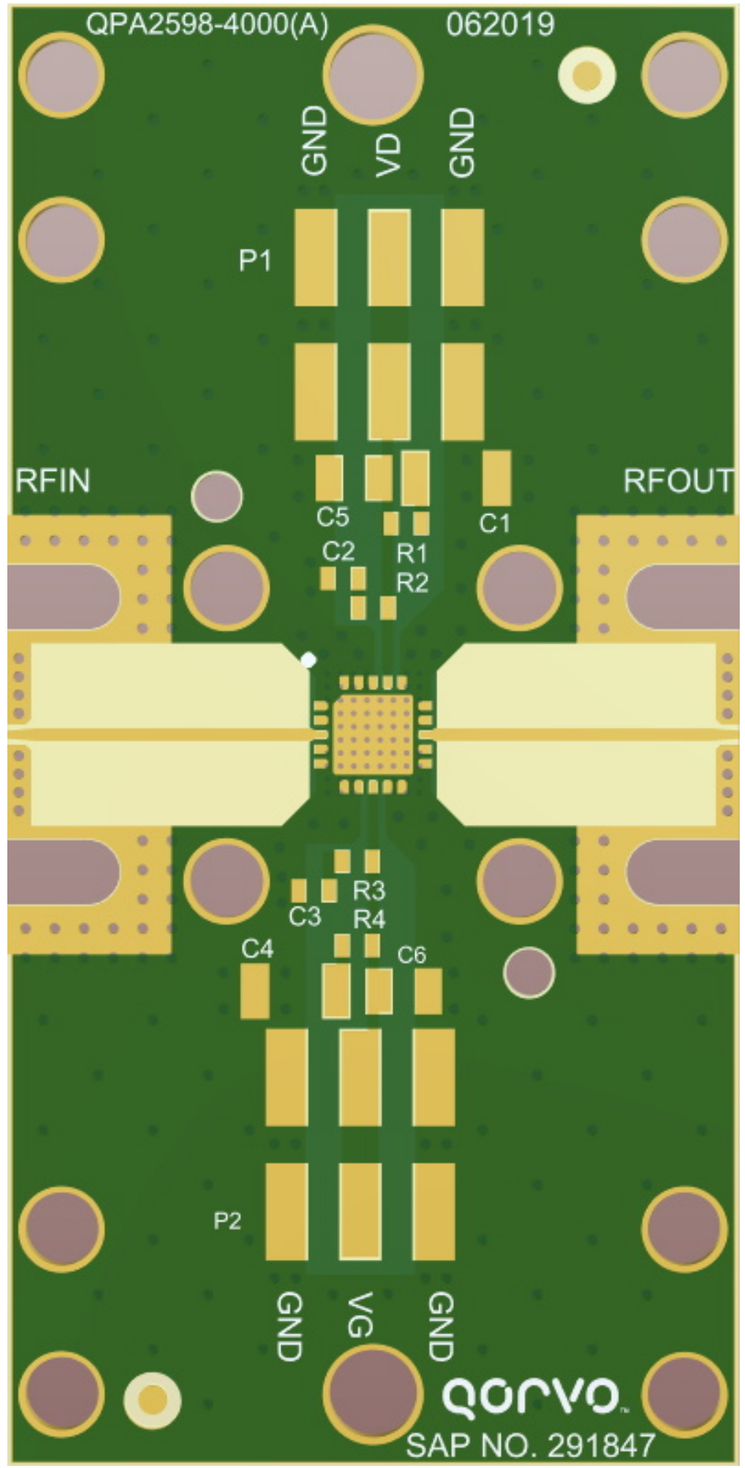
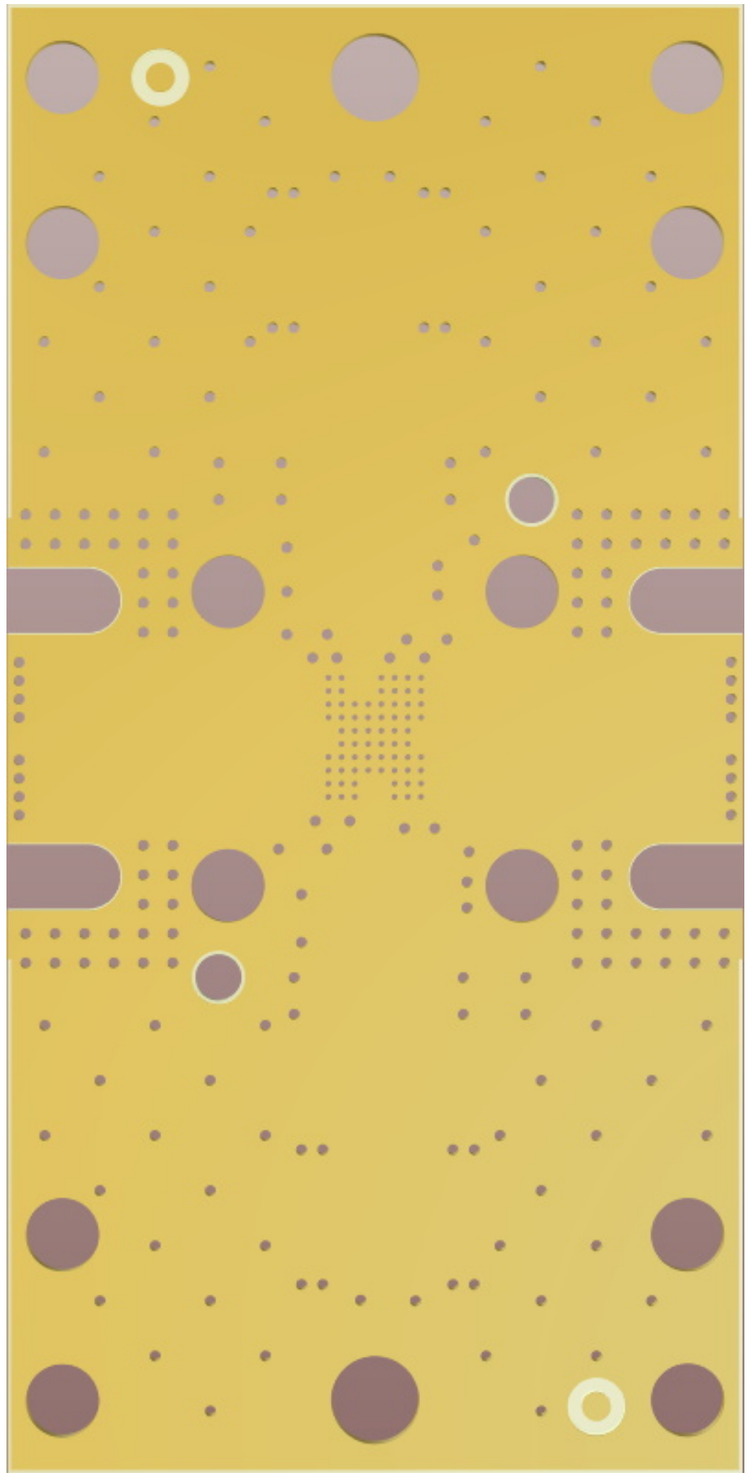
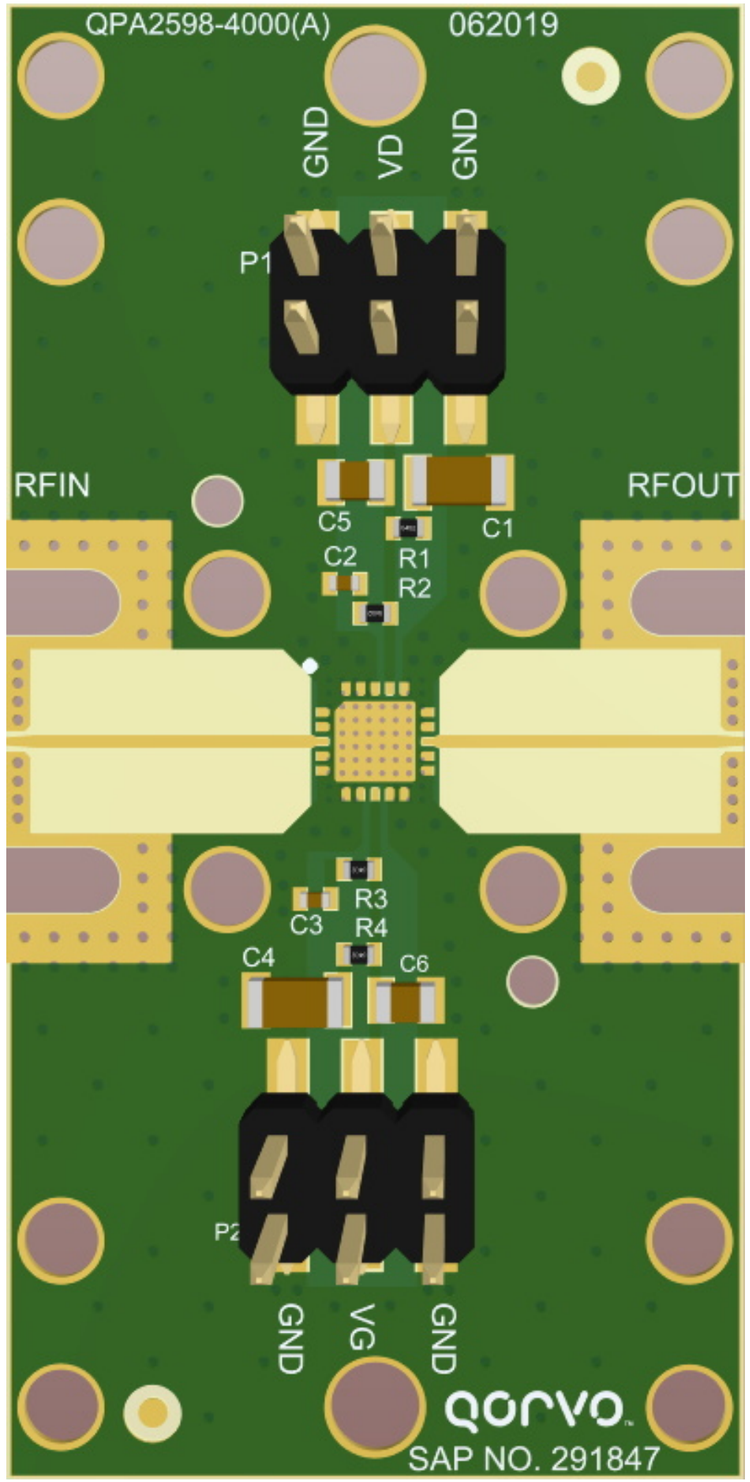
062019
Designator28
GND
VD
GND
P1
RFIN
C5
C1
RFOUT
C2
C3
C4
C6
P2
GND
VG
GND
Designator29
SAP NO. 291847




QPA2598-4000(A)
062019
GND
VD
GND
P1
RFIN
RFOUT
C5
C2
R1
R2
C1
R3
C3
R4
C4
C6
P2
GND
VG
GND
qorvo
SAP NO. 291847




QPA2598-4000(A)
062019
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C2
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R3
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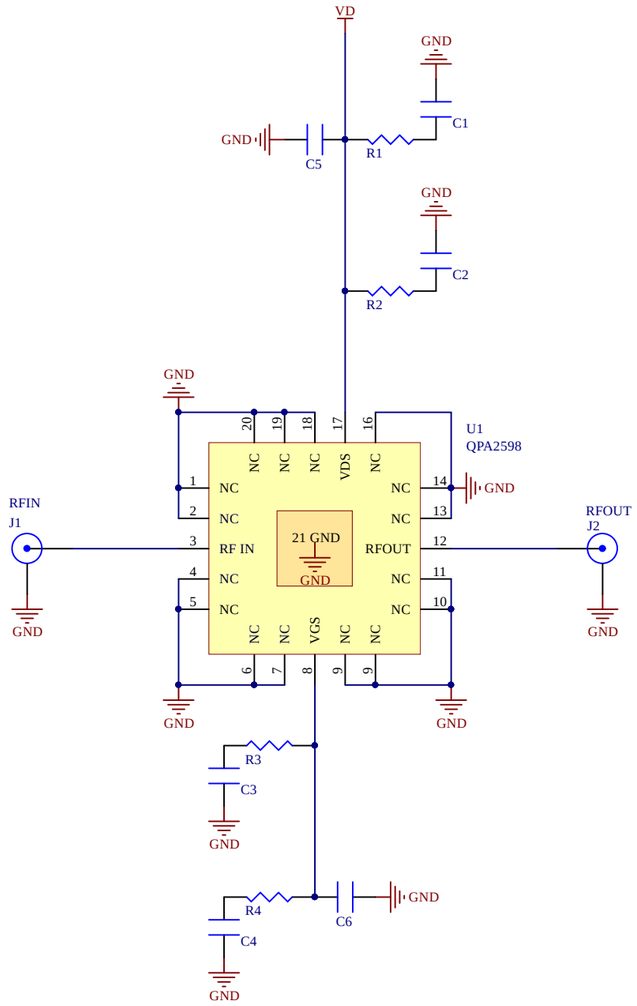
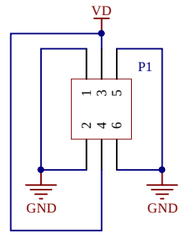
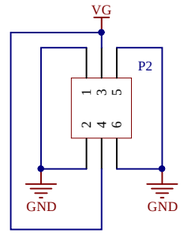
C4
C6
P2
GND
VG
GND
SAP NO. 291847

REVISION HISTORY			
REV	DESCRIPTION	DATE	APPROVAL
A	INITIAL RELEASE	07/24/2019	O.MARRUFO







SAP MATERIAL NUMBER: 291847			
APPROVAL AND RELEASE RECORDS MAINTAINED IN PDE		DATE	
DESIGNER	O.MARRUFO	06/20/2019	
ENGR.	B.ZHAO		
PDE CONTROLLED			

TITLE: QPA2598 EVALUATION PCB DESIGN PACKAGE

SIZE	DOCUMENT NUMBER:	PROTOTYPE INSTANCE:	REV.
B	QPA2598-4000	N/A	A

SCALE: NTS | SHEET 1 OF 1