Guidelines for Using Wafer Level Chip Scale Packaging

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Introduction

This application note is for engineers who design and develop printed circuit boards (PCB) for wafer level chip scale package (WLCSP) devices. These guidelines document the best practices for WLCSP assembly and PCB design to ensure good manufacturing yield and reliable performance. Many factors impact the manufacturing, performance, and reliability of final electronic products, including PCB and solder material selection, manufacturing equipment, and application specification requirements. Therefore, Qorvo encourages you to validate these best practice guidelines through your own product development and qualification process.

Qorvo WLCSP Construction

Qorvo builds its WLCSP devices using several wafer fabrication processes, including aluminum and copper metallization, low-K and non low-K dielectrics, and passivation. It applies the laser marking on the backside of the WLCSP die and attaches the solder balls on the active circuitry side of the die, as shown in Figure 1. The WLCSP device mounts directly to a PCB as shown in Figure 2.

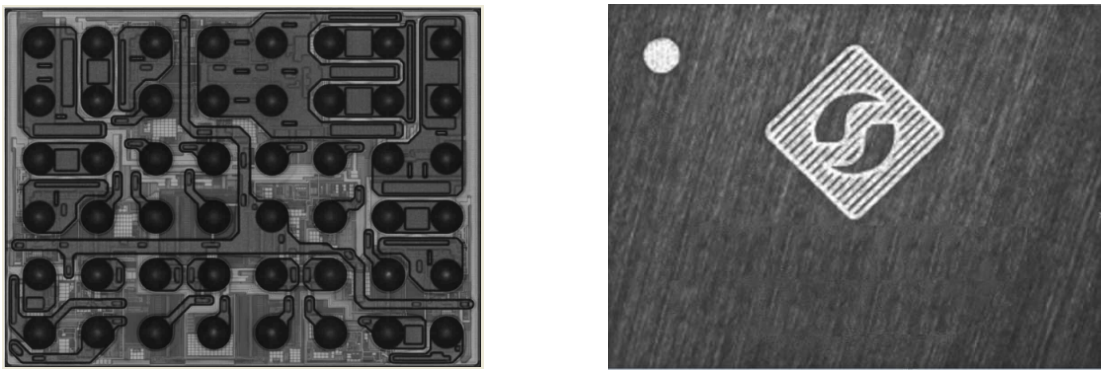

Figure 1: A Qorvo WLCSP ball view (left) and marking/backside w/ pin one locator and a Qorvo (previously Active-Semi) logo view (right)

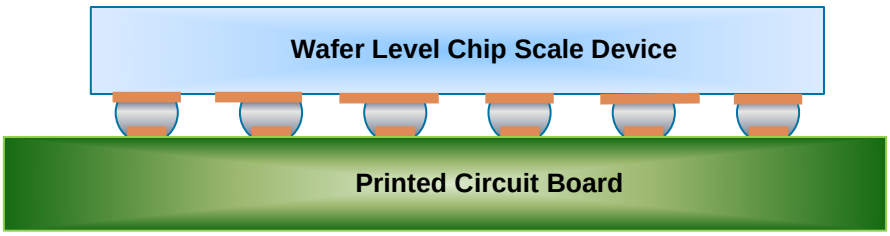

Figure 2: WLCSP Mounted on PCB

WLCSP Configuration

All WLCSP parts from Qorvo, have a standard pitch of 0.5 mm or 0.4 mm. The typical ball diameter, ball height, and silicon thickness dimensions with their tolerances are shown in Table 1.

Dimension	Tolerance	0.5 mm Pitch	0.4 mm Pitch
Bump Diameter	+/- 50 um	270 um	270 um
Bump Height	+/- 25 um	190 um	190 um
Silicon Thickness	+/- 25 um	355 um	355 um
Total Package Height	+/- 50 um	545 um	545 um

Table 1: Qorvo ball mechanical dimensions

All Qorvo solder balls are made with SAC305 (Sn (tin): 96.5%; Ag (silver): 3%; Cu (copper): 0.50%) lead-free (Pb-free) solder alloys.

WLCSP PCB Layout Guidelines

Land Pattern and Solder Mask Design Recommendations

PCB fabrication uses two types of land pad patterns during surface mount assembly (Figure 3).

- Non-solder mask defined (NSMD) – The metal pad on the PCB to which a package ball, pad, or pin attaches is smaller than the solder mask opening. Qorvo recommends customer using Non Solder Mask Defined (NSMD) copper pads design for high density PCB layout.
- Solder mask defined (SMD) – The solder mask opening is smaller than the copper pads.

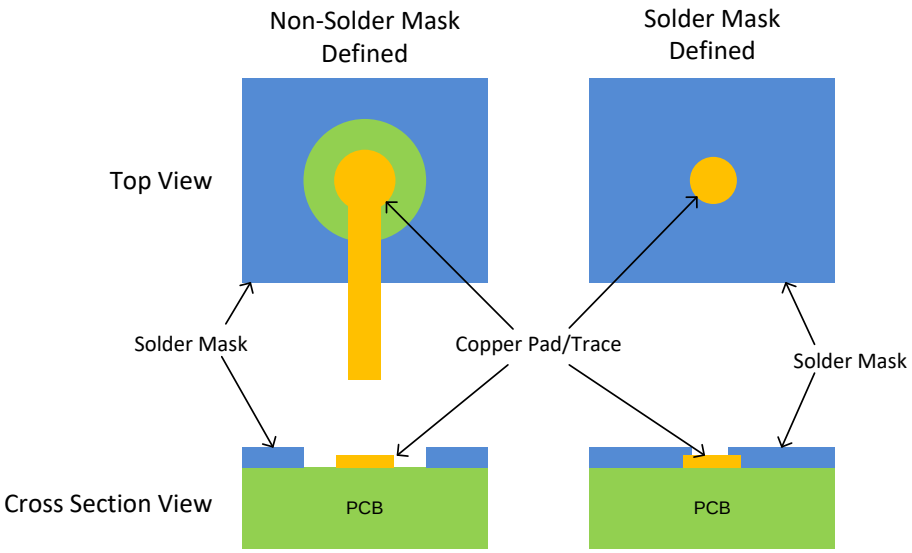

Figure 3: NSMD (left) and SMD (right) Land Patterns

There are two advantages for using NSMD over SMD.

- The copper pad etching process has tighter control than the solder mask opening process. This allows for uniform standoff and final level placement of the device.
- The solder mask opening on NSMD pads is larger than the copper pads, allowing the solder to attach to the sides of the copper pad (as seen in Figure 3) improving the mechanical reliability of the solder joints.

The recommended pad dimensions are shown in Table 2.

Bump Diameter (mm)	Pad Diameter (mm)	Mask Diameter (mm)
0.260 ± 0.05	0.200 ± 0.05	0.300 ± 0.05

Table 2: Recommended Pad Dimensions

There are some disadvantages to NSMD if used in applications requiring underfill or multiple rework operations. In these cases, SMD pads are recommended.

- If underfill is used, the solder mask opening creates moats that allow underfill to deposit between the copper pad and solder mask. This irregular distribution of underfill may introduce stress on the solder mask and the copper trace.
- Depending on the capillary action during the underfilling process, there is potential for underfill voiding at the solder mask opening.
- NSMD pads are prone to peel off after multiple thermal exposures during rework operations.

General Board Design Guildelines

Follow these recommendations for a reliable design:

- Keep the soldermask thickness less than 1 mil (.001in).
- Only use board manufacturers that can maintain a 50 μm +/-5um solder mask opening tolerance on either side of the copper pad.
- For an NSMD pad, keep the trace widths connecting to the pad diameter no more than 60% of the pad diameter.
- The trace routing away from WLCSP device should be balanced in x and y directions to avoid unintentional component movement as a result of unbalanced solder wetting forces.
- Circuit traces routed away from PCB land pads should be no more than 100μm wide in the exposed area inside the solder mask opening. Wider trace widths will reduce device stand-off and impact reliability.
- If the PCB design uses via-in-pad, the via must be filled and plated flat to prevent voiding of the solder joint.
- To achieve higher standoff, the copper layer thickness should be 1/2 oz. (17.5 μm) or less. A copper layer greater than 1 oz. (35 μm) will result in lowering of the effective stand-off, which may compromise solder joint reliability.

Copper Pad Finish

The finish layer on the metal pads has a significant effect on assembly yield and reliability.

- Organic surface preservative (OSP) is recommended as the most appropriate finish for the copper pads. Suggested shelf-life is six months.
- Immersion silver or tin is an acceptable alternative to OSP.
- Electroless nickel immersion gold (ENIG) is acceptable, provided the thickness of gold is limited to 0.02 μm to 0.05 μm to prevent embrittlement.

Board Materials

High-temperature FR4 laminate is preferable to standard FR4 as it enhances package reliability; the coefficient of thermal expansion (CTE) of high-temperature FR4 laminate (12–16 ppm/°C) is lower than that of standard FR4 (14–18 ppm/°C) and is closer to that of silicon (~2.5 ppm/°C).

The actual CTE of a board is design dependent. Numerous factors such as the number of metal layers in the PCB, trace density, laminate material, mounted component's population density, and operating environment affect the thermal expansion. For the greatest reliability,

the PCB laminate glass transition temperature should be above the operating range of the intended application (Tg > 170 °C recommended).

Board Thickness

Board thickness values currently used in the industry range from 0.016 to 0.093 inch (0.4 to 2.3 mm). Thinner boards are more flexible, resulting in greater reliability during thermal cycling and improved thermal fatigue life in comparison to thicker boards.

WLCSP SMT Guidelines

Stencil Design

It is important to follow the stencil design guidelines in IPC-7525 for all assemblies. It is essential to use good-quality stencils to achieve good-quality solder paste printing. Better solder stencil performance can be achieved by using laser-cut or electroformed stencils rather than chemically etched stencils.

For tight pitch components, Qorvo recommends either laser-defined apertures or electroformed stencils, because they give better paste release action and, consequently, provide consistent solder paste volume. The solder stencil opening should be identical for all solder pads in the WLCSP array to prevent unbalanced solder-ball height.

Qorvo recommends the use of X-ray inspection after reflow to ensure proper placement and solder wetting. The process also requires periodic stencil cleaning by solvent during the inline process for consistent paste printing and after every use prior to storage.

Solder Paste

The solder paste printing process transfers solder paste (typically an industry-standard, Pb-free solder paste containing Sn-Ag-Cu) by squeezing the paste over the predefined stencil mask. It is recommended that automated periodic cleaning of the stencil underside is done to improve solder paste volume uniformity and promote better paste release. Avoid manual cleaning, because it will dent and damage the stencil and degrade its paste printing quality.

The best board-level reliability performance occurs when maximum device standoffs exist under the WLCSP. To obtain this, the following practices are recommended:

- Maximize allowable solder paste volume without encountering paste bridging
- Automated optical inspection to monitor solder paste volume uniformity
- No-clean solder paste with a particle size no larger than 40 µm (Type 3)
- No use of solder paste with active or acid-based flux to avoid potential corrosion issues

Package Placement

Typical surface mount pick and place equipment can assemble WLCSP devices to a PCB. WLCSP technology provides robust self-alignment with screen-printed solder paste when the solder ball height is greater than 0.15 mm. When the solder ball standoff is less than 0.15 mm, more caution is required for self-alignment. The proper ratio between the pick and place tool/nozzle and the package size must be observed at a minimum of 80 percent to provide a uniform distribution of stress on the package during pick and placement.

During component pickup from carrier tape, we recommend using a Z-height distance between the WLCSP and the pickup tool. The vacuum pressure should be set at approximately 60 to 70 kpa to lift the WLCSP from the pocket of the carrier tape. This practice prevents direct contact and mechanical over-stress on the WLCSP during pickup. Set the Z-height distance between the WLCSP and the pickup tool to zero or with a minimal gap.

Recommendations concerning placement force of the WLCSP on the PCB for the best success are as follows:

- On equipment without component force adjustments, the Z placement height should be set to avoid overdriving the board location. Optimally, the Z height should be set at one-half the printed solder paste height.
- On equipment with component force adjustments, each solder ball is manufactured to withstand a load force of 35 grams (35 grams/bump). Minimize force on the device by using less than 35 grams/bump. Exceeding 35 grams/bump may reduce reliability because of excessive mechanical stress on the device that causes topside damage on the surface of the WLCSP.
- During component transfer via conveyor, there is a possibility of component displacement or skewing prior to reflow. Optimize conveyor speed and transfer to avoid jerking and fast motion. If the process requires realignment of the package on the board prior to reflow, do not use metal tweezers to correct the component placement. Instead, use a soft tool such as a rubber tipped vacuum pen or equivalent.
- Place local fiducials near the WLCSP device in addition to the board level fiducials to provide for accurate placement.

Reflow

All Qorvo WLCSP devices are 100 percent Pb free (Sn-Ag-Cu). Therefore, Pb-free solder paste with a Pb-free reflow profile is recommended. For the standard application, we recommend the following:

- For an improved soldering response, use a reflow furnace with a nitrogen purge that has an oxygen content below 50 ppm.
- Determine the actual reflow temperatures based on thermal loading effect measurements within the furnace, including the complexity of the components on the board and the board size and thickness. Well-constructed profiling tools must be available to achieve accurate temperature settings.

- For Pb-free (Sn-Ag-Cu or Sn-Ag) solder, the reflow profile is critical. The Sn-Ag-Cu solder alloy melts at ~220 °C. The reflow temperature peak at joint level should be from 15 to 20 °C higher than the melting temperature. Higher reflow temperatures than the qualified temperature can cause delamination and solder joint issues within the package. See Table 3 for more details about maximum reflow temperature.

Process Step	Lead-Free Solder
Ramp rate	3 °C/second
Preheat	150 to 180 °C @ 60 to 180 sec
Time above melting point of solder (~220 °C)	30 to 90 seconds
Peak temperature	255 °C ±5 °C
Time within 5 °C of peak temperature	10 to 20 seconds
Ramp-down rate	Maximum 6 °C/second

Table 3: Recommended Reflow Parameters for Sn-Ag-Cu Paste

- Dwell time in the soldering zone (with temperatures higher than 220 °C) must be kept as short as possible to prevent component and substrate damage. The peak temperature must not exceed 260 °C. Use a controlled atmosphere (N2 or N2H2) during the reflow, especially above 150 °C.

- To avoid any cleaning operation, use a no-clean flux.

- All of Qorvo's WLCSPs are qualified at 260 °C reflow with MSL1. Typical temperature profiles for the Pb-free (Sn-Ag-Cu or Sn-Ag) solder and the corresponding critical reflow parameters are shown in Figure 4 and Table 3.

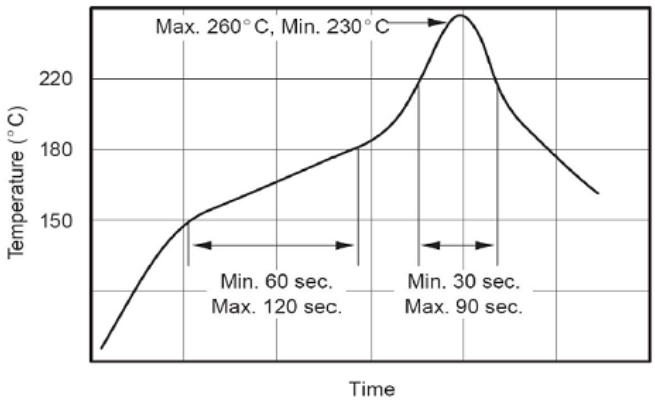

Figure 4: Recommended Reflow Profile for Sn-Ag-Cu Paste

- Ramp-down must not be abrupt and should not exceed the recommended rate to avoid potential UBM cracking due to thermal shock as the parts move out of the reflow oven and into room temperature. Similarly, avoid the installation of high-speed air ionizers at the exit of the reflow oven as they introduce thermal shock to the WLCSP device.

- A good quality solder joint occurs when the solder wets the entire solder pad from the WLCSP solder ball, which makes the surface of the joint smooth and the shape of the solder ball symmetrical. Solder joint inspection after reflow can be done with X-ray to monitor defects such as uniform appearance, bridging, open circuits, and voids. Voids in the solder joint after reflow can occur during the reflow process when the reflow profile is not properly tuned based on the recommended profile. A common failure associated with a poor reflow process and oxidation is a head-in-pillow effect. Proper storage and handling of the WLCSP solder ball and reflow profile optimization can eliminate this source of failure.

References:

- Unisem, "*PCB Land Pattern Design and SMT Process Guideline for WLCSP*"

- Amkor Technology, "*Application Note for Surface Mount Assembly of Amkor's Eutectic and Lead-Free CSPnl™ Wafer Level Chip Scale Packages*."

- Cypress Semiconductor, app note AN69061, "*Design Manufacturing and Handling Guidelines for Cypress Wafer Level Chip Scale Packages.*"

Contact Information

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