APPLICATION NOTE AN-114

ACT88430 Register Definitions – CMI 101

Abstract

This application note identifies and explains the ACT88430 internal registers that help make this IC flexible and configurable for many applications. It provides a short description of each register, its individual bits, their function, and default values. The default register settings in this application note are only valid for the ACT88430VM101. Refer to each datasheet for each specific IC's functional differences from the settings in this document.

Introduction

The ACT88430 is an ActivePMU™ power management unit from Qorvo. It is designed to power a wide range of processors, FPGA's, peripherals, and microcontrollers. The ACT88430 core includes four DC/DC step down converters using integrated power FETs and three LDOs. Each of these regulators can be configured for a wide range of output voltages through the I^2C interface.

Today's applications require more complexity in their startup and sequencing requirements. The ACT88430 I^2C registers allow for customized configurations for these requirements. Although the ACT88430 is programmed at the factory with a default configuration, these settings can be changed through the I^2C interface to provide customized configurations optimized for a specific processor and/or end application. IC configurability includes many options such as output voltage, startup sequencing, startup timing, slew rates, GPIO configuration, fault responses, and more. Qorvo identifies these configurations with a Code Matrix Index, CMI. An IC's CMI is identified by the last three digits at the end of the orderable part number. Note that this application note is specific to the ACT88430's CMI 101. Refer to the datasheet for the specific changes to other CMI versions.

Register Types

The ACT88430 ICs contain the following register types.

Basic Volatile - Customer R/W (Read and Write) and RO (Read only). The customer can modify these register values to change IC functionality. Any changes to these registers are lost when power is recycled. The default values are fixed and cannot be changed.

Basic Non-Volatile - Customer R/W and RO. The customer can modify these register values to change IC functionality. Any changes to these registers are lost when power is recycled. The default values can be modified at the factory to optimize IC functionality for specific applications. Please consult Sales@Qorvo.com for custom options and minimum order quantities.

Factory Non-Volatile – Factory bits. These bits are used by the factory to set IC functionality. The customer can read these bits but cannot write to them. The default values can be modified at the factory to optimize IC functionality for specific applications.

The ACT88430 contains seven major register spaces.

Master (or System) Reg	0x00h to 0x0Ah
Buck1 Reg	0x30h to 0x36h
Buck2 Reg	0x40h to 0x46h
Buck3 Reg	0x50h to 0x56h
Buck4 Reg	0x60h to 0x66h
LDO1 Reg	0x70h to 0x74h
Current Limit Reg	0x79h to 0x7Ch
LDO2 Reg	0x80h to 0x84h
LDO3 Reg	0x88h to 0x8Ch

Register Map Overview

The following table shows an overview of the ACT88430 register map. Note that not all register addresses are sequential.

ADDR(HEX)	7	6	5	4	3	2	1	0
	Master (or System) Registers							
00	nRESET_AUX1_MASK	nRESET_AUX2_MASK	nRESET_MASK	RFU	POK_nMASK	IRQ_nMASK	DVS_EN	PWREN_EN
01	RFU[5:0]						SLP_ENTR	RFU
02	CURRENT_STATE[2:0]			PWREN_STAT	TSD_SHUTDWN	TSD_ALERT	POK_OV	POK_UV
03	RFU[5:0]						GPIO_STAT	MODE_STAT
04	RFU	ILIM_REG[6]	ILIM_REG[5]	ILIM_REG[4]	ILIM_REG[3]	ILIM_REG[2]	ILIM_REG[1]	ILIM_REG[0]
05	RFU	OV_REG[6]	OV_REG[5]	OV_REG[4]	OV_REG[3]	OV_REG[2]	OV_REG[1]	OV_REG[0]
06	FACTORY	UV_REG[6]	UV_REG[5]	UV_REG[4]	UV_REG[3]	UV_REG[2]	UV_REG[1]	UV_REG[0]
07	DO NOT USE							
08	nRST_DLY[2:0]			POK_SET[1:0]		EXT_EN_POL	PWR_DN_MODE	PWR_DN_POL
09	nRESET_AUX1_EN	nRESET_AUX1_L2_EN		nRESET_AUX1_DLY[2:0]			nRESET_AUX2_DLY[2:0]	
0A	EXT_PG_SEL	EN_B4_L3_PWREN	VIN_OV_MASK	TSD_nMASK	UV_nMASK	OV_nMASK	nRESET_AUX1_PD	EXT_PG_POL
	Buck1 Registers							
30	PWR_GOOD	OV	ILIM	RFU	nRESET_FLTMSK	ILIM_FLTMSK	UV_FLTMSK	OV_FLTMSK
31	VSET0[7:0]							
32	VSET1[7:0]							
33	ON	PBINEN	QLTCH	SLEEPEN	DREN		SS_RAMP[2:0]	
34	MODE	RST		DBQL[2:0]			DBOK[2:0]	
35	DBON[3:0]				SLEW[1:0]		DBSTBY[1:0]	
36	PHASE_DELAY	PHASE	FORCE_PWM	ONDLY[2:0]			DRVADJ[1:0]	
	Buck2 Registers							
40	PWR_GOOD	OV	ILIM	RFU	nRESET_FLTMSK	ILIM_FLTMSK	UV_FLTMSK	OV_FLTMSK
41	VSET0[7:0]							
42	VSET1[7:0]							
43	ON	PBINEN	QLTCH	SLEEPEN	DREN		SS_RAMP[2:0]	
44	MODE	RST		DBQL[2:0]			DBOK[2:0]	
45	DBON[3:0]				SLEW[1:0]		DBSTBY[1:0]	
46	PHASE_DELAY	PHASE	FORCE_PWM	ONDLY[2:0]			DRVADJ[1:0]	
	Buck3 Registers							
50	PWR_GOOD	OV	ILIM	RFU	nRESET_FLTMSK	ILIM_FLTMSK	UV_FLTMSK	OV_FLTMSK
51	VSET0[7:0]							
52	VSET1[7:0]							
53	ON	PBINEN	QLTCH	SLEEPEN	DREN		SS_RAMP[2:0]	
54	MODE	RST		DBQL[2:0]			DBOK[2:0]	
55	DBON[3:0]				SLEW[1:0]		DBSTBY[1:0]	
56	PHASE_DELAY	PHASE	FORCE_PWM	ONDLY[2:0]			DRVADJ[1:0]	
	Buck4 Registers							
60	PWR_GOOD	OV	ILIM	RFU	nRESET_FLTMSK	ILIM_FLTMSK	UV_FLTMSK	OV_FLTMSK
61	VSET0[7:0]							
62	VSET1[7:0]							
63	ON	PBINEN	QLTCH	SLEEPEN	DREN		SS_RAMP[2:0]	
64	MODE	RST		DBQL[2:0]			DBOK[2:0]	
65	DBON[3:0]				SLEW[1:0]		DBSTBY[1:0]	
66	PHASE_DELAY	PHASE	FORCE_PWM	ONDLY[2:0]			DRVADJ[1:0]	
	LDO1 Registers							
70	PWR_GOOD	OV	ILIM	RFU	nRESET_FLTMSK	ILIM_FLTMSK	UV_FLTMSK	OV_FLTMSK
71	RFU	VSET0[6:0]						
72	ON	PBINEN	QLTCH	SLEEPEN	DREN	SEL_REF0P8_BUCK2	SS_RAMP[1:0]	
73	MODE	RST		DBQL[2:0]			DBOK[2:0]	
74	DBON[3:0]				ONDLY[2:0]			SEL_REF0P8_BUCK1
	Current Limit Registers							
79	B1_ILIMSET[1:0]		B2_ILIMSET[1:0]		B3_ILIMSET[1:0]		B4_ILIMSET[1:0]	
7A	L1_ILIMSET[1:0]		L2_ILIMSET[1:0]		L3_ILIMSET[1:0]		RFU	EN_PUSH_PULL_IO8
7B	B4_LSASYNC	B3_LSASYNC	B2_LSASYNC	B1_LSASYNC	B4_LP_MODE	B3_LP_MODE	B2_LP_MODE	B1_LP_MODE
7C	B4_HalfFreq	B3_HalfFreq	B2_HalfFreq	B1_HalfFreq	B4_DISLPM	B3_DISLPM	B2_DISLPM	B1_DISLPM
	LDO2 Registers							
80	PWR_GOOD	OV	ILIM	RFU	RFU	ILIM_FLTMSK	UV_FLTMSK	OV_FLTMSK
81	RANGE_LDO2	RANGE_LDO3	VSET0[5:0]					
82	ON	PBINEN	QLTCH	SLEEPEN	DREN	RFU	SS_RAMP[1:0]	
83	MODE	RST		DBQL[2:0]			DBOK[2:0]	
84	DBON[3:0]				ONDLY[2:0]			RFU
	LDO3 Registers							
88	PWR_GOOD	OV	ILIM	RFU	nRESET_FLTMSK	ILIM_FLTMSK	UV_FLTMSK	OV_FLTMSK
89	SEL_REF0P8_BUCK3	RFU	VSET0[5:0]					
8A	ON	PBINEN	QLTCH	SLEEPEN	DREN	SS_BIAS_ING	SS_RAMP[1:0]	
8B	MODE	RST		DBQL[2:0]			DBOK[2:0]	
8C	DBON[3:0]				ONDLY[2:0]			RFU

MSTR00 - Master Configuration Register

Address = 0x00h	Default = 0x00h	Type = Basic Volatile

BIT	7	6	5	4	3	2	1	0
Name	nRESET_AUX1_MASK	nRESET_AUX2_MASK	nRESET_MASK	RFU	POK_nMASK	IRQ_nMASK	DVS_EN	PWREN_EN
Default	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Name	Description	Notes
nRESET_AUX1_MASK	0 - Unmasks nRESET_AUX1 output 1 - Masks nRESET _AUX1 output	When masked, nRESET_AUX1 will not be asserted low when its associated power supplies drop out of regulation.
nRESET_AUX2_MASK	0 - Unmasks nRESET _AUX2 output 1 - Masks nRESET _AUX2 output	When masked, nRESET_AUX2 will not be asserted low when its associated power supplies drop out of regulation.
nRESET_MASK	0 - Unmasks nRESET output 1 - Masks nRESET output	When masked, nRESET will not be asserted low when its associated power supplies drop out of regulation.
RFU	Reserved for Future Use	Do not change this register value. Changing the register value can affect IC functionality.
POK_nMASK	0 - Masks POK output 1 – Unmasks POK output	To enable the POK output pin, POK_nMASK must be set high
IRQ_nMASK	0 - Masks output of IRQ 1 – Unmasks output of IRQ	When IRQ_nMASK=0, IRQ function is masked and IRQ pin can not provide interrupt output. When IRQ_nMASK=1, IRQ function is unmasked and IRQ pin can provide interrupt output.
DVS_EN	0 - Disables EXT_PG pin function 1 - Enables EXT_PG pin function	Function of this bit is disabled in CMI 101. If user want to mask function of EXT_PG pin at start up, Qorvo can enable function of this bit by CMI change. .
PWREN_EN	0 – Diasble PWREN pin function mode. 1 – Enables PWREN pin function	Function of this bit is disabled in CMI 101. If user want to mask function of PWREN pin at start up, Qorvo can enable function of this bit by CMI change.

MSTR01 - Master Configuration Register

Address = 0x01h	Default = 0x00h	Type = Basic Volatile

BIT	7	6	5	4	3	2	1	0
Name	RFU[5:0]						SLP_ENTR	RFU
Default	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Name	Description	Notes
RFU[5:0]	Reserved for Future Use	Do not change this register value. Changing the register value can affect IC functionality.
SLP_ENTR	0 – normal operation 1 – Puts the IC into Sleep mode	This bit must be enabled by PWREN_MODE and PWREN_EN . SLEEP mode is not available in CMI 101.
RFU	Reserved for Future Use	Do not change this register value. Changing the register value can affect IC functionality.

MSTR02 - Master Configuration Register

Address = 0x02h	Default = 0x00h	Type = Basic Volatile

BIT	7	6	5	4	3	2	1	0
Name	CURRENT_STATE[2:0]			PWREN_STAT	TSD_SHUTDWN	TSD_ALERT	POK_OV	POK_UV
Default	000			0	0	0	0	0
Access	RO			RO	RO	RO	RO	RO

Name	Description	Notes
CURRENT_STATE[2:0]	000: RESET - Info only 001: ACTIVE 010: SLEEP – Info only 100: THERMAL - Info only 101: OVUVFLT - Info only	Provides the current state of the ACT88430 internal state machine. Note that the register can only be read when the IC is in ACTIVE mode.
PWREN_STAT	0 – PWREN pin is not asserted 1 – PWREN pin is asserted	Note that this bit identifies whether or not the input pin is asserted. The I2C bit PWREN_POL determines if the input is asserted high or low.
TSD_SHUTDWN	0 – IC temperature is below the thermal shutdown temperature 1 – IC temperature is above the thermal shutdown temperature	If TSD_nMASK = 0, it provides real time status of overtemperature fault status. If TSD_nMASK = 1, it latches a 1 when overtemperature is exceeded until the bit is read via I2C.
TSD_ALERT	0 – IC temperature is below the thermal warn temperature 1 – IC temperature is above the thermal warn temperature	If IRQ_nMASK = 0, it provides real time status of the temperature warn. If IRQ_nMASK = 1, it latches a 1 when an overtemperature warn is exceeded until the bit is read via I2C.
POK_OV	0 – VIN voltage is below the POK_OV threshold 1 - VIN voltage is above the POK_OV threshold	If POK_nMASK = 0, it provides real-time status of POK_OV. If POK_nMASK = 1, it latches a 1 when POK_OV is tripped until the bit is read via I2C.
POK_UV	0 – VIN voltage is above the POK_UV threshold 1 - VIN voltage is below the POK_UV threshold	If POK_nMASK = 0, it provides real-time status of POK_OV. If POK_nMASK = 1, it latches a 1 when POK_UV is tripped until the bit is read via I2C.

MSTR03 - Master Configuration Register

Address = 0x03h	Default = 0x00h	Type = Basic Volatile

BIT	7	6	5	4	3	2	1	0
Name	RFU[5:0]						GPIO_STAT	MODE_STAT
Default	000000						0	0
Access	RO						R/W	R/W

Name	Description	Notes
RFU[5:0]	Reserved for Future Use	Do not change this register value. Changing the register value can affect IC functionality.
GPIO_STAT	0 – GPIO pin is a logic low 1 – GPIO pin is a logic high	
MODE_STAT	0 – MODE pin is a logic low 1 – MODE pin is a logic high	

MSTR04 - Master Configuration Register

Address = 0x04h	Default = 0x00h	Type = Basic Volatile

BIT	7	6	5	4	3	2	1	0
Name	RFU	ILIM_REG[6]	ILIM_REG[5]	ILIM_REG[4]	ILIM_REG[3]	ILIM_REG[2]	ILIM_REG[1]	ILIM_REG[0]
Default	0	0	0	0	0	0	0	0
Access	RO	RO	RO	RO	RO	RO	RO	RO

Name	Description	Notes
RFU	Reserved for Future Use	Do not change this register value. Changing the register value can affect IC functionality.
ILIM_REG[6]	0 - LDO3 not detected current limit. 1 - LDO3 detected current limit.	This is the latched version of LDO3_ILIMSET overcurrent threshold. Overcurrent threshold set by LDO3_ILIMSET. Asserts IRQ unless IRQ is masked. This bit is latched until read via I2C.
ILIM_REG[5]	0 – LDO2 not detected current limit. 1 – LDO2 detected current limit.	This is the latched version of LDO2_ILIMSET overcurrent threshold. Overcurrent threshold set by LDO2_ILIMSET. Asserts IRQ unless IRQ is masked. This bit is latched until read via I2C.
ILIM_REG[4]	0 – LDO1 not detected current limit. 1 – LDO1 detected current limit.	This is the latched version of LDO1_ILIMSET overcurrent threshold. Overcurrent threshold set by LDO1_ILIMSET. Asserts IRQ unless IRQ is masked. This bit is latched until read via I2C.
ILIM_REG[3]	0 – Buck4 not detected current limit. 1 – Buck4 detected current limit.	This is the latched version of BUCK4_ILIMSET overcurrent threshold. Overcurrent threshold set by BUCK4_ILIMSET. Asserts IRQ unless IRQ is masked. This bit is latched until read via I2C.
ILIM_REG[2]	0 – Buck3 not detected current limit. 1 – Buck3 detected current limit.	This is the latched version of BUCK3_ILIMSET overcurrent threshold. Overcurrent threshold set by BUCK3_ILIMSET. Asserts IRQ unless IRQ is masked. This bit is latched until read via I2C.
ILIM_REG[1]	0 – Buck2 not detected current limit. 1 – Buck2 detected current limit.	This is the latched version of BUCK2_ILIMSET overcurrent threshold. Overcurrent threshold set by BUCK2_ILIMSET. Asserts IRQ unless IRQ is masked. This bit is latched until read via I2C.

ILIM_REG[0]	0 – Buck1 not detected current limit. 1 – Buck1 detected current limit.	This is the latched version of BUCK1_ILIMSET overcurrent threshold. Overcurrent threshold set by BUCK1_ILIMSET. Asserts IRQ unless IRQ is masked. This bit is latched until read via I2C.

MSTR05 - Master Configuration Register

Address = 0x05h	Default = 0x00h	Type = Basic Volatile

BIT	7	6	5	4	3	2	1	0
Name	RFU	OV_REG[6]	OV_REG[5]	OV_REG[4]	OV_REG[3]	OV_REG[2]	OV_REG[1]	OV_REG[0]
Default	0	0	0	0	0	0	0	0
Access	RO	RO	RO	RO	RO	RO	RO	RO

Name	Description	Notes
RFU	Reserved for Future Use	Do not change this register value. Changing the register value can affect IC functionality.
OV_REG[6]	0 - LDO3 not detected overvoltage. 1 - LDO3 detected overvoltage.	Asserts IRQ unless IRQ is masked. When high, this bit forces the IC into the OVUVFLT mode unless OV_nMASK = 0. This bit is latched until read via I2C.
OV_REG[5]	0 – LDO2 not detected overvoltage. 1 – LDO2 detected overvoltage.	Asserts IRQ unless IRQ is masked. When high, this bit forces the IC into the OVUVFLT mode unless OV_nMASK = 0. This bit is latched until read via I2C.
OV_REG[4]	0 – LDO1 not detected overvoltage. 1 – LDO1 detected overvoltage.	Asserts IRQ unless IRQ is masked. When high, this bit forces the IC into the OVUVFLT mode unless OV_nMASK = 0. This bit is latched until read via I2C.
OV_REG[3]	0 – Buck4 not detected overvoltage. 1 – Buck4 detected overvoltage.	Asserts IRQ unless IRQ is masked. When high, this bit forces the IC into the OVUVFLT mode unless OV_nMASK = 0. This bit is latched until read via I2C.
OV_REG[2]	0 – Buck3 not detected overvoltage. 1 – Buck3 detected overvoltage.	Asserts IRQ unless IRQ is masked. When high, this bit forces the IC into the OVUVFLT mode unless OV_nMASK = 0. This bit is latched until read via I2C.
OV_REG[1]	0 – Buck2 not detected overvoltage. 1 – Buck2 detected overvoltage.	Asserts IRQ unless IRQ is masked. When high, this bit forces the IC into the OVUVFLT mode unless OV_nMASK = 0. This bit is latched until read via I2C.
OV_REG[0]	0 – Buck1 not detected overvoltage. 1 – Buck1 detected overvoltage.	Asserts IRQ unless IRQ is masked. When high, this bit forces the IC into the OVUVFLT mode unless OV_nMASK = 0. This bit is latched until read via I2C.

MSTR06 - Master Configuration Register

Address = 0x06h	Default = 0x00h	Type = Basic Volatile

BIT	7	6	5	4	3	2	1	0
Name	RFU	UV_REG[6]	UV_REG[5]	UV_REG[4]	UV_REG[3]	UV_REG[2]	UV_REG[1]	UV_REG[0]
Default	0	0	0	0	0	0	0	0
Access	RO	RO	RO	RO	RO	RO	RO	RO

Name	Description	Notes
RFU	Reserved for Future Use	Do not change this register value. Changing the register value can affect IC functionality.
UV_REG[6]	0 - LDO3 not detected undervoltage. 1 - LDO3 detected undervoltage.	This is the inverted LDO3 PWR_GOOD signal. Asserts IRQ unless IRQ is masked. When high, this bit forces the IC into the OVUVFLT mode unless UV_nMASK = 0. This bit is latched until read via I2C.
UV_REG[5]	0 – LDO2 not detected undervoltage. 1 – LDO2 detected undervoltage.	This is the inverted LDO2 PWR_GOOD signal. When high, this bit forces the IC into the OVUVFLT mode unless UV_nMASK = 0. Asserts IRQ unless IRQ is masked. This bit is latched until read via I2C.
UV_REG[4]	0 – LDO1 not detected undervoltage. 1 – LDO1 detected undervoltage.	This is the inverted LDO1 PWR_GOOD signal. When high, this bit forces the IC into the OVUVFLT mode unless UV_nMASK = 0. Asserts IRQ unless IRQ is masked. This bit is latched until read via I2C.
UV_REG[3]	0 – Buck4 not detected undervoltage. 1 – Buck4 detected undervoltage.	This is the inverted BUCK4 PWR_GOOD signal. When high, this bit forces the IC into the OVUVFLT mode unless UV_nMASK = 0. Asserts IRQ unless IRQ is masked. This bit is latched until read via I2C.
UV_REG[2]	0 – Buck3 not detected undervoltage. 1 – Buck3 detected undervoltage.	This is the inverted BUCK3 PWR_GOOD signal. When high, this bit forces the IC into the OVUVFLT mode unless UV_nMASK = 0. Asserts IRQ unless IRQ is masked. This bit is latched until read via I2C.
UV_REG[1]	0 – Buck2 not detected undervoltage. 1 – Buck2 detected undervoltage.	This is the inverted BUCK2 PWR_GOOD signal. When high, this bit forces the IC into the OVUVFLT mode unless UV_nMASK = 0. Asserts IRQ unless IRQ is masked. This bit is latched until read via I2C.
UV_REG[0]	0 – Buck1 not detected undervoltage. 1 – Buck1 detected undervoltage.	This is the inverted BUCK1 PWR_GOOD signal. When high, this bit forces the IC into the OVUVFLT mode unless UV_nMASK = 0. Asserts IRQ unless IRQ is masked. This bit is latched until read via I2C.

MSTR08 - Master Configuration Register

Address = 0x08h	Default = 0xE8h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	nRST_DLY[2:0]			POK_SET[1:0]		EXT_EN_POL	PWR_DN_MODE	PWR_DN_POL
Default	111			01		0	0	0
Access	R/W			R/W		R/W	R/W	R/W

Name	Description		Notes
nRST_DLY[2:0]	000 = 199us 001 = 313us 010 = 427us 011 = 540us 100 = 654us 101 = 768us 110 = 57us 111 = 996us		Sets the nRESET delay time.
POK_SET[1:0]	3.3V Input Setting (VIN_LVL=0)	5V Input Setting (VIN_LVL=1, VIN_FULL_RANGE = 0)	Sets the POK_UV threshold. VIN_LVL and VIN_FULL_RANGE bits determine which table POK_UV uses. They are in a Factory register and are not user accessible. VIN_LVL = 1 and VIN_FULL_RANGE=0 for CMI 101.
	00 = 91% of 3.3V (3.00V) 01 = 88% of 3.3V (2.90V) 10 = 84% of 3.3V (2.77V) 11 = Disable POK_UV	00 = 88% of 5V (4.40V) 01 = 86% of 5V (4.30V) 10 = 84% of 5V (4.20V) 11 = Disable POK_UV	
EXT_EN_POL	0 – Sets EXT_EN polarity to active high 1 – Sets EXT_EN polarity to active low		
PWREN_MODE	0 – Enables putting IC into Sleep mode via the PWREN pin 1 – Enables putting IC into Sleep mode via SLP_ENTR register		Sleep mode is disabled in CMI 101. Changing the value of this bit may result in unexpected IC behavior.
PWREN_POL	0 – Sets polarity of PWREN pin to active high 1 – Sets polarity of PWREN pin to active low		

MSTR09 - Master Configuration Register

Address = 0x09h	Default = 0x3Fh	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	nRESET_AUX1_EN	nRESET_AUX1_L2_EN	nRESET_AUX1_DLY[2:0]			nRESET_AUX2_DLY[2:0]		
Default	0	0	111			111		
Access	R/W	R/W	R/W			R/W		

Name	Description	Notes
nRESET_AUX1_EN	0 – Disables the nRESET_AUX1 output 1 – nRESET_AUX1 functions normally	
nRESET_AUX1_L2_EN	0 – LDO2 POK status does not affect the nRESET_AUX1 output 1 – LDO2 POK status is used as the input trigger to start the nRESET_AUX1 timer.	
nRESET_AUX1_DLY[2:0]	000 = 398us 001 = 626us 010 = 853us 011 = 1081us 100 = 1308us 101 = 1536us 110 = 1764us 111 = 1991us	Sets the nRESET_AUX1 _DLY delay time.
nRESET_AUX2_DLY[2:0]	000 = 199us 001 = 313us 010 = 427us 011 = 540us 100 = 654us 101 = 768us 110 = 882us 111 = 57us	Sets the nRESET_AUX2 _DLY delay time.

MSTR0A - Master Configuration Register

Address = 0x0Ah	Default = 0x10h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	EXT_PG_SEL	EN_B4_L3_PWREN	VIN_OV_MASK	TSD_nMASK	UV_nMASK	OV_nMASK	nRESET_AUX1_PD	EXT_PG_POL
Default	0	0	0	1	0	0	0	0
Access	RO	R/W	R/W	R/W	R/W	R/W	RO	R/W

Name	Description	Notes
EXT_PG_SEL	0 – The EXT_PG pin is referenced to VIO_IN 1 – The EXT_PG pin is referenced to VIN pin	
EN_B4_L3_PWREN	0 – Buck4 and LDO3 follow standard turn on timing when the IC SLEEP mode 1 – Buck4 and LDO3 ignore their programmed delay times and immediately turn on when the IC exits SLEEP mode	
VIN_OV_MASK	0 – Unmasks the Input OV 1 – Masks the Input OV	If VIN_OV_MASK=0 then system enters the RESET state with an input voltage OV condition. If VIN_OV_MASK=1, the system ignores input overvoltage and continue to operate in ACTIVE state
TSD_nMASK	0 – Prevents the IC from entering the THERMAL state 1 – Allows the IC to enter the THERMAL state	When = 0, the IC will not enter the thermal shutdown state. The TSD_SHUTDOWN bit provides the real-time thermal status. When = 1, the IC can enter the Thermal state with an over temperature fault.
UV_nMASK	0 – Masks an undervoltage condition from allowing the IC to enter the UVOVFLT state. 1 – Unmasks an undervoltage condition from allowing the IC to enter the UVOVFLT state.	When UV_nMASK =1, this register allows the IC to enter the UVOVFLT state when any regulator enters an under voltage condition.
OV_nMASK	0 – Masks an overvoltage condition from allowing the IC to enter the UVOVFLT state. 1 – Unmasks an overvoltage condition from allowing the IC to enter the UVOVFLT state.	When OV_nMASK =1, this register allows the IC to enter the UVOVFLT state when any regulator enters an overvoltage condition.
nRESET_AUX1_PD	0 – nRESET_AUX1_PD pin is set to high impedance and operates normally. 1 – nRESET_AUX1_PD pin is manually set to a logic L output and overrides the normal pin functionality.	
EXT_PG_POL	0 – Sets EXT_PG polarity to active high 1 – Sets EXT_PG polarity to active low	The polarity functionality is only valid when EXT_PG is configured as an input by pulling the MODE pin high.

BUCK1 REGISTERS

B1_REG00 – Buck1 Configuration Register

Address = 0x30h	Default = 0x00h	Type = Basic Volatile

BIT	7	6	5	4	3	2	1	0
Name	PWR_GOOD	OV	ILIM	RFU	nRESET_ FLTMSK	ILIM_FLTMSK	UV_FLTMSK	OV_FLTMSK
Default	0	0	0	0	0	0	0	0
Access	RO	RO	RO	R/W	R/W	R/W	R/W	R/W

Name	Description	Notes
PWR_GOOD	0 - Buck1 voltage is below the power good threshold 1 - Buck1 voltage is above the power good threshold	Provides real-time power good status
OV	0 - Buck1 voltage is below the overvoltage threshold 1 - Buck1 voltage is above the overvoltage threshold	Provides real-time overvoltage status
ILIM	0 - Buck1 is below the ILIM threshold 1 - Buck1 is above the ILIM threshold	Provides real-time current limit status
RFU	Reserved for Future Use	Do not change this register value. Changing the register value can affect IC functionality.
nRESET_FLT_MSK	0 - Unmasks the Buck1 POK signal 1 - Masks the Buck1 POK signal	When 1, the Buck1 POK signal is masked and does not go to the master controller. This prevents Buck1 from asserting the nRESET pin when it is disabled or drops out of regulation.
ILIM_FLTMSK	0 - Unmasks the Buck1 ILIM register 1 - Masks the Buck1 ILIM register	When 1, the ILIM fault bit is masked from the master ILIM fault register, MSTR04. Bit ILIM still provides real-time current limit status. Bit PWR_GOOD provides real-time undervoltage status.
UV_FLTMSK	0 - Unmasks the Buck1 UV register 1 - Masks the Buck1 UV register	When 1, the UV fault bit is masked from the master UV fault register, MSTR06.
OV_FLTMSK	0 - Unmasks the Buck1 OV register 1 - Masks the Buck1 OV register	When 1, the OV fault bit is masked from the master OV fault register, MSTR05. Bit OV still provides real-time overvoltage status.

B1_VSET00 – Buck1 Voltage Set0 Register

Address = 0x31h	Default = 0x25h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	VSET0[7:0]							
Default	00100101							
Access	R/W							

Name	Description	Notes
VSET0[7:0]	Buck1 output voltage setting in ACTIVE mode.	Controls the Buck1 output voltage. VSET0 is used in ACTIVE mode. Note that the voltage setting equation is dependent on the Buck1 reference voltage set by register SEL_REF0P8_BUCK1. When SEL_REF0P8_BUCK1 = 0, the Buck1 output voltage is equal to VSET0 * 0.009375 + 0.6V. When SEL_REF0P8_BUCK1 = 1, the Buck1 output voltage is equal to VSET0 * 0.0125 + 0.8V

B1_VSET01 – Buck1 Voltage Set1 Register

Address = 0x32h	Default = 0x25h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	VSET1[7:0]							
Default	00100101							
Access	R/W							

Name	Description	Notes
VSET1[7:0]	Buck1 output voltage setting for dynamic voltage scaling and SLEEP mode.	Controls Buck1 output voltage. VSET1 is used in DVS or SLEEP modes. The output voltage setting uses the same equations as the VSET0 register.

B1_REG03 – Buck1 Configuration Register

Address = 0x33h	Default = 0x51h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	ON	PBINEN	QLTCH	SLEEPEN	DREN	SS_RAMP[2:0]		
Default	0	1	0	1	0	001		
Access	R/W	R/W	R/W	R/W	R/W	R/W		

Name	Description	Notes
ON	Determines startup sequencing from the CMI code	This is a factory expert bit that should not be changed. Modifying this bit may result in unexpected IC behavior.
PBINEN	Determines startup sequencing from the CMI code	This is a factory expert bit that should not be changed. Modifying this bit may result in unexpected IC behavior.
QLTCH	0 – Buck1 shuts down when its sequenced input shuts down 1 – Buck1 stays on when its sequenced input shuts down	
SLEEPEN	0 – Buck1 stays on when the IC enters Sleep mode 1 – Buck1 turns off when the IC enters Sleep mode	
DREN	0 – Buck1 POK signal does not trigger EXT_EN pin 1 – Buck1 POK signal triggers EXT_EN pin	.
SS_RAMP[2:0]	000 = 150us 001 = 200us 010 = 250us 011 = 300us 100 = 350us 101 = 395us 110 = 440us 111 = 485us	Buck1 softstart ramp timing.

B1_REG04 – Buck1 Configuration Register

Address = 0x34h	Default = 0x80h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	MODE	RST	DBQL[2:0]			DBOK[2:0]		
Default	1	0	000			000		
Access	R/W	RO	R/W			R/W		

Name	Description	Notes
MODE	Determines startup sequencing from the CMI code	This is a factory expert bit that should not be changed. Modifying this bit may result in unexpected IC behavior.
RST	0 – Buck1 does not affect nRESET_AUX1 output 1 – Buck1 turning off asserts nRESET_AUX1 output low	
DBQL[2:0]	Determines startup sequencing from the CMI code	This is a factory expert bit that should not be changed. Modifying this bit may result in unexpected IC behavior.
DBOK[2:0]	Determines startup sequencing from the CMI code	This is a factory expert bit that should not be changed. Modifying this bit may result in unexpected IC behavior.

B1_REG05 – Buck1 Configuration Register

Address = 0x35h	Default = 0x18h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	DBON[3:0]				SLEW[1:0]		DBSTBY[1:0]	
Default	0001				10		00	
Access	R/W				R/W		R/W	

Name	Description	Notes
DBON[3:0]	Determines startup sequencing from the CMI code	This is a factory expert bit that should not be changed. Modifying this bit may result in unexpected IC behavior.
SLEW[1:0]	00 = not allowed 01 = 14mV/us 10 = 3.5mV/us 11 = 0.88mV/us	Sets Buck1 slew rate when changing between VSET0 and VSET1 voltages. During the transition between voltages, PWR_GOOD, OV, and ILIM are automatically masked to avoid nRESET assertion.
DBSTBY[1:0]	Determines DVS inputs from the CMI code	This is a factory expert bit that should not be changed. Modifying this bit may result in unexpected IC behavior.

B1_REG06 – Buck1 Configuration Register

Address = 0x36h	Default = 0x83h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	PHASE_DELAY	PHASE	RFU =	ONDLY[2:0]			DRVADJ[1:0]	
Default	1	0	0	000			11	
Access	R/W	R/W	R/W	R/W			R/W	

Name	Description	Notes
PHASE_DELAY	0 – Aligns converter switching to the main clock edge 1 – Delays converter switching 100ns from the main clock edge	The PHASE_DELAY bit aligns the converter switching to the clock edge or to a 100ns delay from the clock edge.
PHASE	0 – Aligns converter switching to the main clock rising edge 1 – Aligns converter switching to the main clock falling edge	The PHASE bit aligns the converter switching to the rising or falling clock edge.
RFU	Reserved for Future Use	Do not change this register value. Changing the register value can affect IC functionality.
ONDLY[2:0]	000 = 41µs 001 = 113 µs 010 = 213 µs 011 = 313 µs 100 = 413 µs 101 = 513 µs 110 = 613 µs 111 = 713 µs	Programs the delay time between the Buck1 input trigger and when it turns on.
DRVADJ[1:0]	00 = 3.5ns rise time, 5.6ns fall time 01 = 2.8ns rise time, 4.5ns fall time 10 = 2.5ns rise time, 3.6ns fall time 11 = 2.3ns rise time, 3.0ns fall time	Sets the Buck1 switching rise and fall times. Faster rise times give higher efficiency while slower times give lower noise and EMI. These times change with Vin, load current,

		inductor value, etc and are intended to provide relative timing between settings.

BUCK2 REGISTERS

Note: Buck2, Buck3, Buck4 have the same registers but the default register values may be different

B2_REG00 – Buck2 Configuration Register

Buck2 Address = 0x40h	Default = 0x00h	Type = Basic Volatile

BIT	7	6	5	4	3	2	1	0
Name	PWR_GOOD	OV	ILIM	RFU	nRESET_ FLTMSK	ILIM_FLTMSK	UV_FLTMSK	OV_FLTMSK
Default	0	0	0	0	0	0	0	0
Access	RO	RO	RO	RO	R/W	R/W	R/W	R/W

Name	Description	Notes
PWR_GOOD	0 – Buck2 voltage is below the power good threshold 1 – Buck2 voltage is above the power good threshold	Provides real-time power good status
OV	0 – Buck2 voltage is below the overvoltage threshold 1 – Buck2 voltage is above the overvoltage threshold	Provides real-time overvoltage status
ILIM	0 – Buck2 is below the ILIM threshold 1 – Buck2 is above the ILIM threshold	Provides real-time current limit status
RFU	Reserved for Future Use	Do not change this register value. Changing the register value can affect IC functionality.
nRESET_FLTMSK	0 - Unmasks the Buck2 POK signal 1 - Masks the Buck2 POK signal	When 1, the Buck2 POK signal is masked and does not go to the master controller. This prevents Buck2 from asserting the nRESET pin when it is disabled or drops out of regulation.
ILIM_FLTMSK	0 - Unmasks the Buck2 ILIM register 1 - Masks the Buck2 ILIM register	When 1, the ILIM fault bit is masked from the master ILIM fault register, MSTR04. Bit ILIM still provides real-time current limit status.
UV_FLTMSK	0 - Unmasks the Buck2 UV register 1 - Masks the Buck2 UV register	When 1, the UV fault bit is masked from the master UV fault register, MSTR06. Bit PWR_GOOD provides real-time undervoltage status.
OV_FLTMSK	0 - Unmasks the Buck2 OV register 1 - Masks the Buck2 OV register	When 1, the OV fault bit is masked from the master OV fault register, MSTR05. Bit OV still provides real-time overvoltage status.

B2_VSET00 – Buck2 Voltage Set0 Register

Buck2 Address = 0x41h	Default = 0x25h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	VSET0[7:0]							
Default	00100101							
Access	R/W							

Name	Description	Notes
VSET0[7:0]	Buck2 output voltage setting in ACTIVE mode.	Controls the Buck2 output voltage. VSET0 is used in ACTIVE mode. Note that the voltage setting equation is dependent on the Buck2 reference voltage set by register SEL_REF0P8_BUCK2. When SEL_REF0P8_BUCK2 = 0, the Buck2 output voltage is equal to VSET0 * 0.009375 + 0.6V. When SEL_REF0P8_BUCK2 = 1, the Buck2 output voltage is equal to VSET0 * 0.0125 + 0.8V

B2_VSET01 – Buck2 Voltage Set1 Register

Address = 0x42h	Default = 0x25h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	VSET1[7:0]							
Default	00100101							
Access	R/W							

Name	Description	Notes
VSET1[7:0]	Buck2 output voltage setting for dynamic voltage scaling and SLEEP mode.	Controls Buck2 output voltage. VSET1 is used in DVS or SLEEP modes. The output voltage setting uses the same equations as the VSET0 register.

B2_REG03 – Buck2 Configuration Register

Address = 0x43h	Default = 0x51h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	ON	PBINEN	QLTCH	SLEEPEN	DREN	SS_RAMP[2:0]		
Default	0	1	0	1	0	001		
Access	R/W	R/W	R/W	R/W	R/W	R/W		

Name	Description	Notes
ON	Determines startup sequencing from the CMI code	This is a factory expert bit that should not be changed. Modifying this bit may result in unexpected IC behavior.
PBINEN	Determines startup sequencing from the CMI code	This is a factory expert bit that should not be changed. Modifying this bit may result in unexpected IC behavior.
QLTCH	0 – Buck2 shuts down when its sequenced input shuts down 1 – Buck2 stays on when its sequenced input shuts down	
SLEEPEN	0 – Buck2 stays on when the IC enters Sleep mode 1 – Buck2 turns off when the IC enters Sleep mode	
DREN	0 – Buck2 POK signal does not trigger EXT_EN pin 1 – Buck2 POK signal triggers EXT_EN pin	
SS_RAMP[2:0]	000 = 150us 001 = 200us 010 = 250us 011 = 300us 100 = 350us 101 = 395us 110 = 440us 111 = 485us	Buck2 softstart ramp timing.

B2_REG04 – Buck2 Configuration Register

Address = 0x44h	Default = 0x80h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	MODE	RST	DBQL[2:0]			DBOK[2:0]		
Default	1	0	000			000		
Access	R/W	RO	R/W			R/W		

Name	Description	Notes
MODE	Determines startup sequencing from the CMI code	This is a factory expert bit that should not be changed. Modifying this bit may result in unexpected IC behavior.
RST	0 – Buck2 does not affect nRESET_AUX1 output 1 – Buck2 turning off asserts nRESET_AUX1 output low	
DBQL[2:0]	Determines startup sequencing from the CMI code	This is a factory expert bit that should not be changed. Modifying this bit may result in unexpected IC behavior.
DBOK[2:0]	Determines startup sequencing from the CMI code	This is a factory expert bit that should not be changed. Modifying this bit may result in unexpected IC behavior.

B2_REG05 – Buck2 Configuration Register

Address = 0x45h	Default = 0x18h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	DBON[3:0]				SLEW[1:0]		DBSTBY[1:0]	
Default	0001				10		00	
Access	R/W				R/W		R/W	

Name	Description	Notes
DBON[3:0]	Determines startup sequencing from the CMI code	This is a factory expert bit that should not be changed. Modifying this bit may result in unexpected IC behavior.
SLEW[1:0]	00 = not allowed 01 = 14mV/us 10 = 3.5mV/us 11 = 0.88mV/us	Sets Buck2 slew rate when changing between VSET0 and VSET1 voltages. During the transition between voltages, PWR_GOOD, OV, and ILIM are automatically masked to avoid nRESET assertion.
DBSTBY[1:0]	Determines DVS inputs from the CMI code	This is a factory expert bit that should not be changed. Modifying this bit may result in unexpected IC behavior.

B2_REG06 – Buck2 Configuration Register

Address = 0x46h	Default = 0x02h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	PHASE_DELAY	PHASE	RFU	ONDLY[2:0]			DRVADJ[1:0]	
Default	0	0	0	000			10	
Access	R/W	R/W	R/W	R/W			R/W	

Name	Description	Notes
PHASE_DELAY	0 – Aligns converter switching to the main clock edge 1 – Delays converter switching 100ns from the main clock edge	The PHASE_DELAY bit aligns the converter switching to the clock edge or to a 100ns delay from the clock edge.
PHASE	0 – Aligns converter switching to the main clock rising edge 1 – Aligns converter switching to the main clock falling edge	The PHASE bit aligns the converter switching to the rising or falling clock edge.
RFU	Reserved for Future Use	Do not change this register value. Changing the register value can affect IC functionality.
ONDLY[2:0]	000 = 41µs 001 = 113 µs 010 = 213 µs 011 = 313 µs 100 = 413 µs 101 = 513 µs 110 = 613 µs 111 = 713 µs	Programs the delay time between the Buck2 input trigger and when it turns on.
DRVADJ[1:0]	00 = 3ns rise time, 5.5ns fall time 01 = 2.6ns rise time, 3.7ns fall time 10 = 2.4ns rise time, 3.3ns fall time 11 = 2.3ns rise time, 3.0ns fall time	Sets the Buck2 switching rise and fall times. Faster rise time give higher efficiency while slower times give lower noise and EMI. These times change with Vin, load current, inductor value, etc and are intended to provide relative timing between settings.

BUCK3 REGISTERS

B3_REG00 – Buck3 Configuration Register

Buck3 Address = 0x50h	Default = 0x00h	Type = Basic Volatile

BIT	7	6	5	4	3	2	1	0
Name	PWR_GOOD	OV	ILIM	RFU	nRESET_ FLTMSK	ILIM_FLTMSK	UV_FLTMSK	OV_FLTMSK
Default	0	0	0	0	0	0	0	0
Access	RO	RO	RO	RO	R/W	R/W	R/W	R/W

Name	Description	Notes
PWR_GOOD	0 – Buck3 voltage is below the power good threshold 1 – Buck3 voltage is above the power good threshold	Provides real-time power good status
OV	0 – Buck3 voltage is below the overvoltage threshold 1 – Buck3 voltage is above the overvoltage threshold	Provides real-time overvoltage status
ILIM	0 – Buck3 is below the ILIM threshold 1 – Buck3 is above the ILIM threshold	Provides real-time current limit status
RFU	Reserved for Future Use	Do not change this register value. Changing the register value can affect IC functionality.
nRESET_FLTMSK	0 - Unmasks the Buck3 nRESET fault 1 - Masks the Buck3 nRESET fault	When 1, the Buck3 POK signal is masked and does not go to the master controller. This prevents Buck3 from asserting the nRESET pin when it is disabled or drops out of regulation.
ILIM_FLTMSK	0 - Unmasks the Buck3 ILIM register 1 - Masks the Buck3 ILIM register	When 1, the ILIM fault bit is masked from the master ILIM fault register, MSTR04. Bit ILIM still provides real-time current limit status.
UV_FLTMSK	0 - Unmasks the Buck3 UV register 1 - Masks the Buck3 UV register	When 1, the UV fault bit is masked from the master UV fault register, MSTR06. Bit PWR_GOOD provides real-time undervoltage status.
OV_FLTMSK	0 - Unmasks the Buck3 OV register 1 - Masks the Buck3 OV register	When 1, the OV fault bit is masked from the master OV fault register, MSTR05. Bit OV still provides real-time overvoltage status.

B3_VSET00 – Buck3 Voltage Set0 Register

Buck3 Address = 0x51h	Default = 0x25h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	VSET0[7:0]							
Default	00100101							
Access	R/W							

Name	Description	Notes
VSET0[7:0]	Buck3 output voltage setting in ACTIVE mode.	Controls the Buck3 output voltage. VSET0 is used in ACTIVE mode. Note that the voltage setting equation is dependent on the Buck3 reference voltage set by register SEL_REF0P8_BUCK3. When SEL_REF0P8_BUCK3 = 0, the Buck3 output voltage is equal to VSET0 * 0.009375 + 0.6V. When SEL_REF0P8_BUCK3 = 1, the Buck3 output voltage is equal to VSET0 * 0.0125 + 0.8V

B3_VSET01 – Buck3 Voltage Set1 Register

Address = 0x52h	Default = 0x25h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	VSET1[7:0]							
Default	00100101							
Access	R/W							

Name	Description	Notes
VSET1[7:0]	Buck3 output voltage setting for dynamic voltage scaling and SLEEP mode.	Controls Buck3 output voltage. VSET1 is used in DVS or SLEEP modes. The output voltage setting uses the same equations as the VSET0 register.

B3_REG03 – Buck3 Configuration Register

Address = 0x53h	Default = 0x51h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	ON	PBINEN	QLTCH	SLEEPEN	DREN	SS_RAMP[2:0]		
Default	0	1	0	1	0	001		
Access	R/W	R/W	R/W	R/W	R/W	R/W		

Name	Description	Notes
ON	Determines startup sequencing from the CMI code	This is a factory expert bit that should not be changed. Modifying this bit may result in unexpected IC behavior.
PBINEN	Determines startup sequencing from the CMI code	This is a factory expert bit that should not be changed. Modifying this bit may result in unexpected IC behavior.
QLTCH	0 – Buck3 shuts down when its sequenced input shuts down 1 – Buck3 stays on when its sequenced input shuts down	
SLEEPEN	0 – Buck3 stays on when the IC enters Sleep mode 1 – Buck3 turns off when the IC enters Sleep mode	
DREN	0 – Buck3 POK signal does not trigger EXT_EN pin 1 – Buck3 POK signal triggers EXT_EN pin	
SS_RAMP[2:0]	000 = 150us 001 = 200us 010 = 250us 011 = 300us 100 = 350us 101 = 395us 110 = 440us 111 = 485us	Buck3 softstart ramp timing.

B3_REG04 – Buck3 Configuration Register

Address = 0x54h	Default = 0x80h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	MODE	RST	DBQL[2:0]			DBOK[2:0]		
Default	1	0	000			000		
Access	R/W	RO	R/W			R/W		

Name	Description	Notes
MODE	Determines startup sequencing from the CMI code	This is a factory expert bit that should not be changed. Modifying this bit may result in unexpected IC behavior.
RST	0 – Buck3 does not affect nRESET_AUX1 output. 1 – Buck3 turning off asserts nRESET_AUX1 output low	
DBQL[2:0]	Determines startup sequencing from the CMI code	This is a factory expert bit that should not be changed. Modifying this bit may result in unexpected IC behavior.
DBOK[2:0]	Determines startup sequencing from the CMI code	This is a factory expert bit that should not be changed. Modifying this bit may result in unexpected IC behavior.

B3_REG05 – Buck3 Configuration Register

Address = 0x55h	Default = 0x18h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	DBON[3:0]				SLEW[1:0]		DBSTBY[1:0]	
Default	0001				10		00	
Access	R/W				R/W		R/W	

Name	Description	Notes
DBON[3:0]	Determines startup sequencing from the CMI code	This is a factory expert bit that should not be changed. Modifying this bit may result in unexpected IC behavior.
SLEW[1:0]	00 = not allowed 01 = 14mV/us 10 = 3.5mV/us 11 = 0.88mV/us	Sets Buck3 slew rate when changing between VSET0 and VSET1 voltages. During the transition between voltages, PWR_GOOD, OV, and ILIM are automatically masked to avoid nRESET assertion.
DBSTBY[1:0]	Determines DVS inputs from the CMI code	This is a factory expert bit that should not be changed. Modifying this bit may result in unexpected IC behavior.

B3_REG06 – Buck3 Configuration Register

Address = 0x56h	Default = 0x02h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	PHASE_DELAY	PHASE	RFU	ONDLY[2:0]			DRVADJ[1:0]	
Default	0	0	0	000			10	
Access	R/W	R/W	R/W	R/W			R/W	

Name	Description	Notes
PHASE_DELAY	0 – Aligns converter switching to the main clock edge 1 – Delays converter switching 100ns from the main clock edge	The PHASE_DELAY bit aligns the converter switching to the clock edge or to a 100ns delay from the clock edge.
PHASE	0 – Aligns converter switching to the main clock rising edge 1 – Aligns converter switching to the main clock falling edge	The PHASE bit aligns the converter switching to the rising or falling clock edge.
RFU	Reserved for Future Use	Do not change this register value. Changing the register value can affect IC functionality.
ONDLY[2:0]	000 = 41µs 001 = 113 µs 010 = 213 µs 011 = 313 µs 100 = 413 µs 101 = 513 µs 110 = 613 µs 111 = 713 µs	Programs the delay time between the Buck3 input trigger and when it turns on.
DRVADJ[1:0]	00 = 3ns rise time, 5.5ns fall time 01 = 2.6ns rise time, 3.7ns fall time 10 = 2.4ns rise time, 3.3ns fall time 11 = 2.3ns rise time, 3.0ns fall time	Sets the Buck3 switching rise and fall times. Faster rise time give higher efficiency while slower times give lower noise and EMI. These times change with Vin, load current, inductor value, etc and are intended to provide relative timing between settings.

BUCK4 REGISTERS

B4_REG00 – Buck4 Configuration Register

Buck4 Address = 0x60h	Default = 0x00h	Type = Basic Volatile

BIT	7	6	5	4	3	2	1	0
Name	PWR_GOOD	OV	ILIM	RFU	nRESET_ FLTMSK	ILIM_FLTMSK	UV_FLTMSK	OV_FLTMSK
Default	0	0	0	0	0	0	0	0
Access	RO	RO	RO	RO	R/W	R/W	R/W	R/W

Name	Description	Notes
PWR_GOOD	0 – Buck4 voltage is below the power good threshold 1 – Buck4 voltage is above the power good threshold	Provides real-time power good status
OV	0 – Buck4 voltage is below the overvoltage threshold 1 – Buck4 voltage is above the overvoltage threshold	Provides real-time overvoltage status
ILIM	0 – Buck4 is below the ILIM threshold 1 – Buck4 is above the ILIM threshold	Provides real-time current limit status
RFU	Reserved for Future Use	Do not change this register value. Changing the register value can affect IC functionality.
nRESET_FLTMSK	0 - Unmasks the Buck4 nRESET fault 1 - Masks the Buck4 nRESET fault	When 1, the Buck4 POK signal is masked and does not go to the master controller. This prevents Buck4 from asserting the nRESET pin when it is disabled or drops out of regulation.
ILIM_FLTMSK	0 - Unmasks the Buck4 ILIM register 1 - Masks the Buck4 ILIM register	When 1, the ILIM fault bit is masked from the master ILIM fault register, MSTR04. Bit ILIM still provides real-time current limit status.
UV_FLTMSK	0 - Unmasks the Buck4 UV register 1 - Masks the Buck4 UV register	When 1, the UV fault bit is masked from the master UV fault register, MSTR06. Bit PWR_GOOD provides real-time undervoltage status.
OV_FLTMSK	0 - Unmasks the Buck4 OV register 1 - Masks the Buck4 OV register	When 1, the OV fault bit is masked from the master OV fault register, MSTR05. Bit OV still provides real-time overvoltage status.

B4_VSET00 – Buck4 Voltage Set0 Register

Buck4 Address = 0x61h	Default = 0x20h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	VSET0[7:0]							
Default	00100000							
Access	R/W							

Name	Description	Notes
VSET0[7:0]	Buck4 output voltage setting in ACTIVE mode.	Controls the Buck4 output voltage. VSET0 is used in ACTIVE mode. The Buck4 output voltage is equal to VSET0 * 0.0125 + 0.8V

B4_VSET01 – Buck4 Voltage Set1 Register

Address = 0x62h	Default = 0x18h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	VSET1[7:0]							
Default	00011000							
Access	R/W							

Name	Description	Notes
VSET1[7:0]	Buck4 output voltage setting for dynamic voltage scaling and SLEEP mode.	Controls Buck4 output voltage. VSET1 is used in DVS or SLEEP modes. The output voltage setting uses the same equations as the VSET0 register.

B4_REG03 – Buck4 Configuration Register

Address = 0x63h	Default = 0x67h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	ON	PBINEN	QLTCH	SLEEPEN	DREN	SS_RAMP[2:0]		
Default	0	1	1	0	0	111		
Access	R/W	R/W	R/W	R/W	R/W	R/W		

Name	Description	Notes
ON	Determines startup sequencing from the CMI code	This is a factory expert bit that should not be changed. Modifying this bit may result in unexpected IC behavior.
PBINEN	Determines startup sequencing from the CMI code	This is a factory expert bit that should not be changed. Modifying this bit may result in unexpected IC behavior.
QLTCH	0 – Buck4 shuts down when its sequenced input shuts down 1 – Buck4 stays on when its sequenced input shuts down	
SLEEPEN	0 – Buck4 stays on when the IC enters Sleep mode 1 – Buck4 turns off when the IC enters Sleep mode	
DREN	0 – Buck4 POK signal does not trigger EXT_EN pin 1 – Buck4 POK signal triggers EXT_EN pin 0 - Unmasks the Buck4 POK signal 1 - Masks the Buck4 POK signal	
SS_RAMP[2:0]	000 = 25us 001 = 51us 010 = 76us 011 = 102us 100 = 127us 101 = 153us 110 = 178us 111 = 204us	Buck4 softstart ramp timing.

B4_REG04 – Buck4 Configuration Register

Address = 0x64h	Default = 0x80h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	MODE	RST	DBQL[2:0]			DBOK[2:0]		
Default	1	0	000			000		
Access	R/W	RO	R/W			R/W		

Name	Description	Notes
MODE	Determines startup sequencing from the CMI code	This is a factory expert bit that should not be changed. Modifying this bit may result in unexpected IC behavior.
RST	0 – Buck4 does not affect nRESET_AUX1 output 1 – Buck4 turning off asserts nRESET_AUX1 output low	
DBQL[2:0]	Determines startup sequencing from the CMI code	This is a factory expert bit that should not be changed. Modifying this bit may result in unexpected IC behavior.
DBOK[2:0]	Determines startup sequencing from the CMI code	This is a factory expert bit that should not be changed. Modifying this bit may result in unexpected IC behavior.

B4_REG05 – Buck4 Configuration Register

Address = 0x65h	Default = 0x19h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	DBON[3:0]				SLEW[1:0]		DBSTBY[1:0]	
Default	0001				10		01	
Access	R/W				R/W		R/W	

Name	Description	Notes
DBON[3:0]	Determines startup sequencing from the CMI code	This is a factory expert bit that should not be changed. Modifying this bit may result in unexpected IC behavior.
SLEW[1:0]	00 = not allowed 01 = 14mV/us 10 = 3.5mV/us 11 = 0.88mV/us	Sets Buck4 slew rate when changing between VSET0 and VSET1 voltages. During the transition between voltages, PWR_GOOD, OV, and ILIM are automatically masked to avoid nRESET assertion.
DBSTBY[1:0]	Determines DVS inputs from the CMI code	This is a factory expert bit that should not be changed. Modifying this bit may result in unexpected IC behavior.

B4_REG06 – Buck4 Configuration Register

Address = 0x66h	Default = 0x02h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	PHASE_DELAY	PHASE	RFU	ONDLY[2:0]			DRVADJ[1:0]	
Default	0	0	0	000			10	
Access	R/W	R/W	R/W	R/W			R/W	

Name	Description	Notes
PHASE_DELAY	0 – Aligns converter switching to the main clock edge 1 – Delays converter switching 100ns from the main clock edge	The PHASE_DELAY bit aligns the converter switching to the clock edge or to a 100ns delay from the clock edge.
PHASE	0 – Aligns converter switching to the main clock rising edge 1 – Aligns converter switching to the main clock falling edge	The PHASE bit aligns the converter switching to the rising or falling clock edge.
RFU	Reserved for Future Use	Do not change this register value. Changing the register value can affect IC functionality.
ONDLY[2:0]	000 = 41µs 001 = 113 µs 010 = 213 µs 011 = 313 µs 100 = 413 µs 101 = 513 µs 110 = 613 µs 111 = 713 µs	Programs the delay time between the Buck4 input trigger and when it turns on.
DRVADJ[1:0]	00 = 3ns rise time, 5.5ns fall time 01 = 2.6ns rise time, 3.7ns fall time 10 = 2.4ns rise time, 3.3ns fall time 11 = 2.3ns rise time, 3.0ns fall time	Sets the Buck4 switching rise and fall times. Faster rise time give higher efficiency while slower times give lower noise and EMI. These times change with Vin, load current, inductor value, etc and are intended to provide relative timing between settings.

LDO1 REGISTERS

LDO1_REG00 – LDO1 Configuration Register

LDO1 Address = 0x70h	Default = 0x00h	Type = Basic Volatile

BIT	7	6	5	4	3	2	1	0
Name	PWR_GOOD	OV	ILIM	RFU	nRESET_FLTMSK	ILIM_FLTMSK	UV_FLTMSK	OV_FLTMSK
Default	0	0	0	0	0	0	0	0
Access	RO	RO	RO	RO	R/W	R/W	R/W	R/W

Name	Description	Notes
PWR_GOOD	0 – LDO1 voltage is below the power good threshold 1 – LDO1 voltage is above the power good threshold	Provides real-time power good status
OV	0 – LDO1 voltage is below the overvoltage threshold 1 – LDO1 voltage is above the overvoltage threshold	Provides real-time overvoltage status
ILIM	0 – LDO1 is below the ILIM threshold 1 – LDO1 is above the ILIM threshold	Provides real-time current limit status
RFU	Reserved for Future Use	Do not change this register value. Changing the register value can affect IC functionality.
nRESET_FLTMSK	0 - Unmasks the LDO1 nRESET fault 1 - Masks the LDO1 nRESET fault	When 1, the LDO1 POK signal is masked and does not go to the master controller. This prevents LDO1 from asserting the nRESET pin when it is disabled or drops out of regulation.
ILIM_FLTMSK	0 - Unmasks the LDO1 ILIM register 1 - Masks the LDO1 ILIM register	When 1, the ILIM fault bit is masked from the master ILIM fault register, MSTR04. Bit ILIM still provides real-time current limit status.
UV_FLTMSK	0 - Unmasks the LDO1 UV register 1 - Masks the LDO1 UV register	When 1, the UV fault bit is masked from the master UV fault register, MSTR06. Bit PWR_GOOD provides real-time undervoltage status.
OV_FLTMSK	0 - Unmasks the LDO1 OV register 1 - Masks the LDO1 OV register	When 1, the OV fault bit is masked from the master OV fault register, MSTR05. Bit OV still provides real-time overvoltage status.

LDO1_VSET – LDO1 Voltage Set0 Register

LDO1 Address = 0x71h	Default = 0x28h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	RFU	VSET0[6:0]						
Default	0	0101000						
Access	R/W	R/W						

Name	Description	Notes
RFU	Reserved for Future Use	Do not change this register value. Changing the register value can affect IC functionality.
VSET0[6:0]	LDO1 output voltage setting.	Controls the LDO1 output voltage. The output voltage is equal to VSET0 * 0.025 + 2.0V

LDO1_REG02 – LDO1 Configuration Register

Address = 0x72h	Default = 0x61h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	ON	PBINEN	QLTCH	SLEEPEN	DREN	SEL_REF0P8_BUCK2	SS_RAMP[1:0]	
Default	0	1	1	0	0	0	01	
Access	R/W	R/W	R/W	R/W	R/W	RO	R/W	

Name	Description			Notes
ON	Determines startup sequencing from the CMI code			This is a factory expert bit that should not be changed. Modifying this bit may result in unexpected IC behavior.
PBINEN	Determines startup sequencing from the CMI code			This is a factory expert bit that should not be changed. Modifying this bit may result in unexpected IC behavior.
QLTCH	0 – LDO1 shuts down when its sequenced input shuts down 1 – LDO1 stays on when its sequenced input shuts down			
SLEEPEN	0 – LDO1 stays on when the IC enters Sleep mode 1 – LDO1 turns off when the IC enters Sleep mode			
DREN	0 – LDO1 POK signal does not trigger EXT_EN pin 1 – LDO1 POK signal triggers EXT_EN pin			
SEL_REF0P8_BUCK2	0 – Sets the Buck2 reference voltage to 0.6V 1 – Sets the Buck2 reference voltage to 0.8V			
SS_RAMP[1:0]	Vout=1.8V	Vout=2.5V	Vout=3.3V	LDO1 softstart ramp timing. Note that the timing is variable depending on the output voltage setpoint.
	00 = 240us 01 = 330us 10 = 450us 11 = 575us	00 = not allowed 01 = 385us 10 = 465us 11 = 600us	00 = not allowed 01 = 450us 10 = 525us 11 = 660us	

LDO1_REG03 – LDO1 Configuration Register

Address = 0x73h	Default = 0x80h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	MODE	RST	DBQL[2:0]			DBOK[2:0]		
Default	1	0	000			000		
Access	R/W	RO	R/W			R/W		

Name	Description	Notes
MODE	Determines startup sequencing from the CMI code	This is a factory expert bit that should not be changed. Modifying this bit may result in unexpected IC behavior.
RST	0 – LDO1 does not affect nRESET_AUX1 output 1 – LDO1 turning off asserts nRESET_AUX1 output low	
DBQL[2:0]	Determines startup sequencing from the CMI code	This is a factory expert bit that should not be changed. Modifying this bit may result in unexpected IC behavior.
DBOK[2:0]	Determines startup sequencing from the CMI code	This is a factory expert bit that should not be changed. Modifying this bit may result in unexpected IC behavior.

LDO1_REG04 – LDO1 Configuration Register

Address = 0x74h	Default = 0x10h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	DBON[3:0]				ONDLY[2:0]			SEL_REF0P8_BUCK1
Default	0001				000			0
Access	R/W				R/W			R/W

Name	Description	Notes
DBON[3:0]	Determines startup sequencing from the CMI code	This is a factory expert bit that should not be changed. Modifying this bit may result in unexpected IC behavior.
ONDLY[2:0]	000 = 41µs 001 = 113 µs 010 = 213 µs 011 = 313 µs 100 = 413 µs 101 = 513 µs 110 = 613 µs 111 = 713 µs	Programs the delay time between the LDO1 input trigger and when it turns on.
SEL_REF0P8_BUCK1	0 – Sets the Buck1 reference voltage to 0.6V 1 – Sets the Buck1 reference voltage to 0.8V	

Current Limit REGISTERS

Current Limit_REG00 – Current Limit Configuration Register

Address = 0x79h	Default = 0x6Ah	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	B1_ILIMSET[1:0]		B2_ILIMSET[1:0]		B3_ILIMSET[1:0]		B4_ILIMSET[1:0]	
Default	01		10		10		10	
Access	R/W		R/W		R/W		R/W	

Name	Description	Notes
B1_ILIMSET[1:0]	00 = 5.3A 01 = 4.6A 10 = 3.8A 11 = 3.0A	Buck1 cycle-by-cycle peak current limit threshold.
B2_ILIMSET[1:0]	00 = 4.0A 01 = 4.0A 10 = 3.0A 11 = 2.0A	Buck2 cycle-by-cycle peak current limit threshold.
B3_ILIMSET[1:0]	00 = 4.0A 01 = 4.0A 10 = 3.0A 11 = 2.0A	Buck3 cycle-by-cycle peak current limit threshold.
B4_ILIMSET[1:0]	00 = 4.0A 01 = 4.0A 10 = 3.0A 11 = 2.0A	Buck4 cycle-by-cycle peak current limit threshold.

Current Limit_REG01 – Current Limit Configuration Register

Address = 0x7Ah	Default = 0XE8h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	L1_ILIMSET[1:0]		L2_ILIMSET[1:0]		L3_ILIMSET[1:0]		RFU	EN_PUSH_PULL_IO8
Default	11		10		10		0	0
Access	R/W		R/W		R/W		R/W	R/W

Name	Description	Notes
L1_ILIMSET[1:0]	00 = 350mA 01 = 500mA 10 = 630mA 11 = 1000mA	LDO1 output current limit.
L2_ILIMSET[1:0]	00 = 110mA 01 = 150mA 10 = 210mA 11 = 315mA	LDO2 output current limit.
L3_ILIMSET[1:0]	00 = 130mA 01 = 183mA 10 = 255mA 11 = 390mA	LDO3 output current limit.
RFU	Reserved for Future Use	Do not change this register value. Changing the register value can affect IC functionality.
EN_PUSH_PULL_IO8	0 - Disables push-pull output function for EXT_EN pin 1 – Enables push-pull output function for EXT_EN pin	

Current Limit_REG02 – Current Limit Configuration Register

Address = 0x7Bh	Default = 0x0Fh	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	B4_LSASYNC	B3_LSASYNC	B2_LSASYNC	B1_LSASYNC	B4_LP_ MODE	B3_LP_ MODE	B2_LP_MODE	B1_LP_MODE
Default	0	0	0	0	1	1	1	1
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Name	Description	Notes
B4_LSASYNC	0 - Normal synchronous operation 1 – Buck4 low side FET does not turn on when in Burst mode	
B3_LSASYNC	0 - Normal synchronous operation 1 – Buck3 low side FET does not turn on when in Burst mode	
B2_LSASYNC	0 - Normal synchronous operation 1 – Buck2 low side FET does not turn on when in Burst mode	
B1_LSASYNC	0 - Normal synchronous operation 1 – Buck1 low side FET does not turn on when in Burst mode	
B4_LP_MODE	0 – Normal Burst Mode operation. 1 – Consumes less power in Burst Mode operation. Enables full low power mode to reduce current to lowest possible level.	When set to 0, the IC consumes more power in Burst Mode, but will have better performance transitioning from Burst Mode to normal operation.
B3_LP_MODE	0 – Normal Burst Mode operation. 1 – Consumes less power in Burst Mode operation. Enables full low power mode to reduce current to lowest possible level.	When set to 0, the IC consumes more power in Burst Mode, but will have better performance transitioning from Burst Mode to normal operation.
B2_LP_MODE	0 – Normal Burst Mode operation. 1 – Consumes less power in Burst Mode operation. Enables full low power mode to reduce current to lowest possible level.	When set to 0, the IC consumes more power in Burst Mode, but will have better performance transitioning from Burst Mode to normal operation.
B1_LP_MODE	0 – Normal Burst Mode operation. 1 – Consumes less power in Burst Mode operation. Enables full low power mode to reduce current to lowest possible level.	When set to 0, the IC consumes more power in Burst Mode, but will have better performance transitioning from Burst Mode to normal operation.

Current Limit_REG03 – Current Limit Configuration Register

Address = 0x7Ch	Default = 0xF0h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	B4_HalfFreq	B3_HalfFreq	B2_HalfFreq	B1_HalfFreq	B4_DISLPM	B3_DISLPM	B2_DISLPM	B1_DISLPM
Default	0	0	0	1	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Name	Description	Notes
B4_HalfFreq	0 – Sets Buck4 switch frequency to 2.25Mhz 1 - Sets Buck4 switch frequency to 1.125Mhz	Allows lower frequency operation to improve efficiency
B3_HalfFreq	0 – Sets Buck3 switch frequency to 2.25Mhz 1 - Sets Buck3 switch frequency to 1.125Mhz	Allows lower frequency operation to improve efficiency
B2_HalfFreq	0 – Sets Buck2 switch frequency to 2.25Mhz 1 - Sets Buck2 switch frequency to 1.125Mhz	Allows lower frequency operation to improve efficiency
B1_HalfFreq	0 – Sets Buck1 switch frequency to 2.25Mhz 1 - Sets Buck1 switch frequency to 1.125Mhz	Allows lower frequency operation to improve efficiency
B4_DISLPM	0 - Enables the Buck4 low power mode. 1 - Disables the Buck4 low power mode.	
B3_DISLPM	0 - Enables the Buck3 low power mode. 1 - Disables the Buck3 low power mode.	
B2_DISLPM	0 - Enables the Buck2 low power mode 1 - Disables the Buck2 low power mode.	
B1_DISLPM	0 - Enables the Buck1 low power mode. 1 - Disables the Buck1 low power mode.	

LDO2 REGISTERS

LDO2_REG00 – LDO2 Configuration Register

Address = 0x80h	Default = 0x00h	Type = Basic Volatile

BIT	7	6	5	4	3	2	1	0
Name	PWR_GOOD	OV	ILIM	RFU[1:0]		ILIM_FLTMSK	UV_FLTMSK	OV_FLTMSK
Default	0	0	0	0		0	0	0
Access	RO	RO	RO	R/W		R/W	R/W	R/W

Name	Description	Notes
PWR_GOOD	0 – LDO2 voltage is below the power good threshold 1 – LDO2 voltage is above the power good threshold	Provides real-time power good status
OV	0 – LDO2 voltage is below the overvoltage threshold 1 – LDO2 voltage is above the overvoltage threshold	Provides real-time overvoltage status
ILIM	0 – LDO2 is below the ILIM threshold 1 – LDO2 is above the ILIM threshold	Provides real-time current limit status
RFU[1:0]	Reserved for Future Use	Do not change this register value. Changing the register value can affect IC functionality.
ILIM_FLTMSK	0 - Unmasks the LDO2 ILIM register 1 - Masks the LDO2 ILIM register	When 1, the LDO2 ILIM fault bit is masked from the master ILIM fault register, MSTR04. Bit ILIM still provides real-time current limit status.
UV_FLTMSK	0 - Unmasks the LDO2 UV register 1 - Masks the LDO2 UV register	When 1, the LDO2 UV fault bit is masked from the master UV fault register, MSTR06. Bit PWR_GOOD provides real-time undervoltage status.
OV_FLTMSK	0 - Unmasks the LDO2 OV register 1 - Masks the LDO2 OV register	When 1, the LDO2 OV fault bit is masked from the master OV fault register, MSTR05. Bit OV still provides real-time overvoltage status.

LDO2_VSET – LDO2 Voltage Set0 Register

Address = 0x81h	Default = 0xA8h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	RANGE_LDO2	RANGE_LDO3	VSET0[5:0]					
Default	1	0	101000					
Access	RO	R/W						

Name	Description	Notes
RANGE_LDO2	0 – LDO2 Output voltage range is 2V to 3.575V 1 – LDO2 Output voltage range is 0.8V to 2.375V	
RANGE_LDO3	0 – LDO2 Output voltage range is 2V to 3.575V 1 – LDO2 Output voltage range is 0.8V to 2.375V	
VSET0[5:0]	LDO2 output voltage setting.	Controls the LDO2 output voltage. When RANGE_LDO2 = 0, the LDO2 output voltage is equal to VSET0 * 0.025 + 2.0V When RANGE_LDO2 = 1, the LDO2 output voltage is equal to VSET0 * 0.025 + 0.8V

LDO2_REG02 – LDO2 Configuration Register

Address = 0x82h	Default = 0x63h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	ON	PBINEN	QLTCH	SLEEPEN	DREN	RFU	SS_RAMP[1:0]	
Default	1	1	1	0	0	0	11	
Access	R/W	R/W	R/W	R/W	R/W	RO	R/W	

Name	Description			Notes
ON	Determines startup sequencing from the CMI code			This is a factory expert bit that should not be changed. Modifying this bit may result in unexpected IC behavior.
PBINEN	Determines startup sequencing from the CMI code			This is a factory expert bit that should not be changed. Modifying this bit may result in unexpected IC behavior.
QLTCH	0 – LDO2 shuts down when its sequenced input shuts down 1 – LDO2 stays on when its sequenced input shuts down			
SLEEPEN	0 – LDO2 stays on when the IC enters Sleep mode 1 – LDO2 turns off when the IC enters Sleep mode			
DREN	0 – LDO2 POK signal does not trigger EXT_EN pin 1 – LDO2 POK signal triggers EXT_EN pin			
RFU	Reserved for Future Use			Do not change this register value. Changing the register value can affect IC functionality.
SS_RAMP[1:0]	Vout=1.8V	Vout=2.5V	Vout=3.3V	LDO2 softstart ramp timing.

	00 = 110us 01 = 110us 10 = 165us 11 = 215us	00 = 130us 01 = 133us 10 = 170us 11 = 220us	00 = 200us 01 = 200us 10 = 210us 11 = 235us	

LDO2_REG03 – LDO2 Configuration Register

Address = 0x83h	Default = 0x80h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	MODE	RST	DBQL[2:0]			DBOK[2:0]		
Default	1	0	000			000		
Access	R/W	RO	R/W			R/W		

Name	Description	Notes
MODE	Determines startup sequencing from the CMI code	This is a factory expert bit that should not be changed. Modifying this bit may result in unexpected IC behavior.
RST	0 – LDO2 does not affect nRESET_AUX1 output 1 – LDO2 turning off asserts nRESET_AUX1 output low	
DBQL[2:0]	Determines startup sequencing from the CMI code	This is a factory expert bit that should not be changed. Modifying this bit may result in unexpected IC behavior.
DBOK[2:0]	Determines startup sequencing from the CMI code	This is a factory expert bit that should not be changed. Modifying this bit may result in unexpected IC behavior.

LDO2_REG04 – LDO2 Configuration Register

Address = 0x84h	Default = 0x10h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	DBON[3:0]				ONDLY[2:0]			RFU
Default	0001				000			0
Access	R/W				R/W			R/W

Name	Description	Notes
DBON[3:0]	Determines startup sequencing from the CMI code	This is a factory expert bit that should not be changed. Modifying this bit may result in unexpected IC behavior.
ONDLY[2:0]	000 = 41µs 001 = 113 µs 010 = 213 µs 011 = 313 µs 100 = 413 µs 101 = 513 µs 110 = 613 µs 111 = 713 µs	Programs the delay time between the LDO2 input trigger and when it turns on.
RFU	Reserved for Future Use	Do not change this register value. Changing the register value can affect IC functionality.

LDO3 REGISTERS

LDO3_REG00 – LDO3 Configuration Register

Address = 0x88h	Default = 0x00h	Type = Basic Volatile

BIT	7	6	5	4	3	2	1	0
Name	PWR_GOOD	OV	ILIM	RFU	nRESET_FLTMSK	ILIM_FLTMSK	UV_FLTMSK	OV_FLTMSK
Default	0	0	0	0	0	0	0	0
Access	RO	RO	RO	RO	R/W	R/W	R/W	R/W

Name	Description	Notes
PWR_GOOD	0 – LDO3 voltage is below the power good threshold 1 – LDO3 voltage is above the power good threshold	Provides real-time power good status
OV	0 – LDO3 voltage is below the overvoltage threshold 1 – LDO3 voltage is above the overvoltage threshold	Provides real-time overvoltage status
ILIM	0 – LDO3 is below the ILIM threshold 1 – LDO3 is above the ILIM threshold	Provides real-time current limit status
RFU	Reserved for Future Use	Do not change this register value. Changing the register value can affect IC functionality.
nRESET_FLTMSK	0 - Unmasks the LDO3 nRESET fault 1 - Masks the LDO3 nRESET fault	When 1, the LDO3 POK signal is masked and does not go to the master controller. This prevents LDO3 from asserting the nRESET pin when it is disabled or drops out of regulation.
ILIM_FLTMSK	0 - Unmasks the LDO3 ILIM register 1 - Masks the LDO3 ILIMregister	When 1, the LDO3 ILIM fault bit is masked from the master ILIM fault register, MSTR04. Bit ILIM still provides real-time current limit status.
UV_FLTMSK	0 - Unmasks the LDO3 UV register 1 - Masks the LDO3 UV register	When 1, the LDO3 UV fault bit is masked from the master UV fault register, MSTR06. Bit PWR_GOOD provides real-time undervoltage status.
OV_FLTMSK	0 - Unmasks the LDO3 OV register 1 - Masks the LDO3 OV register	When 1, the LDO3 OV fault bit is masked from the master OV fault register, MSTR05. Bit OV still provides real-time overvoltage status.

LDO3_VSET – LDO3 Voltage Set0 Register

Address = 0x89h	Default = 0x14h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	SEL_REF0P8_BUCK3	RFU	VSET0[5:0]					
Default	0	0	010100					
Access	R/R		R/W					

Name	Description	Notes
SEL_REF0P8_BUCK3	0 – Sets the Buck3 reference voltage to 0.6V 1 – Sets the Buck3 reference voltage to 0.8V	
RFU	Reserved for Future Use	Do not change this register value. Changing the register value can affect IC functionality.
VSET0[5:0]	LDO3 output voltage setting.	Controls the LDO3 output voltage. When RANGE_LDO3 = 0, the LDO3 output voltage is equal to VSET0 * 0.025 + 2.0V When RANGE_LDO3 = 1, the LDO3 output voltage is equal to VSET0 * 0.025 + 0.8V

LDO3_REG02 – LDO3 Configuration Register

Address = 0x8Ah	Default = 0x63h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	ON	PBINEN	QLTCH	SLEEPEN	DREN	SS_BIAS_INC	SS_RAMP[1:0]	
Default	0	1	1	0	0	0	11	
Access	R/W	R/W	R/W	R/W	R/W	RO	R/W	

Name	Description				Notes
ON	Determines startup sequencing from the CMI code				This is a factory expert bit that should not be changed. Modifying this bit may result in unexpected IC behavior.
PBINEN	Determines startup sequencing from the CMI code				This is a factory expert bit that should not be changed. Modifying this bit may result in unexpected IC behavior.
QLTCH	0 – LDO3 shuts down when its sequenced input shuts down 1 – LDO3 stays on when its sequenced input shuts down				
SLEEPEN	0 – LDO3 stays on when the IC enters Sleep mode 1 – LDO3 turns off when the IC enters Sleep mode				
DREN	0 – LDO3 POK signal does not trigger EXT_EN pin 1 – LDO3 POK signal triggers EXT_EN pin				
SS_BIAS_INC	0 – Adjusts the LDO3 softstart time to the longer softstart time range. 1 – Adjusts the LDO3 softstart time to the shorter softstart time range.				Refer to the DS EC table for details on the softstart time.
SS_RAMP[1:0]	Vout=0.9V SS_BIAS_INC=1	Vout=1.8V	Vout=2.5V	Vout=3.3V	LDO3 softstart ramp timing.
	00 = 36us 01 = 64us 10 = 96us 11 = 126us	00 = us 01 = us 10 = us 11 = us	00 = 110us 01 = 150us 10 = 210us 11 = 315us	00 = 200us 01 = 200us 10 = 210us 11 = 235us	

LDO3_REG03 – LDO3 Configuration Register

Address = 0x8Bh	Default = 0x80h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	MODE	RST	DBQL[2:0]			DBOK[2:0]		
Default	1	0	000			000		
Access	R/W	RO	R/W			R/W		

Name	Description	Notes
MODE	Determines startup sequencing from the CMI code	This is a factory expert bit that should not be changed. Modifying this bit may result in unexpected IC behavior.
RST	0 – LDO3 does not affect nRESET_AUX1 output 1 – LDO3 turning off asserts nRESET_AUX1 output low	
DBQL[2:0]	Determines startup sequencing from the CMI code	This is a factory expert bit that should not be changed. Modifying this bit may result in unexpected IC behavior.
DBOK[2:0]	Determines startup sequencing from the CMI code	This is a factory expert bit that should not be changed. Modifying this bit may result in unexpected IC behavior.

LDO3_REG04 – LDO3 Configuration Register

Address = 0x8Ch	Default = 0x10h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	DBON[3:0]				ONDLY[2:0]			RFU
Default	0001				000			0
Access	R/W				R/W			R/W

Name	Description	Notes
DBON[3:0]	Determines startup sequencing from the CMI code	This is a factory expert bit that should not be changed. Modifying this bit may result in unexpected IC behavior.
ONDLY[2:0]	000 = 41µs 001 = 113 µs 010 = 213 µs 011 = 313 µs 100 = 413 µs 101 = 513 µs 110 = 613 µs 111 = 713 µs	Programs the delay time between the LDO3 input trigger and when it turns on.
RFU	Reserved for Future Use	Do not change this register value. Changing the register value can affect IC functionality.

Referenced Documents

The reference documents below take precedence over the contents of this application note and should always be consulted for the latest information.

ACT88430 Data Sheet

Contact Information

For the latest specifications, additional product information, worldwide sales and distribution locations:

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