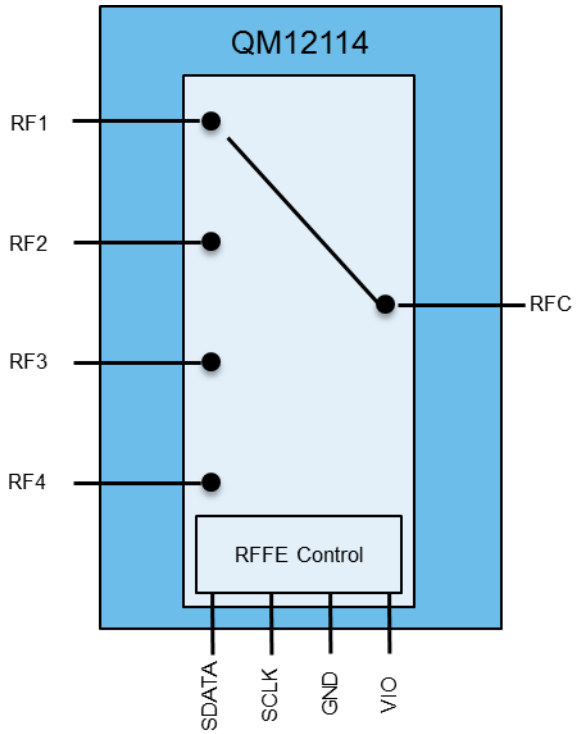
QM12114
SP4T RFFE GSM HIGH POWER SWITCH

Product Description

The QM12114 is a low loss, high isolation SP4T switch with performance optimized for GSM, CDMA, WCDMA, & LTE applications requiring high linearity and high power handling. The QM12114 is packaged in a compact 1.1mm x 1.1mm, 9-pin module which allows for a small solution size with no need for external DC blocking capacitors (when no external DC is applied to the device ports).

Functional Block Diagram



9 Pin 1.1 x 1.1 x 0.44 mm Package

Feature Overview

- Low Insertion Loss
- High Port-to-Port Isolation
- RFFE compatible
- Capable of 1.8V operation
- HBM Rating > 1kV on all ports
- Compact size: 1.1mm x 1.1mm x 0.44mm
- Supports NR bands (n7, n40, n41, n77, n78 and n79)
- DC blocking capacitors are not required in typical applications

Applications

- Cellular Handset Applications
- Cellular Modems and USB Devices
- Multi-Mode GSM, EDGE, WCDMA, and LTE Applications

Ordering Information

PART NO.	DESCRIPTION
QM12114SB	5-pc Sample Bag
QM12114SR	100-pc, 7” Reel
QM12114TR13-5K	5000-pc, 13” Reel
QM12114DK	Fully Assembled Evaluation Kit

Absolute Maximum Ratings

PARAMETER	RATING
Storage Temperature	-65 to +150 °C
Operating Temperature	-30 to +90°C
V_{IO}	2.5 V
SDATA, SCLK	2.5 V
Maximum Power Handling	39 dBm, 1:1 VSWR, +25°C, 25% duty cycle

Operation of this device outside the parameter ranges given above may cause permanent damage.

Recommended Operating Conditions

PARAMETER	MIN.	TYP.	MAX.	UNITS
V_{IO} Supply Voltage	1.65	1.8	1.95	V
V_{IO} Supply Current (Active Mode)	-	30	60	µA
V_{IO} Supply Current (Low Power Mode)	-	3	10	µA
SDATA, SCLK Logic Low (Input)	0.00	0.00	0.3 x VIO	V
SDATA, SCLK Logic High (Input)	0.7 x VIO	1.8	VIO	V
SDATA Logic Low (Output)	0.00	0.00	0.2 x VIO	V
SDATA Logic High (Output)	0.8 x VIO	1.8	VIO	V
SDATA, SCLK Logic High Current	-	0.1	5	µA
Turn-On Time	-	-	20	µs
Switching Speed	-	2	4	µs

Electrical specifications are measured at specified test conditions. Specifications are not guaranteed over all recommended operating conditions.

Electrical Specifications

Test conditions unless otherwise stated: all unused RF ports terminated in 50Ω, Input and Output = 50Ω, T = 25°C, V_{IO} = 1.8V, SDATA/SCLK = 1.8 V / 0 V

PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Frequency Range		698		6000	MHz
Insertion Loss					
RF1/2/3/4 to RFCOM	698 MHz to 960 MHz	-	0.23	0.42	dB
RF1/2/3/4 to RFCOM	1700 MHz to 2700 MHz	-	0.33	0.50	dB
RF1/2/3/4 to RFCOM – **Band n7**	2500 MHz to 2690 MHz	-	0.33	0.50	dB
RF1/2/3/4 to RFCOM – **Band n40**	2300 MHz to 2400 MHz	-	0.33	0.50	dB
RF1/2/3/4 to RFCOM* – **Band n41**	2496 MHz to 2690 MHz	-	0.33	0.50	dB
RF1/2/3/4 to RFCOM* – **Band n77**	3300 MHz to 4200 MHz	-	0.44	0.72	dB
RF1/2/3/4 to RFCOM* – **Band n78**	3300 MHz to 3800 MHz	-	0.44	0.72	dB
RF1/2/3/4 to RFCOM* – **Band n79**	4400 MHz to 5000 MHz	-	0.6	-	dB
RF1/2/3/4 to RFCOM*	5000 MHz to 6000 MHz	-	0.6	-	dB
Frequency Range		698		960	MHz
Isolation					
RF1 to RF2	Logic State: RF1 to RFCOM	45	53	-	dB
RF1 to RF3		37	44	-	dB
RF1 to RF4		41	47	-	dB
RFCOM to RF2		38	46	-	dB
RFCOM to RF3		31	40	-	dB
RFCOM to RF4		31	40	-	dB
RF2 to RF1	Logic State: RF2 to RFCOM	47	53	-	dB
RF2 to RF3		40	47	-	dB
RF2 to RF4		38	45	-	dB
RFCOM to RF1		37	47	-	dB
RFCOM to RF3		31	40	-	dB
RFCOM to RF4		31	40	-	dB
RF3 to RF1	Logic State: RF3 to RFCOM	33	39	-	dB
RF3 to RF2		45	52	-	dB
RF3 to RF4		45	53	-	dB
RFCOM to RF1		37	47	-	dB
RFCOM to RF2		38	46	-	dB
RFCOM to RF4		31	40	-	dB
RF4 to RF1	Logic State: RF4 to RFCOM	45	52	-	dB
RF4 to RF2		33	39	-	dB
RF4 to RF3		45	53	-	dB
RFCOM to RF1		37	47	-	dB
RFCOM to RF2		38	46	-	dB
RFCOM to RF3		31	40	-	dB

Frequency Range		1700		2700	MHz
	Band n7	2500		2690	MHz
	Band n40	2300		2400	MHz
	Band n41	2496		2690	MHz
Isolation					
RF1 to RF2	Logic State: RF1 to RFCOM	29	38	-	dB
RF1 to RF3		23	31	-	dB
RF1 to RF4		27	36	-	dB
RFCOM to RF2		25	35	-	dB
RFCOM to RF3		20	29	-	dB
RFCOM to RF4		20	29	-	dB
RF2 to RF1	Logic State: RF2 to RFCOM	29	37	-	dB
RF2 to RF3		27	35	-	dB
RF2 to RF4		23	32	-	dB
RFCOM to RF1		25	34	-	dB
RFCOM to RF3		20	29	-	dB
RFCOM to RF4		20	29	-	dB
RF3 to RF1	Logic State: RF3 to RFCOM	22	29	-	dB
RF3 to RF2		29	38	-	dB
RF3 to RF4		28	36	-	dB
RFCOM to RF1		25	34	-	dB
RFCOM to RF2		25	35	-	dB
RFCOM to RF4		20	29	-	dB
RF4 to RF1	Logic State: RF4 to RFCOM	29	37	-	dB
RF4 to RF2		22	30	-	dB
RF4 to RF3		27	36	-	dB
RFCOM to RF1		25	34	-	dB
RFCOM to RF2		25	35	-	dB
RFCOM to RF3		20	29	-	dB
Frequency Range	**Band n77**	3300		4200	MHz
	Band n78	3200		3800	MHz
Isolation					
RF1 to RF2	Logic State: RF1 to RFCOM	23	29	-	dB
RF1 to RF3		17	23	-	dB
RF1 to RF4		22	27	-	dB
RFCOM to RF2		21	28	-	dB
RFCOM to RF3		16	23	-	dB
RFCOM to RF4		16	23	-	dB
RF2 to RF1	Logic State: RF2 to RFCOM	23	29	-	dB
RF2 to RF3		22	28	-	dB
RF2 to RF4		18	23	-	dB
RFCOM to RF1		21	27	-	dB
RFCOM to RF3		16	23	-	dB
RFCOM to RF4		16	23	-	dB
		18	23	-	dB

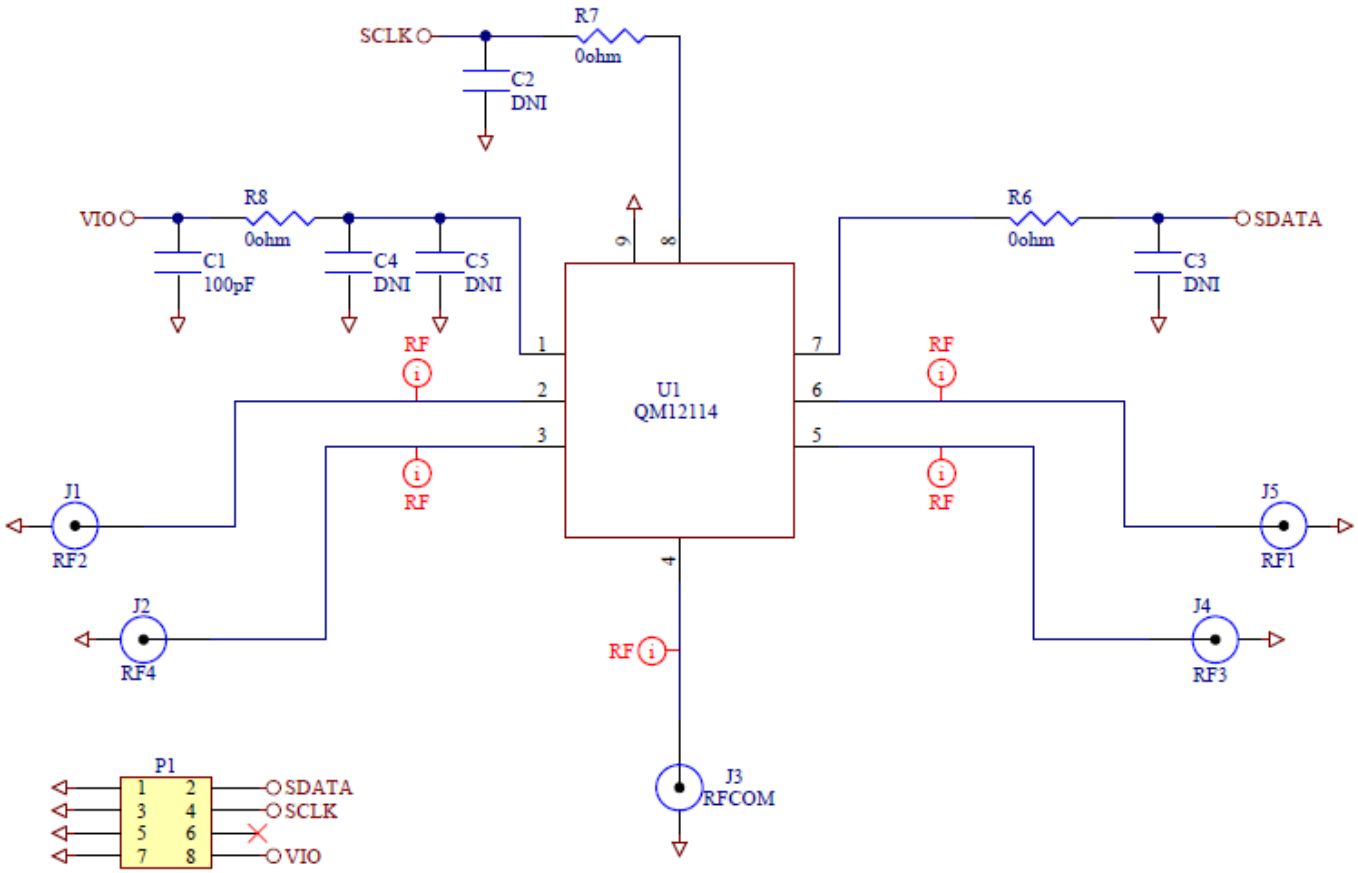
RF3 to RF1	Logic State: RF3 to RFCOM	18	23	-	dB
RF3 to RF2		23	29	-	dB
RF3 to RF4		21	27	-	dB
RFCOM to RF1		21	27	-	dB
RFCOM to RF2		21	28	-	dB
RFCOM to RF4		16	23	-	dB
RF4 to RF1	Logic State: RF4 to RFCOM	23	29	-	dB
RF4 to RF2		18	23	-	dB
RF4 to RF3		21	27	-	dB
RFCOM to RF1		21	27	-	dB
RFCOM to RF2		21	28	-	dB
RFCOM to RF3		16	23	-	dB
Frequency Range	**Band n79**	4400		5000	MHz
Isolation					
RF1 to RF2	Logic State: RF1 to RFCOM	-	23	-	dB
RF1 to RF3		-	18	-	dB
RF1 to RF4		-	24	-	dB
RFCOM to RF2		-	23	-	dB
RFCOM to RF3		-	18	-	dB
RFCOM to RF4		-	18	-	dB
RF2 to RF1	Logic State: RF2 to RFCOM	-	23	-	dB
RF2 to RF3		-	23	-	dB
RF2 to RF4		-	18	-	dB
RFCOM to RF1		-	22	-	dB
RFCOM to RF3		-	18	-	dB
RFCOM to RF4		-	19	-	dB
RF3 to RF1	Logic State: RF3 to RFCOM	-	18	-	dB
RF3 to RF2		-	23	-	dB
RF3 to RF4		-	22	-	dB
RFCOM to RF1		-	24	-	dB
RFCOM to RF2		-	23	-	dB
RFCOM to RF4		-	19	-	dB
RF4 to RF1	Logic State: RF4 to RFCOM	-	23	-	dB
RF4 to RF2		-	19	-	dB
RF4 to RF3		-	22	-	dB
RFCOM to RF1		-	22	-	dB
RFCOM to RF2		-	18	-	dB
RFCOM to RF3		-	24	-	dB

Frequency Range		5000		6000	MHz
Isolation					
RF1 to RF2	Logic State: RF1 to RFCOM	-	22	-	dB
RF1 to RF3		-	16	-	dB
RF1 to RF4		-	23	-	dB
RFCOM to RF2		-	22	-	dB
RFCOM to RF3		-	17	-	dB
RFCOM to RF4		-	17	-	dB
RF2 to RF1	Logic State: RF2 to RFCOM	-	22	-	dB
RF2 to RF3		-	22	-	dB
RF2 to RF4		-	17	-	dB
RFCOM to RF1		-	22	-	dB
RFCOM to RF3		-	17	-	dB
RFCOM to RF4		-	17	-	dB
RF3 to RF1	Logic State: RF3 to RFCOM	-	17	-	dB
RF3 to RF2		-	22	-	dB
RF3 to RF4		-	20	-	dB
RFCOM to RF1		-	22	-	dB
RFCOM to RF2		-	22	-	dB
RFCOM to RF4		-	17	-	dB
RF4 to RF1	Logic State: RF4 to RFCOM	-	22	-	dB
RF4 to RF2		-	18	-	dB
RF4 to RF3		-	20	-	dB
RFCOM to RF1		-	22	-	dB
RFCOM to RF2		-	22	-	dB
RFCOM to RF3		-	17	-	dB
PARAMETER	**CONDITIONS**	**MIN.**	**TYP.**	**MAX.**	**UNITS**
Harmonics					
3Fo (B17)	fo = 704MHz; P_{in} = 25dBm; CW	-	-88	-70	dBm
2Fo (B8)	fo = 897.5MHz; P_{in} = 25dBm; CW	-	-99	-76	dBm
2Fo (GSM 850/900)	fo = 824 – 915MHz; Pin = 35dBm; CW	-	-69	-55	dBm
3Fo (GSM 850/900)	fo = 824 – 915MHz; Pin = 35dBm; CW	-	-56	-45	dBm
≥ 4Fo - 12.75GHz (GSM 850/900)	fo = 824 – 915MHz; Pin = 35dBm; CW	-	-94	-60	dBm
2Fo (GSM DCS/PCS)	fo = 1710 – 1980MHz; Pin = 32dBm; CW	-	-72	-57	dBm
3Fo (GSM DCS/PCS)	fo = 1710 – 1980MHz; Pin = 32dBm; CW	-	-62	-45	dBm
≥ 4Fo - 12.75GHz (GSM DCS/PCS)	fo = 1710 – 1980MHz; Pin = 32dBm; CW	-	-102	-60	dBm
IMD2	Ftx = 20dBm; Fint = -15dBm				
Band VIII	Ftx = 880 MHz, Fint = 1805 MHz, Fmeas = 925 MHz, Measure on all Pins	-	-123	-110	dBm
Band II	Ftx = 1880 MHz, Fint = 3840 MHz, Fmeas = 1960 MHz, Measure on all Pins	-	-121	-110	dBm
Band VII	Ftx = 2535 MHz, Fint = 5190 MHz, Fmeas = 2655 MHz, Measure on all Pins	-	-123	-110	dBm

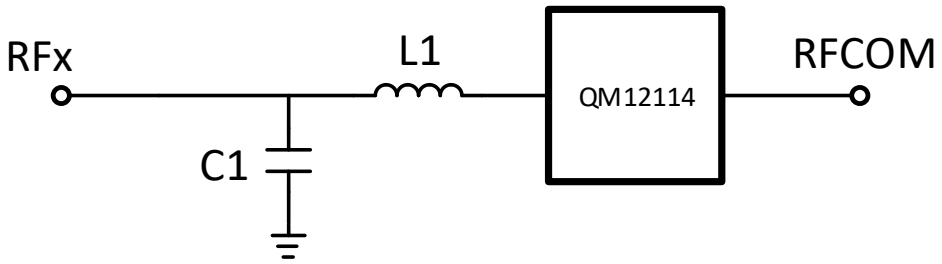
IMD3	Ftx = 20dBm; Fint = -15dBm				
Band VIII	Ftx = 897.5 MHz, Fint = 852.5 MHz, Fmeas = 942.5 MHz, Measure on all Pins	-	-124	-110	dBm
Band II	Ftx = 1880 MHz, Fint = 1800 MHz, Fmeas = 1960 MHz, Measure on all Pins	-	-126	-110	dBm
Band VII	Ftx = 2535 MHz, Fint = 2415 MHz, Fmeas = 2655 MHz, Measure on all Pins	-	-125	-110	dBm
Return Loss					
RF1, RF2, RF3, RF4, RFCOM	698 MHz to 960 MHz	15	21		dB
RF1, RF2, RF3, RF4, RFCOM	1700 MHz to 2700 MHz	13	17		dB
RF1, RF2, RF3, RF4, RFCOM	3200 MHz to 3800 MHz	10	15		dB

*See tuning schematic for 5000MHz to 6000MHz insertion loss

Application Circuit Schematic

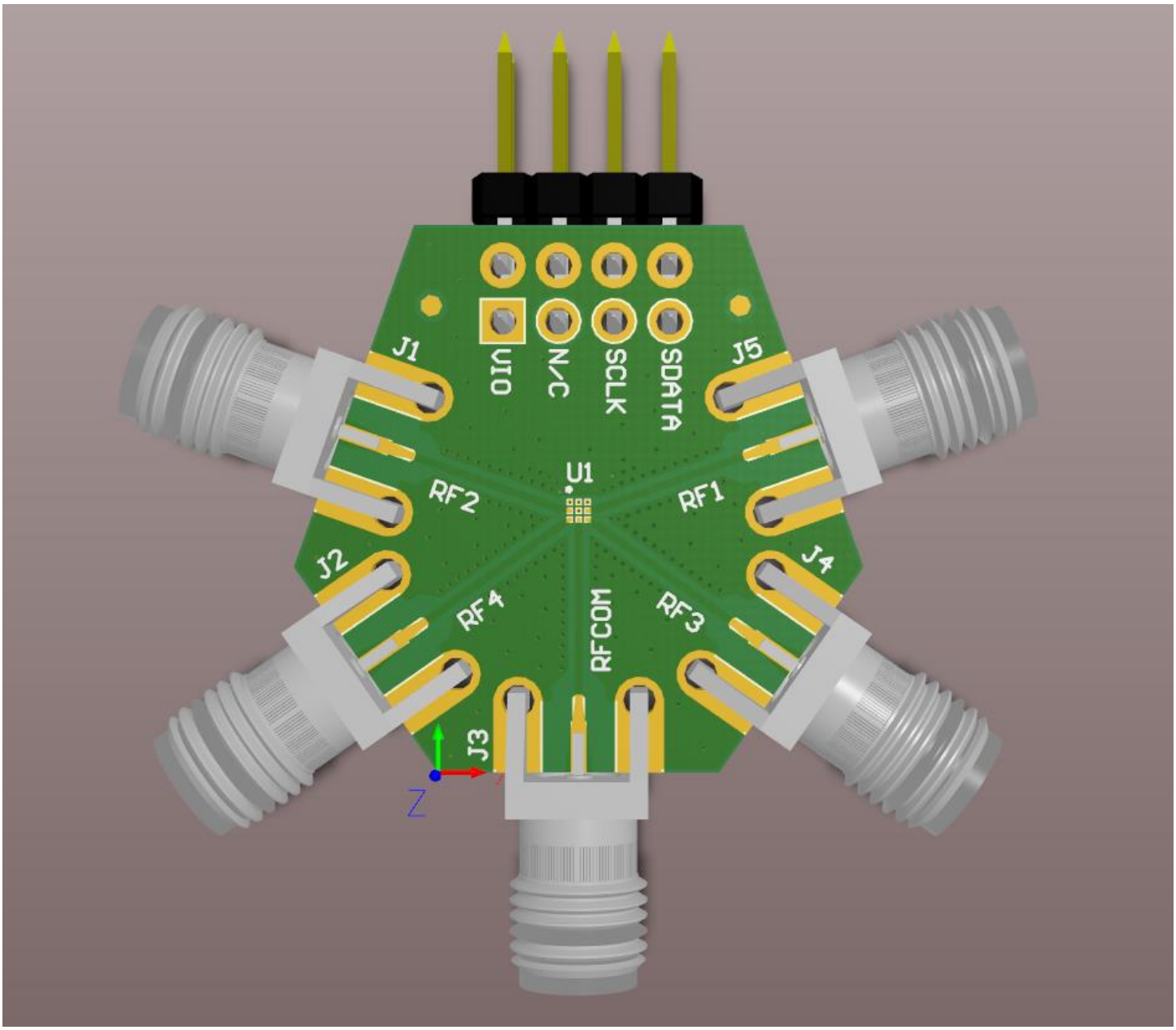


Tuning Schematic for HB to UHB

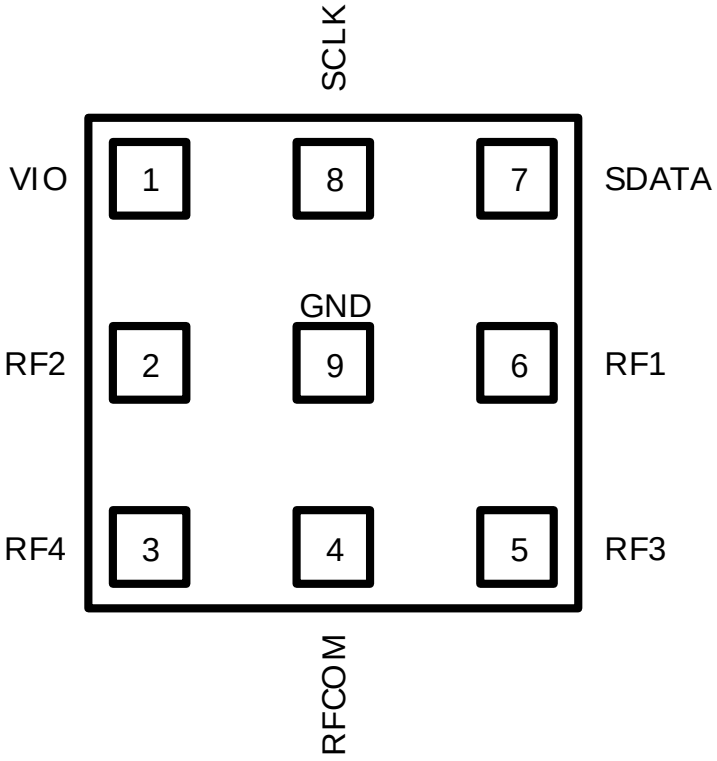


NAME	VALUE	PACKAGE	DESCRIPTION
C1	0.5pF	0201	Matching for optimized RF performance*
L1	1.5nH	0201	Matching for optimized RF performance*

* Matching elements are subject to change based on specific system application


VIO
N/C
SCLK
SDATA
J1
J5
U1
RF2
RF1
J2
J4
RF4
RFCOM
RF3
J3
Z

Pin Configuration and Description



Top View

PIN NO.	LABEL	DESCRIPTION
1	VIO	Voltage Supply
2	RF2	RF port
3	RF4	RF port
4	RFCOM	RF common port
5	RF3	RF port
6	RF1	RF port
7	SDATA	RFFE Data Signal
8	SCLK	RFFE Data Signal
9	GND	Ground

RFFE Register Map

Register 0x0000 – SW_CTRL0

Bit(s)	Field Name	Description	Reset	B/G	Trig	R/W
7:4	SPARE	Reserved for future use	0x0	No	0 - 2	R/W
6:0	SW_CTRL	0x00: Isolation 0x01: RF1 - RFC 0x02: RF2 - RFC 0x04: RF3 - RFC 0x08: RF4 - RFC	0x00	No	0-2	R/W

Register 0x0001 – SPARE

Bit(s)	Field Name	Description	Reset	B/G	Trig	R/W
7:0	SPARE	Reserved for future use	0x00	No	0 - 2	R/W

Register 0x001A – RFFE_STATUS

Bit(s)	Field Name	Description	Reset	B/G	Trig	R/W
7	UDR_RST	Setting this bit initiates a software reset *Note: On software reset, this register and all User Defined registers (UDRs) are reset. This bit will always read as 0.*	0	No	No	W
6	CMD_FR_P_ERR	Command Frame received with a parity error	0	No	No	R/W
5	CMD_LEN_ERR	Command Sequence received with an incorrect length	0	No	No	R/W
4	ADDR_FR_P_ERR	Address Frame received with a parity error	0	No	No	R/W
3	DATA_FR_P_ERR	Data Frame received with a parity error	0	No	No	R/W
2	RD_INVLD_ADDR	Read Command Sequence received with an invalid address	0	No	No	R/W
1	WR_INVLD_ADDR	Write Command Sequence received with an invalid address	0	No	No	R/W
0	BID_GID_ERR	Read Command Sequence received with a BSID or GSID	0	No	No	R/W
		Note: Reading this register resets this register.				

Register 0x001B – GSID

Bit(s)	Field Name	Description	Reset	B/G	Trig	R/W
7:4	GSID0[3:0]	Group Slave ID0	0x0	No	No	R/W
3:0	GSID1[3:0]	Group Slave ID1	0x0	No	No	R/W

Register 0x001C — PM_TRIG

Bit(s)	Field Name	Description	Reset	B/G	Trig	R/W
7:6	PWR_MODE[1:0]	00: ACTIVE - Normal Operation 01: STARTUP - Reset all registers to default settings 10: ACTIVE - Low Power - Antenna in isolation 11: STARTUP - Reset all registers to default settings *Note: Setting PWR_MODE to STARTUP is identical to a hardware reset initiated by the VIO signal.*	0b10	B/G	No	R/W
5:3	TriggerMask[2:0]	Setting bit TriggerMask[N] disables Trigger[N] TriggerMask[N] updates before Trigger[N] is processed *Note: When Trigger[N] is disabled, writing to a register associated with Trigger[N] sends data directly to that register.* *If a register is associated with multiple triggers, then all associated triggers must be disabled to allow direct writes to the associated register.*	0b000	No	No	R/W
2:0	Trigger[2:0]	Setting bit Trigger[N] loads Trigger[N]'s associated registers *Note: When Trigger[N] is enabled, writing to a register associated with Trigger[N] sends data to that register's shadow. Setting the Trigger[N] bit loads data from shadow. All triggers are processed immediately and simultaneously and then cleared. Trigger[0], [1], and [2] will always read as 0.*	0b000	B/G	No	W

Register 0x001D — PRODUCT_ID

Bit(s)	Field Name	Description	Reset	B/G	Trig	R/W
7:0	PROD_ID[7:0]	Lower eight bits of Product Number *Note: These are read-only registers. However, as part of the special programming sequence for writing USID, a write command sequence is performed on one or both registers, but does not update them. See MIPI 6.6.2 for details.*	0x17	No	No	R

Register 0x001E — MANUFACTURER_ID

Bit(s)	Field Name	Description	Reset	B/G	Trig	R/W
7:0	MFG_ID[7:0]	Lower eight bits of MIPI Manufacturer ID *Note: These are read-only registers. However, as part of the special programming sequence for writing USID, a write command sequence is performed on one or both registers, but does not update them. See MIPI 6.6.2 for details.*	0x34	No	No	R

Register 0x001F – MAN_USID

Bit(s)	Field Name	Description	Reset	B/G	Trig	R/W
7:6	RESERVED	Reserved for future use	0b00	No	No	R
5:4	MFG_ID[9:8]	Upper two bits of MIPI Manufacturer ID *Note: This is a read-only register. However, as part of the special programming sequence for writing USID, a write command sequence is performed on this register, but does not update it. See MIPI 6.6.2 for details.*	0b01	No	No	R
3:0	USID[3:0]	Programmable Unique Slave ID *Note: USID is only writeable using a special programming sequence. See MIPI 6.6.2 for details.*	0x8	No	No	R/W

Register 0x0021 – REVISION_ID

Bit(s)	Field Name	Description	Reset	B/G	Trig	R/W
7:6	MAJOR_REV[1:0]	Major Revisions - all layer	0b00	No	No	R
5:4	MINOR_REV[1:0]	Minor Revisions - metal only	0b00	No	No	R
3:0	MISC_REV[3:0]	Misc Revisions - mask variants	0b0001	No	No	R
		Note: The REVISION_ID register contains this product's revision number which is set by Qorvo according to manufacture date. The value may change throughout the product life cycle.				

Power On and Off Sequence

It is very important that the user adheres to the correct timing sequences in order to avoid damaging the device. Figures are NOT drawn to scale.

1. Once VIO is powered down to 0V, wait a minimum of 10 µs to reapply power to VIO. (see figure 3)

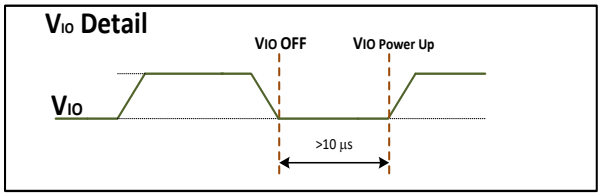


Figure 1 Digital Supply Detail

2. VIO must be applied for a minimum of 120 ns before sending SDATA/SCLK to ensure correct data transmission. (see figure 5)
3. VIO must be applied for a minimum of 15 µs before applying RF power. (see figure 5)
4. Wait a minimum of 5 µs after RFFE bus is idle to apply an RF signal. (see figure 5)

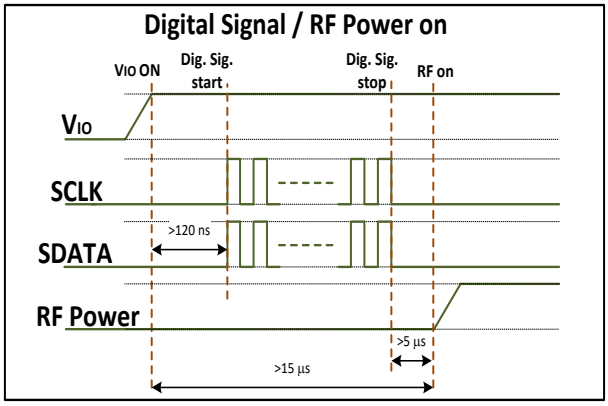


Figure 2 Digtial Signal / RF Power-On Detail

5. RF power must not be applied during switching events. To ensure this, remove RF power before completing a register write that will change the switch mode. (see figure 6)

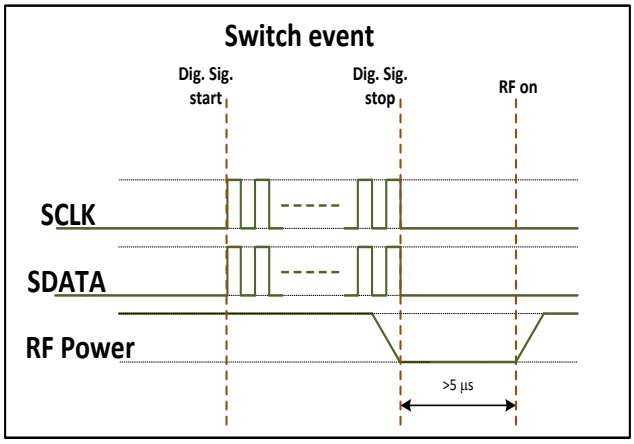


Figure 3 Switch Event Timing

6. If “Low Power Mode” is utilized, there must be a delay of 10 μs before exiting “Low Power Mode”. (see figure 7)

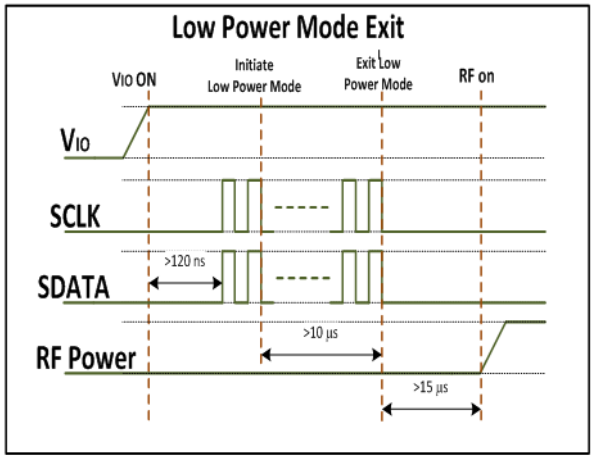
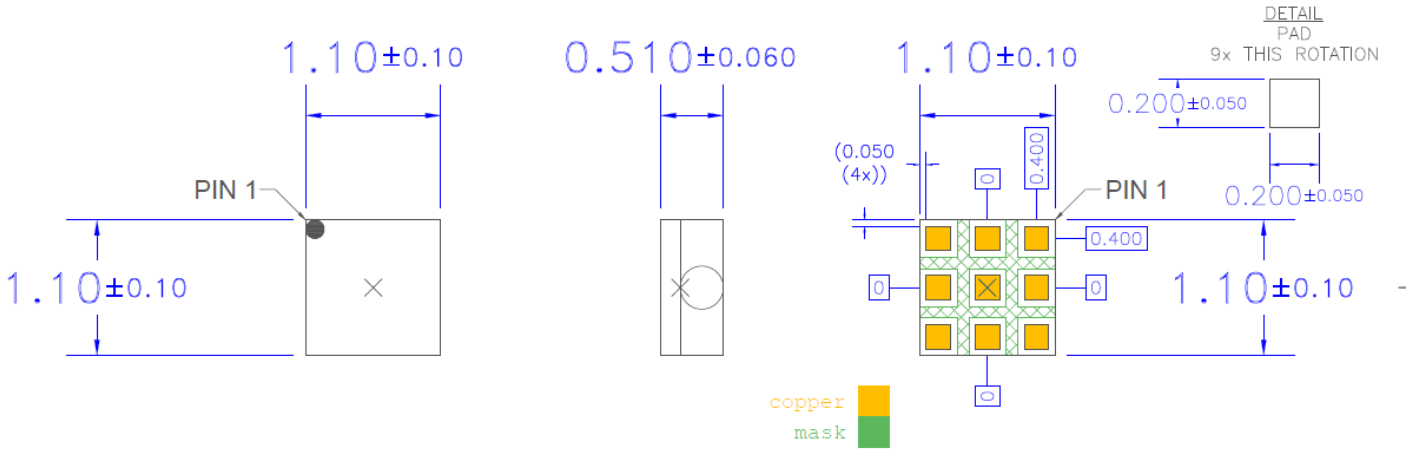


Figure 4 Low Power Mode Exit Timing

Mechanical Information

Package Drawing



TOP VIEW | SIDE VIEW | BOTTOM VIEW

RECOMMENDED LAND PATTERN | RECOMMENDED LAND PATTERN MASK

Notes:

1. All dimensions are in milimeters. Angles are in degrees.
2. Dimension and tolerance formats conform to ASME Y14.4M-1994.
3. The terminal #1 identifier and terminal numbering conform to JESD 95-1 SPP-012.

Handling Precautions

PARAMETER	RATING	STANDARD
ESD – Human Body Model (HBM)	Class 1C	ESDA/JEDEC JS-001-2012
MSL – Moisture Sensitivity Level	Level 3	IPC/JEDEC J-STD-020

Caution!

ESD sensitive device

Solderability

Compatible with both lead-free (260 °C max. reflow temperature) and tin/lead (245 °C max. reflow temperature) soldering processes.

Package lead plating: Electrolytic plated Au over Ni

RoHS Compliance

This part is compliant with the 2011/65/EU RoHS directive (Restrictions on the Use of Certain Hazardous Substances in Electrical and Electronic Equipment), as amended by Directive 2015/863/EU.

This product also has the following attributes:

- Lead free
- Halogen Free (Chlorine, Bromine)
- Antimony Free
- TBBP-A ($C_{15}H_{12}Br_4O_2$) Free
- SVHC Free

Revision History

Revision Code	Comments
DS20170830	Initial Release
DS20200504	Updated DS with n7, n40, n41, n77, n78, n79 frequencies

Contact Information

For the latest specifications, additional product information, worldwide sales and distribution locations:

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