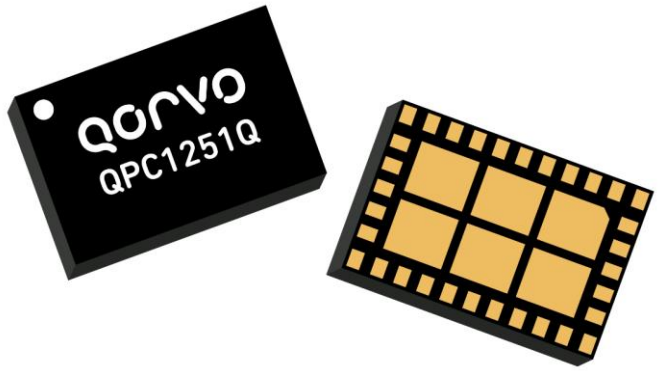
QPC1251Q

BROADBAND HIGH LINEARITY e-CALL ANTENNA ROUTING SWITCH

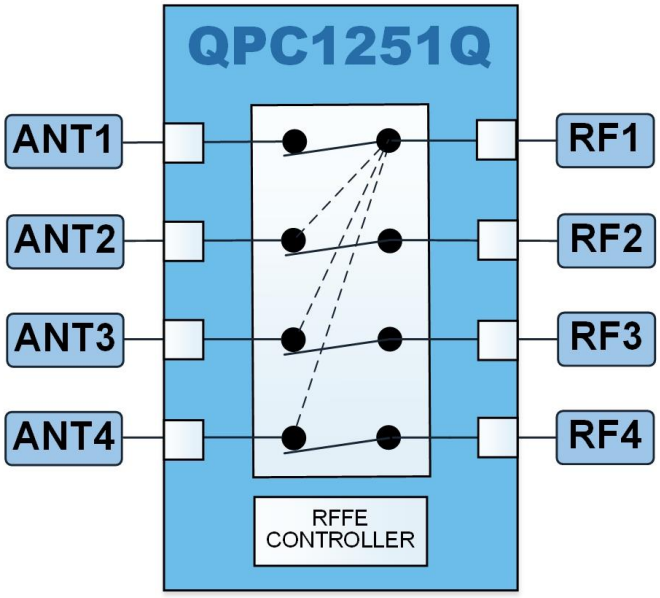
Product Overview

The QPC1251Q is a low loss, high linearity antenna routing switch that is designed to enable Emergency Calling (e-Call) functionality in the telematics control unit (TCU). In the case of an emergency situation where antennas may become damaged or covered, the QPC1251Q allows a primary cellular link to be switched to other antennas in the automobile to establish emergency communication. The control interface for the QPC1251Q is an RFFE serial control system that is compliant with the V2.1 MIPI standard.



32 Pin 4.0 x 6.0 X 0.58 mm Module

Functional Block Diagram



Switches shown in normal operation mode

Dashed lines indicate e-Call modes

Key Features

- Qualified to AEC-Q100 Grade 2
- Excellent insertion loss and Isolation performance
- High linearity
- RFFE V2.1 control interface
- Broadband performance suitable for multiple air Interfaces including 5G applications up to 6 GHz
- Very low current consumption
- DC blocking capacitors not required in typical application
- Single Vio supply
- Hot Switching Input power up to +37 dBm

Applications

- eCall switching applications
- Telematic Control Unit Modules

Part Number	Description
QPC1251QSB	5 Piece Sample Bag
QPC1251QSR	100 Piece 7” Short Reel
QPC1251QDK	Design Kit
QPC1251QTR13	13" tape and reel, 2500

Absolute Maximum Ratings

Parameter	Conditions	Rating
Storage Temperature		-40 to +125 °C
V_{IO}, SDATA, SCLK, & SID		-0.5 to +2.2 V
Maximum Input Power	Momentary Infrequent Occurence, 1:1 VSWR, 50% DC, +105°C	+36.0 dBm
	CW Power, 1:1 VSWR, 100%DC, +25°C, Continuous Operation	+36.0 dBm
	CW Power, 1:1 VSWR, 50% DC, +105°C, Continuous Operation	+34.5 dBm
	CW Power, 1:1 VSWR, 100% DC, +105°C, Continuous Operation	+32.5 dBm
Hot-Switching Input Power	CW Power, 1:1 VSWR, 50% DC, -40 to +105C, > 1E6 cycles	+37.0 dBm

Operation of this device outside the parameter ranges given above may cause permanent damage.

Recommended Operating Conditions

Parameter	Min.	Typ.	Max.	Units
Operating Ambient Temperature	-40	25	+105	˚C
V_{IO} Interface Supply Voltage High	1.65	1.8	1.95	V
V_{IO} Interface Supply Voltage Low	0	0	0.45	V
SDATA, SCLK – Voltage High	0.8 x V_{IO}	1.8	V_{IO}	V
SDATA, SCLK – Voltage Low	0.00	0.00	0.2 x V_{IO}	V
V_{IO} Interface Supply current		25	40	µA
Switching Time -- Switch RF path from 10% to 90%		3.5	5.5	µS

Electrical specifications are measured at specified test conditions. Specifications are not guaranteed over all recommended operating conditions.

Electrical Specifications[1]

Test conditions unless otherwise stated: all unused RF ports terminated in 50Ω, Input and Output = 50Ω, T = 25°C, V_{IO}/SDATA/SCLK = 1.8 V / 0 V

PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Insertion Loss					
RF1-ANT1 (primary path)	617 – 960 MHz		0.65	1.1	dB
RF1-ANT2/3/4 (e-Call modes)	617 – 960 MHz		0.65	1.1	dB
RF2-ANT2	617 – 960 MHz		0.4	0.8	dB
RF3-ANT3	617 – 960 MHz		0.4	0.8	dB
RF4-ANT4	617 – 960 MHz		0.6	1.0	dB

PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Insertion Loss					
RF1-ANT1 (primary path)	1427 – 2690 MHz		0.8	1.2	dB
RF1-ANT2/3/4 (e-Call modes)	1427 – 2690 MHz		0.8	1.2	dB
RF2-ANT2	1427 – 2690 MHz		0.55	1.0	dB
RF3-ANT3	1427 – 2690 MHz		0.55	1.0	dB
RF4-ANT4	1427 – 2690 MHz		0.75	1.05	dB

PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Insertion Loss					
RF1-ANT1 (primary path)	3300 – 6000 MHz		0.95	1.5	dB
RF1-ANT2/3/4 (e-Call modes)	3300 – 6000 MHz		0.95	1.5	dB
RF2-ANT2	3300 – 6000 MHz		0.7	1.4	dB
RF3-ANT3	3300 – 6000 MHz		0.7	1.4	dB
RF4-ANT4	3300 – 6000 MHz		0.9	1.5	dB

PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Isolation					
Any Active Port to any other Active Port	617 MHz to 960 MHz	40	45		dB
	1427 MHz to 2690 MHz	35	40		dB
	3300 MHz to 6000 MHz	25	30		dB

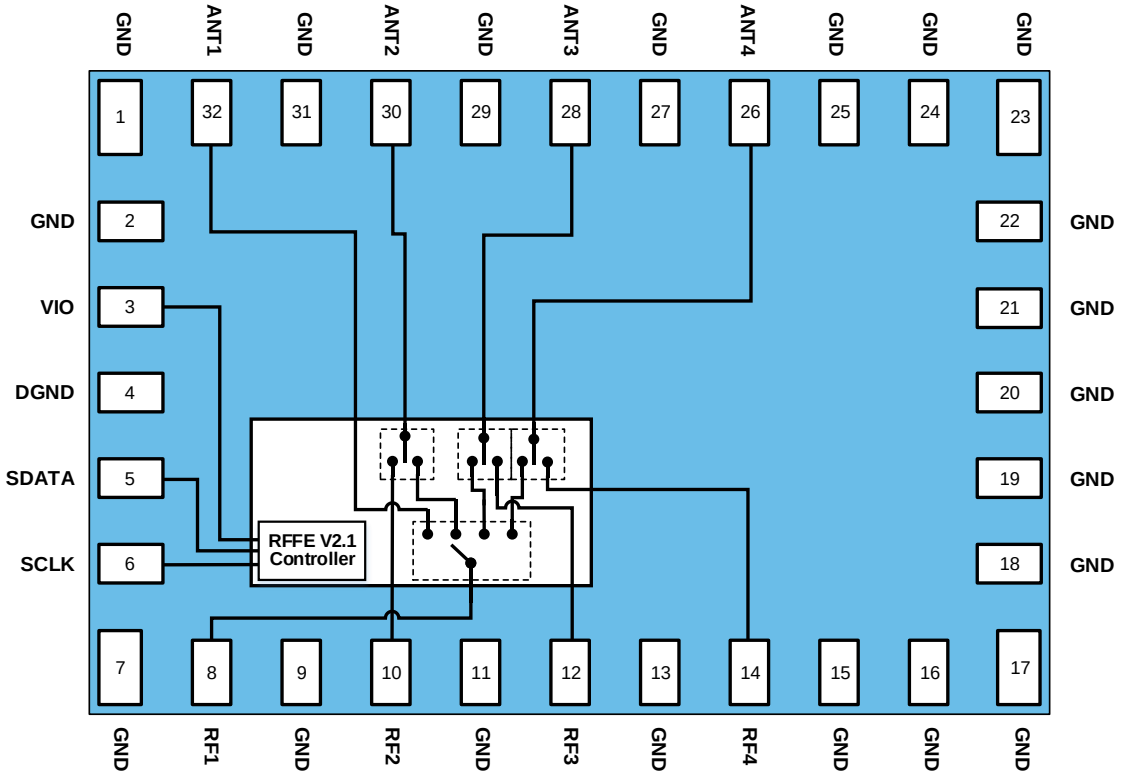
PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Harmonics	**Any Active Path**				
2nd Harmonic	Freq = 915 MHz; P_{IN} = 36 dBm		-95		dBc
3rd Harmonic			-80		dBc
2nd Harmonic	Freq = 1980 MHz; P_{IN} = 33 dBm		-95		dBc
3rd Harmonic			-85		dBc
2nd Harmonic	Freq = 2400 MHz; P_{IN} = 33 dBm		-100	-90	dBc
3rd Harmonic			-90	-78	dBc

PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Intermodulation	**Any Active Path**				
INPUT IP2	f1=2550MHz, f2=120MHz, Pin1=20dBm, Pin2=-15dBm, Rx=2670MHz		120		dBm
INPUT IP3	f1=2535MHz, f2=2415MHz, Pin1=Pin2=25dBm/tone, Rx=2655MHz		72		dBm

PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Return Loss	**Any Active Path**				
	617 MHz to 960 MHz		-24		dB
	1427 MHz to 2700 MHz		-22		dB
	3300 MHz to 6000 MHz		-17		dB

1) Recommended EVB schematic/layout/BOM/PCB to be followed in order to achieve specified performance.

Pin Configuration and Description



Top View

Pin-out Description

PIN	LABEL	DESCRIPTION
3	VIO	Supply voltage for the MIPI RFFE serial interface
5	SDATA	Data I/O signal for the MIPI RFFE serial interface
6	SCLK	Serial interface clock input signal
8	RF1	Cellular modem RF port connection
10	RF2	Cellular modem RF port connection
12	RF3	Cellular modem RF port connection
14	RF4	Cellular modem RF port connection
26	ANT4	Antenna port connection
28	ANT3	Antenna port connection
30	ANT2	Antenna port connection
32	ANT1	Antenna port connection
1, 2, 7, 9, 11, 13, 15, 16, 17, 18, 19, 20, 21, 22, 23, 24, 25, 27, 29, 31	GND	Pins connected to module ground
4	DGND	Digital Ground
GND PAD	GND PAD	Ground

Switch Control Logic Truth Table

Antenna connections				RFFE Reg(0x01)							
ANT1	ANT2	ANT3	ANT4	r0_b7	r0_b6	r0_b5	r0_b4	r0_b3	r0_b2	r0_b1	r0_b0
OFF	OFF	OFF	OFF	0	0	0	0	0	0	0	0
RF1	OFF	OFF	OFF	0	0	0	0	0	0	0	1
RF1	OFF	OFF	RF4	0	0	0	0	0	0	1	0
RF1	OFF	RF3	OFF	0	0	0	0	0	1	0	0
RF1	OFF	RF3	RF4	0	0	0	0	0	1	0	1
RF1	RF2	OFF	OFF	0	0	0	0	0	1	1	1
RF1	RF2	OFF	RF4	0	0	0	0	1	0	0	0
RF1	RF2	RF3	OFF	0	0	0	0	1	0	1	0
RF1	RF2	RF3	RF4	0	0	0	0	1	0	1	1
OFF	RF1	OFF	OFF	0	0	0	0	1	1	0	1
OFF	RF1	OFF	RF4	0	0	0	0	1	1	1	0
OFF	RF1	RF3	OFF	0	0	0	1	0	0	0	0
OFF	RF1	RF3	RF4	0	0	0	1	0	0	0	1
OFF	OFF	RF1	OFF	0	0	0	1	0	0	1	1
OFF	OFF	RF1	RF4	0	0	0	1	0	1	0	0
OFF	RF2	RF1	OFF	0	0	0	1	0	1	1	0
OFF	RF2	RF1	RF4	0	0	0	1	0	1	1	1
OFF	OFF	OFF	RF1	0	0	0	1	1	0	0	1
OFF	OFF	RF3	RF1	0	0	0	1	1	0	1	0
OFF	RF2	OFF	RF1	0	0	0	1	1	0	1	1
OFF	RF2	RF3	RF1	0	0	0	1	1	1	0	0
OFF	OFF	OFF	RF4	0	0	0	1	1	1	0	1
OFF	OFF	RF3	OFF	0	0	0	1	1	1	1	1
OFF	OFF	RF3	RF4	0	0	1	0	0	0	0	0
OFF	RF2	OFF	OFF	0	0	1	0	0	0	1	0
OFF	RF2	OFF	RF4	0	0	1	0	0	0	1	1
OFF	RF2	RF3	OFF	0	0	1	0	0	1	0	1
OFF	RF2	RF3	RF4	0	0	1	0	0	1	1	0

MIPI RFFE Register Configuration

Reg00 (0x00) – Reserved

Bit(s)	Field Name	Description	Reset	B/G	Trig	R/WM
7:0	SPARE	Reserved for future use	0x00	No	0	R/WM
		Note: See Truth Table for example of operation				

Reg01 (0x01) – ECALL CONFIG

Bit(s)	Field Name	Description	Reset	B/G	Trig	R/WM
7:0	ECALL_SELECT[7:0]	RF Switch Path Connections 0b00000000 (0x00) Switch OFF state; High Isolation 0b00000001 (0x01) ANT1-RF1 0b00000010 (0x02) ANT1-RF1, ANT4-RF4 0b00000100 (0x04) ANT1-RF1, ANT3-RF3 0b00000101 (0x05) ANT1-RF1, ANT3-RF3, ANT4-RF4 0b00000111 (0x07) ANT1-RF1, ANT2-RF2 0b00001000 (0x08) ANT1-RF1, ANT2-RF2, ANT4-RF4 0b00001010 (0x0A) ANT1-RF1, ANT2-RF2, ANT3-RF3 0b00001011 (0x0B) ANT1-RF1, ANT2-RF2, ANT3-RF3, ANT4-RF4 0b00001101 (0x0D) ANT2-RF1 0b00001110 (0x0E) ANT2-RF1, ANT4-RF4 0b00010000 (0x10) ANT2-RF1, ANT3-RF3 0b00010001 (0x11) ANT2-RF1, ANT3-RF3, ANT4-RF4 0b00010011 (0x13) ANT3-RF1 0b00010100 (0x14) ANT3-RF1, ANT4-RF4 0b00010110 (0x16) ANT3-RF1, ANT2-RF2 0b00010111 (0x17) ANT3-RF1, ANT2-RF2, ANT4-RF4 0b00011001 (0x19) ANT4-RF1 0b00011010 (0x1A) ANT4-RF1, ANT3-RF3 0b00011011 (0x1B) ANT4-RF1, ANT2-RF2 0b00011100 (0x1C) ANT4-RF1, ANT2-RF2, ANT3-RF3 0b00011101 (0x1D) ANT4-RF4 0b00011111 (0x1F) ANT3-RF3 0b00100000 (0x20) ANT3-RF3, ANT4-RF4 0b00100010 (0x22) ANT2-RF2 0b00100011 (0x23) ANT2-RF2, ANT4-RF4 0b00100101 (0x25) ANT2-RF2, ANT3-RF3 0b00100110 (0x26) ANT2-RF2, ANT3-RF3, ANT4-RF4	0x00	No	1	R/W
		Note: See Truth Table for example of operation				

Reg28 (0x1C) – PM_TRIG

Bit(s)	Field Name	Description	Reset	B/G	Trig	R/W
7	PWR_MODE[7]	0: Normal Operation (ACTIVE) 1: Low Power - Antenna Switch State Floating	1	B/G	No	R/W
6	PWR_STATE[6]	0: Normal Operation (ACTIVE) 1: INITIALIZATION STATE - Reset all registers to default settings *Note: This bit always reads 0. Writing a 1 to this bit forces a reset.*	0	B/G	No	R/W
5:3	TriggerMask[2:0]	Setting bit TriggerMask[N] disables Trigger[N] TriggerMask[N] updates before Trigger[N] is processed *Note: When Trigger[N] is disabled, writing to a register associated with Trigger[N] sends data directly to that register. If a register is associated with multiple triggers, then all associated triggers must be disabled to allow direct writes to the associated register.*	0b000	No	No	R/W
2:0	Trigger[2:0]	Setting bit Trigger[N] loads Trigger[N]'s associated registers *Note: When Trigger[N] is enabled, writing to a register associated with Trigger[N] sends data to that register's shadow. Setting the Trigger[N] bit loads data from shadow. All triggers are processed immediately and simultaneously and then cleared. Trigger[0], [1], and [2] will always read as 0.*	0b000	B/G	No	R/W

Reg29 (0x1D) – PRODUCT_ID

Bit(s)	Field Name	Description	Reset	B/G	Trig	R/W
7:0	PROD_ID[7:0]	Lower eight bits of Product Number *Note: These are read-only registers. However, as part of the special programming sequence for writing USID, a write command sequence is performed on one or both registers, but does not update them. See MIPI 6.6.2 for details.*	0x4C	No	No	R

Reg30 (0x1E) – MANUFACTURER_ID

Bit(s)	Field Name	Description	Reset	B/G	Trig	R/W
7:0	MFG_ID[7:0]	Lower eight bits of MIPI Manufacturer ID *Note: These are read-only registers. However, as part of the special programming sequence for writing USID, a write command sequence is performed on one or both registers, but does not update them. See MIPI 6.6.2 for details.*	0xC6	No	No	R

Reg31 (0x1F) – MANUFACTURER_US_ID

Bit(s)	Field Name	Description	Reset	B/G	Trig	R/W
7:4	MFG_ID[11:8]	Upper four bits of MIPI Manufacturer ID *Note: This is a read-only register. However, as part of the special programming sequence for writing USID, a write command sequence is performed on this register, but does not update it. See MIPI 6.6.2 for details.*	0x3	No	No	R
3:0	USID[3:0]	Unique Slave ID	0xA	No	No	R

Reg32 (0x20) – EXT_PRODUCT_ID

Bit(s)	Field Name	Description	Reset	B/G	Trig	R/W
7:0	EXT_PROD_ID[15:8]	Upper eight bits of Product Number *Note: These are read-only registers. However, as part of the special programming sequence for writing USID, a write command sequence is performed on one or both registers, but does not update them. See MIPI 6.6.2 for details.*	0x00	No	No	R

Reg34 (0x22) – GROUP_ID2

Bit(s)	Field Name	Description	Reset	B/G	Trig	R/W
7:4	GSID0[3:0]	Group Slave ID0	0x0	No	No	R/W
3:0	GSID1[3:0]	Group Slave ID1	0x0	No	No	R/W

Reg35 (0x23) – UDR_RST

Bit(s)	Field Name	Description	Reset	B/G	Trig	R/W
7	SW_RESET[7]	Setting this bit initiates a software reset *Note: On software reset, this register and all User Defined registers (UDRs) are reset. This bit will always read as 0.*	0	B/G	No	R/W
6:0	RESERVED		0x00	No	No	R/W

Power on Sequence

It is very important that the user adheres to the correct timing sequences in order to avoid damaging the device. Figures are NOT drawn to scale.

1. Once VIO is powered down to 0V, wait a minimum of 10 µs to reapply power to VIO. (see Figure: Digital Supply Detail)

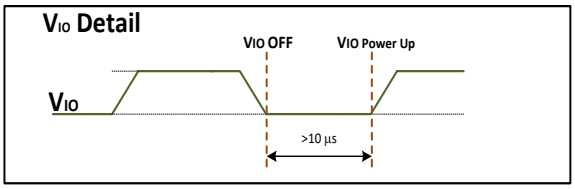


Figure: Digital Supply Detail

2. VIO must be applied for a minimum of 120 ns before sending SDATA/SCLK to ensure correct data transmission. (see Figure: RF Power-Up Detail)
3. VIO must be applied for a minimum of 15 µs before applying RF power. (see Figure: Digital Signal / RF Power-On Detail)
4. Wait a minimum of 5 µs after RFFE bus is idle to apply an RF signal. (see Figure: RF Power-Up Detail)

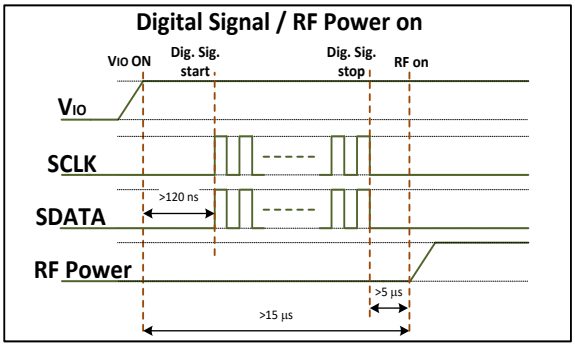


Figure: Digital Signal / RF Power-On Detail

5. RF power must not be applied during switching events. To ensure this, remove RF power before completing a register write that will change the switch mode. (see Figure: Switch Event Timing)

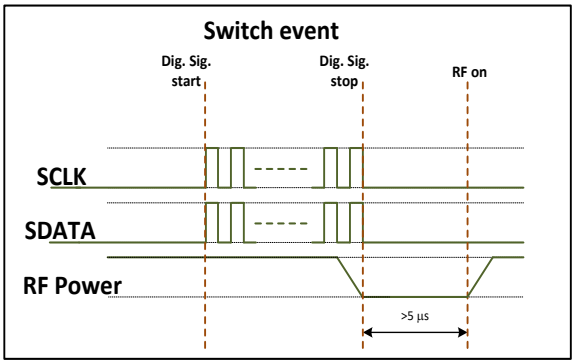


Figure: Switch Event Timing

6. If “Low Power Mode” is utilized, there must be a delay of 10 µs before exiting “Low Power Mode”. (see Figure: Low-Power Mode Exit Timimg)

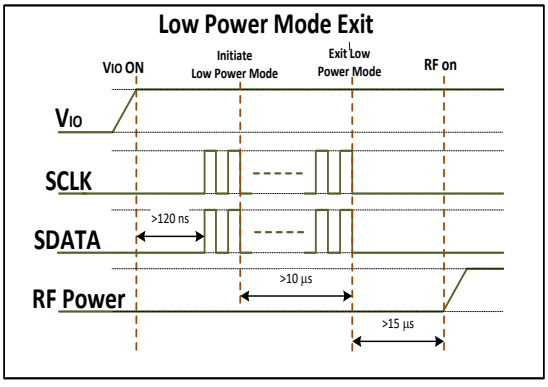
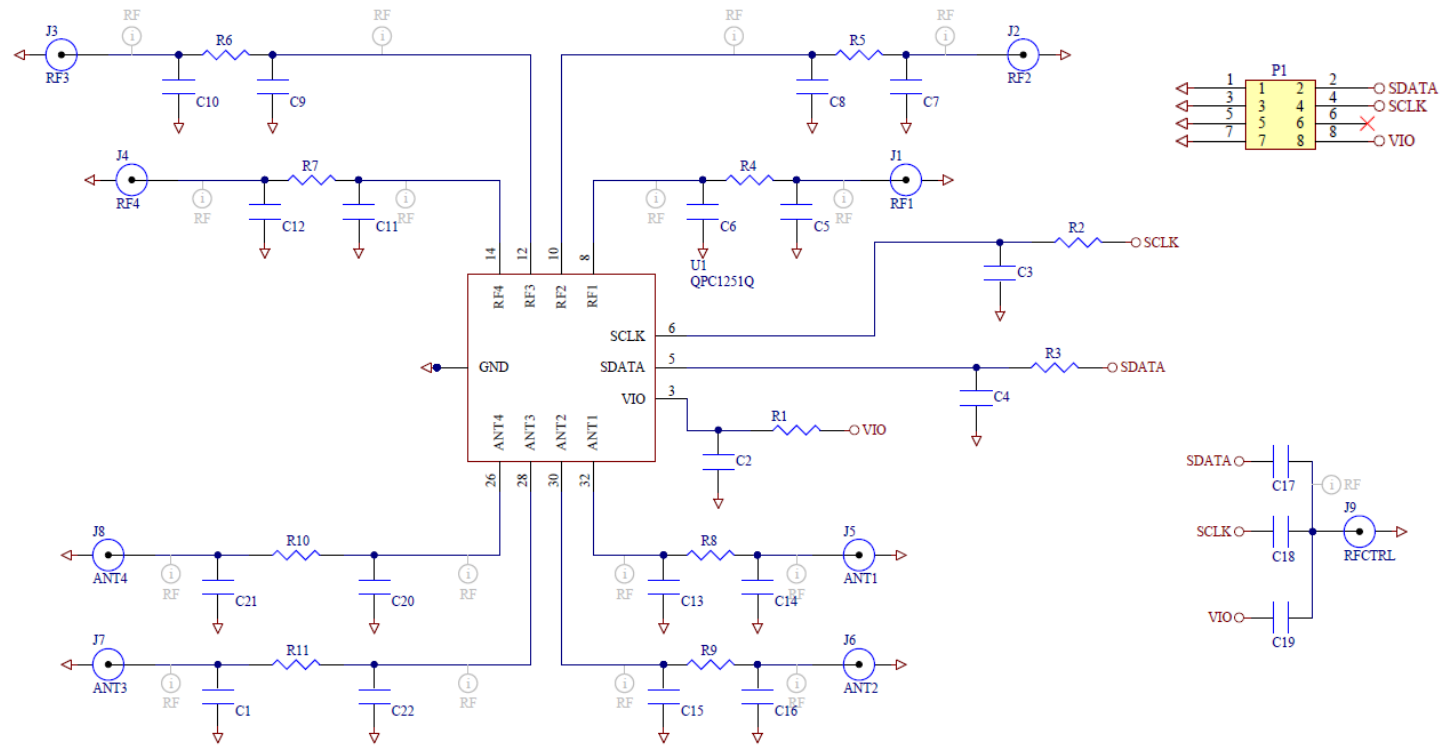


Figure: Low-Power Mode Exit Timing

Application Schematic

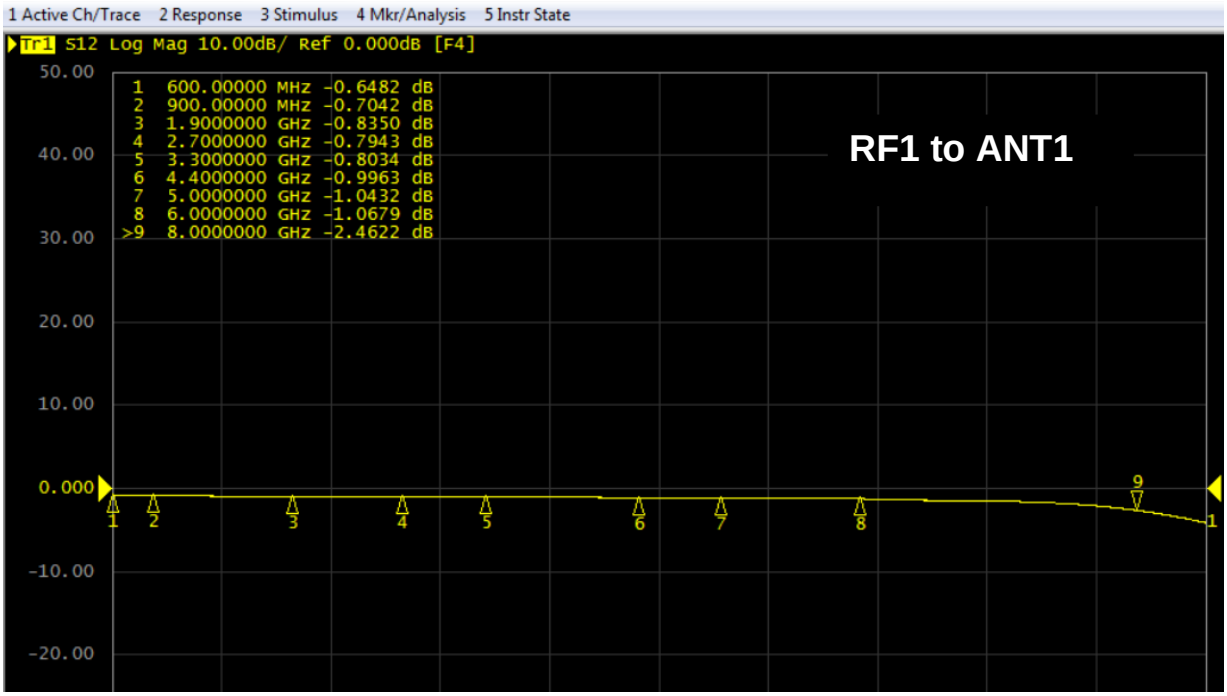


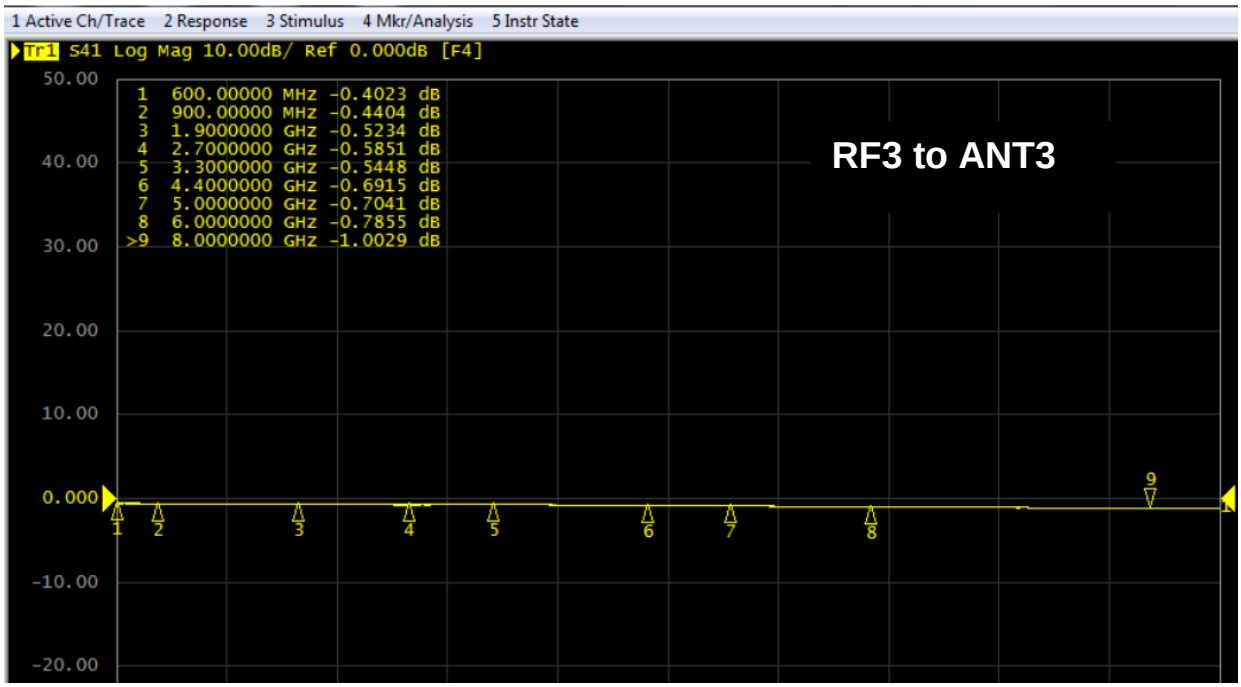
Note: In a typical application blocking caps are not required on any port. If external voltage is applied to an RF pin then recommend a blocking cap added to RF pin.

Evaluation Board BOM

Material#	Rev	Qty	Ref Des	Description
QPC1251QSB	A	1	U1	Automotive eCall Antenna Routing Switch
293219	A	1	PCB	PCB, QPC1251Q
287325	A	1	C2	CAP, 0.01uF, 10%, 16V, X7R, 0201
21253		11	R1, R2, R3, R4, R5, R6, R7, R8, R9, R10,R11	RES, 0 OHM, 5%, 1/20W, 0201
262452		9	J1, J2, J3, J4, J5, J6, J7, J8, J9	CONN, SMA, EL MINI FLT 0.068" SPE-000303
274947	A	1	P1	CONN, HDR, SHRD, RT-ANG, 2x4, 0.100"
4XXX1		19	C1, C5, C6, C7, C8, C9, C10, C11, C12, C13, C14, C15, C16, C17, C18, C19, C20...	NOT POPULATED ITEM-1
4XXX2		2	C3,C4	NOT POPULATED ITEM-2

Evaluation Board Performance

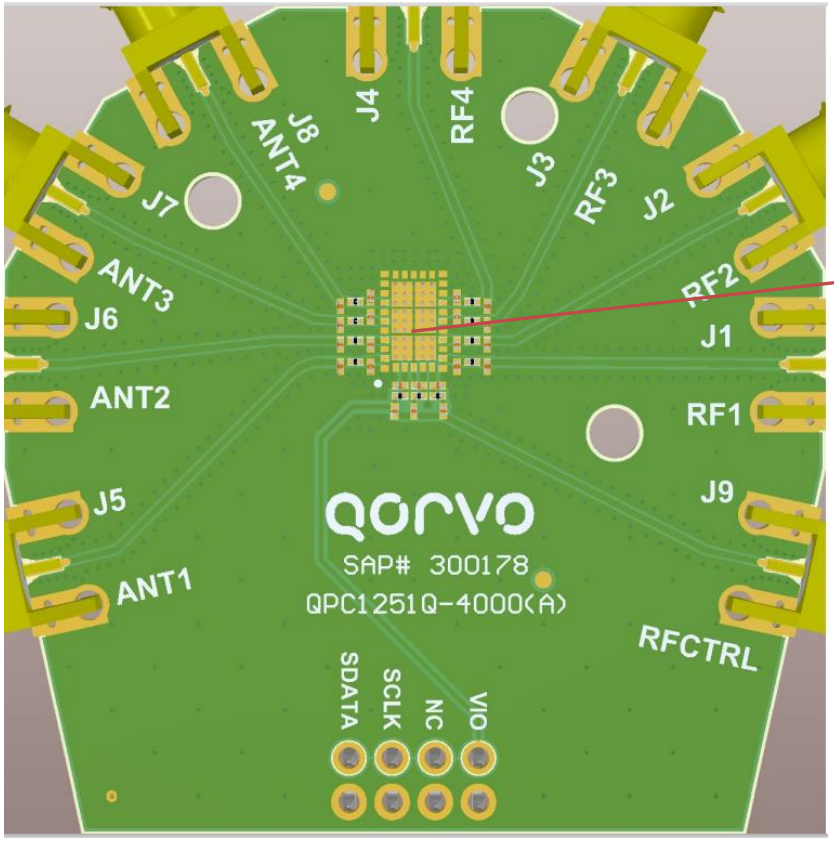


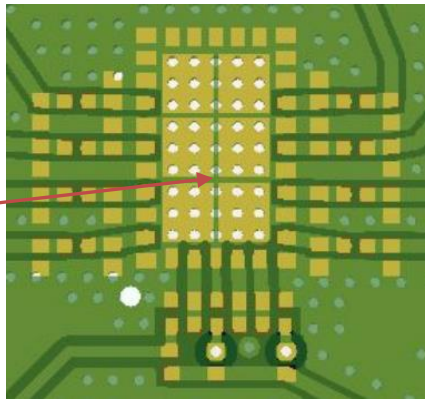


Evaluation Board Information

Layer	Name	Material	Thickness	Constant	Board Layer Stack
1	Top Overlay				
2	Top Solder	Solder Resist	0.40mil	3.5	
3	L1	Copper	1.40mil		
4	Dielectric1	RO4003	8.00mil	3.66	
5	L2	Copper	1.40mil		
6	Dielectric 3	FR-4	42.00mil	4.26	
7	L3	Copper	1.40mil		
8	Dielectric 2	FR-4	8.00mil	4.26	
9	L4	Copper	1.40mil		
10	Bottom Solder	Solder Resist	0.40mil	3.5	
11	Bottom Overlay				

TOTAL THICKNESS: .062+/- 10%

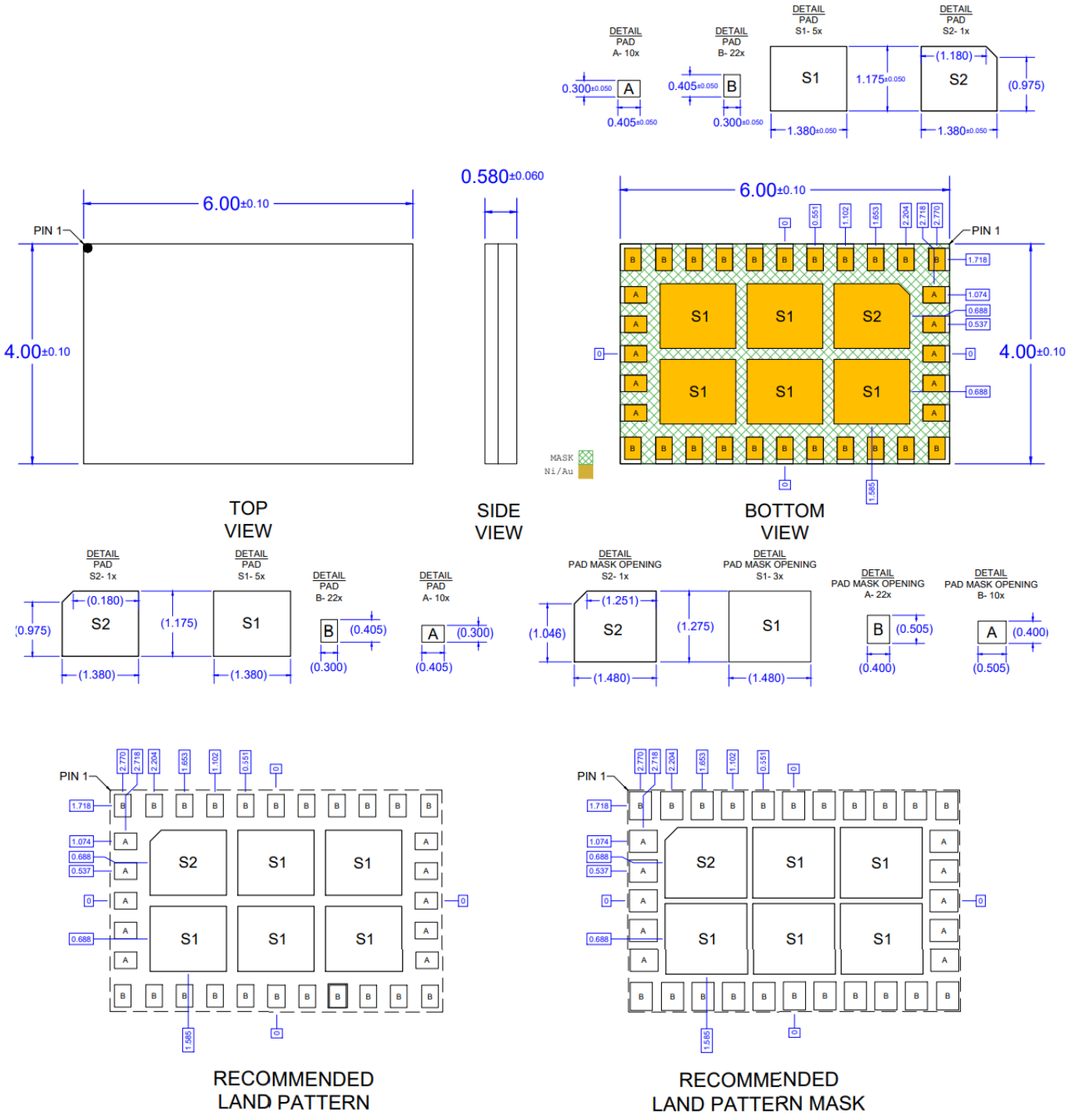




Vias placed under the Device for Electrical GND and Thermal Conductivity

Package Outline Drawing

Dimension in millimeters.



Branding Drawing

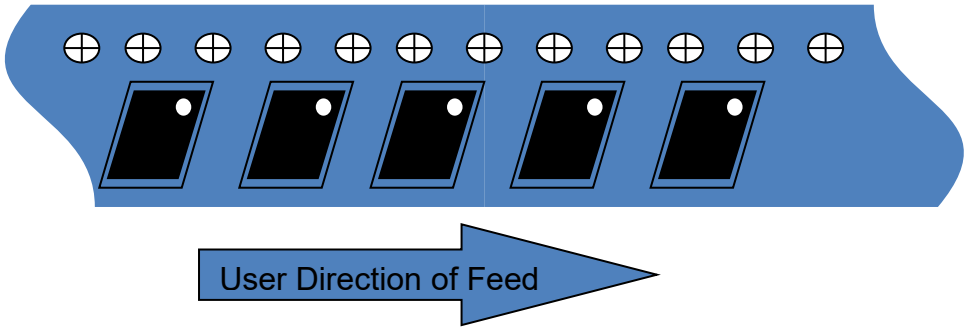
Dimension in millimeters.

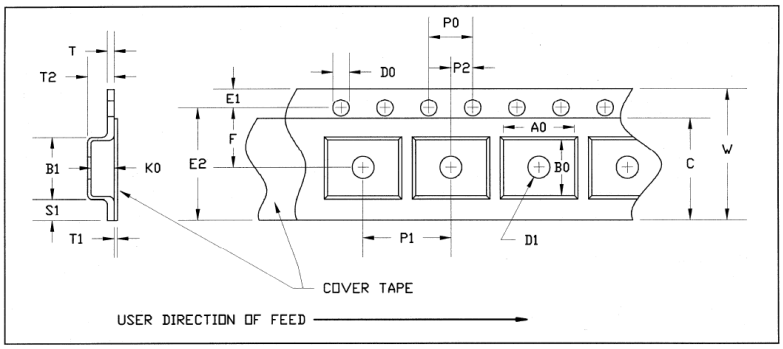
- Pin 1 Indicator
  Qorvo Logo - Use Q5D
  Trace Code to be assigned by SubCon

Tape and Reel Information – Carrier and Cover Tape Dimensions

Tape and reel specifications for this part are also available on the Qorvo website.

Standard T/R size = 2500 pieces on a 13” reel.

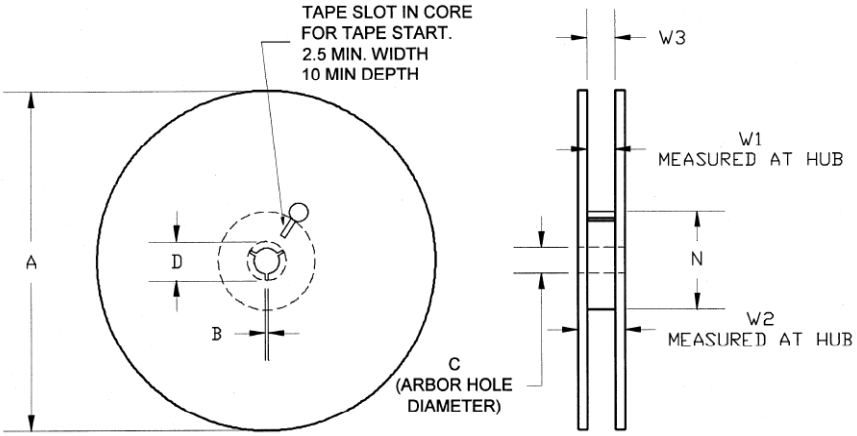




Feature	Measure	Symbol	Size (in)	Size (mm)
Cavity	Length	A0	0.167	4.25
	Width	B0	0.246	6.25
	Depth	K0	0.051	1.30
	Pitch	P1	0.315	8.0
Centerline Distance	Cavity to Perforation - Length Direction	P2	0.079	2.0
	Cavity to Perforation - Width Direction	F	0.217	5.50
Cover Tape	Width	C	0.362	9.20
Carrier Tape	Width	W	0.472	12.0

Tape and Reel Information – Reel Dimensions

Packaging reels are used to prevent damage to devices during shipping and storage, loaded carrier tape is typically wound onto a plastic take-up reel. The reel size is 13" diameter. The reels are made from high-impact injection-molded polystyrene (HIPS), which offers mechanical and ESD protection to packaged devices.

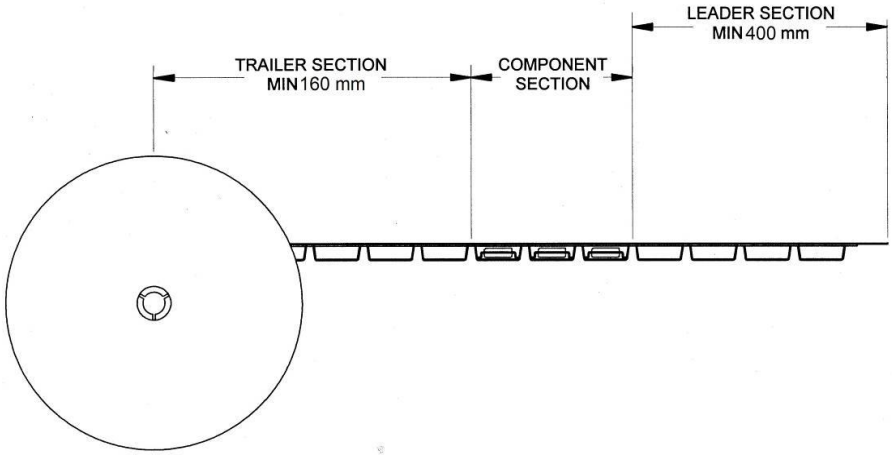


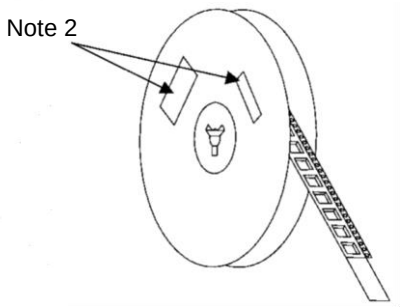
Feature	Measure	Symbol	Size (in)	Size (mm)
Flange	Diameter	A	12.992	330
	Thickness	W2	.717	18.2
	Space Between Flange	W1	.504	12.8
Hub	Outer Diameter	N	4.016	102.0
	Arbor Hole Diameter	C	0.512	13.0
	Key Slit Width	B	0.079	2.0
	Key Slit Diameter	D	.795	20.2

Tape and Reel Information – Tape Length and Label Placement

Tape and reel specifications for this part are also available on the Qorvo website.

Standard T/R size = 2500 pieces on a 13" reel.





Notes:

1. Empty part cavities at the trailing and leading ends are sealed with cover tape. See EIA 481.
2. Labels are placed on the flange opposite the sprockets in the carrier tape.

Handling Precautions

Parameter	Rating	Standard
ESD – Human Body Model (HBM)	Class 1A; 500V	ANSI/ESD/JEDEC JS-001
ESD – Charged Device Model (CDM)	Class C3; 1000V	ANSI/ESD/JEDEC JS-002
MSL – Moisture Sensitivity Level	MSL3	IPC/JEDEC J-STD-020

Caution!

ESD sensitive device

Solderability

Compatible with both lead-free (260 °C max. reflow temperature) and tin/lead (245 °C max. reflow temperature) soldering processes.

Package lead plating: Electroless Nickel Electroless Palladium Immersion Gold

RoHS Compliance

This part is compliant with the 2011/65/EU RoHS directive (Restrictions on the Use of Certain Hazardous Substances in Electrical and Electronic Equipment), as amended by Directive 2015/863/EU. This product also has the following attributes:

- Product uses RoHS Exemption 7c-I to meet RoHS Compliance requirements
- Halogen Free (Chlorine, Bromine)
- Antimony Free
- TBBP-A ($C_{15}H_{12}Br_4O_2$) Free
- PFOS Free
- SVHC Free

Revision History

Revision	Description
Draft 1.0	Initial datasheet proposal based on Volkswagen feedback for non-DSDA functionality
Draft 2.0	Updated package pinout and logic table
Draft 3.0	Updated package, pinout, logic table and general items
Draft 4.0	Updated pinout for better alignment for DSDA follow-on, logic table for additional states
Draft 5.0	Updated part functional block diagram to reflect actual switch configuration
Draft 6.0	Added package outline drawing
Draft 7.0	Updated format, prep for upload in PDE, added RFFE commands, EVB info
1/29/20	Updated Register convention names; added RF plots and Tape and Reel info; added power sequening
2/7/20	Updated HEX address to take out extra 0s
4/21/20	Updated Oderable parts and REG0x01 bit1 trigger, was bit0
5/6/20	Updated harmonic testing at 2400MHz
6/7/20	Release RevA
5/17/22	Release RevB; Removed Preliminary in prep for Production; added ESD numbers; revised orderable part numbers; removed programmability to the USID; Added VIO current spec; Updated Tape and Reel info. Updated Min/Max/Typ specs per latest PT runs and RVTM data. Updated Branding diagram. Changed verbage for High isolation state REG01 state 0x00; Changed verbage for Low Power mode REG28 to take out high isolation.

Contact Information

For the latest specifications, additional product information, worldwide sales and distribution locations:

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