APPLICATION NOTE AN125

ACT88760 Register Definitions – CMI 102

Abstract

This application note identifies and explains the ACT88760 internal registers that help make this IC flexible and configurable for many applications. It provides a short description of each register, its individual bits, their function, and default values. The default register settings in this application note are only valid for the ACT88760-102. Refer to each datasheet for each specific IC's functional differences from the settings in this document.

Introduction

The ACT88760 is a high Integration PMIC for Video/AR/VR Applications. It integrates seven high efficiency switching regulators into a single PMIC. It also has six linear regulators – LDOs or load switches. Two LDOs - LDO5 & 6 can also be configured as a load switches (LSW). There are ten GPIOs pins that are configurable and used for a variety of system functions. Each of these regulators can be configured for a wide range of output voltages through the I^2C interface.

Today's applications require more complexity in their startup and sequencing requirements. The ACT88760 I^2C registers allow for customized configurations for these requirements. Although the ACT88760 is programmed at the factory with a default configuration, these settings can be changed through the I^2C interface to provide customized configurations optimized for a specific end application. IC configurability includes many options such as output voltage, startup sequencing, startup timing, slew rates, GPIO configuration, fault responses, and more. Qorvo identifies these configurations with a Code Matrix Index, CMI. An IC's CMI is identified by the last three digits at the end of the orderable part number. Note that this application note is specific to the ACT88760's CMI 101. Refer to the datasheet for the specific changes to other CMI versions.

Register Types

The ACT88760 ICs contain the following register types.

Basic Volatile - Customer R/W (Read and Write) and RO (Read only). The customer can modify these register values to change IC functionality. Any changes to these registers are lost when power is recycled. The default values are fixed and cannot be changed.

Basic Non-Volatile - Customer R/W and RO. The customer can modify these register values to change IC functionality. Any changes to these registers are lost when power is recycled. The default values can be modified at the factory to optimize IC functionality for specific applications. Please consult Sales@Qorvo.com for custom options and minimum order quantities.

The ACT88760 contains 11 major register spaces.

Table 1: ACT88760 Register Addresses for CMI102

Register Space	7-Bit Device Slave I2C Address	Register Address Range
SYSTEM & GPIO	0x25h	0x00h to 0x34h
BUCK1 Reg	0x25h	0x40h to 0x47h
BUCK2 Reg	0x25h	0x60h to 0x67h
BUCK3 Reg	0x25h	0x80h to 0x87h
BUCK4 Reg	0x25h	0xA0h to 0xA7h
BUCK5 Reg	0x25h	0xC0h to 0xC7h
BUCK6 Reg	0x25h	0xE0h to 0xE7h
BUCK7 Reg	0x28h	0x00h to 0x07h
LDO1_LDO2	0x28h	0x20h to 0x2Ah
LDO3_LDO5	0x28h	0x40h to 0x4Ah
LDO4_LDO6	0x28h	0x60h to 0x6Ah

To ensure compatibility with a wide range of systems, the ACT88760 uses standard I²C commands. The ACT88760 always operates as a slave device and is addressed using a 7-bit slave address followed by an eighth bit, which indicates whether the transaction is a read-operation or a write-operation. Due to the number of registers, the IC breaks them up into two separate register banks. The upper bank contains registers for system level functions (GPIOs, system monitoring, over temperature thresholds) and Bucks 1-6. The lower bank contains registers for Buck 7 and LDOs1-6. The AC88760 uses two addresses as shown in Table 2. Refer to each specific CMI for the IC's slave address.

Table 2: ACT88760 I²C Addresses

7-Bit Slave Address (Master, GPIOs, Buck1-6)		**8-Bit Write Address**	**8-Bit Read Address**
0x25h	010 0101b	0x4Ah	0x4Bh
0x27h	010 0111b	0x4Eh	0x4Fh
0x67h	110 0111b	0xCEh	0xCFh
0x6Bh	110 1011b	0xD6h	0xD7h
7-Bit Slave Address (Buck7, LDO 1-6)		**8-Bit Write Address**	**8-Bit Read Address**
0x26h	010 0110b	0x4Ch	0x4Dh
0x28h	010 1000b	0x50h	0x51h
0x68h	110 1000b	0xD0h	0xD1h
0x6Ch	110 1100b	0xD8h	0xD9h

Register Map Overview

The following table shows an overview of the ACT88760 register map. Note that not all register addresses are sequential.

ACT88760 MASTER REGISTERS & PBIO REGISTERS ADDRESS I2C1 00 - 34								
AADR (HEX)	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
00	ROM STAT	WD TIMER ALERT	TWARN (Warning)	VSYSSTAT (latch)	VIN_POK_OV	PBASTAT	VSYSWARN (latch)	PBDSTAT
01	ROM INT MSK	WD ALERT MSK	TMSK (Interrupt Mask)	VSYSMSK	VIN_POK_OV_MASK	PBAMSK	VSYSWARN MASK	PBDMSK
02	FACTORY MODE	RFU	VSYSWARN Real time	VSYSDAT	DVS_FROM_I2C_DB[11]	DVS_FROM_I2C_DB[10]	DVS_FROM_I2C_DB[9]	PBDAT
03	GPIO8 STAT	GPIO7 STAT	GPIO6 STAT	GPIO5 STAT	GPIO4 STAT	GPIO3 STAT	GPIO2 STAT	GPIO1 STAT
04	GPIO8 Toggled	GPIO7 Toggled	GPIO6 Toggled	GPIO5 Toggled	GPIO4 Toggled	GPIO3 Toggled	GPIO2 Toggled	GPIO1 Toggled
05	GPIO8 MASK	GPIO7 MASK	GPIO6 MASK	GPIO5 MASK	GPIO4 MASK	GPIO3 MASK	GPIO2 MASK	GPIO1 MASK
06	INTADR							
07	MR	SLEEP	RESET_GPIOs_EDGE_MODE	DPSLP	AUTO_CLEAR	POWER OFF	WDPCEN	WDSREN
2B	GPIO9 STAT	GPIO9 Toggle	GPIO9 MASK	GPIO10 STAT	GPIO10 Toggle	GPIO10 MASK	GPIO11 STAT	GPIO11 Toggle
2C	BK1_DVS_I2C[1:0]		BK2_DVS_I2C[1:0]		BK7_DVS_I2C[1:0]		GPIO11 MASK	**BAND_SEL**
09	TRST_DLY[2:0]			POWERCYCLE_TIME_SET[1:0]		POWEROFF_TIME_SET[1:0]		DIS OV UV SHUTDOWN
0A	EN POWERCYCLE	EN POWEROFF	ROM_EN	VSYSMON[4:0]				
0B	IO1_DLY[1:0]		IO2_DLY[1:0]		IO3_DLY[1:0]		IO4_DLY[1:0]	
0C	IO5_DLY[1:0]		IO6_DLY[1:0]		IO7_DLY[1:0]		WDTIME	RETRY TIME
0D	MODE1				MUX1			
0E	MODE2				MUX2			
0F	MODE3				MUX3			
10	MODE4				MUX4			
11	MODE5				MUX5			
12	MODE6				MUX6			
13	MODE7				MUX7			
14	POK_OV[2:0]			VSYSWARN[4:0]				
27	MODE8				MUX8			
28	MODE9				MUX9			
29	MODE10				MUX 10			
2A	MODE11				**MUX 11**			
33	LED_CURRENT_SET_GPIO9[3:0]				LED_CURRENT_SET_GPIO10[3:0]			
34	nSAVE_IQ_MSTR	EN_PUSH_PULL_GPIO8	EN_PUSH_PULL_GPIO7	EN_PUSH_PULL_GPIO6	EN_PUSH_PULL_GPIO4	EN_PUSH_PULL_GPIO3	EN_PUSH_PULL_GPIO2	EN_PUSH_PULL_GPIO1

BUCK1 ADDRESS I2C1 40-47								
ADDR (HEX)	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
40	POK	OV	ILIM	ILIM_WARN	UV_FLTMSK	OV_FLTMSK	ILIM_FLTMSK	ILIM_WARN_FLTMSK
41	FORCE_LPM_FONT	DIS_LPM_FONT	PULL_UP_GPIO2	DIS_PULLDOWN	PULL_UP_GPIO6	EN_MINPK_LPM	DRV_ADJ[1:0]	
42	EN_OutPD	VSET0[6:0]						
	IPD_SET[0]	VSET2[6:0]						
43	RFU	VSET1[6:0]						
	IPD_SET[1]	VSET3[6:0]						
44	ON	PBINEN	QLTCH	SLEEP EN	AUXIN EN	DP SLEEP EN	ILIM_SET	FORCEPWM
45	MODE	RST	DBQL			DBOK		
46	DBON				SST	DISLPM	Vout_Range	RFU
47	PULL_UP_GPIO11	PHASE	ON DELAY[2:0]			OFF DELAY[2:0]		

BUCK2 ADDRESS I2C1 60-67								
ADDR(HEX)	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
60	POK	OV	ILIM	ILIM_WARN	UV_FLTMSK	OV_FLTMSK	ILIM_FLTMSK	ILIM_WARN_FLTMSK
61	FORCE_LPM_FONT	DIS_LPM_FONT	RFU	DIS_PULLDOWN	RFU	EN_MINPK_LPM	DRV_ADJ[1:0]	
62	EN_OutPD	VSET0[6:0]						
	IPD_SET[0]	VSET2[6:0]						
63	RFU	VSET1[6:0]						
	IPD_SET[1]	VSET3[6:0]						
64	ON	PBINEN	QLTCH	SLEEP EN	AUXIN EN	DP SLEEP EN	ILIM_SET	FORCEPWM
65	MODE	RST	DBQL			DBOK		
66	DBON				SST	DISLPM	Vout_Range	RFU
67	RFU	PHASE	ON DELAY[2:0]			OFF DELAY[2:0]		

BUCK3 ADDRESS I2C1 80-87								
ADDR (HEX)	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
80	POK	OV	ILIM	ILIM_WARN	UV_FLTMSK	OV_FLTMSK	ILIM_FLTMSK	ILIM_WARN_FLTMSK
81	FORCE_LPM_FONT	DIS_LPM_FONT	MUX TILE ON to POK	DIS_PULLDOWN	Vout_Range	EN_MINPK_LPM	DRV_ADJ[1:0]	
82	EN_OutPD	VSET0[6:0]						
83	IPD_SET[0]	VSET1[6:0]						
84	ON	PBINEN	QLTCH	SLEEP EN	AUXIN EN	DP SLEEP EN	ILIM_SET	FORCEPWM
85	MODE	RST	DBQL			DBOK		
86	DBON				SST	DISLPM	DBSTBY	
87	IPD_SET[1]	PHASE	ON DELAY[2:0]			OFF DELAY[2:0]		

BUCK4 ADDRESS I2C1 80-87

ADDR(HEX)	7	6	5	4	3	2	1	0
A0	POK	OV	ILIM	ILIM_WARN	UV_FLTMSK	OV_FLTMSK	ILIM_FLTMSK	ILIM_WARN_FLTMSK
A1	FORCE_LPM_FONT	DIS_LPM_FONT	MUX TILE ON to POK	DIS_PULLDOWN	Vout_Range	EN_MINPK_LPM	DRV_ADJ[1:0]	
A2	EN_OutPD	VSET0[6:0]						
A3	IPD_SET[0]	VSET1[6:0]						
A4	ON	PBINEN	QLTCH	SLEEP EN	AUXIN EN	DP SLEEP EN	ILIM_SET	FORCEPWM
A5	MODE	RST	DBQL			DBOK		
A6	DBON				SST	DISLPM	DBSTBY	
A7	IPD_SET[1]	PHASE	ON DELAY[2:0]			OFF DELAY[2:0]		

BUCK5 ADDRESS I2C1 C0-C7

ADDR(HEX)	7	6	5	4	3	2	1	0
C0	POK	OV	ILIM	ILIM_WARN	UV_FLTMSK	OV_FLTMSK	ILIM_FLTMSK	ILIM_WARN_FLTMSK
C1	FORCE_LPM_FONT	DIS_LPM_FONT	MUX TILE ON to POK	DIS_PULLDOWN	EN_OutPD	EN_MINPK_LPM	DRV_ADJ[1:0]	
C2	IPD_SET[0]	VSET0[6:0]						
C3	IPD_SET[1]	VSET1[6:0]						
C4	ON	PBINEN	QLTCH	SLEEP EN	AUXIN EN	DP SLEEP EN	ILIM_SET	FORCEPWM
C5	MODE	RST	DBQL			DBOK		
C6	DBON				SST	DISLPM	DBSTBY	
C7	AdjTFONT	PHASE	ON DELAY[2:0]			OFF DELAY[2:0]		

BUCK6 ADDRESS I2C1 E0-E7

ADDR (HEX)	7	6	5	4	3	2	1	0
E0	POK	OV	ILIM	ILIM_WARN	UV_FLTMSK	OV_FLTMSK	ILIM_FLTMSK	ILIM_WARN_FLTMSK
E1	FORCE_LPM_FONT	DIS_LPM_FONT	MUX TILE ON to POK	DIS_PULLDOWN	EN_OutPD	EN_MINPK_LPM	DRV_ADJ[1:0]	
E2	IPD_SET[0]	VSET0[6:0]						
E3	IPD_SET[1]	VSET1[6:0]						
E4	ON	PBINEN	QLTCH	SLEEP EN	AUXIN EN	DP SLEEP EN	ILIM_SET	FORCEPWM
E5	MODE	RST	DBQL			DBOK		
E6	DBON				SST	DISLPM	DBSTBY	
E7	AdjTFONT	PHASE	ON DELAY[2:0]			OFF DELAY[2:0]		

BUCK7 ADDRESS I2C2 00-07

ADDR (HEX)	7	6	5	4	3	2	1	0
00	POK	OV	ILIM	ILIM_WARN	UV_FLTMSK	OV_FLTMSK	ILIM_FLTMSK	ILIM_WARN_FLTMSK
01	FORCE_LPM_FONT	DIS_LPM_FONT	RFU	DIS_PULLDOWN	RFU	EN_MINPK_LPM	DRV_ADJ[1:0]	
02	EN_OutPD	VSET0[6:0]						
	IPD_SET[0]	VSET2[6:0]						
03	RFU	VSET1[6:0]						
	IPD_SET[1]	VSET3[6:0]						
04	ON	PBINEN	QLTCH	SLEEP EN	AUXIN EN	DP SLEEP EN	ILIM_SET	FORCEPWM
05	MODE	RST	DBQL			DBOK		
06	DBON				SST	DISLPM	Vout_Range	RFU
07	RFU	PHASE	ON DELAY[2:0]			OFF DELAY[2:0]		

LDO12 REGISTERS ADDRESS I2C2 20-2A

ADDR (HEX)	7	6	5	4	3	2	1	0
20	PWR_GOOD_LDO1	OV_LDO1	ILIM_LDO1	RFU	UV_FLTMSK_LDO1	OV_FLTMSK_LDO1	ILIM_FLTMSK_LDO1	RFU
21	RFU	RANGE_LDO1	LDO1 VSET[5:0]					
22	ON LDO1 (DEFAULT 1)	PBIN EN LDO1	AUXIN EN LDO1	SLEEP EN LDO1	DPSLEEP EN LDO1	DBQL LDO1 [2:0]		
23	ON DELAY LDO1 [2:0]			OFF DELAY LDO1 [2:0]			MODE LDO1	RST LDO1
24	DBON LDO1[3:0]				DBOK LDO1[3:0]			
25	ILIM SHUTDOWN DIS_LDO1	RFU	RFU	DIS_Charge_option_LDO1	DIS_PULLDOWN_LDO2	DIS_PULLDOWN_LDO1	SST_LDO1	QLTCH LDO1
26	PWR_GOOD_LDO2	OV_LDO2	ILIM_LDO2	RFU	UV_FLTMSK_LDO2	OV_FLTMSK_LDO2	ILIM_FLTMSK_LDO2	RFU
27	RFU	RANGE_LDO2	LDO2 VSET[5:0]					
28	ON LDO2 (DEFAULT 1)	PBIN EN LDO2	AUXIN EN LDO2	SLEEP EN LDO2	DPSLEEP EN LDO2	DBQL LDO2 [2:0]		
29	ON DELAY LDO2 [2:0]			OFF DELAY LDO2 [2:0]			MODE LDO2	RST LDO2
2A	DBON LDO2 [3:0]				DBOK LDO2 [3:0]			

LDO53 REGISTERS ADDRESS I2C2 40-4A

ADDR (HEX)	7	6	5	4	3	2	1	0
40	PWR_GOOD_LDO5	OV_LDO5	ILIM_LDO5	RFU	UV_FLTMSK_LDO5	OV_FLTMSK_LDO5	ILIM_FLTMSK_LDO5	RFU
41	LDO5_RANGE	RFU	LDO5 VSET[5:0]					
42	ON LDO5 (DEFAULT 1)	PBIN EN LDO5	AUXIN EN LDO5	SLEEP EN LDO5	DPSLEEP EN LDO5	DBQL LDO5 [2:0]		
43	ON DELAY LDO5 [2:0]			OFF DELAY LDO5 [2:0]			MODE LDO5	RST LDO5
44	DBON LDO5[3:0]				DBOK LDO5[3:0]			
45	ILIM SHUTDOWN DIS_LDO5	PULL_UP_GPIO4	PULL_UP_GPIO3	DIS_PULLDOWN_LDO5	PULL_UP_GPIO1	ILIM_SCL_LDO5	SST_LDO5	QLTCH LDO5
46	PWR_GOOD_LDO3	OV_LDO3	ILIM_LDO3	RFU	UV_FLTMSK_LDO3	OV_FLTMSK_LDO3	ILIM_FLTMSK_LDO3	RFU
47	LDO3_RANGE	RFU	LDO3 VSET[5:0]					
48	ON LDO3 (DEFAULT 1)	PBIN EN LDO3	AUXIN EN LDO3	SLEEP EN LDO3	DPSLEEP EN LDO3	DBQL LDO3 [2:0]		
49	ON DELAY LDO3 [2:0]			OFF DELAY LDO3 [2:0]			MODE LDO3	RST LDO3
4A	DBON LDO3 [3:0]				DBOK LDO3 [3:0]			

	LDO64 REGISTERS ADDRESS I2C2 60-6A							
ADDR (HEX)	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
60	PWR_GOOD_LDO5	OV_LDO5	ILIM_LDO5	RFU	UV_FLTMSK_LDO5	OV_FLTMSK_LDO5	ILIM_FLTMSK_LDO5	RFU
61	LDO6_VOUT_RANGE	RFU	LDO6 VSET[5:0]					
62	ON LDO6 (DEFAULT 1)	PBIN EN LDO6	AUXIN EN LDO6	SLEEP EN LDO6	DPSLEEP EN LDO6	DBQL LDO6 [2:0]		
63	ON DELAY LDO6 [2:0]				OFF DELAY LDO6 [2:0]		MODE LDO6	RST LDO6
64	DBON LDO6[3:0]				DBOK LDO6[3:0]			
65	ILIM SHUTDOWN DIS_LDO6	PULL_UP_GPIO8	PULL_UP_GPIO7	DIS_PULLDOWN_LDO6	PULL_UP_GPIO5	ILIM_SCL_LDO6	SST_LDO6	QLTCH LDO6
66	PWR_GOOD_LDO4	OV_LDO4	ILIM_LDO4	RFU	UV_FLTMSK_LDO4	OV_FLTMSK_LDO4	ILIM_FLTMSK_LDO4	RFU
67	LDO4_RANGE	RFU	LDO4 VSET[5:0]					
68	ON LDO4 (DEFAULT 1)	PBIN EN LDO4	AUXIN EN LDO4	SLEEP EN LDO4	DPSLEEP EN LDO4	DBQL LDO4 [2:0]		
69	ON DELAY LDO4 [2:0]				OFF DELAY LDO4 [2:0]		MODE LDO4	RST LDO4
6A	DBON LDO4 [3:0]				DBOK LDO4 [3:0]			

Master & PBIO (Push Button & I/O) Configuration Registers

MSTR00 - Master Configuration Register

Address = 0x00h	Default = 0x00h	Type = Basic Volatile

BIT	7	6	5	4	3	2	1	0
Name	RFU	WD TIMER ALERT	TWARN	VSYSSTAT (latch)	VIN_POK_ OV	PBASTAT	VSYSWARN (latch)	PBDSTAT
Default	0	0	0	0	0	0	0	0
Access	RO	RO	RO	RO	RO	RO	RO	RO

Name	Description	Notes
RFU	Reserved for Future Use	This register returns a 0 when read
WD TIMER ALERT	Watch Dog Timer Alert status. Active high to report the timer is expired (7.4s). 0 = Watchdog timer has not expired 1 = Watchdog timer has expired	When this bit = 1, an interrupt is generated on the nIRQ pin if WD ALERT MSK = 0.
TWARN	Thermal Interrupt Status. 0 = Junction temperature < TWARN Threshold 1 = Junction temperature > TWARN Threshold	When this bit = 1, an interrupt is generated on the nIRQ pin if TMSK = 0.
VSYSSTAT (latch)	VSYSMON Status 0 = VIN > VSYS_MON 1 = VIN < VSYS_MON SYSSTAT is latched to 1 at falling edge of VIN and cleared to 0 after reading this byte when VIN > VSYS_MON.	When this bit = 1, an interrupt is generated on the nIRQ pin if VSYSMSK = 0. VSYSMON is programmed with the VSYSMON bits in the 0x0Ah [4:0] register.
VIN_POK_OV	VIN Over Voltage Status 0 = VIN < VIN_POK_OV threshold 1 = VIN > VIN_POK_OV threshold	When this bit = 1, an interrupt is generated on the nIRQ pin if VIN_POK_OV_MASK = 0. VIN_POK_OV is programmed with the POK_OV bits in the 0x14h [7:5] register.
PBASTAT	Push-Button mode only. Push Button Assert Status. 0 = Push button is not asserted 1 = Push button was asserted	When the push button is pressed, PBASTAT is set and triggers an interrupt on nIRQ if the PBAMSK = 0.
VSYSWARN (latch)	VSYSWARN Status 0 = VIN > VSYS_WARN 1 = VIN < VSYS_WARN SYSWARN is latched to 1 at falling edge of VIN and clear to 0 after reading this byte when VIN is > SYS_WARN.	When this bit = 1, an interrupt is generated on the nIRQ pin if VSYSWARN MASK = 0. VSYSWARN is programmed with the VSYSWARN bits in the 0x14h [4:0] register.
PBDSTAT	Push-Button mode only. Push Button De-assert Status 0 = Push-Button is not de-asserted 1 = Push button was de-asserted	When the push button is released, PBDSTAT is set and triggers and interrupt on nIRQ if the PBDMSK = 0.

MSTR01 - Master Configuration Register

Address = 0x01h	Default = 0xFFh	Type = Basic Volatile

BIT	7	6	5	4	3	2	1	0
Name	RFU	WD ALERT MSK	TMSK	VSYSMSK	VIN_POK_OV_MASK	PBAMSK	VSYSWARN MASK	PBDMSK
Default	1	1	1	1	1	1	1	1
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Name	Description	Notes
RFU	Reserved for Future Use	This register returns a 0 when read
WD ALERT MSK	Watch Dog timer Alert Mask. 0 = Unmasks the WD ALERT interrupt 1 = Masks the WD ALERT interrupt	When 1, the WD ALERT interrupt is masked. WD ALERT STAT provides real-time watchdog status.
TMSK	Thermal Interrupt Mask 0 = Unmasks the TWARN thermal interrupt 1 = Masks the TWARN thermal interrupt	When 1, the TWARN interrupt is masked. TWARN still provides real-time temperature warn status.
VSYSMSK	SYSMON Interrupt Mask 0 = Unmasks the VSYSSTAT interrupt 1 = Masks the VSYSTAT interrupt	When 1, the VSYSTAT interrupt is masked. VSYSTAT still provides real-time UV warn status.
VIN_POK_OV_MASK	VIN POK OV Interrupt Mask 0 = Unmasks the VIN POK OV interrupt 1 = Masks the VIN POK OV interrupt	When 1, the VIN POK OV interrupt is masked. VIN POK OV still provides real-time status.
PBAMSK	Push - Button Assert Interrupt Mask 0 = Unmasks the PBASTAT interrupt 1 = Masks the PBASTAT interrupt	When 1, the PBASTAT interrupt is masked. PBASTAT still provides real-time status.
VSYSWARN MASK	VSYSWARN Interrupt Mask 0 = Unmasks the VSYSWARN interrupt 1 = Masks the VSYSWARN interrupt	When 1, the VSYSWARN interrupt is masked. VSYSWARN still provides real-time status.
PBDMSK	Push - Button De-Assert Interrupt Mask 0 = Unmasks the PBDSTAT interrupt 1 = Masks the PBDSTAT interrupt	When 1, the PBDSTAT interrupt is masked. PBDSTAT still provides real-time status.

MSTR02 - Master Configuration Register

Address = 0x02h	Default = 0x01h	Type = Basic Volatile

BIT	7	6	5	4	3	2	1	0
Name	FACTORY MODE/Qorvo Use Only	RFU	VSYSWARN_RT	VSYSDAT	DVS FROM I2C DB11	DVS FROM I2C DB10	DVS FROM I2C DB9	PBDAT
Default	0	0	0	0	0	0	0	1
Access	R/W	RO	R/W	R/W	R/W	R/W	R/W	R/W

Name	Description	Notes
FACTORY MODE	0 = IC is in normal operating mode 1 = IC is in factory programming mode	Qorvo use only
RFU	Reserved for Future Use	This register returns a 0 when read
VSYSWARN_RT	VSYSWARN Real Time Data 0 = VIN voltage is under VSYSWARN 1 = VIN voltage is above VSYSWARN	This bit provides the real time WSYSTWARN status.
VSYSDAT	VSYSMON Real Time Data 0 = VIN voltage is under VSYSMON 1 = VIN voltage is above VSYSMON	This bit provides the real time VSYSMON status.
DVS FROM I2C DB11	Control DB11 if I2C_EN_DVS was set. 0 = De-asserts DB11 1 = Asserts DB11	Do not change this register value. Changing the register value can affect IC functionality.
DVS FROM I2C DB10	Control DB10 if I2C_EN_DVS was set. 0 = De-asserts DB11 1 = Asserts DB11	Do not change this register value. Changing the register value can affect IC functionality.
DVS FROM I2C DB9	Control DB9 if I2C_EN_DVS was set. 0 = De-asserts DB11 1 = Asserts DB11	Do not change this register value. Changing the register value can affect IC functionality.
PBDAT	Push - Button Real Time Data 0 = Push button is de-asserted low. 1 = Push button is asserted high.	This bit provides the real time pushbutton de-asserted status.

MSTR03 - Master Configuration Register

Address = 0x03h	Default = 0x00h	Type = Basic Volatile

BIT	7	6	5	4	3	2	1	0
Name	GPIO8_STAT	GPIO7_STAT	GPIO6_STAT	GPIO5_STAT	GPIO4_STAT	GPIO3_STAT	GPIO2_STAT	GPIO1_STAT
Default	0	0	0	0	0	0	0	0
Access	RO	RO	RO	RO	RO	RO	RO	RO

Name	Description	Notes
GPIO8_STAT	GPIO8 real time status	Only the bits associated with the GPIOs that are configured as inputs are valid. The other bits are undefined and return a random value when read.
GPIO7_STAT	GPIO7 real time status	
GPIO6_STAT	GPIO6 real time status	
GPIO5_STAT	GPIO5 real time status	
GPIO4_STAT	GPIO4 real time status	
GPIO3_STAT	GPIO3 real time status	
GPIO2_STAT	GPIO2 real time status	
GPIO1_STAT	GPIO1 real time status	

MSTR04 - Master Configuration Register

Address = 0x04h	Default = 0x00h	Type = Basic Volatile

BIT	7	6	5	4	3	2	1	0
Name	GPIO8_Toggled	GPIO7_Toggled	GPIO6_Toggled	GPIO5_Toggled	GPIO4_Toggled	GPIO3_Toggled	GPIO2_Toggled	GPIO1_Toggled
Default	0	0	0	0	0	0	0	0
Access	RO	RO	RO	RO	RO	RO	RO	RO

Name	Description	Notes
GPIO8_Toggled	Set to1 when detect GPIO8 status change. Read back to clear to 0.	Only the bits associated with the GPIOs that are configured as inputs are valid. The other bits are undefined and return a random value when read.
GPIO7_Toggled	Set to1 when detect GPIO7 change status. Read back to clear to 0.	
GPIO6_Toggled	Set to1 when detect GPIO6 change status. Read back to clear to 0.	
GPIO5_Toggled	Set to1 when detect GPIO5 change status. Read back to clear to 0.	
GPIO4_Toggled	Set to1 when detect GPIO4 change status. Read back to clear to 0.	
GPIO3_Toggled	Set to1 when detect GPIO3 change status. Read back to clear to 0.	
GPIO2_Toggled	Set to1 when detect GPIO2 change status. Read back to clear to 0.	
GPIO1_Toggled	Set to1 when detect GPIO1 change status. Read back to clear to 0.	

MSTR05 - Master Configuration Register

Address = 0x05h	Default = 0x7Fh	Type = Basic Volatile

BIT	7	6	5	4	3	2	1	0
Name	GPIO8_MSK	GPIO7_MSK	GPIO6_MSK	GPIO5_MSK	GPIO4_MSK	GPIO3_MSK	GPIO2_MSK	GPIO1_MSK
Default	0	1	1	1	1	1	1	1
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Name	Description	Notes
GPIOx_MSK	0 = Triggers the interrupt when GPIOx Input status changes 1 = Not trigger the interrupt when GPIOx Input status changes	GPIOx can generate individual interrupts when GPIOx is configured as input.

MSTR06 - Master Configuration Register

Address = 0x06h	Default = 0x00h	Type = Basic Volatile

BIT	7	6	5	4	3	2	1	0
Name	INTADR [7:0]							
Default	00000000							
Access	RO							

Name	Description	Notes
INTADR [7:0]	Indicate the address of which tile generated the interrupt. 0x00: MSTR or BUCK7 0x01: GPIO 0x40: BUCK1 0x60: BUCK2 0x80: BUCK3 0xA0: BUCK4 0xC0: BUCK5 0xE0: BUCK6	Note that interrupts from the LDOs do not affect this register. The user must manually check each LDO's registers to identify the interrupt.

MSTR07 - Master Configuration Register

Address = 0x07h	Default = 0x00h	Type = Basic Volatile

BIT	7	6	5	4	3	2	1	0
Name	MR	SLEEP	RSTIO_EDMD	DPSLP	AUTO_CLEAR	POWER_OFF	WDPCEN	WDSREN
Default	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Name	Description	Notes
MR	Repower cycle when write this bit to 1. Clear all VM register, move to POWER OFF state and re-power on after 0.5s.	
SLEEP	0 = Not enter SLEEP mode 1 = Enter SLEEP mode	
RSTIO_EDMD	Reset GPIOs Edge Mode Write to 1 to reset GPIOs which is configured as input edge mode.	This bit is automatic clear to 0 if bit AUTO_CLEAR = 1.
DPSLP	0 = Not enter DEEP SLEEP mode 1 = Enter DEEP SLEEP mode	
AUTO_CLEAR	0 = Not automatic clear the RSTIO_EDMD bit. 1 = Automatic clear the RSTIO_EDMD bit to 0 after 100us.	
POWER_OFF	Default is 0. 1 = Clear all VM register, IC move to POWER OFF state. Write from 1 to 0 to move the IC from POWER OFF to POWER ON state.	
WDPCEN	0 = Not enable watch dog power cycle. 1 = Enable power cycles (turn off REGs follow sequence, after 0.5s turn-on again) if watch dog timer expired (8s).	
WDSREN	0 = Not enable watch dog soft rest. 1 = Enable soft reset if watch dog timer expired(8s).	

MSTR2B - Master Configuration Register

Address = 0x2Bh	Default = 0x24h	Type = Basic Volatile

BIT	7	6	5	4	3	2	1	0
Name	GPIO9_STAT	GPIO9_ Toggled	GPIO9_MSK	GPIO10_STAT	GPIO10_ Toggled	GPIO10_MSK	GPIO11_STAT	GPIO11_ Toggled
Default	0	0	1	0	0	1	0	0
Access	RO	RO	R/W	RO	RO	R/W	RO	RO

Name	Description	Notes
GPIO9_STAT	GPIO9 real time status	
GPIO9_ Toggled	Detect GPIO9 toggle 1 = Detected GPIO9 change status. 0 = Not detect GPIO9 change status.	This bit only shows correct status of GPIOs when it is configured as input. Read back to clear to 0.
GPIO9_MSK	GPIO9 can generate interrupt individually when GPIO9 is configured as input. 0 = Trigger the interrupt when GPIO9 Input change status 1 = Not trigger the interrupt when GPIO9 Input change status	
GPIO10_STAT	GPIO10 real time status	
GPIO10_ Toggled	Detect GPIO10 toggle 1 = Detected GPIO10 change status. 0 = Not detect GPIO10 change status.	This bit only shows correct status of GPIOs when it is configured as input. Read back to clear to 0.
GPIO10_MSK	GPIO10 can generate interrupt individually when GPIO10 is configured as input. 0 = Trigger the interrupt when GPIO10 Input change status 1 = Not trigger the interrupt when GPIO10 Input change status	
GPIO11_STAT	GPIO11 real time status	
GPIO11_ Toggled	Detect GPIO11 toggle 1 = Detected GPIO11 change status. 0 = Not detect GPIO11 change status.	Read back to clear to 0.

MSTR2C - Master Configuration Register

Address = 0x2Ch	Default = 0x02h	Type = Basic Volatile

BIT	7	6	5	4	3	2	1	0
Name	BK1DvsI2C [1:0]		BK2DvsI2C [1:0]		BK7DvsI2C [1:0]		GPIO11_MSK	BAND_SEL
Default	00		00		00		1	0
Access	R/W		R/W		R/W		R/W	R/W

Name	Description	Notes
BK1DvsI2C [1:0]	Select VSET for BUCK1 I2C DVS: 00: select VSET0 01: select VSET1 10: select VSET2 11: select VSET3	
BK2DvsI2C [1:0]	Select VSET for BUCK2 I2C DVS: 00: select VSET0 01: select VSET1 10: select VSET2 11: select VSET3	
BK7DvsI2C [1:0]	Select VSET for BUCK7 I2C DVS: 00: select VSET0 01: select VSET1 10: select VSET2 11: select VSET3	
GPIO11_MSK	GPIO11 can generate interrupt individually when GPIO11 is configured as input. 0 = Trigger the interrupt when GPIO11 Input change status 1 = Not trigger the interrupt when GPIO11 Input change status	
BAND_SEL	0 = Enable reading/ writing for VSET0/VSET1 of BUCK127. 1 = Enable reading/ writing for VSET2/VSET3 of BUCK127	The Qorvo GUI automatically sets this bit based on reading/writing VSET0/VSET1 or VSET2/VSET3. If not using the GUI, the user must correctly set this bit before reading or writing the corresponding VSETx.

MSTR09 - Master Configuration Register

Address = 0x09h	Default = 0x40h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	TRST_DLY [2:0]			PwrCycTime [1:0]		PwrOffTime [1:0]		DisOvUvShdn
Default	010			00		00		0
Access	R/W			R/W		R/W		R/W

Name	Description	Notes
TRST_DLY [2:0]	Setting delay for reset 000: 5ms 001: 10ms 010: 20ms 011: 40ms 100: 0.5ms 101: 1ms 110: 2.5ms 111: 100ms	
PwrCycTime [1:0]	Setting timer for power cycle: 00: 1s < t < 4s (trigger at released). 01: 4s < t < 8s (trigger at released). 10: 8s, trigger at exact 8s. 11: 12s, trigger at exact 12s.	
PwrOffTime [1:0]	Setting timer for power off: 00: 1s < t < 4s (trigger at released). 01: 1s < t < 4s (trigger at released). 10: 8s, trigger at exact 8s. 11: 12s, trigger at exact 12s.	
DisOvUvShdn	Disable UVOV of REGs	

MSTR0A - Master Configuration Register

Address = 0x0Ah	Default = 0x03h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	EN_PwrCys	EN_PwrOff	RFU	VSYSMON [4:0]				
Default	0	0	0	00011				
Access	R/W	R/W	R/W	R/W				

Name	Description	Notes
EN_PwrCys	0 = Disable Power Cycle by Push-Button 1 = Enable Power Cycle by Push-Button	
EN_PwrOff	0 = Disable Power OFF by Push-Button 1 = Enable Power OFF by Push-Button	
RFU	Reserved for Future Use	Do not change this register value. Changing the register value can affect IC functionality.
VSYSMON [4:0]	00000 = 2.6V to 10101 = 4.7V Step size = 0.1V per bit 10110 to 11111: 4.7V	VSYSMON rising threshold setting. All values above 10110b set to 4.7V

MSTR0B - Master Configuration Register

Address = 0x0Bh	Default = 0x00h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	GPIO1Dly		GPIO2Dly		GPIO3Dly		GPIO4Dly	
Default	00		00		00		00	
Access	R/W		R/W		R/W		R/W	

Name	Description	Notes
GPIOxDly	Delay setting for both input mode/ output OD mode of GPIOx. 00: 0ms 01: 1ms 10: 2ms 11: 4ms	

MSTR0C - Master Configuration Register

Address = 0x0Ch	Default = 0x00h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	GPIO5Dly		GPIO6Dly		GPIO7Dly		RFU	RETRY_TIME
Default	00		00		00		0	0
Access	R/W		R/W		R/W		R/W	R/W

Name	Description	Notes
GPIOxDly	Delay setting for both input mode/ output OD mode of GPIOx. 00: 0ms 01: 1ms 10: 2ms 11: 4ms	
RFU	Reserved for Future Use	Do not change this register value. Changing the register value can affect IC functionality.
RETRY_TIME	Retry timer setting 0: 100ms 1: 250ms	.

MSTR0D - Master Configuration Register

Address = 0x0Dh	Default = 0x45h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	MODE1 [3:0]				MUX1 [3:0]			
Default	0100				0101			
Access	R/W				R/W			

Name	Description	Notes
MODE1 [3:0]	Determines startup sequencing from the CMI code	This is a factory expert bit that should not be changed. Modifying this bit may result in unexpected IC behavior.
MUX1 [3:0]	Determines startup sequencing from the CMI code	This is a factory expert bit that should not be changed. Modifying this bit may result in unexpected IC behavior.

MSTR0E - Master Configuration Register

Address = 0x0Eh	Default = 0x47h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	MODE2 [3:0]				MUX2 [3:0]			
Default	0100				0111			
Access	R/W				R/W			

Name	Description	Notes
MODE2 [3:0]	Determines startup sequencing from the CMI code	This is a factory expert bit that should not be changed. Modifying this bit may result in unexpected IC behavior.
MUX2 [3:0]	Determines startup sequencing from the CMI code	This is a factory expert bit that should not be changed. Modifying this bit may result in unexpected IC behavior.

MSTR0F - Master Configuration Register

Address = 0x0Fh	Default = 0x19h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	MODE3 [3:0]				MUX3 [3:0]			
Default	0001				1001			
Access	R/W				R/W			

Name	Description	Notes
MODE3 [3:0]	Determines startup sequencing from the CMI code	This is a factory expert bit that should not be changed. Modifying this bit may result in unexpected IC behavior.
MUX3 [3:0]	Determines startup sequencing from the CMI code	This is a factory expert bit that should not be changed. Modifying this bit may result in unexpected IC behavior.

MSTR10 - Master Configuration Register

Address = 0x10h	Default = 0x1Ah	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	MODE4 [3:0]				MUX4 [3:0]			
Default	0001				1010			
Access	R/W				R/W			

Name	Description	Notes
MODE4 [3:0]	Determines startup sequencing from the CMI code	This is a factory expert bit that should not be changed. Modifying this bit may result in unexpected IC behavior.
MUX4 [3:0]	Determines startup sequencing from the CMI code	This is a factory expert bit that should not be changed. Modifying this bit may result in unexpected IC behavior.

MSTR11 - Master Configuration Register

Address = 0x11h	Default = 0x2Bh	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	MODE5 [3:0]				MUX5 [3:0]			
Default	0010				1011			
Access	R/W				R/W			

Name	Description	Notes
MODE5 [3:0]	Determines startup sequencing from the CMI code	This is a factory expert bit that should not be changed. Modifying this bit may result in unexpected IC behavior.
MUX5 [3:0]	Determines startup sequencing from the CMI code	This is a factory expert bit that should not be changed. Modifying this bit may result in unexpected IC behavior.

MSTR12 - Master Configuration Register

Address = 0x12h	Default = 0xB4h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	MODE6 [3:0]				MUX6 [3:0]			
Default	1011				0100			
Access	R/W				R/W			

Name	Description	Notes
MODE6 [3:0]	Determines startup sequencing from the CMI code	This is a factory expert bit that should not be changed. Modifying this bit may result in unexpected IC behavior.
MUX6 [3:0]	Determines startup sequencing from the CMI code	This is a factory expert bit that should not be changed. Modifying this bit may result in unexpected IC behavior.

MSTR13 - Master Configuration Register

Address = 0x13h	Default = 0x26h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	MODE7 [3:0]				MUX7 [3:0]			
Default	0010				0110			
Access	R/W				R/W			

Name	Description	Notes
MODE7 [3:0]	Determines startup sequencing from the CMI code	This is a factory expert bit that should not be changed. Modifying this bit may result in unexpected IC behavior.
MUX7 [3:0]	Determines startup sequencing from the CMI code	This is a factory expert bit that should not be changed. Modifying this bit may result in unexpected IC behavior.

MSTR14 - Master Configuration Register

Address = 0x14h	Default = 0xE4h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	POK_OV [2:0]		VsysWarn [4:0]					
Default	111		00100					
Access	R/W		R/W					

Name	Description	Notes
POK_OV [2:0]	VIN POK OV setting 000: 3.50V 001: 3.80V 010: 4.11V 011: 4.40V 100: 4.70V 101: 5.00V 110: 5.30V 111: 5.60V	
VsysWarn [4:0]	VSYSWARN setting (rising) 00000: 2.7V to 11110: 5.7, step size = 0.1V 11110 to 11111: 5.7V	

MSTR27 - Master Configuration Register

Address = 0x27h	Default = 0x0Dh	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	MODE8 [3:0]				MUX8 [3:0]			
Default	0000				11101			
Access	R/W				R/W			

Name	Description	Notes
MODE8 [3:0]	Determines startup sequencing from the CMI code	This is a factory expert bit that should not be changed. Modifying this bit may result in unexpected IC behavior.
MUX8 [3:0]	Determines startup sequencing from the CMI code	This is a factory expert bit that should not be changed. Modifying this bit may result in unexpected IC behavior.

MSTR28 - Master Configuration Register

Address = 0x28h	Default = 0x6Ch	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	MODE9 [3:0]				MUX9 [3:0]			
Default	0110				1100			
Access	R/W				R/W			

Name	Description	Notes
MODE9 [3:0]	Determines startup sequencing from the CMI code	This is a factory expert bit that should not be changed. Modifying this bit may result in unexpected IC behavior.
MUX9 [3:0]	Determines startup sequencing from the CMI code	This is a factory expert bit that should not be changed. Modifying this bit may result in unexpected IC behavior.

MSTR29 - Master Configuration Register

Address = 0x29h	Default = 0x10h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	MODE10 [3:0]				MUX10 [3:0]			
Default	0001				0000			
Access	R/W				R/W			

Name	Description	Notes
MODE10 [3:0]	Determines startup sequencing from the CMI code	This is a factory expert bit that should not be changed. Modifying this bit may result in unexpected IC behavior.
MUX10 [3:0]	Determines startup sequencing from the CMI code	This is a factory expert bit that should not be changed. Modifying this bit may result in unexpected IC behavior.

MSTR2A - Master Configuration Register

Address = 0x2Ah	Default = 0x01h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	MODE11 [3:0]				MUX11 [3:0]			
Default	0000				0001			
Access	R/W				R/W			

Name	Description	Notes
MODE11 [3:0]	Determines startup sequencing from the CMI code	This is a factory expert bit that should not be changed. Modifying this bit may result in unexpected IC behavior.
MUX11 [3:0]	Determines startup sequencing from the CMI code	This is a factory expert bit that should not be changed. Modifying this bit may result in unexpected IC behavior.

MSTR33 - Master Configuration Register

Address = 0x33h	Default = 0x00h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	GPIO9_ILed [3:0]				GPIO10_ILed [3:0]			
Default	0000				0000			
Access	R/W				R/W			

Name	Description	Notes
GPIOX_ILed [3:0]	LED current setting for the GPIOx: 000: 0mA 001: 0.5mA 010: 1mA 011:1.5mA 100: 2mA 101: 3mA 110:4mA 111:6mA	

MSTR34 - Master Configuration Register

Address = 0x34h	Default = 0x80h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	nSaveIqMstr	EN_PP_GPIO8	EN_PP_GPIO7	EN_PP_GPIO6	EN_PP_GPIO4	EN_PP_GPIO3	EN_PP_GPIO2	EN_PP_GPIO1
Default	1	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Name	Description	Notes
nSaveIqMstr	EN SAVE CURRENT MSTR 0 = Shutdown some circuit (VINT REG, OSC…) to save current in POWER OFF state. 1 = Turn-on circuit on MSTR in POWER OFF state, include REF, OSC, VINT REG....	"EN_SAVE_CURRENT_MSTR" need set to 1.
EN_PP_GPIOx	0 = GPIOx will be Open drain 1 = Enable push pull option when the GPIOx set as output mode	

B1_REG40 – Buck1 Configuration Register

Address = 0x40h	Default = 0x0Fh	Type = Basic Volatile

BIT	7	6	5	4	3	2	1	0
Name	POK	OV	ILIM	ILIM_WARN	UV_FLTMSK	OV_FLTMSK	ILIM_FLTMSK	IlimWarnFM
Default	0	0	0	0	1	1	1	1
Access	RO	RO	RO	RO	R/W	R/W	R/W	R/W

Name	Description	Notes
POK	POK status. 0 = Buck1 voltage is below the power good threshold 1 =Buck1 voltage is above the power good threshold	Provides real-time power good status
OV	OV status. 0 = Buck1 voltage is below the overvoltage threshold 1 =Buck1 voltage is over the overvoltage threshold	Provides real-time overvoltage status
ILIM	ILIM status. 0 = Buck1 is below the ILIM threshold 1 = Buck1 is above the ILIM threshold	Provides real-time current limit status
ILIM_WARN	ILIM Warning status. 0 = Buck1 is below the ILIM warn threshold 1 = Buck1 is above the ILIM warn threshold	Provides real-time current limit warning status
UV_FLTMSK	Mask VOUT UV interrupt and fault: 0 = Unmask VOUT UV interrupt 1 = Default mask VOUT UV interrupt	When 1, the VOUT UV fault is masked, the fault signal will not be sent to the master.
OV_FLTMSK	Mask VOUT OV interrupt and fault: 0 = Unmask VOUT OV interrupt 1 = Default mask VOUT OV interrupt	When 1, the VOUT OV fault is masked, the fault signal will not be sent to the master. B1_OV still provide real-time status.
ILIM_FLT_MSK	Mask ILIM warning interrupt and fault: 0 = Unmask ILM warning interrupt 1 = Default mask ILIM warning interrupt	When 1, the ILIM fault is masked, the fault signal will not be sent to the master. ILIM still provides real-time current limit status.
IlimWarnFM	Mask ILIM warning interrupt and fault: 0 = Unmask ILM warning interrupt 1 = Default mask ILIM warning interrupt	When 1, the ILIM_WARN fault is masked, the fault signal will not be sent to the master. ILIM_WARN still provides real-time current limit warn status.

B1_REG41 – Buck1 Configuration Register

Address = 0x41h	Default = 0x28h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	ForceLpmFont	DisLpmFont	PullUpGPIO2	DisPullDown	PullUpGPIO6	EnMinpkLpm	DRV_ADJ [1:0]	
Default	0	0	1	0	1	0	00	
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	

Name	Description	Notes
ForceLpmFont	Force to work in LPM FONT (Fix ON TIME). 0 = Depend on the state in the SLEEP or NOT. It will work in LPM FONT Mode when enter SLEEP/DSLEEP. 1 = Force to work in LPM FONT	LPM FONT is ULPM mode. This bit only have effect when DisLpmFont =0.
DisLpmFont	Disable LPM FONT Mode 0 = Enable LPM FONT 1 = Disable LPM FONT	
PullUpGPIO2	Internal Pull up selection. 0 = no internal pull up 1 = internal pull up the GPIO to VIO with 86kOhm	
DisPullDown	Option to disable PullDown Resistor when BUCK is turned-off. 0 = Discharge VOUT with 5ohm when BUCK is off 1 = Don't discharge VOUT when turn-off BUCK	When = 0, the discharge resistor is connected to Vout when Buck1 is turned off.
PullUpGPIO6	Internal Pull up selection. 0 = no internal pull up 1 = internal pull up the GPIO to VIO with 86kOhm	
EnMinpkLpm	Use MINPK for LPM mode. 0 = Disable 1 = Enable	Only set this bit to 1 when duty is higher than 75%. Need to set EN_MINPK=1
DRV_ADJ [1:0]	Adjust Gate Driver (Rising and Falling SW) 00: Slowest 11: Fastest	

B1_REG42_0 – Buck1 Configuration Register

Address = 0x42_0h	Default = 0x3Ch	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	EN_OutPD	VSET0[6:0]						
Default	0	0111100						
Access	R/W	R/W						

Name	Description	Notes
EN_OutPD	Enable pull down current at VOUT to avoid low frequency signal (2Hz to 20kHz) 0 = Disable 1 = Enable	
VSET0[6:0]	VOUT = 0.5V + VSET [] * 0.005V (Range = 0) VOUT = 0.5V + VSET [] * 0.025V (Range = 1)	

B1_REG43_0 – Buck1 Configuration Register

Address = 0x43_0h	Default = 0x32h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	RFU	VSET1[6:0]						
Default	0	0110010						
Access	RO	R/W						

Name	Description	Notes
RFU	Reserved for Future Use	Do not change this register value. Changing the register value can affect IC functionality.
VSET1[6:0]	VOUT = 0.5V + VSET [] * 0.005V (Range = 0) VOUT = 0.5V + VSET [] * 0.025V (Range = 1)	

B1_REG42_1 – Buck1 Configuration Register

Address = 0x42_1h	Default = 0x28h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	IPD_SET [0]	VSET2[6:0]						
Default	0	0101000						
Access	R/W	R/W						

Name	Description	Notes
IPD_SET [0]	Set pull down current by IPD_SET [1:0]: 00: 12mA 01: 27mA 10: 37mA 11: 47mA	IPD_SET [1] at 0x43_1 bit7. IPD_SET [0] and IPD_SET [1] are used together to set the pulldown current.
VSET2[6:0]	VOUT = 0.5V + VSET [] * 0.005V (Range = 0) VOUT = 0.5V + VSET [] * 0.025V (Range = 1)	

B1_REG43_1 – Buck1 Configuration Register

Address = 0x43_1h	Default = 0x1Eh	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	IPD_SET [1]	VSET3[6:0]						
Default	0	0011110						
Access	R/W	R/W						

Name	Description	Notes
IPD_SET [1]	Set pull down current by IPD_SET [1:0]: 00: 12mA 01: 27mA 10: 37mA 11: 47mA	IPD_SET [0] and IPD_SET [1] are used together to set the pulldown current.
VSET3[6:0]	VOUT = 0.5V + VSET [] * 0.005V (Range = 0) VOUT = 0.5V + VSET [] * 0.025V (Range = 1)	

B1_REG44 – Buck1 Configuration Register

Address = 0x44h	Default = 0xB6h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	ON	PBINEN	QLITCH	SLEEPEN	AUXINEN	DPSLPEN	ILIM_SET	FORCEPWM
Default	1	0	1	1	0	1	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Name	Description	Notes
ON	0 = Buck1 is enabled through normal sequencing routing 1 = Buck1 I2C enable bit that bypasses normal sequencing	This functionality is dependent on the overall IC configuration. Consult the factory for details.
PBINEN	0 = Does not respond to push button mode 1 = Responds to turn on automatically with push button input.	Do not change this bit. Modifying this bit may result in unexpected IC behavior.
QLTCH	0 = Buck1 shuts down when its sequencing trigger input shuts down 1 = Buck1 stays on when its sequencing trigger input shuts down	
SLEEPEN	Enable Buck1 in SLEEP mode 0 = Buck1 stays on when the IC enters Sleep mode 1 = Buck1 turns off when the IC enters Sleep mode	
AUXINEN	0 = Buck1 turn on/off cannot be controlled with auxiliary input. 1 = Buck1 turn on/off can be controlled with auxiliary input.	Control bit to use internal gb_aux line as control input for turn on/off.
DPSLPEN	Enable Buck1 in Deep SLEEP mode 0 = Buck1 stays on when the IC enters DP SLEEP mode 1 = Buck1 turns off when the IC enters DP SLEEP mode	
ILIM_SET	Setting for current limit: 0 = Peak current limit set to 3.80A 1 = Peak current limit set to 5.00A	
FORCEPWM	Force Buck work in PWM mode. 0 = Not force work in PWM mode 1 = Force work in PWM mode	

B1_REG45 – Buck1 Configuration Register

Address = 0x45h	Default = 0xF8h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	MODE	RST	DBQL [2:0]			DBOK [2:0]		
Default	1	1	111			000		
Access	R/W	R/W	R/W			R/W		

Name	Description	Notes
MODE	Determines startup sequencing from the CMI code	Do not change this bit.
RST	0 = Buck1 does not affect nRESET output 1 = Buck1 POK affects nRESET output	RST bit determines if the regulator power okay (POK) signal is required to go high before the nRESET output from the PMIC can assert.
DBQL [2:0]	Determines startup sequencing from the CMI code	This is a factory expert bit that should not be changed. Modifying this bit may result in unexpected IC behavior.
DBOK [2:0]	Determines startup sequencing from the CMI code	This is a factory expert bit that should not be changed. Modifying this bit may result in unexpected IC behavior.

B1_REG46 – Buck1 Configuration Register

Address = 0x46h	Default = 0x00h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	DBON [3:0]				SST	DISLPM	Vout_Range	RFU
Default	0000				0	1	00	0
Access	R/W				R/W	R/W	R/W	RO

Name	Description	Notes
DBON [3:0]	Determines startup sequencing from the CMI code	Do not change this bit. Modifying this bit may result in unexpected IC behavior.
SST	Soft start time option 0 = 500us 1 = 250us	
DISLPM	Disable Low Power Mode. 0 = Enable LPM 1 = Disable LPM	If disable lower power mode, Buck1 will work in DCM or CCM depend on the output load.
Vout_Range	Select Vout Range: 0: Vout = 0.5V ~1.135V 1: Vout = 0.5V ~ 3.675V	
RFU	Reserved for Future Use	Do not change this register value. Changing the register value can affect IC functionality.

B1_REG47 – Buck1 Configuration Register

Address = 0x47h	Default = 0x90h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	PullUpGPIO11	PHASE	ONDELAY [2:0]			OFFDELAY [2:0]		
Default	1	0	010			000		
Access	R/W	R/W	R/W			R/W		

Name	Description	Notes
PullUpGPIO11	0 = no internal pull up 1 = internal pull up the GPIO to VIO with 86kOhm	Internal Pull up selection.
PHASE	0 = Aligns converter switching to the main clock rising edge 1 = Aligns converter switching to the main clock falling edge	Main Clock has duty = 50%, PHASE=1 shifts BUCK1 switching by 180 deg
ONDELAY [2:0]	MSB_ONDELAY [2:0]: 0_000: 28.5 us 0_001: 28.5 us 0_010: 114 us 0_011: 228 us 0_100: 456 us 0_101: 912 us 0_110: 1824 us 0_111: 3648 us 1_000: 0us 1_001: 500us 1_010: 1000us 1_011: 2000us 1_100: 4000us 1_101: 8000us 1_110: 16000us 1_111: 32000us	MSB setting of 0/1 is only factory accessible register bit and requires factory programming.
OFFDELAY [2:0]	MSB_OFFDELAY [2:0]: 0_000: 28.5 us 0_001: 28.5 us 0_010: 114 us 0_011: 228 us 0_100: 456 us 0_101: 912 us 0_110: 1824 us 0_111: 3648 us 1_000: 0us 1_001: 500us 1_010: 1000us 1_011: 2000us 1_100: 4000us 1_101: 8000us 1_110: 16000us 1_111: 32000us	MSB setting of 0/1 is only factory accessible register bit and requires factory programming.

B2_REG60 – BUCK2 Configuration Register

Address = 0x60h	Default = 0x0Fh	Type = Basic Volatile

BIT	7	6	5	4	3	2	1	0
Name	POK	OV	ILIM	ILIM_WARN	UV_FLTMSK	OV_FLTMSK	ILIM_FLTMSK	IlimWarnFM
Default	0	0	0	0	1	1	1	1
Access	RO	RO	RO	RO	R/W	R/W	R/W	R/W

Name	Description	Notes
POK	POK status. 0 = BUCK2 voltage is below the power good threshold 1 =BUCK2 voltage is above the power good threshold	Provides real-time power good status
OV	OV status. 0 = BUCK2 voltage is below the overvoltage threshold 1 =BUCK2 voltage is over the overvoltage threshold	Provides real-time overvoltage status
ILIM	ILIM status. 0 = BUCK2 is below the ILIM threshold 1 = BUCK2 is above the ILIM threshold	Provides real-time current limit status
ILIM_WARN	ILIM Warning status. 0 = BUCK2 is below the ILIM warn threshold 1 = BUCK2 is above the ILIM warn threshold	Provides real-time current limit warning status
UV_FLTMSK	Mask VOUT UV interrupt and fault: 0 = Unmask VOUT UV interrupt 1 = Default mask VOUT UV interrupt	When 1, the VOUT UV fault is masked, the fault signal will not be sent to the master.
OV_FLTMSK	Mask VOUT OV interrupt and fault: 0 = Unmask VOUT OV interrupt 1 = Default mask VOUT OV interrupt	When 1, the VOUT OV fault is masked, the fault signal will not be sent to the master. B2_OV still provide real-time status.
ILIM_FLT_MSK	Mask ILIM warning interrupt and fault: 0 = Unmask ILM warning interrupt 1 = Default mask ILIM warning interrupt	When 1, the ILIM fault is masked, the fault signal will not be sent to the master. ILIM still provides real-time current limit status.
IlimWarnFM	Mask ILIM warning interrupt and fault: 0 = Unmask ILM warning interrupt 1 = Default mask ILIM warning interrupt	When 1, the ILIM_WARN fault is masked, the fault signal will not be sent to the master. ILIM_WARN still provides real-time current limit warn status.

B2_REG61 – BUCK2 Configuration Register

Address = 0x61h	Default = 0x00h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	ForceLpmFont	DisLpmFont	RFU	DisPullDown	RFU	EnMinpkLpm	DRV_ADJ [1:0]	
Default	0	0	0	0	0	0	00	
Access	R/W	R/W	RO	R/W	RO	R/W	R/W	

Name	Description	Notes
ForceLpmFont	Force to work in LPM FONT (Fix ON TIME). 0 = Depend on the state in the SLEEP or NOT. It will work in LPM FONT Mode when enter SLEEP/DSLEEP. 1 = Force to work in LPM FONT	LPM FONT is ULPM mode. This bit only have effect when DisLpmFont =0.
DisLpmFont	Disable LPM FONT Mode 0 = Enable LPM FONT 1 = Disable LPM FONT	
RFU	Reserved for Future Use	Do not change this register value. Changing the register value can affect IC functionality.
DisPullDown	Option to disable PullDown Resistor when BUCK is turned-off. 0 = Discharge VOUT with 5ohm when BUCK is off 1 = Don't discharge VOUT when turn-off BUCK	When = 0, the discharge resistor is connected to Vout when BUCK2 is turned off.
RFU	Reserved for Future Use	Do not change this register value. Changing the register value can affect IC functionality.
EnMinpkLpm	Use MINPK for LPM mode. 0 = Disable 1 = Enable	Only set this bit to 1 when duty is higher than 75%. Need to set EN_MINPK=1
DRV_ADJ [1:0]	Adjust Gate Driver (Rising and Falling SW) 00: Slowest 11: Fastest	

B2_REG62_0 – BUCK2 Configuration Register

Address = 0x62_0h	Default = 0x3Ch	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	EN_OutPD	VSET0[6:0]						
Default	0	0111100						
Access	R/W	R/W						

Name	Description	Notes
EN_OutPD	Enable pull down current at VOUT to avoid low frequency signal (2Hz to 20kHz) 0 = Disable 1 = Enable	
VSET0[6:0]	VOUT = 0.5V + VSET [] * 0.005V (Range = 0) VOUT = 0.5V + VSET [] * 0.025V (Range = 1)	

B2_REG63_0 – BUCK2 Configuration Register

Address = 0x63_0h	Default = 0x32h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	RFU	VSET1[6:0]						
Default	0	0110010						
Access	RO	R/W						

Name	Description	Notes
RFU	Reserved for Future Use	Do not change this register value. Changing the register value can affect IC functionality.
VSET1[6:0]	VOUT = 0.5V + VSET [] * 0.005V (Range = 0) VOUT = 0.5V + VSET [] * 0.025V (Range = 1)	

B2_REG62_1 – BUCK2 Configuration Register

Address = 0x62_1h	Default = 0x28h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	IPD_SET [0]	VSET2[6:0]						
Default	0	0101000						
Access	R/W	R/W						

Name	Description	Notes
IPD_SET [0]	Set pull down current by IPD_SET [1:0]: 00: 12mA 01: 27mA 10: 37mA 11: 47mA	IPD_SET [1] at 0x63_1 bit7. IPD_SET [0] and IPD_SET [1] are used together to set the pulldown current.
VSET2[6:0]	VOUT = 0.5V + VSET [] * 0.005V (Range = 0) VOUT = 0.5V + VSET [] * 0.025V (Range = 1)	

B2_REG63_1 – BUCK2 Configuration Register

Address = 0x63_1h	Default = 0x1Eh	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	IPD_SET [1]	VSET3[6:0]						
Default	0	0011110						
Access	R/W	R/W						

Name	Description	Notes
IPD_SET [1]	Set pull down current by IPD_SET [1:0]: 00: 12mA 01: 27mA 10: 37mA 11: 47mA	IPD_SET [0] and IPD_SET [1] are used together to set the pulldown current.
VSET3[6:0]	VOUT = 0.5V + VSET [] * 0.005V (Range = 0) VOUT = 0.5V + VSET [] * 0.025V (Range = 1)	

B2_REG64 – BUCK2 Configuration Register

Address = 0x64h	Default = 0xB6h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	ON	PBINEN	QLITCH	SLEEPEN	AUXINEN	DPSLPEN	ILIM_SET	FORCEPWM
Default	1	0	1	1	0	1	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Name	Description	Notes
ON	0 = BUCK2 is enabled through normal sequencing routing 1 = BUCK2 I2C enable bit that bypasses normal sequencing	This functionality is dependent on the overall IC configuration. Consult the factory for details.
PBINEN	0 = Does not respond to push button mode 1 = Responds to turn on automatically with push button input.	Do not change this bit. Modifying this bit may result in unexpected IC behavior.
QLTCH	0 = BUCK2 shuts down when its sequencing trigger input shuts down 1 = BUCK2 stays on when its sequencing trigger input shuts down	
SLEEPEN	Enable BUCK2 in SLEEP mode 0 = BUCK2 stays on when the IC enters Sleep mode 1 = BUCK2 turns off when the IC enters Sleep mode	
AUXINEN	0 = BUCK2 turn on/off cannot be controlled with auxiliary input. 1 = BUCK2 turn on/off can be controlled with auxiliary input.	Control bit to use internal gb_aux line as control input for turn on/off.
DPSLPEN	Enable BUCK2 in Deep SLEEP mode 0 = BUCK2 stays on when the IC enters DP SLEEP mode 1 = BUCK2 turns off when the IC enters DP SLEEP mode	
ILIM_SET	Setting for current limit: 0 = Peak current limit set to 3.80A 1 = Peak current limit set to 5.00A	
FORCEPWM	Force Buck work in PWM mode. 0 = Not force work in PWM mode 1 = Force work in PWM mode	

B2_REG65 – BUCK2 Configuration Register

Address = 0x65h	Default = 0xF8h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	MODE	RST	DBQL [2:0]			DBOK [2:0]		
Default	1	1	111			000		
Access	R/W	R/W	R/W			R/W		

Name	Description	Notes
MODE	Determines startup sequencing from the CMI code	Do not change this bit.
RST	0 = Buck2 does not affect nRESET output 1 = Buck2 POK affects nRESET output	RST bit determines if the regulator power okay (POK) signal is required to go high before the nRESET output from the PMIC can assert.
DBQL [2:0]	Determines startup sequencing from the CMI code	This is a factory expert bit that should not be changed. Modifying this bit may result in unexpected IC behavior.
DBOK [2:0]	Determines startup sequencing from the CMI code	This is a factory expert bit that should not be changed. Modifying this bit may result in unexpected IC behavior.

B2_REG66 – BUCK2 Configuration Register

Address = 0x66h	Default = 0x00h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	DBON [3:0]				SST	DISLPM	Vout_Range	RFU
Default	0000				0	1	00	0
Access	R/W				R/W	R/W	R/W	RO

Name	Description	Notes
DBON [3:0]	Determines startup sequencing from the CMI code	Do not change this bit. Modifying this bit may result in unexpected IC behavior.
SST	Soft start time option 0 = 500us 1 = 250us	
DISLPM	Disable Low Power Mode. 0 = Enable LPM 1 = Disable LPM	If disable lower power mode, BUCK2 will work in DCM or CCM depend on the output load.
Vout_Range	Select Vout Range: 0: Vout = 0.5V ~1.135V 1: Vout = 0.5V ~ 3.675V	
RFU	Reserved for Future Use	Do not change this register value. Changing the register value can affect IC functionality.

B2_REG67 – BUCK2 Configuration Register

Address = 0x67h	Default = 0x10h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	RFU	PHASE	ONDELAY [2:0]			OFFDELAY [2:0]		
Default	0	0	010			000		
Access	RO	R/W	R/W			R/W		

Name	Description	Notes
RFU	Reserved for Future Use	Do not change this register value. Changing the register value can affect IC functionality.
PHASE	0 = Aligns converter switching to the main clock rising edge 1 = Aligns converter switching to the main clock falling edge	Main Clock has duty = 50%, PHASE=1 shifts BUCK2 switching by 180 deg
ONDELAY [2:0]	MSB_ONDELAY [2:0]: 0_000: 28.5 us 0_001: 28.5 us 0_010: 114 us 0_011: 228 us 0_100: 456 us 0_101: 912 us 0_110: 1824 us 0_111: 3648 us 1_000: 0us 1_001: 500us 1_010: 1000us 1_011: 2000us 1_100: 4000us 1_101: 8000us 1_110: 16000us 1_111: 32000us	MSB setting of 0/1 is only factory accessible register bit and requires factory programming.
OFFDELAY [2:0]	MSB_OFFDELAY [2:0]: 0_000: 28.5 us 0_001: 28.5 us 0_010: 114 us 0_011: 228 us 0_100: 456 us 0_101: 912 us 0_110: 1824 us 0_111: 3648 us 1_000: 0us 1_001: 500us 1_010: 1000us 1_011: 2000us 1_100: 4000us 1_101: 8000us 1_110: 16000us 1_111: 32000us	MSB setting of 0/1 is only factory accessible register bit and requires factory programming.

B3_REG80 – BUCK3 Configuration Register

Address = 0x80h	Default = 0x0Fh	Type = Basic Volatile

BIT	7	6	5	4	3	2	1	0
Name	POK	OV	ILIM	ILIM_WARN	UV_FLTMSK	OV_FLTMSK	ILIM_FLTMSK	IlimWarnFM
Default	0	0	0	0	1	1	1	1
Access	RO	RO	RO	RO	R/W	R/W	R/W	R/W

Name	Description	Notes
POK	POK status. 0 = BUCK3 voltage is below the power good threshold 1 =BUCK3 voltage is above the power good threshold	Provides real-time power good status
OV	OV status. 0 = BUCK3 voltage is below the overvoltage threshold 1 =BUCK3 voltage is over the overvoltage threshold	Provides real-time overvoltage status
ILIM	ILIM status. 0 = BUCK3 is below the ILIM threshold 1 = BUCK3 is above the ILIM threshold	Provides real-time current limit status
ILIM_WARN	ILIM Warning status. 0 = BUCK3 is below the ILIM warn threshold 1 = BUCK3 is above the ILIM warn threshold	Provides real-time current limit warning status
UV_FLTMSK	Mask VOUT UV interrupt and fault: 0 = Unmask VOUT UV interrupt 1 = Default mask VOUT UV interrupt	When 1, the VOUT UV fault is masked, the fault signal will not be sent to the master.
OV_FLTMSK	Mask VOUT OV interrupt and fault: 0 = Unmask VOUT OV interrupt 1 = Default mask VOUT OV interrupt	When 1, the VOUT OV fault is masked, the fault signal will not be sent to the master. B3_OV still provide real-time status.
ILIM_FLT_MSK	Mask ILIM warning interrupt and fault: 0 = Unmask ILM warning interrupt 1 = Default mask ILIM warning interrupt	When 1, the ILIM fault is masked, the fault signal will not be sent to the master. ILIM still provides real-time current limit status.
IlimWarnFM	Mask ILIM warning interrupt and fault: 0 = Unmask ILM warning interrupt 1 = Default mask ILIM warning interrupt	When 1, the ILIM_WARN fault is masked, the fault signal will not be sent to the master. ILIM_WARN still provides real-time current limit warn status.

B3_REG81 – BUCK3 Configuration Register

Address = 0x81h	Default = 0x08h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	ForceLpmFont	DisLpmFont	TileOnToPok	DisPullDown	Vout_Range	EnMinpkLpm	DRV_ADJ [1:0]	
Default	0	0	0	0	1	0	00	
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	

Name	Description	Notes
ForceLpmFont	Force to work in LPM FONT (Fix ON TIME). 0 = Depend on the state in the SLEEP or NOT. It will work in LPM FONT Mode when enter SLEEP/DSLEEP. 1 = Force to work in LPM FONT	LPM FONT is ULPM mode. This bit only have effect when DisLpmFont =0.
DisLpmFont	Disable LPM FONT Mode 0 = Enable LPM FONT 1 = Disable LPM FONT	
TileOnToPok	0 = Use actual POK 1 = Use TILE ON as POK	
DisPullDown	Option to disable PullDown Resistor when BUCK is turned-off. 0 = Discharge VOUT with 5ohm when BUCK is off 1 = Don't discharge VOUT when turn-off BUCK	When = 0, the discharge resistor is connected to Vout when BUCK3 is turned off.
Vout_Range	Select Vout Range: 0: Vout = 0.5V ~1.135V 1: Vout = 0.5V ~3.675V	
EnMinpkLpm	Use MINPK for LPM mode. 0 = Disable 1 = Enable	Only set this bit to 1 when duty is higher than 75%. Need to set EN_MINPK=1
DRV_ADJ [1:0]	Adjust Gate Driver (Rising and Falling SW) 00: Slowest 11: Fastest	

B3_REG82 – BUCK3 Configuration Register

Address = 0x82h	Default = 0x14h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	EN_OutPD	VSET0[6:0]						
Default	0	0010100						
Access	R/W	R/W						

Name	Description	Notes
EN_OutPD	Enable pull down current at VOUT to avoid low frequency signal (2Hz to 20kHz) 0 = Disable 1 = Enable	
VSET0[6:0]	VOUT = 0.5V + VSET [] * 0.005V (Range = 0) VOUT = 0.5V + VSET [] * 0.025V (Range = 1)	

B3_REG83 – BUCK3 Configuration Register

Address = 0x83h	Default = 0x10h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	IPD_SET [0]	VSET1[6:0]						
Default	0	0010000						
Access	R/W	R/W						

Name	Description	Notes
IPD_SET [0]	Set pull down current by IPD_SET [1:0]: 00: 12mA 01: 27mA 10: 37mA 11: 47mA	IPD_SET [0] and IPD_SET [1] are used together to set the pulldown current.
VSET1[6:0]	VOUT = 0.5V + VSET [] * 0.005V (Range = 0) VOUT = 0.5V + VSET [] * 0.025V (Range = 1)	

B3_REG84 – BUCK3 Configuration Register

Address = 0x84h	Default = 0xA6h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	ON	PBINEN	QLITCH	SLEEPEN	AUXINEN	DPSLPEN	ILIM_SET	FORCEPWM
Default	1	0	1	0	0	1	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Name	Description	Notes
ON	0 = BUCK3 is enabled through normal sequencing routing 1 = BUCK3 I2C enable bit that bypasses normal sequencing	This functionality is dependent on the overall IC configuration. Consult the factory for details.
PBINEN	0 = Does not respond to push button mode 1 = Responds to turn on automatically with push button input.	Do not change this bit. Modifying this bit may result in unexpected IC behavior.
QLTCH	0 = BUCK3 shuts down when its sequencing trigger input shuts down 1 = BUCK3 stays on when its sequencing trigger input shuts down	
SLEEPEN	Enable BUCK3 in SLEEP mode 0 = BUCK3 stays on when the IC enters Sleep mode 1 = BUCK3 turns off when the IC enters Sleep mode	
AUXINEN	0 = BUCK3 turn on/off cannot be controlled with auxiliary input. 1 = BUCK3 turn on/off can be controlled with auxiliary input.	Control bit to use internal gb_aux line as control input for turn on/off.
DPSLPEN	Enable BUCK3 in Deep SLEEP mode 0 = BUCK3 stays on when the IC enters DP SLEEP mode 1 = BUCK3 turns off when the IC enters DP SLEEP mode	
ILIM_SET	Setting for current limit: 0 = Peak current limit set to 3.50A 1 = Peak current limit set to 4.50A	
FORCEPWM	Force Buck work in PWM mode. 0 = Not force work in PWM mode 1 = Force work in PWM mode	

B3_REG85 – BUCK3 Configuration Register

Address = 0x85h	Default = 0xFAh	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	MODE	RST	DBQL [2:0]			DBOK [2:0]		
Default	1	1	111			010		
Access	R/W	R/W	R/W			R/W		

Name	Description	Notes
MODE	Determines startup sequencing from the CMI code	Do not change this bit.
RST	0 = BUCK3 does not affect nRESET output 1 = BUCK3 POK affects nRESET output	RST bit determines if the regulator power okay (POK) signal is required to go high before the nRESET output from the PMIC can assert.
DBQL [2:0]	Determines startup sequencing from the CMI code	This is a factory expert bit that should not be changed. Modifying this bit may result in unexpected IC behavior.
DBOK [2:0]	Determines startup sequencing from the CMI code	This is a factory expert bit that should not be changed. Modifying this bit may result in unexpected IC behavior.

B3_REG86 – BUCK3 Configuration Register

Address = 0x86h	Default = 0x03h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	DBON [3:0]				SST	DISLPM	DBSTBY [1:0]	
Default	0000				0	0	11	
Access	R/W				R/W	R/W	R/W	

Name	Description	Notes
DBON [3:0]	Determines startup sequencing from the CMI code	Do not change this bit. Modifying this bit may result in unexpected IC behavior.
SST	Soft start time option 0 = 500us 1 = 250us	
DISLPM	Disable Low Power Mode. 0 = Enable LPM 1 = Disable LPM	If disable lower power mode, BUCK3 will work in DCM or CCM depend on the output load.
DBSTBY [1:0]	Determines DVS inputs from the CMI code	Do not change this bit. Modifying this bit may result in unexpected IC behavior.

B3_REG87 – BUCK3 Configuration Register

Address = 0x87h	Default = 0x18h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	IPD_SET [1]	PHASE	ONDELAY [2:0]			OFFDELAY [2:0]		
Default	0	0	011			000		
Access	R/W	R/W	R/W			R/W		

Name	Description	Notes
IPD_SET [1]	Set pull down current: 00: 12mA 01: 27mA 10: 37mA 11: 47mA	IPD_SET [0] and IPD_SET [1] are used together to set the pulldown current.
PHASE	0 = Aligns converter switching to the main clock rising edge 1 = Aligns converter switching to the main clock falling edge	Main Clock has duty = 50%, PHASE=1 shifts BUCK3 switching by 180 deg
ONDELAY [2:0]	MSB_ONDELAY [2:0]: 0_000: 28.5 us 0_001: 28.5 us 0_010: 114 us 0_011: 228 us 0_100: 456 us 0_101: 912 us 0_110: 1824 us 0_111: 3648 us 1_000: 0 1_001: 500us 1_010: 1000us 1_011: 2000us 1_100: 4000us 1_101: 8000us 1_110: 16000us 1_111: 32000us	MSB setting of 0/1 is only factory accessible register bit and requires factory programming.
OFFDELAY [2:0]	MSB_OFFDELAY [2:0]: 0_000: 28.5 us 0_001: 28.5 us 0_010: 114 us 0_011: 228 us 0_100: 456 us 0_101: 912 us 0_110: 1824 us 0_111: 3648 us 1_000: 0 1_001: 500us 1_010: 1000us 1_011: 2000us 1_100: 4000us 1_101: 8000us 1_110: 16000us 1_111: 32000us	MSB setting of 0/1 is only factory accessible register bit and requires factory programming.

B4_REGA0 – BUCK4 Configuration Register

Address = 0xA0h	Default = 0x0Fh	Type = Basic Volatile

BIT	7	6	5	4	3	2	1	0
Name	POK	OV	ILIM	ILIM_WARN	UV_FLTMSK	OV_FLTMSK	ILIM_FLTMSK	IlimWarnFM
Default	0	0	0	0	1	1	1	1
Access	RO	RO	RO	RO	R/W	R/W	R/W	R/W

Name	Description	Notes
POK	POK status. 0 = BUCK4 voltage is below the power good threshold 1 =BUCK4 voltage is above the power good threshold	Provides real-time power good status
OV	OV status. 0 = BUCK4 voltage is below the overvoltage threshold 1 =BUCK4 voltage is over the overvoltage threshold	Provides real-time overvoltage status
ILIM	ILIM status. 0 = BUCK4 is below the ILIM threshold 1 = BUCK4 is above the ILIM threshold	Provides real-time current limit status
ILIM_WARN	ILIM Warning status. 0 = BUCK4 is below the ILIM warn threshold 1 = BUCK4 is above the ILIM warn threshold	Provides real-time current limit warning status
UV_FLTMSK	Mask VOUT UV interrupt and fault: 0 = Unmask VOUT UV interrupt 1 = Default mask VOUT UV interrupt	When 1, the VOUT UV fault is masked, the fault signal will not be sent to the master.
OV_FLTMSK	Mask VOUT OV interrupt and fault: 0 = Unmask VOUT OV interrupt 1 = Default mask VOUT OV interrupt	When 1, the VOUT OV fault is masked, the fault signal will not be sent to the master. B4_OV still provide real-time status.
ILIM_FLT_MSK	Mask ILIM warning interrupt and fault: 0 = Unmask ILM warning interrupt 1 = Default mask ILIM warning interrupt	When 1, the ILIM fault is masked, the fault signal will not be sent to the master. ILIM still provides real-time current limit status.
IlimWarnFM	Mask ILIM warning interrupt and fault: 0 = Unmask ILM warning interrupt 1 = Default mask ILIM warning interrupt	When 1, the ILIM_WARN fault is masked, the fault signal will not be sent to the master. ILIM_WARN still provides real-time current limit warn status.

B4_REGA1 – BUCK4 Configuration Register

Address = 0xA1h	Default = 0x08h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	ForceLpmFont	DisLpmFont	TileOnToPok	DisPullDown	Vout_Range	EnMinpkLpm	DRV_ADJ [1:0]	
Default	0	0	0	0	1	0	00	
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	

Name	Description	Notes
ForceLpmFont	Force to work in LPM FONT (Fix ON TIME). 0 = Depend on the state in the SLEEP or NOT. It will work in LPM FONT Mode when enter SLEEP/DSLEEP. 1 = Force to work in LPM FONT	LPM FONT is ULPM mode. This bit only have effect when DisLpmFont =0.
DisLpmFont	Disable LPM FONT Mode 0 = Enable LPM FONT 1 = Disable LPM FONT	
TileOnToPok	0 = Use actual POK 1 = Use TILE ON as POK	
DisPullDown	Option to disable PullDown Resistor when BUCK is turned-off. 0 = Discharge VOUT with 5ohm when BUCK is off 1 = Don't discharge VOUT when turn-off BUCK	When = 0, the discharge resistor is connected to Vout when BUCK4 is turned off.
Vout_Range	Select Vout Range: 0: Vout = 0.5V ~1.135V 1: Vout = 0.5V ~3.675V	
EnMinpkLpm	Use MINPK for LPM mode. 0 = Disable 1 = Enable	Only set this bit to 1 when duty is higher than 75%. Need to set EN_MINPK=1
DRV_ADJ [1:0]	Adjust Gate Driver (Rising and Falling SW) 00: Slowest 11: Fastest	

B4_REGA2 – BUCK4 Configuration Register

Address = 0xA2h	Default = 0x34h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	EN_OutPD	VSET0[6:0]						
Default	0	0110100						
Access	R/W	R/W						

Name	Description	Notes
EN_OutPD	Enable pull down current at VOUT to avoid low frequency signal (2Hz to 20kHz) 0 = Disable 1 = Enable	
VSET0[6:0]	VOUT = 0.5V + VSET [] * 0.005V (Range = 0) VOUT = 0.5V + VSET [] * 0.025V (Range = 1)	

B4_REGA3 – BUCK4 Configuration Register

Address = 0x83h	Default = 0x34h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	IPD_SET [0]	VSET1[6:0]						
Default	0	0110100						
Access	R/W	R/W						

Name	Description	Notes
IPD_SET [0]	Set pull down current by IPD_SET [1:0]: 00: 12mA 01: 27mA 10: 37mA 11: 47mA	IPD_SET [1] at 0xA7 bit7. IPD_SET [0] and IPD_SET [1] are used together to set the pulldown current.
VSET1[6:0]	VOUT = 0.5V + VSET [] * 0.005V (Range = 0) VOUT = 0.5V + VSET [] * 0.025V (Range = 1)	

B4_REGA4 – BUCK4 Configuration Register

Address = 0xA4h	Default = 0xB6h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	ON	PBINEN	QLITCH	SLEEPEN	AUXINEN	DPSLPEN	ILIM_SET	FORCEPWM
Default	1	0	1	1	0	1	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Name	Description	Notes
ON	0 = BUCK4 is enabled through normal sequencing routing 1 = BUCK4 I2C enable bit that bypasses normal sequencing	This functionality is dependent on the overall IC configuration. Consult the factory for details.
PBINEN	0 = Does not respond to push button mode 1 = Responds to turn on automatically with push button input.	Do not change this bit. Modifying this bit may result in unexpected IC behavior.
QLTCH	0 = BUCK4 shuts down when its sequencing trigger input shuts down 1 = BUCK4 stays on when its sequencing trigger input shuts down	
SLEEPEN	Enable BUCK4 in SLEEP mode 0 = BUCK4 stays on when the IC enters Sleep mode 1 = BUCK4 turns off when the IC enters Sleep mode	
AUXINEN	0 = BUCK4 turn on/off cannot be controlled with auxiliary input. 1 = BUCK4 turn on/off can be controlled with auxiliary input.	Control bit to use internal gb_aux line as control input for turn on/off.
DPSLPEN	Enable BUCK4 in Deep SLEEP mode 0 = BUCK4 stays on when the IC enters DP SLEEP mode 1 = BUCK4 turns off when the IC enters DP SLEEP mode	
ILIM_SET	Setting for current limit: 0 = Peak current limit set to 3.50A 1 = Peak current limit set to 4.50A	
FORCEPWM	Force Buck work in PWM mode. 0 = Not force work in PWM mode 1 = Force work in PWM mode	

B4_REGA5 – BUCK4 Configuration Register

Address = 0xA5h	Default = 0xB8h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	MODE	RST	DBQL [2:0]			DBOK [2:0]		
Default	1	0	111			000		
Access	R/W	R/W	R/W			R/W		

Name	Description	Notes
MODE	Determines startup sequencing from the CMI code	Do not change this bit.
RST	0 = BUCK4 does not affect nRESET output 1 = BUCK4 POK affects nRESET output	RST bit determines if the regulator power okay (POK) signal is required to go high before the nRESET output from the PMIC can assert.
DBQL [2:0]	Determines startup sequencing from the CMI code	This is a factory expert bit that should not be changed. Modifying this bit may result in unexpected IC behavior.
DBOK [2:0]	Determines startup sequencing from the CMI code	This is a factory expert bit that should not be changed. Modifying this bit may result in unexpected IC behavior.

B4_REGA6 – BUCK4 Configuration Register

Address = 0xA6h	Default = 0x03h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	DBON [3:0]				SST	DISLPM	DBSTBY [1:0]	
Default	0000				0	0	11	
Access	R/W				R/W	R/W	R/W	

Name	Description	Notes
DBON [3:0]	Determines startup sequencing from the CMI code	Do not change this bit. Modifying this bit may result in unexpected IC behavior.
SST	Soft start time option 0 = 500us 1 = 250us	
DISLPM	Disable Low Power Mode. 0 = Enable LPM 1 = Disable LPM	If disable lower power mode, BUCK4 will work in DCM or CCM depend on the output load.
DBSTBY [1:0]	Determines DVS inputs from the CMI code	Do not change this bit. Modifying this bit may result in unexpected IC behavior.

B4_REGA7 – BUCK4 Configuration Register

Address = 0xA7h	Default = 0x0Ah	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	IPD_SET [1]	PHASE	ONDELAY [2:0]			OFFDELAY [2:0]		
Default	0	0	001			010		
Access	R/W	R/W	R/W			R/W		

Name	Description	Notes
IPD_SET [1]	Set pull down current: 00: 12mA 01: 27mA 10: 37mA 11: 47mA	IPD_SET [0] and IPD_SET [1] are used together to set the pulldown current. IPD_SET [0] and IPD_SET [1] are used together to set the pulldown current.
PHASE	0 = Aligns converter switching to the main clock rising edge 1 = Aligns converter switching to the main clock falling edge	Main Clock has duty = 50%, PHASE=1 shifts BUCK4 switching by 180 deg
ONDELAY [2:0]	MSB_ONDELAY [2:0]: 0_000: 28.5 us 0_001: 28.5 us 0_010: 114 us 0_011: 228 us 0_100: 456 us 0_101: 912 us 0_110: 1824 us 0_111: 3648 us 1_000: 0us 1_001: 500us 1_010: 1000us 1_011: 2000us 1_100: 4000us 1_101: 8000us 1_110: 16000us 1_111: 32000us	MSB setting of 0/1 is only factory accessible register bit and requires factory programming.
OFFDELAY [2:0]	MSB_OFFDELAY [2:0]: 0_000: 28.5 us 0_001: 28.5 us 0_010: 114 us 0_011: 228 us 0_100: 456 us 0_101: 912 us 0_110: 1824 us 0_111: 3648 us 1_000: 0us 1_001: 500us 1_010: 1000us 1_011: 2000us 1_100: 4000us 1_101: 8000us 1_110: 16000us 1_111: 32000us	MSB setting of 0/1 is only factory accessible register bit and requires factory programming.

B5_REGC0 – BUCK5 Configuration Register

Address = 0xC0h	Default = 0x0Fh	Type = Basic Volatile

BIT	7	6	5	4	3	2	1	0
Name	POK	OV	ILIM	ILIM_WARN	UV_FLTMSK	OV_FLTMSK	ILIM_FLTMSK	IlimWarnFM
Default	0	0	0	0	1	1	1	1
Access	RO	RO	RO	RO	R/W	R/W	R/W	R/W

Name	Description	Notes
POK	POK status. 0 = BUCK5 voltage is below the power good threshold 1 =BUCK5 voltage is above the power good threshold	Provides real-time power good status
OV	OV status. 0 = BUCK5 voltage is below the overvoltage threshold 1 =BUCK5 voltage is over the overvoltage threshold	Provides real-time overvoltage status
ILIM	ILIM status. 0 = BUCK5 is below the ILIM threshold 1 = BUCK5 is above the ILIM threshold	Provides real-time current limit status
ILIM_WARN	ILIM Warning status. 0 = BUCK5 is below the ILIM warn threshold 1 = BUCK5 is above the ILIM warn threshold	Provides real-time current limit warning status
UV_FLTMSK	Mask VOUT UV interrupt and fault: 0 = Unmask VOUT UV interrupt 1 = Default mask VOUT UV interrupt	When 1, the VOUT UV fault is masked, the fault signal will not be sent to the master.
OV_FLTMSK	Mask VOUT OV interrupt and fault: 0 = Unmask VOUT OV interrupt 1 = Default mask VOUT OV interrupt	When 1, the VOUT OV fault is masked, the fault signal will not be sent to the master. B5_OV still provide real-time status.
ILIM_FLT_MSK	Mask ILIM warning interrupt and fault: 0 = Unmask ILM warning interrupt 1 = Default mask ILIM warning interrupt	When 1, the ILIM fault is masked, the fault signal will not be sent to the master. ILIM still provides real-time current limit status.
IlimWarnFM	Mask ILIM warning interrupt and fault: 0 = Unmask ILM warning interrupt 1 = Default mask ILIM warning interrupt	When 1, the ILIM_WARN fault is masked, the fault signal will not be sent to the master. ILIM_WARN still provides real-time current limit warn status.

B5_REGC1 – BUCK5 Configuration Register

Address = 0xC1h	Default = 0x00h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	ForceLpmFont	DisLpmFont	TileOnToPok	DisPullDown	EN_OutPD	EnMinpkLpm	DRV_ADJ [1:0]	
Default	0	0	0	0	0	0	00	
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	

Name	Description	Notes
ForceLpmFont	Force to work in LPM FONT (Fix ON TIME). 0 = Depend on the state in the SLEEP or NOT. It will work in LPM FONT Mode when enter SLEEP/DSLEEP. 1 = Force to work in LPM FONT	LPM FONT is ULPM mode. This bit only have effect when DisLpmFont =0.
DisLpmFont	Disable LPM FONT Mode 0 = Enable LPM FONT 1 = Disable LPM FONT	
TileOnToPok	0 = Use actual POK 1 = Use TILE ON as POK	
DisPullDown	Option to disable PullDown Resistor when BUCK is turned-off. 0 = Discharge VOUT with 5ohm when BUCK is off 1 = Don't discharge VOUT when turn-off BUCK	When = 0, the discharge resistor is connected to Vout when BUCK5 is turned off.
EN_OutPD	Enable pull down current at Vout to avoid low frequency signal (2Hz to 20kHz) 0 = Disable 1 = Enable	
EnMinpkLpm	Use MINPK for LPM mode. 0 = Disable 1 = Enable	Only set this bit to 1 when duty is higher than 75%. Need to set EN_MINPK=1
DRV_ADJ [1:0]	Adjust Gate Driver (Rising and Falling SW) 00: Slowest 11: Fastest	

B5_REGC2 – BUCK5 Configuration Register

Address = 0xC2h	Default = 0x58h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	IPD_SET [0]	VSET0[6:0]						
Default	0	1011000						
Access	R/W	R/W						

Name	Description	Notes
IPD_SET [0]	Set pull down current by IPD_SET [1:0]: 00: 12mA 01: 27mA 10: 37mA 11: 47mA	IPD_SET [1] at 0xC3 bit7. IPD_SET [0] and IPD_SET [1] are used together to set the pulldown current.
VSET0[6:0]	VOUT = 0.5V + VSET [] * 0.025V	

B5_REGC3 – BUCK5 Configuration Register

Address = 0xC3h	Default = 0x50h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	IPD_SET [1]	VSET1[6:0]						
Default	0	1010000						
Access	R/W	R/W						

Name	Description	Notes
IPD_SET [1]	Set pull down current by IPD_SET [1:0]: 00: 12mA 01: 27mA 10: 37mA 11: 47mA	IPD_SET [0] and IPD_SET [1] are used together to set the pulldown current.
VSET1[6:0]	VOUT = 0.5V + VSET [] * 0.025V	

B5_REGC4 – BUCK5 Configuration Register

Address = 0xC4h	Default = 0xB6h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	ON	PBINEN	QLITCH	SLEEPEN	AUXINEN	DPSLPEN	ILIM_SET	FORCEPWM
Default	1	0	1	1	0	1	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Name	Description	Notes
ON	0 = BUCK5 is enabled through normal sequencing routing 1 = BUCK5 I2C enable bit that bypasses normal sequencing	This functionality is dependent on the overall IC configuration. Consult the factory for details.
PBINEN	0 = Does not respond to push button mode 1 = Responds to turn on automatically with push button input.	Do not change this bit. Modifying this bit may result in unexpected IC behavior.
QLTCH	0 = BUCK5 shuts down when its sequencing trigger input shuts down 1 = BUCK5 stays on when its sequencing trigger input shuts down	
SLEEPEN	Enable BUCK5 in SLEEP mode 0 = BUCK5 stays on when the IC enters Sleep mode 1 = BUCK5 turns off when the IC enters Sleep mode	
AUXINEN	0 = BUCK5 turn on/off cannot be controlled with auxiliary input. 1 = BUCK5 turn on/off can be controlled with auxiliary input.	Control bit to use internal gb_aux line as control input for turn on/off.
DPSLPEN	Enable BUCK5 in Deep SLEEP mode 0 = BUCK5 stays on when the IC enters DP SLEEP mode 1 = BUCK5 turns off when the IC enters DP SLEEP mode	
ILIM_SET	Setting for current limit: 0 = Peak current limit set to 2.0A 1 = Peak current limit set to 3.0A	
FORCEPWM	Force Buck work in PWM mode. 0 = Not force work in PWM mode 1 = Force work in PWM mode	

B5_REGC5 – BUCK5 Configuration Register

Address = 0xC5h	Default = 0x90h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	MODE	RST	DBQL [2:0]			DBOK [2:0]		
Default	1	0	010			000		
Access	R/W	R/W	R/W			R/W		

Name	Description	Notes
MODE	Determines startup sequencing from the CMI code	This is a factory expert bit that should not be changed. Modifying this bit may result in unexpected IC behavior.
RST	0 = BUCK5 does not affect nRESET output 1 = BUCK5 POK affects nRESET output	RST bit determines if the regulator power okay (POK) signal is required to go high before the nRESET output from the PMIC can assert.
DBQL [2:0]	Determines startup sequencing from the CMI code	This is a factory expert bit that should not be changed. Modifying this bit may result in unexpected IC behavior.
DBOK [2:0]	Determines startup sequencing from the CMI code	This is a factory expert bit that should not be changed. Modifying this bit may result in unexpected IC behavior.

B5_REGC6 – BUCK5 Configuration Register

Address = 0xC6h	Default = 0x03h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	DBON [3:0]				SST	DISLPM	DBSTBY [1:0]	
Default	0000				0	0	11	
Access	R/W				R/W	R/W	R/W	

Name	Description	Notes
DBON [3:0]	Determines startup sequencing from the CMI code	Do not change this bit. Modifying this bit may result in unexpected IC behavior.
SST	Soft start time option 0 = 500us 1 = 250us	
DISLPM	Disable Low Power Mode. 0 = Enable LPM 1 = Disable LPM	If disable lower power mode, BUCK5 will work in DCM or CCM depend on the output load.
DBSTBY [1:0]	Determines DVS inputs from the CMI code	Do not change this bit. Modifying this bit may result in unexpected IC behavior.

B5_REGC7 – BUCK5 Configuration Register

Address = 0xC7h	Default = 0x0Ah	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	AdjTFONT	PHASE	ONDELAY [2:0]			OFFDELAY [2:0]		
Default	0	0	001			010		
Access	R/W	R/W	R/W			R/W		

Name	Description	Notes
AdjTFONT	0 = Not adjust the Ton 1 = Increase Ton 40% in FONT mode	
PHASE	0 = Aligns converter switching to the main clock rising edge 1 = Aligns converter switching to the main clock falling edge	Main Clock has duty = 50%, PHASE=1 shifts BUCK5 switching by 180 deg
ONDELAY [2:0]	MSB_ONDELAY [2:0]: 0_000: 28.5 us 0_001: 28.5 us 0_010: 114 us 0_011: 228 us 0_100: 456 us 0_101: 912 us 0_110: 1824 us 0_111: 3648 us 1_000: 0us 1_001: 500us 1_010: 1000us 1_011: 2000us 1_100: 4000us 1_101: 8000us 1_110: 16000us 1_111: 32000us	MSB setting of 0/1 is only factory accessible register bit and requires factory programming.
OFFDELAY [2:0]	MSB_OFFDELAY [2:0]: 0_000: 28.5 us 0_001: 28.5 us 0_010: 114 us 0_011: 228 us 0_100: 456 us 0_101: 912 us 0_110: 1824 us 0_111: 3648 us 1_000: 0us 1_001: 500us 1_010: 1000us 1_011: 2000us 1_100: 4000us 1_101: 8000us 1_110: 16000us 1_111: 32000us	MSB setting of 0/1 is only factory accessible register bit and requires factory programming.

B6_REGE0 – BUCK6 Configuration Register

Address = 0xE0h	Default = 0x0Fh	Type = Basic Volatile

BIT	7	6	5	4	3	2	1	0
Name	POK	OV	ILIM	ILIM_WARN	UV_FLTMSK	OV_FLTMSK	ILIM_FLTMSK	IlimWarnFM
Default	0	0	0	0	1	1	1	1
Access	RO	RO	RO	RO	R/W	R/W	R/W	R/W

Name	Description	Notes
POK	POK status. 0 = BUCK6 voltage is below the power good threshold 1 =BUCK6 voltage is above the power good threshold	Provides real-time power good status
OV	OV status. 0 = BUCK6 voltage is below the overvoltage threshold 1 =BUCK6 voltage is over the overvoltage threshold	Provides real-time overvoltage status
ILIM	ILIM status. 0 = BUCK6 is below the ILIM threshold 1 = BUCK6 is above the ILIM threshold	Provides real-time current limit status
ILIM_WARN	ILIM Warning status. 0 = BUCK6 is below the ILIM warn threshold 1 = BUCK6 is above the ILIM warn threshold	Provides real-time current limit warning status
UV_FLTMSK	Mask VOUT UV interrupt and fault: 0 = Unmask VOUT UV interrupt 1 = Default mask VOUT UV interrupt	When 1, the VOUT UV fault is masked, the fault signal will not be sent to the master.
OV_FLTMSK	Mask VOUT OV interrupt and fault: 0 = Unmask VOUT OV interrupt 1 = Default mask VOUT OV interrupt	When 1, the VOUT OV fault is masked, the fault signal will not be sent to the master. B6_OV still provide real-time status.
ILIM_FLT_MSK	Mask ILIM warning interrupt and fault: 0 = Unmask ILM warning interrupt 1 = Default mask ILIM warning interrupt	When 1, the ILIM fault is masked, the fault signal will not be sent to the master. ILIM still provides real-time current limit status.
IlimWarnFM	Mask ILIM warning interrupt and fault: 0 = Unmask ILM warning interrupt 1 = Default mask ILIM warning interrupt	When 1, the ILIM_WARN fault is masked, the fault signal will not be sent to the master. ILIM_WARN still provides real-time current limit warn status.

B6_REGE1 – BUCK6 Configuration Register

Address = 0xE1h	Default = 0x00h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	ForceLpmFont	DisLpmFont	TileOnToPok	DisPullDown	EN_OutPD	EnMinpkLpm	DRV_ADJ [1:0]	
Default	0	0	0	0	0	0	00	
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	

Name	Description	Notes
ForceLpmFont	Force to work in LPM FONT (Fix ON TIME). 0 = Depend on the state in the SLEEP or NOT. It will work in LPM FONT Mode when enter SLEEP/DSLEEP. 1 = Force to work in LPM FONT	LPM FONT is ULPM mode. This bit only have effect when DisLpmFont =0.
DisLpmFont	Disable LPM FONT Mode 0 = Enable LPM FONT 1 = Disable LPM FONT	
TileOnToPok	0 = Use actual POK 1 = Use TILE ON as POK	
DisPullDown	Option to disable PullDown Resistor when BUCK is turned-off. 0 = Discharge VOUT with 5ohm when BUCK is off 1 = Don't discharge VOUT when turn-off BUCK	When = 0, the discharge resistor is connected to Vout when BUCK6 is turned off.
EN_OutPD	Enable pull down current at Vout to avoid low frequency signal (2Hz to 20kHz) 0 = Disable 1 = Enable	
EnMinpkLpm	Use MINPK for LPM mode. 0 = Disable 1 = Enable	Only set this bit to 1 when duty is higher than 75%. Need to set EN_MINPK=1
DRV_ADJ [1:0]	Adjust Gate Driver (Rising and Falling SW) 00: Slowest 11: Fastest	

B6_REGE2 – BUCK6 Configuration Register

Address = 0xE2h	Default = 0x70h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	IPD_SET [0]	VSET0[6:0]						
Default	0	1110000						
Access	R/W	R/W						

Name	Description	Notes
IPD_SET [0]	Set pull down current by IPD_SET [1:0]: 00: 12mA 01: 27mA 10: 37mA 11: 47mA	IPD_SET [1] at 0xE3 bit7. IPD_SET [0] and IPD_SET [1] are used together to set the pulldown current.
VSET0[6:0]	VOUT = 0.5V + VSET [] * 0.025V	

B6_REGE3 – BUCK6 Configuration Register

Address = 0xE3h	Default = 0x70h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	IPD_SET [1]	VSET1[6:0]						
Default	0	1110000						
Access	R/W	R/W						

Name	Description	Notes
IPD_SET [1]	Set pull down current by IPD_SET [1:0]: 00: 12mA 01: 27mA 10: 37mA 11: 47mA	IPD_SET [0] and IPD_SET [1] are used together to set the pulldown current.
VSET1[6:0]	VOUT = 0.5V + VSET [] * 0.025V	

B6_REGE4 – BUCK6 Configuration Register

Address = 0xE4h	Default = 0xA2h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	ON	PBINEN	QLITCH	SLEEPEN	AUXINEN	DPSLPEN	ILIM_SET	FORCEPWM
Default	1	0	1	0	0	0	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Name	Description	Notes
ON	0 = BUCK6 is enabled through normal sequencing routing 1 = BUCK6 I2C enable bit that bypasses normal sequencing	This functionality is dependent on the overall IC configuration. Consult the factory for details.
PBINEN	0 = Does not respond to push button mode 1 = Responds to turn on automatically with push button input.	Do not change this bit. Modifying this bit may result in unexpected IC behavior.
QLTCH	0 = BUCK6 shuts down when its sequencing trigger input shuts down 1 = BUCK6 stays on when its sequencing trigger input shuts down	
SLEEPEN	Enable BUCK6 in SLEEP mode 0 = BUCK6 stays on when the IC enters Sleep mode 1 = BUCK6 turns off when the IC enters Sleep mode	
AUXINEN	0 = BUCK6 turn on/off cannot be controlled with auxiliary input. 1 = BUCK6 turn on/off can be controlled with auxiliary input.	Control bit to use internal gb_aux line as control input for turn on/off.
DPSLPEN	Enable BUCK6 in Deep SLEEP mode 0 = BUCK6 stays on when the IC enters DP SLEEP mode 1 = BUCK6 turns off when the IC enters DP SLEEP mode	
ILIM_SET	Setting for current limit: 0 = Peak current limit set to 2.0A 1 = Peak current limit set to 3.0A	
FORCEPWM	Force Buck work in PWM mode. 0 = Not force work in PWM mode 1 = Force work in PWM mode	

B6_REGE5 – BUCK6 Configuration Register

Address = 0xE5h	Default = 0xD0h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	MODE	RST	DBQL [2:0]			DBOK [2:0]		
Default	1	1	010			000000		
Access	R/W	R/W	R/W			R/W		

Name	Description	Notes
MODE	Determines startup sequencing from the CMI code	This is a factory expert bit that should not be changed. Modifying this bit may result in unexpected IC behavior.
RST	0 = BUCK6 does not affect nRESET output 1 = BUCK6 POK affects nRESET output	RST bit determines if the regulator power okay (POK) signal is required to go high before the nRESET output from the PMIC can assert.
DBQL [2:0]	Determines startup sequencing from the CMI code	This is a factory expert bit that should not be changed. Modifying this bit may result in unexpected IC behavior.
DBOK [2:0]	Determines startup sequencing from the CMI code	This is a factory expert bit that should not be changed. Modifying this bit may result in unexpected IC behavior.

B6_REGE6 – BUCK6 Configuration Register

Address = 0xE6h	Default = 0x03h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	DBON [3:0]				SST	DISLPM	DBSTBY [1:0]	
Default	0000				0	0	11	
Access	R/W				R/W	R/W	R/W	

Name	Description	Notes
DBON [3:0]	Determines startup sequencing from the CMI code	This is a factory expert bit that should not be changed. Modifying this bit may result in unexpected IC behavior.
SST	Soft start time option 0 = 500us 1 = 250us	
DISLPM	Disable Low Power Mode. 0 = Enable LPM 1 = Disable LPM	If disable lower power mode, BUCK6 will work in DCM or CCM depend on the output load.
DBSTBY [1:0]	Determines DVS inputs from the CMI code	Do not change this bit. Modifying this bit may result in unexpected IC behavior.

B6_REGE7 – BUCK6 Configuration Register

Address = 0xE7h	Default = 0x10h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	AdjTFONT	PHASE	ONDELAY [2:0]			OFFDELAY [2:0]		
Default	0	0	010			000		
Access	R/W	R/W	R/W			R/W		

Name	Description	Notes
AdjTFONT	0 = Not adjust the Ton 1 = Increase Ton 40% in FONT mode	
PHASE	0 = Aligns converter switching to the main clock rising edge 1 = Aligns converter switching to the main clock falling edge	Main Clock has duty = 50%, PHASE=1 shifts BUCK6 switching by 180 deg
ONDELAY [2:0]	MSB_ONDELAY [2:0]: 0_000: 28.5 us 0_001: 28.5 us 0_010: 114 us 0_011: 228 us 0_100: 456 us 0_101: 912 us 0_110: 1824 us 0_111: 3648 us 1_000: 0us 1_001: 500us 1_010: 1000us 1_011: 2000us 1_100: 4000us 1_101: 8000us 1_110: 16000us 1_111: 32000us	MSB setting of 0/1 is only factory accessible register bit and requires factory programming.
OFFDELAY [2:0]	MSB_OFFDELAY [2:0]: 0_000: 28.5 us 0_001: 28.5 us 0_010: 114 us 0_011: 228 us 0_100: 456 us 0_101: 912 us 0_110: 1824 us 0_111: 3648 us 1_000: 0us 1_001: 500us 1_010: 1000us 1_011: 2000us 1_100: 4000us 1_101: 8000us 1_110: 16000us 1_111: 32000us	MSB setting of 0/1 is only factory accessible register bit and requires factory programming.

B7_REG00 – BUCK7 Configuration Register

Address = 0x00h	Default = 0x0Fh	Type = Basic Volatile

BIT	7	6	5	4	3	2	1	0
Name	POK	OV	ILIM	ILIM_WARN	UV_FLTMSK	OV_FLTMSK	ILIM_FLTMSK	IlimWarnFM
Default	0	0	0	0	1	1	1	1
Access	RO	RO	RO	RO	R/W	R/W	R/W	R/W

Name	Description	Notes
POK	POK status. 0 = BUCK7 voltage is below the power good threshold 1 =BUCK7 voltage is above the power good threshold	Provides real-time power good status
OV	OV status. 0 = BUCK7 voltage is below the overvoltage threshold 1 =BUCK7 voltage is over the overvoltage threshold	Provides real-time overvoltage status
ILIM	ILIM status. 0 = BUCK7 is below the ILIM threshold 1 = BUCK7 is above the ILIM threshold	Provides real-time current limit status
ILIM_WARN	ILIM Warning status. 0 = BUCK7 is below the ILIM warn threshold 1 = BUCK7 is above the ILIM warn threshold	Provides real-time current limit warning status
UV_FLTMSK	Mask VOUT UV interrupt and fault: 0 = Unmask VOUT UV interrupt 1 = Default mask VOUT UV interrupt	When 1, the VOUT UV fault is masked, the fault signal will not be sent to the master.
OV_FLTMSK	Mask VOUT OV interrupt and fault: 0 = Unmask VOUT OV interrupt 1 = Default mask VOUT OV interrupt	When 1, the VOUT OV fault is masked, the fault signal will not be sent to the master. B7_OV still provide real-time status.
ILIM_FLT_MSK	Mask ILIM warning interrupt and fault: 0 = Unmask ILM warning interrupt 1 = Default mask ILIM warning interrupt	When 1, the ILIM fault is masked, the fault signal will not be sent to the master. ILIM still provides real-time current limit status.
IlimWarnFM	Mask ILIM warning interrupt and fault: 0 = Unmask ILM warning interrupt 1 = Default mask ILIM warning interrupt	When 1, the ILIM_WARN fault is masked, the fault signal will not be sent to the master. ILIM_WARN still provides real-time current limit warn status.

B7_REG01 – BUCK7 Configuration Register

Address = 0x01h	Default = 0x00h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	ForceLpmFont	DisLpmFont	RFU	DisPullDown	RFU	EnMinpkLpm	DRV_ADJ [1:0]	
Default	0	0	0	0	0	0	00	
Access	R/W	R/W	RO	R/W	RO	R/W	R/W	

Name	Description	Notes
ForceLpmFont	Force to work in LPM FONT (Fix ON TIME). 0 = Depend on the state in the SLEEP or NOT. It will work in LPM FONT Mode when enter SLEEP/DSLEEP. 1 = Force to work in LPM FONT	LPM FONT is ULPM mode. This bit only have effect when DisLpmFont =0.
DisLpmFont	Disable LPM FONT Mode 0 = Enable LPM FONT 1 = Disable LPM FONT	
RFU	Reserved for Future Use	Do not change this register value. Changing the register value can affect IC functionality.
DisPullDown	Option to disable PullDown Resistor when BUCK is turned-off. 0 = Discharge VOUT with 5ohm when BUCK is off 1 = Don't discharge VOUT when turn-off BUCK	When = 0, the discharge resistor is connected to Vout when BUCK7 is turned off.
RFU	Reserved for Future Use	Do not change this register value. Changing the register value can affect IC functionality.
EnMinpkLpm	Use MINPK for LPM mode. 0 = Disable 1 = Enable	Only set this bit to 1 when duty is higher than 75%. Need to set EN_MINPK=1
DRV_ADJ [1:0]	Adjust Gate Driver (Rising and Falling SW) 00: Slowest 11: Fastest	

B7_REG02_0 – BUCK7 Configuration Register

Address = 0x02_0h	Default = 0x3Ch	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	EN_OutPD	VSET0[6:0]						
Default	0	0111100						
Access	R/W	R/W						

Name	Description	Notes
EN_OutPD	Enable pull down current at VOUT to avoid low frequency signal (2Hz to 20kHz) 0 = Disable 1 = Enable	
VSET0[6:0]	VOUT = 0.5V + VSET [] * 0.005V (Range = 0) VOUT = 0.5V + VSET [] * 0.025V (Range = 1)	

B7_REG03_0 – BUCK7 Configuration Register

Address = 0x03_0h	Default = 0x32h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	RFU	VSET1[6:0]						
Default	0	0110010						
Access	RO	R/W						

Name	Description	Notes
RFU	Reserved for Future Use	Do not change this register value. Changing the register value can affect IC functionality.
VSET1[6:0]	VOUT = 0.5V + VSET [] * 0.005V (Range = 0) VOUT = 0.5V + VSET [] * 0.025V (Range = 1)	

B7_REG02_1 – BUCK7 Configuration Register

Address = 0x02_1h	Default = 0x28h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	IPD_SET [0]	VSET2[6:0]						
Default	0	0101000						
Access	R/W	R/W						

Name	Description	Notes
IPD_SET [0]	Set pull down current by IPD_SET [1:0]: 00: 12mA 01: 27mA 10: 37mA 11: 47mA	IPD_SET [1] at 0x03_1 bit7. IPD_SET [0] and IPD_SET [1] are used together to set the pulldown current.
VSET2[6:0]	VOUT = 0.5V + VSET [] * 0.005V (Range = 0) VOUT = 0.5V + VSET [] * 0.025V (Range = 1)	

B7_REG03_1 – BUCK7 Configuration Register

Address = 0x03_1h	Default = 0x1Eh	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	IPD_SET [1]	VSET3[6:0]						
Default	0	0011110						
Access	R/W	R/W						

Name	Description	Notes
IPD_SET [1]	Set pull down current by IPD_SET [1:0]: 00: 12mA 01: 27mA 10: 37mA 11: 47mA	IPD_SET [0] and IPD_SET [1] are used together to set the pulldown current.
VSET3[6:0]	VOUT = 0.5V + VSET [] * 0.005V (Range = 0) VOUT = 0.5V + VSET [] * 0.025V (Range = 1)	

B7_REG44 – BUCK7 Configuration Register

Address = 0x04h	Default = 0xA2h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	ON	PBINEN	QLITCH	SLEEPEN	AUXINEN	DPSLPEN	ILIM_SET	FORCEPWM
Default	1	0	1	0	0	0	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Name	Description	Notes
ON	0 = BUCK7 is enabled through normal sequencing routing 1 = BUCK7 I2C enable bit that bypasses normal sequencing	This functionality is dependent on the overall IC configuration. Consult the factory for details.
PBINEN	0 = Does not respond to push button mode 1 = Responds to turn on automatically with push button input.	Do not change this bit. Modifying this bit may result in unexpected IC behavior.
QLTCH	0 = BUCK7 shuts down when its sequencing trigger input shuts down 1 = BUCK7 stays on when its sequencing trigger input shuts down	
SLEEPEN	Enable BUCK7 in SLEEP mode 0 = BUCK7 stays on when the IC enters Sleep mode 1 = BUCK7 turns off when the IC enters Sleep mode	
AUXINEN	0 = BUCK7 turn on/off cannot be controlled with auxiliary input. 1 = BUCK7 turn on/off can be controlled with auxiliary input.	Control bit to use internal gb_aux line as control input for turn on/off.
DPSLPEN	Enable BUCK7 in Deep SLEEP mode 0 = BUCK7 stays on when the IC enters DP SLEEP mode 1 = BUCK7 turns off when the IC enters DP SLEEP mode	
ILIM_SET	Setting for current limit: 0 = Peak current limit set to 3.80A 1 = Peak current limit set to 5.00A	
FORCEPWM	Force Buck work in PWM mode. 0 = Not force work in PWM mode 1 = Force work in PWM mode	

B7_REG05 – BUCK7 Configuration Register

Address = 0x05h	Default = 0xD0h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	MODE	RST	DBQL [2:0]			DBOK [2:0]		
Default	1	1	010			000		
Access	R/W	R/W	R/W			R/W		

Name	Description	Notes
MODE	Determines startup sequencing from the CMI code	This is a factory expert bit that should not be changed. Modifying this bit may result in unexpected IC behavior.
RST	0 = BUCK7 does not affect nRESET output 1 = BUCK7 POK affects nRESET output	RST bit determines if the regulator power okay (POK) signal is required to go high before the nRESET output from the PMIC can assert.
DBQL [2:0]	Determines startup sequencing from the CMI code	This is a factory expert bit that should not be changed. Modifying this bit may result in unexpected IC behavior.
DBOK [2:0]	Determines startup sequencing from the CMI code	This is a factory expert bit that should not be changed. Modifying this bit may result in unexpected IC behavior.

B7_REG06 – BUCK7 Configuration Register

Address = 0x06h	Default = 0x00h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	DBON [3:0]				SST	DISLPM	Vout_Range	RFU
Default	0000				0	1	00	0
Access	R/W				R/W	R/W	R/W	R/W

Name	Description	Notes
DBON [3:0]	Determines startup sequencing from the CMI code	Do not change this bit. Modifying this bit may result in unexpected IC behavior.
SST	Soft start time option 0 = 500us 1 = 250us	
DISLPM	Disable Low Power Mode. 0 = Enable LPM 1 = Disable LPM	If disable lower power mode, BUCK7 will work in DCM or CCM depend on the output load.
Vout_Range	Select Vout Range: 0: Vout = 0.5V ~1.135V 1: Vout = 0.5V ~ 3.675V	
RFU	Reserved for Future Use	Do not change this register value. Changing the register value can affect IC functionality.

B7_REG07 – BUCK7 Configuration Register

Address = 0x07h	Default = 0x10h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	RFU	PHASE	ONDELAY [2:0]			OFFDELAY [2:0]		
Default	0	0	010			000		
Access	RO	R/W	R/W			R/W		

Name	Description	Notes
RFU	Reserved for Future Use	Do not change this register value. Changing the register value can affect IC functionality.
PHASE	0 = Aligns converter switching to the main clock rising edge 1 = Aligns converter switching to the main clock falling edge	Main Clock has duty = 50%, PHASE=1 shifts BUCK7 switching by 180 deg
ONDELAY [2:0]	MSB_ONDELAY [2:0]: 0_000: 28.5 us 0_001: 28.5 us 0_010: 114 us 0_011: 228 us 0_100: 456 us 0_101: 912 us 0_110: 1824 us 0_111: 3648 us 1_000: 0us 1_001: 500us 1_010: 1000us 1_011: 2000us 1_100: 4000us 1_101: 8000us 1_110: 16000us 1_111: 32000us	MSB setting of 0/1 is only factory accessible register bit and requires factory programming.
OFFDELAY [2:0]	MSB_OFFDELAY [2:0]: 0_000: 28.5 us 0_001: 28.5 us 0_010: 114 us 0_011: 228 us 0_100: 456 us 0_101: 912 us 0_110: 1824 us 0_111: 3648 us 1_000: 0us 1_001: 500us 1_010: 1000us 1_011: 2000us 1_100: 4000us 1_101: 8000us 1_110: 16000us 1_111: 32000us	MSB setting of 0/1 is only factory accessible register bit and requires factory programming.

LDO12_REG20 – LDO12 Configuration Register

Address = 0x20h	Default = 0x0Eh	Type = Basic Volatile

BIT	7	6	5	4	3	2	1	0
Name	PwrGood_L1	OV_L1	ILIM_L1	RFU	UV_FltMsk_L1	OV_FltMsk_L1	IlimFltMsk_L1	RFU
Default	0	0	0	0	1	1	1	0
Access	RO	RO	RO	RO	R/W	R/W	R/W	RO

Name	Description	Notes
PwrGood_L1	0 = LDO1 voltage is below the power good threshold 1 = LDO1 voltage is above the power good threshold	Provides real-time power good status
OV_L1	0 = LDO1 voltage is below the overvoltage threshold 1 = LDO1 voltage is above the overvoltage threshold	Provides real-time overvoltage status
ILIM_L1	0 = LDO1 is below the ILIM threshold 1 = LDO1 is above the ILIM threshold	Provides real-time current limit status
RFU	Reserved for future use	Do not change this register value. Changing the register value can affect IC functionality.
UV_FltMsk_L1	0 = Unmasks the LDO1 UV fault 1 = Masks the LDO1 UV fault	When 1, the LDO UV fault is masked, the fault signal will not be sent to the master.
OV_FltMsk_L1	0 = Unmasks the LDO1 OV fault 1 = Masks the LDO1 OV fault	When 1, the LDO1 OV fault is masked, the fault signal will not be sent to the master. OV_L1 still provides real-time OV status.
IlimFltMsk_L1	0 = Unmasks the LDO1 ILIM fault 1 = Masks the LDO1 ILIM fault	When 1, the LDO1 ILIM fault is masked, the fault signal will not be sent to the master. ILIM_L1 still provides real-time overcurrent status.
RFU	Reserved for Future Use	Do not change this register value. Changing the register value can affect IC functionality.

LDO12_REG21 – LDO12 Configuration Register

Address = 0x21h	Default = 0x70h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	RFU	RANGE_L1	VSET_L1 [5:0]					
Default	0	1	110000					
Access	RO	R/W	R/W					

Name	Description	Notes
RFU	Reserved for Future Use	Do not change this register value. Changing the register value can affect IC functionality.
RANGE_L1	0 = Vout from 0.5 to 1.2875 1 = Vout from 1.2 to 1.9875	RANGE LDO1
VSET_L1 [5:0]	LDO1 output voltage setting. VOUT = 0.5V + VSET_L1 [5:0] * 0.0125V (RANGE = 0) VOUT = 1.2V + VSET_L1 [5:0] * 0.0125V (RANGE = 1)	

LDO12_REG22 – LDO12 Configuration Register

Address = 0x22h	Default = 0x9Ah	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	ON_L1	PBINEN_L1	AUXINEN_L1	SLEEPEN_L1	DPSLPEN_L1	DBQL_L1 [2:0]		
Default	1	0	0	1	1	010		
Access	R/W	R/W	R/W	R/W	R/W	R/W		

Name	Description	Notes
ON_L1	0 = LDO1 is enabled through normal sequencing routing 1 = LDO1 I2C enable bit that bypasses normal sequencing	This functionality is dependent on the overall IC configuration. Consult the factory for details.
PBINEN_L1	0 = Does not respond to push button mode 1 = Responds to turn on automatically with push button input.	
AUXINEN_L1	0 = Cannot be turned on/off using Auxiliary Input 1 = Can be turned on/off using Auxiliary Input	Allows the output to be turned on and off by a GPIO input.
SLEEPEN_L1	0 = LDO1 stays on when the IC enters Sleep mode 1 = LDO1 turns off when the IC enters Sleep mode	
DPSLPEN_L1	0 – LDO1 stays on when the IC enters DEEP SLEEP mode 1 – LDO1 turns off when the IC enters DEEP SLEEP mode	
DBQL_L1 [2:0]	Determines startup sequencing from the CMI code	This is a factory expert bit that should not be changed. Modifying this bit may result in unexpected IC behavior.

LDO12_REG23 – LDO12 Configuration Register

Address = 0x23h	Default = 0x6Eh	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	OnDelay_L1 [2:0]			OffDelay_L1 [2:0]			MODE_L1	RST_L1
Default	011			011			1	0
Access	R/W			R/W			R/W	R/W

Name	Description	Notes
OnDelay_L1 [2:0]	MSB_ONDELAY [2:0]: 0_000: 28.5 us 0_001: 28.5 us 0_010: 114 us 0_011: 228 us 0_100: 456 us 0_101: 912 us 0_110: 1824 us 0_111: 3648 us 1_000: 0us 1_001: 500us 1_010: 1000us 1_011: 2000us 1_100: 4000us 1_101: 8000us 1_110: 16000us 1_111: 32000us	MSB setting of 0/1 is only factory accessible register bit and requires factory programming.
OffDelay_L1 [2:0]	MSB_OFFDELAY [2:0]: 0_000: 28.5 us 0_001: 28.5 us 0_010: 114 us 0_011: 228 us 0_100: 456 us 0_101: 912 us 0_110: 1824 us 0_111: 3648 us 1_000: 0us 1_001: 500us 1_010: 1000us 1_011: 2000us 1_100: 4000us 1_101: 8000us 1_110: 16000us 1_111: 32000us	MSB setting of 0/1 is only factory accessible register bit and requires factory programming.
MODE_L1	Determines startup sequencing from the CMI code	This is a factory expert bit that should not be changed. Modifying this bit may result in unexpected IC behavior.
RST_L1	0 = LDO1 does not affect nRESET output 1 = LDO1 POK affects nRESET output	RST bit determines if the regulator power okay (POK) signal is required to go high before the nRESET output from the PMIC can assert.

LDO12_REG24 – LDO12 Configuration Register

Address = 0x24h	Default = 0x01h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	DBON_L1 [3:0]				DBOK_L1 [3:0]			
Default	0000				0001			
Access	R/W				R/W			

Name	Description	Notes
DBON_L1 [3:0]	Determines startup sequencing from the CMI code	This is a factory expert bit that should not be changed. Modifying this bit may result in unexpected IC behavior.
DBOK_L1 [3:0]	Determines startup sequencing from the CMI code	This is a factory expert bit that should not be changed. Modifying this bit may result in unexpected IC behavior.

LDO12_REG25 – LDO12 Configuration Register

Address = 0x25h	Default = 0x83h	Type = Basic Volatile

BIT	7	6	5	4	3	2	1	0
Name	LimSD_Dis_L1	RFU	RFU	DisChrgOptL1	DisPulldownL2	DisPulldownL1	SST_L1	QLTCH_L1
Default	1	0	0	0	0	0	1	1
Access	R/W	RO	RO	R/W	R/W	R/W	R/W	R/W

Name	Description	Notes
LimSD_Dis_L1	0 = Enable the shutdown by current limit of LDO1. 1 = Disable the shutdown by current limit of LDO1.	
RFU	Reserved for Future Use	Do not change this register value. Changing the register value can affect IC functionality.
DisChrgOptL1	Discharge resistor option when LDO is turned-off. 0 = Discharge VOUT when turn-off, Rdis=9.4 Ohm 1 = Discharge VOUT when turn-off. Rdis=18.8 Ohm	
DisPulldownL2	Option to disable Pulldown Resistor when LDO2 is turned-off. 0 = Enable pulldown function 1 = Disable pulldown function	
DisPulldownL1	Option to disable Pulldown Resistor when LDO1 is turned-off. 0 = Enable pulldown function 1 = Disable pulldown function	
SST_L1	Soft start time of LDO1: 0: 250us 1: 500us.	
QLTCH_L1	0 = LDO1 shuts down when its sequencing trigger input shuts down 1 = LDO1 stays on when its sequencing trigger input shuts down	

LDO12_REG26 – LDO12 Configuration Register

Address = 0x26h	Default = 0x0Eh	Type = Basic Volatile

BIT	7	6	5	4	3	2	1	0
Name	PwrGood_L2	OV_L2	ILIM_L2	RFU	UV_FltMsk_L2	OV_FltMsk_L2	IlimFltMsk_L2	RFU
Default	0	0	0	0	1	1	1	0
Access	RO	RO	RO	RO	R/W	R/W	R/W	RO

Name	Description	Notes
PwrGood_L2	0 = LDO2 voltage is below the power good threshold 1 = LDO2 voltage is above the power good threshold	Provides real-time power good status
OV_L2	0 = LDO2 voltage is below the overvoltage threshold 1 = LDO2 voltage is above the overvoltage threshold	Provides real-time overvoltage status
ILIM_L2	0 = LDO2 is below the ILIM threshold 1 = LDO2 is above the ILIM threshold	Provides real-time current limit status
RFU	Reserved for future use	Do not change this register value. Changing the register value can affect IC functionality.
UV_FltMsk_L2	0 = Unmasks the LDO2 UV fault 1 = Masks the LDO2 UV fault	When 1, the LDO UV fault is masked, the fault signal will not be sent to the master.
OV_FltMsk_L2	0 = Unmasks the LDO2 OV fault 1 = Masks the LDO2 OV fault	When 1, the LDO2 OV fault is masked, the fault signal will not be sent to the master. OV_L2 still provides real-time OV status.
IlimFltMsk_L2	0 = Unmasks the LDO2 ILIM fault 1 = Masks the LDO2 ILIM fault	When 1, the LDO2 ILIM fault is masked, the fault signal will not be sent to the master. ILIM_L2 still provides real-time overcurrent status.
RFU	Reserved for Future Use	Do not change this register value. Changing the register value can affect IC functionality.

LDO12_REG27 – LDO12 Configuration Register

Address = 0x27h	Default = 0x40h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	RFU	RANGE_L2	VSET_L2 [5:0]					
Default	0	1	00000					
Access	RO	R/W	R/W					

Name	Description	Notes
RFU	Reserved for Future Use	Do not change this register value. Changing the register value can affect IC functionality.
RANGE_L2	0 = Vout from 0.5 to 1.2875 1 = Vout from 1.2 to 1.9875	RANGE LDO2
VSET_L2 [5:0]	LDO2 output voltage setting. VOUT = 0.5V + VSET_L2 [5:0] * 0.0125V (RANGE = 0) VOUT = 1.2V + VSET_L2 [5:0] * 0.0125V (RANGE = 1)	

LDO12_REG28 – LDO12 Configuration Register

Address = 0x28h	Default = 0x9Ah	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	ON_L2	PBINEN_L2	AUXINEN_L2	SLEEPEN_L2	DPSLPEN_L2	DBQL_L2 [2:0]		
Default	1	0	0	1	1	010		
Access	R/W	R/W	R/W	R/W	R/W	R/W		

Name	Description	Notes
ON_L2	0 = LDO2 is enabled through normal sequencing routing 1 =LDO2 I2C enable bit that bypasses normal sequencing	This functionality is dependent on the overall IC configuration. Consult the factory for details.
PBINEN_L2	0 = Does not respond to push button mode 1 = Responds to turn on automatically with push button input.	
AUXINEN_L2	0 = Cannot be turned on/off using Auxiliary Input 1 = Can be turned on/off using Auxiliary Input	Allows the output to be turned on and off by a GPIO input.
SLEEPEN_L2	0 = LDO2 stays on when the IC enters Sleep mode 1 = LDO2 turns off when the IC enters Sleep mode	
DPSLPEN_L2	0 – LDO2 stays on when the IC enters DEEP SLEEP mode 1 – LDO2 turns off when the IC enters DEEP SLEEP mode	
DBQL_L2 [2:0]	Determines startup sequencing from the CMI code	This is a factory expert bit that should not be changed. Modifying this bit may result in unexpected IC behavior.

LDO12_REG29 – LDO12 Configuration Register

Address = 0x29h	Default = 0x6Eh	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	OnDelay_L2 [2:0]			OffDelay_L2 [2:0]			MODE_L2	RST_L2
Default	011			011			1	0
Access	R/W			R/W			R/W	R/W

Name	Description	Notes
OnDelay_L2 [2:0]	MSB_ONDELAY [2:0]: 0_000: 28.5 us 0_001: 28.5 us 0_010: 114 us 0_011: 228 us 0_100: 456 us 0_101: 912 us 0_110: 1824 us 0_111: 3648 us 1_000: 0us 1_001: 500us 1_010: 1000us 1_011: 2000us 1_100: 4000us 1_101: 8000us 1_110: 16000us 1_111: 32000us	MSB setting of 0/1 is only factory accessible register bit and requires factory programming.
OffDelay_L2 [2:0]	MSB_OFFDELAY [2:0]: 0_000: 28.5 us 0_001: 28.5 us 0_010: 114 us 0_011: 228 us 0_100: 456 us 0_101: 912 us 0_110: 1824 us 0_111: 3648 us 1_000: 0us 1_001: 500us 1_010: 1000us 1_011: 2000us 1_100: 4000us 1_101: 8000us 1_110: 16000us 1_111: 32000us	MSB setting of 0/1 is only factory accessible register bit and requires factory programming.
MODE_L2	Determines startup sequencing from the CMI code	This is a factory expert bit that should not be changed. Modifying this bit may result in unexpected IC behavior.
RST_L2	0 = LDO2 does not affect nRESET output 1 = LDO2 POK affects nRESET output	RST bit determines if the regulator power okay (POK) signal is required to go high before the nRESET output from the PMIC can assert.

LDO12_REG2A – LDO12 Configuration Register

Address = 0x2Ah	Default = 0x00h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	DBON_L2 [3:0]				DBOK_L2 [3:0]			
Default	0000				0000			
Access	R/W				R/W			

Name	Description	Notes
DBON_L2 [3:0]	Determines startup sequencing from the CMI code	This is a factory expert bit that should not be changed. Modifying this bit may result in unexpected IC behavior.
DBOK_L2 [3:0]	Determines startup sequencing from the CMI code	This is a factory expert bit that should not be changed. Modifying this bit may result in unexpected IC behavior.

LDO35_REG40 – LDO35 Configuration Register

Address = 0x40h	Default = 0x0Eh	Type = Basic Volatile

BIT	7	6	5	4	3	2	1	0
Name	PwrGood_L5	OV_L5	ILIM_L5	RFU	UV_FltMsk_L5	OV_FltMsk_L5	IlimFltMsk_L5	RFU
Default	0	0	0	0	1	1	1	0
Access	RO	RO	RO	RO	R/W	R/W	R/W	RO

Name	Description	Notes
PwrGood_L5	0 = LDO5 voltage is below the power good threshold 1 = LDO5 voltage is above the power good threshold	Provides real-time power good status
OV_L5	0 = LDO5 voltage is below the overvoltage threshold 1 = LDO5 voltage is above the overvoltage threshold	Provides real-time overvoltage status
ILIM_L5	0 = LDO5 is below the ILIM threshold 1 = LDO5 is above the ILIM threshold	Provides real-time current limit status
RFU	Reserved for future use	Do not change this register value. Changing the register value can affect IC functionality.
UV_FltMsk_L5	0 = Unmasks the LDO5 UV fault 1 = Masks the LDO5 UV fault	When 1, the LDO UV fault is masked, the fault signal will not be sent to the master.
OV_FltMsk_L5	0 = Unmasks the LDO5 OV fault 1 = Masks the LDO5 OV fault	When 1, the LDO5 OV fault is masked, the fault signal will not be sent to the master. OV_L5 still provides real-time OV status.
IlimFltMsk_L5	0 = Unmasks the LDO5 ILIM fault 1 = Masks the LDO5 ILIM fault	When 1, the LDO5 ILIM fault is masked, the fault signal will not be sent to the master. ILIM_L5 still provides real-time overcurrent status.
RFU	Reserved for Future Use	Do not change this register value. Changing the register value can affect IC functionality.

LDO35_REG41 – LDO35 Configuration Register

Address = 0x41h	Default = 0xBFh	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	RANGE_L5	RFU	VSET_L5 [5:0]					
Default	1	0	111111					
Access	R/W	RO	R/W					

Name	Description	Notes
RANGE_L5	0 = Vout from 0.5 to 1.2875 1 = Vout from 1 to 4.15	RANGE LDO5
RFU	Reserved for Future Use	Do not change this register value. Changing the register value can affect IC functionality.
VSET_L5 [5:0]	LDO5 output voltage setting. VOUT = 0.5V + VSET_L5 [5:0] * 0.0125V (RANGE = 0) VOUT = 1V + VSET_L5 [5:0] * 0.05V (RANGE = 1)	

LDO35_REG42 – LDO35 Configuration Register

Address = 0x42h	Default = 0x1Eh	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	ON_L5	PBINEN_L5	AUXINEN_L5	SLEEPEN_L5	DPSLPEN_L5	DBQL_L5 [2:0]		
Default	0	0	0	1	1	110		
Access	R/W	R/W	R/W	R/W	R/W	R/W		

Name	Description	Notes
ON_L5	0 = LDO5 is enabled through normal sequencing routing 1 = LDO5 I2C enable bit that bypasses normal sequencing	This functionality is dependent on the overall IC configuration. Consult the factory for details.
PBINEN_L5	0 = Does not respond to push button mode 1 = Responds to turn on automatically with push button input.	
AUXINEN_L5	0 = Cannot be turned on/off using Auxiliary Input 1 = Can be turned on/off using Auxiliary Input	Allows the output to be turned on and off by a GPIO input.
SLEEPEN_L5	0 = LDO5 stays on when the IC enters Sleep mode 1 = LDO5 turns off when the IC enters Sleep mode	
DPSLPEN_L5	0 – LDO5 stays on when the IC enters DEEP SLEEP mode 1 – LDO5 turns off when the IC enters DEEP SLEEP mode	
DBQL_L5 [2:0]	Determines startup sequencing from the CMI code	This is a factory expert bit that should not be changed. Modifying this bit may result in unexpected IC behavior.

LDO35_REG43 – LDO35 Configuration Register

Address = 0x43h	Default = 0x12h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	OnDelay_L5 [2:0]			OffDelay_L5 [2:0]			MODE_L5	RST_L5
Default	000			100			1	0
Access	R/W			R/W			R/W	R/W

Name	Description	Notes
OnDelay_L5 [2:0]	MSB_ONDELAY [2:0]: 0_000: 28.5 us 0_001: 28.5 us 0_010: 114 us 0_011: 228 us 0_100: 456 us 0_101: 912 us 0_110: 1824 us 0_111: 3648 us 1_000: 0us 1_001: 500us 1_010: 1000us 1_011: 2000us 1_100: 4000us 1_101: 8000us 1_110: 16000us 1_111: 32000us	MSB setting of 0/1 is only factory accessible register bit and requires factory programming.
OffDelay_L5 [2:0]	MSB_OFFDELAY [2:0]: 0_000: 28.5 us 0_001: 28.5 us 0_010: 114 us 0_011: 228 us 0_100: 456 us 0_101: 912 us 0_110: 1824 us 0_111: 3648 us 1_000: 0us 1_001: 500us 1_010: 1000us 1_011: 2000us 1_100: 4000us 1_101: 8000us 1_110: 16000us 1_111: 32000us	MSB setting of 0/1 is only factory accessible register bit and requires factory programming.
MODE_L5	Determines startup sequencing from the CMI code	This is a factory expert bit that should not be changed. Modifying this bit may result in unexpected IC behavior.
RST_L5	0 = LDO5 does not affect nRESET output 1 = LDO5 POK affects nRESET output	RST bit determines if the regulator power okay (POK) signal is required to go high before the nRESET output from the PMIC can assert.

LDO35_REG44 – LDO35 Configuration Register

Address = 0x44h	Default = 0x60h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	DBON_L5 [3:0]				DBOK_L5 [3:0]			
Default	0110				0000			
Access	R/W				R/W			

Name	Description	Notes
DBON_L5 [3:0]	Determines startup sequencing from the CMI code	This is a factory expert bit that should not be changed. Modifying this bit may result in unexpected IC behavior.
DBOK_L5 [3:0]	Determines startup sequencing from the CMI code	This is a factory expert bit that should not be changed. Modifying this bit may result in unexpected IC behavior.

LDO35_REG45 – LDO35 Configuration Register

Address = 0x45h	Default = 0x8Fh	Type = Basic Volatile

BIT	7	6	5	4	3	2	1	0
Name	LimSD_Dis_L5	PullUpGPIO4	PullUpGPIO3	Dis_PD_L5	PullUpGPIO1	ILIM_SCL_L5	SST_L5	QLTCH_L5
Default	1	0	0	0	1	1	1	1
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Name	Description	Notes
LimSD_Dis_L5	0 = Enable the shutdown by current limit of LDO5. 1 = Disable the shutdown by current limit of LDO5.	
PullUpGPIO4	Internal Pull up selection. 0 = no internal pull up 1 = internal pull up the GPIO to VIO with 86kOhm	
PullUpGPIO3	Internal Pull up selection. 0 = no internal pull up 1 = internal pull up the GPIO to VIO with 86kOhm	
Dis_PD_L5	Option to disable Pulldown Resistor when LDO is turned-off. 0 = Discharge VOUT when turn-off. 1 = Don't discharge VOUT when turn-off.	
PullUpGPIO1	Internal Pull up selection. 0 = no internal pull up 1 = internal pull up the GPIO to VIO with 86kOhm	
ILIM_SCL_L5	Current limit setting for LDO/PLSW mode: 0: 350mA 1: 450mA	
SST_L5	Soft start time of LDO5: 0: 250us 1: 500us.	
QLTCH_L5	0 = LDO5 shuts down when its sequencing trigger input shuts down 1 = LDO5 stays on when its sequencing trigger input shuts down	

LDO35_REG46 – LDO35 Configuration Register

Address = 0x46h	Default = 0x0Eh	Type = Basic Volatile

BIT	7	6	5	4	3	2	1	0
Name	PwrGood_L3	OV_L3	ILIM_L3	RFU	UV_FltMsk_L3	OV_FltMsk_L3	IlimFltMsk_L3	RFU
Default	0	0	0	0	1	1	1	0
Access	RO	RO	RO	RO	R/W	R/W	R/W	RO

Name	Description	Notes
PwrGood_L3	0 = LDO3 voltage is below the power good threshold 1 = LDO3 voltage is above the power good threshold	Provides real-time power good status
OV_L3	0 = LDO3 voltage is below the overvoltage threshold 1 = LDO3 voltage is above the overvoltage threshold	Provides real-time overvoltage status
ILIM_L3	0 = LDO3 is below the ILIM threshold 1 = LDO3 is above the ILIM threshold	Provides real-time current limit status
RFU	Reserved for future use	Do not change this register value. Changing the register value can affect IC functionality.
UV_FltMsk_L3	0 = Unmasks the LDO3 UV fault 1 = Masks the LDO3 UV fault	When 1, the LDO UV fault is masked, the fault signal will not be sent to the master.
OV_FltMsk_L3	0 = Unmasks the LDO3 OV fault 1 = Masks the LDO3 OV fault	When 1, the LDO3 OV fault is masked, the fault signal will not be sent to the master. OV_L3 still provides real-time OV status.
IlimFltMsk_L3	0 = Unmasks the LDO3 ILIM fault 1 = Masks the LDO3 ILIM fault	When 1, the LDO3 ILIM fault is masked, the fault signal will not be sent to the master. ILIM_L3 still provides real-time overcurrent status.
RFU	Reserved for Future Use	Do not change this register value. Changing the register value can affect IC functionality.

LDO35_REG47 – LDO35 Configuration Register

Address = 0x47h	Default = 0xAEh	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	RANGE_L3	RFU	VSET_L3 [5:0]					
Default	1	0	101110					
Access	R/W	RO	R/W					

Name	Description	Notes
RANGE_L3	0 = Vout from 0.5 to 1.2875 1 = Vout from 1 to 4.15	RANGE LDO3
RFU	Reserved for Future Use	Do not change this register value. Changing the register value can affect IC functionality.
VSET_L3 [5:0]	LDO3 output voltage setting. VOUT = 0.5V + VSET_L3 [5:0] * 0.0125V (RANGE = 0) VOUT = 1V + VSET_L3 [5:0] * 0.05V (RANGE = 1)	

LDO35_REG48 – LDO35 Configuration Register

Address = 0x48h	Default = 0x80h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	ON_L3	PBINEN_L3	AUXINEN_L3	SLEEPEN_L3	DPSLPEN_L3	DBQL_L3 [2:0]		
Default	1	0	0	0	0	000		
Access	R/W	R/W	R/W	R/W	R/W	R/W		

Name	Description	Notes
ON_L3	0 = LDO3 is enabled through normal sequencing routing 1 = LDO3 I2C enable bit that bypasses normal sequencing	This functionality is dependent on the overall IC configuration. Consult the factory for details.
PBINEN_L3	0 = Does not respond to push button mode 1 = Responds to turn on automatically with push button input.	
AUXINEN_L3	0 = Cannot be turned on/off using Auxiliary Input 1 = Can be turned on/off using Auxiliary Input	Allows the output to be turned on and off by a GPIO input.
SLEEPEN_L3	0 = LDO3 stays on when the IC enters Sleep mode 1 = LDO3 turns off when the IC enters Sleep mode	
DPSLPEN_L3	0 – LDO3 stays on when the IC enters DEEP SLEEP mode 1 – LDO3 turns off when the IC enters DEEP SLEEP mode	
DBQL_L3 [2:0]	Determines startup sequencing from the CMI code	This is a factory expert bit that should not be changed. Modifying this bit may result in unexpected IC behavior.

LDO35_REG49 – LDO35 Configuration Register

Address = 0x49h	Default = 0x23h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	OnDelay_L3 [2:0]			OffDelay_L3 [2:0]			MODE_L3	RST_L3
Default	001			000			1	1
Access	R/W			R/W			R/W	R/W

Name	Description	Notes
OnDelay_L3 [2:0]	MSB_ONDELAY [2:0]: 0_000: 28.5 us 0_001: 28.5 us 0_010: 114 us 0_011: 228 us 0_100: 456 us 0_101: 912 us 0_110: 1824 us 0_111: 3648 us 1_000: 0us 1_001: 500us 1_010: 1000us 1_011: 2000us 1_100: 4000us 1_101: 8000us 1_110: 16000us 1_111: 32000us	MSB setting of 0/1 is only factory accessible register bit and requires factory programming.
OffDelay_L3 [2:0]	MSB_OFFDELAY [2:0]: 0_000: 28.5 us 0_001: 28.5 us 0_010: 114 us 0_011: 228 us 0_100: 456 us 0_101: 912 us 0_110: 1824 us 0_111: 3648 us 1_000: 0us 1_001: 500us 1_010: 1000us 1_011: 2000us 1_100: 4000us 1_101: 8000us 1_110: 16000us 1_111: 32000us	MSB setting of 0/1 is only factory accessible register bit and requires factory programming.
MODE_L3	Determines startup sequencing from the CMI code	This is a factory expert bit that should not be changed. Modifying this bit may result in unexpected IC behavior.
RST_L3	0 = LDO3 does not affect nRESET output 1 = LDO3 POK affects nRESET output	RST bit determines if the regulator power okay (POK) signal is required to go high before the nRESET output from the PMIC can assert.

LDO35_REG4A – LDO35 Configuration Register

Address = 0x4Ah	Default = 0x00h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	DBON_L3 [3:0]				DBOK_L3 [3:0]			
Default	0000				0000			
Access	R/W				R/W			

Name	Description	Notes
DBON_L3 [3:0]	Determines startup sequencing from the CMI code	This is a factory expert bit that should not be changed. Modifying this bit may result in unexpected IC behavior.
DBOK_L3 [3:0]	Determines startup sequencing from the CMI code	This is a factory expert bit that should not be changed. Modifying this bit may result in unexpected IC behavior.

LDO46_REG60 – LDO46 Configuration Register

Address = 0x60h	Default = 0x0Eh	Type = Basic Volatile

BIT	7	6	5	4	3	2	1	0
Name	PwrGood_L6	OV_L6	ILIM_L6	RFU	UV_FltMsk_L6	OV_FltMsk_L6	IlimFltMsk_L6	RFU
Default	0	0	0	0	1	1	1	0
Access	RO	RO	RO	RO	R/W	R/W	R/W	RO

Name	Description	Notes
PwrGood_L6	0 = LDO6 voltage is below the power good threshold 1 = LDO6 voltage is above the power good threshold	Provides real-time power good status
OV_L6	0 = LDO6 voltage is below the overvoltage threshold 1 = LDO6 voltage is above the overvoltage threshold	Provides real-time overvoltage status
ILIM_L6	0 = LDO6 is below the ILIM threshold 1 = LDO6 is above the ILIM threshold	Provides real-time current limit status
RFU	Reserved for future use	Do not change this register value. Changing the register value can affect IC functionality.
UV_FltMsk_L6	0 = Unmasks the LDO6 UV fault 1 = Masks the LDO6 UV fault	When 1, the LDO UV fault is masked, the fault signal will not be sent to the master.
OV_FltMsk_L6	0 = Unmasks the LDO6 OV fault 1 = Masks the LDO6 OV fault	When 1, the LDO6 OV fault is masked, the fault signal will not be sent to the master. OV_L6 still provides real-time OV status.
IlimFltMsk_L6	0 = Unmasks the LDO6 ILIM fault 1 = Masks the LDO6 ILIM fault	When 1, the LDO6 ILIM fault is masked, the fault signal will not be sent to the master. ILIM_L6 still provides real-time overcurrent status.
RFU	Reserved for Future Use	Do not change this register value. Changing the register value can affect IC functionality.

LDO46_REG61 – LDO46 Configuration Register

Address = 0x61h	Default = 0xBFh	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	RANGE_L6	RFU	VSET_L6 [5:0]					
Default	1	0	111111					
Access	R/W	RO	R/W					

Name	Description	Notes
RANGE_L6	0 = Vout from 0.5 to 1.2875 1 = Vout from 1 to 4.15	RANGE LDO6
RFU	Reserved for Future Use	Do not change this register value. Changing the register value can affect IC functionality.
VSET_L6 [5:0]	LDO6 output voltage setting. VOUT = 0.5V + VSET_L6 [5:0] * 0.0125V (RANGE = 0) VOUT = 1V + VSET_L6 [5:0] * 0.05V (RANGE = 1)	

LDO46_REG62 – LDO46 Configuration Register

Address = 0x62h	Default = 0x1Eh	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	ON_L6	PBINEN_L6	AUXINEN_L6	SLEEPEN_L6	DPSLPEN_L6	DBQL_L6 [2:0]		
Default	0	0	0	1	1	110		
Access	R/W	R/W	R/W	R/W	R/W	R/W		

Name	Description	Notes
ON_L6	0 = LDO6 is enabled through normal sequencing routing 1 = LDO6 I2C enable bit that bypasses normal sequencing	This functionality is dependent on the overall IC configuration. Consult the factory for details.
PBINEN_L6	0 = Does not respond to push button mode 1 = Responds to turn on automatically with push button input.	
AUXINEN_L6	0 = Cannot be turned on/off using Auxiliary Input 1 = Can be turned on/off using Auxiliary Input	Allows the output to be turned on and off by a GPIO input.
SLEEPEN_L6	0 = LDO6 stays on when the IC enters Sleep mode 1 = LDO6 turns off when the IC enters Sleep mode	
DPSLPEN_L6	0 – LDO6 stays on when the IC enters DEEP SLEEP mode 1 – LDO6 turns off when the IC enters DEEP SLEEP mode	
DBQL_L6 [2:0]	Determines startup sequencing from the CMI code	This is a factory expert bit that should not be changed. Modifying this bit may result in unexpected IC behavior.

LDO46_REG63 – LDO46 Configuration Register

Address = 0x63h	Default = 0x52h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	OnDelay_L6 [2:0]			OffDelay_L6 [2:0]			MODE_L6	RST_L6
Default	010			100			1	0
Access	R/W			R/W			R/W	R/W

Name	Description	Notes
OnDelay_L6 [2:0]	MSB_ONDELAY [2:0]: 0_000: 28.5 us 0_001: 28.5 us 0_010: 114 us 0_011: 228 us 0_100: 456 us 0_101: 912 us 0_110: 1824 us 0_111: 3648 us 1_000: 0us 1_001: 500us 1_010: 1000us 1_011: 2000us 1_100: 4000us 1_101: 8000us 1_110: 16000us 1_111: 32000us	MSB setting of 0/1 is only factory accessible register bit and requires factory programming.
OffDelay_L6 [2:0]	MSB_OFFDELAY [2:0]: 0_000: 28.5 us 0_001: 28.5 us 0_010: 114 us 0_011: 228 us 0_100: 456 us 0_101: 912 us 0_110: 1824 us 0_111: 3648 us 1_000: 0us 1_001: 500us 1_010: 1000us 1_011: 2000us 1_100: 4000us 1_101: 8000us 1_110: 16000us 1_111: 32000us	MSB setting of 0/1 is only factory accessible register bit and requires factory programming.
MODE_L6	Determines startup sequencing from the CMI code	This is a factory expert bit that should not be changed. Modifying this bit may result in unexpected IC behavior.
RST_L6	0 = LDO6 does not affect nRESET output 1 = LDO6 POK affects nRESET output	RST bit determines if the regulator power okay (POK) signal is required to go high before the nRESET output from the PMIC can assert.

LDO46_REG64 – LDO46 Configuration Register

Address = 0x64h	Default = 0x60h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	DBON_L6 [3:0]				DBOK_L6 [3:0]			
Default	0110				0000			
Access	R/W				R/W			

Name	Description	Notes
DBON_L6 [3:0]	Determines startup sequencing from the CMI code	This is a factory expert bit that should not be changed. Modifying this bit may result in unexpected IC behavior.
DBOK_L6 [3:0]	Determines startup sequencing from the CMI code	This is a factory expert bit that should not be changed. Modifying this bit may result in unexpected IC behavior.

LDO46_REG65 – LDO46 Configuration Register

Address = 0x65h	Default = 0xE7h	Type = Basic Volatile

BIT	7	6	5	4	3	2	1	0
Name	LimSD_Dis_L6	PullUpGPIO8	PullUpGPIO7	Dis_PD_L6	RFU	ILIM_SCL_L6	SST_L6	QLTCH_L6
Default	1	1	1	0	0	1	1	1
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Name	Description	Notes
LimSD_Dis_L6	0 = Enable the shutdown by current limit of LDO6. 1 = Disable the shutdown by current limit of LDO6.	
PullUpGPIO8	Internal Pull up selection. 0 = no internal pull up 1 = internal pull up the GPIO to VIO with 86kOhm	
PullUpGPIO7	Internal Pull up selection. 0 = no internal pull up 1 = internal pull up the GPIO to VIO with 86kOhm	
Dis_PD_L6	Option to disable Pulldown Resistor when LDO is turned-off. 0 = Discharge VOUT when turn-off. 1 = Don't discharge VOUT when turn-off.	
RFU	Reserved for Future Use	Do not change this register value. Changing the register value can affect IC functionality.
ILIM_SCL_L6	Current limit setting for LDO/PLSW mode: 0: 350mA 1: 450mA	
SST_L6	Soft start time of LDO6: 0: 250us 1: 500us.	
QLTCH_L6	0 = LDO6 shuts down when its sequencing trigger input shuts down 1 = LDO6 stays on when its sequencing trigger input shuts down	

LDO46_REG66 – LDO46 Configuration Register

Address = 0x66h	Default = 0x0Eh	Type = Basic Volatile

BIT	7	6	5	4	3	2	1	0
Name	PwrGood_L4	OV_L4	ILIM_L4	RFU	UV_FltMsk_L4	OV_FltMsk_L4	IlimFltMsk_L4	RFU
Default	0	0	0	0	1	1	1	0
Access	RO	RO	RO	RO	R/W	R/W	R/W	RO

Name	Description	Notes
PwrGood_L4	0 = LDO4 voltage is below the power good threshold 1 = LDO4 voltage is above the power good threshold	Provides real-time power good status
OV_L4	0 = LDO4 voltage is below the overvoltage threshold 1 = LDO4 voltage is above the overvoltage threshold	Provides real-time overvoltage status
ILIM_L4	0 = LDO4 is below the ILIM threshold 1 = LDO4 is above the ILIM threshold	Provides real-time current limit status
RFU	Reserved for future use	Do not change this register value. Changing the register value can affect IC functionality.
UV_FltMsk_L4	0 = Unmasks the LDO4 UV fault 1 = Masks the LDO4 UV fault	When 1, the LDO UV fault is masked, the fault signal will not be sent to the master.
OV_FltMsk_L4	0 = Unmasks the LDO4 OV fault 1 = Masks the LDO4 OV fault	When 1, the LDO4 OV fault is masked, the fault signal will not be sent to the master. OV_L4 still provides real-time OV status.
IlimFltMsk_L4	0 = Unmasks the LDO4 ILIM fault 1 = Masks the LDO4 ILIM fault	When 1, the LDO4 ILIM fault is masked, the fault signal will not be sent to the master. ILIM_L4 still provides real-time overcurrent status.
RFU	Reserved for Future Use	Do not change this register value. Changing the register value can affect IC functionality.

LDO46_REG67 – LDO46 Configuration Register

Address = 0x67h	Default = 0xAEh	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	RANGE_L4	RFU	VSET_L4 [5:0]					
Default	1	0	101110					
Access	R/W	RO	R/W					

Name	Description	Notes
RANGE_L4	0 = Vout from 0.5 to 1.2875 1 = Vout from 1 to 4.15	RANGE LDO4
RFU	Reserved for Future Use	Do not change this register value. Changing the register value can affect IC functionality.
VSET_L4 [5:0]	LDO4 output voltage setting. VOUT = 0.5V + VSET_L4 [5:0] * 0.0125V (RANGE = 0) VOUT = 1V + VSET_L4 [5:0] * 0.05V (RANGE = 1)	

LDO46_REG68 – LDO46 Configuration Register

Address = 0x68h	Default = 0x80h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	ON_L4	PBINEN_L4	AUXINEN_L4	SLEEPEN_L4	DPSLPEN_L4	DBQL_L4 [2:0]		
Default	1	0	0	0	0	000		
Access	R/W	R/W	R/W	R/W	R/W	R/W		

Name	Description	Notes
ON_L4	0 = LDO4 is enabled through normal sequencing routing 1 = LDO4 I2C enable bit that bypasses normal sequencing	This functionality is dependent on the overall IC configuration. Consult the factory for details.
PBINEN_L4	0 = Does not respond to push button mode 1 = Responds to turn on automatically with push button input.	
AUXINEN_L4	0 = Cannot be turned on/off using Auxiliary Input 1 = Can be turned on/off using Auxiliary Input	Allows the output to be turned on and off by a GPIO input.
SLEEPEN_L4	0 = LDO4 stays on when the IC enters Sleep mode 1 = LDO4 turns off when the IC enters Sleep mode	
DPSLPEN_L4	0 – LDO4 stays on when the IC enters DEEP SLEEP mode 1 – LDO4 turns off when the IC enters DEEP SLEEP mode	
DBQL_L4 [2:0]	Determines startup sequencing from the CMI code	This is a factory expert bit that should not be changed. Modifying this bit may result in unexpected IC behavior.

LDO46_REG69 – LDO46 Configuration Register

Address = 0x69h	Default = 0x43h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	OnDelay_L4 [2:0]			OffDelay_L4 [2:0]			MODE_L4	RST_L4
Default	010			000			1	1
Access	R/W			R/W			R/W	R/W

Name	Description	Notes
OnDelay_L4 [2:0]	MSB_ONDELAY [2:0]: 0_000: 28.5 us 0_001: 28.5 us 0_010: 114 us 0_011: 228 us 0_100: 456 us 0_101: 912 us 0_110: 1824 us 0_111: 3648 us 1_000: 0us 1_001: 500us 1_010: 1000us 1_011: 2000us 1_100: 4000us 1_101: 8000us 1_110: 16000us 1_111: 32000us	MSB setting of 0/1 is only factory accessible register bit and requires factory programming.
OffDelay_L4 [2:0]	MSB_OFFDELAY [2:0]: 0_000: 28.5 us 0_001: 28.5 us 0_010: 114 us 0_011: 228 us 0_100: 456 us 0_101: 912 us 0_110: 1824 us 0_111: 3648 us 1_000: 0 1_001: 500us 1_010: 1000us 1_011: 2000us 1_100: 4000us 1_101: 8000us 1_110: 16000us 1_111: 32000us	MSB setting of 0/1 is only factory accessible register bit and requires factory programming.
MODE_L4	Determines startup sequencing from the CMI code	This is a factory expert bit that should not be changed. Modifying this bit may result in unexpected IC behavior.
RST_L4	0 = LDO4 does not affect nRESET output 1 = LDO4 POK affects nRESET output	RST bit determines if the regulator power okay (POK) signal is required to go high before the nRESET output from the PMIC can assert.

LDO46_REG6A – LDO46 Configuration Register

Address = 0x6Ah	Default = 0x07h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	DBON_L4 [3:0]				DBOK_L4 [3:0]			
Default	0000				0111			
Access	R/W				R/W			

Name	Description	Notes
DBON_L4 [3:0]	Determines startup sequencing from the CMI code	This is a factory expert bit that should not be changed. Modifying this bit may result in unexpected IC behavior.
DBOK_L4 [3:0]	Determines startup sequencing from the CMI code	This is a factory expert bit that should not be changed. Modifying this bit may result in unexpected IC behavior.

Referenced Documents

The reference documents below take precedence over the contents of this application note and should always be consulted for the latest information.

ACT88760 Data Sheet

Contact Information

For the latest specifications, additional product information, worldwide sales and distribution locations:

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