QPA2966

2 – 18 GHz 20 Watt GaN Amplifier

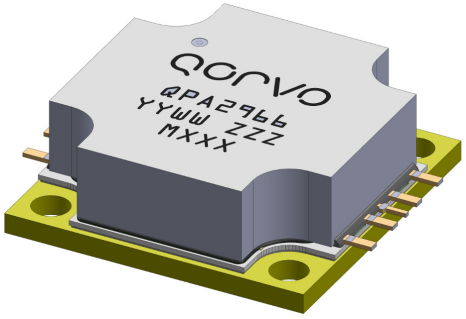
Product Overview

Qorvo's QPA2966 is a packaged wideband power amplifier, fabricated on Qorvo's QGaN15 GaN on SiC process. The QPA2966 operates from 2 to 18 GHz, providing 20 W of saturated power with 12 dB large signal gain and 20 % power-added efficiency at 22 V drain bias.

The QPA2966 is in a 10-lead 0.6 x 0.6 x 0.205 inch bolt-down package with a Cu base for superior thermal management. To simplify system integration, QPA2966 is fully matched to 50 ohms including integrated DC blocking capacitors and a RF choke.

The combination of wideband power, gain and efficiency provides system designers the flexibility to improve system performance while reducing size and cost. QPA2966 is ideally suited for wideband communications systems, electronic warfare, test instrumentation and radar applications across both military and commercial markets.

Lead free and RoHS compliant.

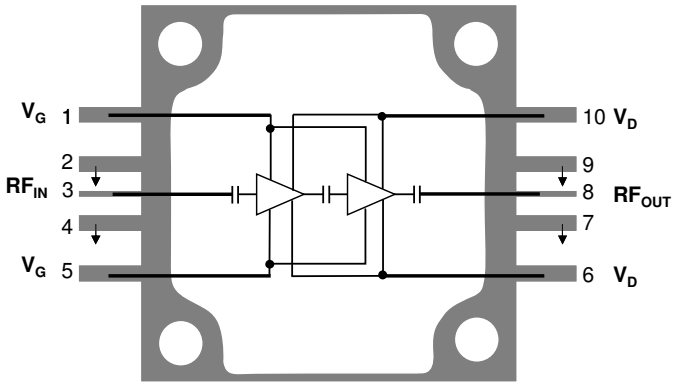


Key Features

- Frequency Range: 2 – 18 GHz
- P_{SAT} (P_{IN} = 31 dBm): 43 dBm
- PAE (P_{IN} = 31 dBm): 20 %
- Power Gain (P_{IN} = 31 dBm): 12 dB
- Small Signal Gain: 19 dB
- Bias: CW, V_D = 22 V, I_{DQ} = 3360 mA
- Package Dimensions: 0.6 x 0.6 x 0.205 in

Performance is typical across frequency. Please reference electrical specification table and data plots for more details.

Functional Block Diagram



,Applications

- Communication Systems
- Electronic Warfare
- Radar
- Test Equipment

Ordering Information

Part No.	Description
QPA2966	2 - 18 GHz 20 Watt GaN Amplifier
QPA2966EVB	Evaluation Board for QPA2966

Absolute Maximum Ratings

Parameter	Value / Range
Drain Voltage (V_D)	29.5 V
Gate Voltage Range (V_G)	–5 to 0 V
Drain Current (I_D)	5695 mA
Gate Current (I_G)	20 mA
Power Dissipation (P_{DISS}), T_{BASE} = 85°C	77.5 W
Input Power (P_{IN}), 50 Ω, V_D = 22 V, I_{DQ} = 3360 mA, T_{BASE} = 85°C	37 dBm
Input Power (P_{IN}), 3:1 VSWR, V_D = 22 V, I_{DQ} = 3360 mA, T_{BASE} = 85°C	37 dBm
Mounting Temperature	Refer to Assembly Notes, page 25
Storage Temperature	–55 to 150 °C

Operation of this device outside the parameter ranges given above may cause permanent damage. These are stress ratings only, and functional operation of the device at these conditions is not implied.

Recommended Operating Conditions

Parameter	Min	Typ	Max	Units
Drain Voltage (V_D)		22	22	V
Drain Current, Quiescent (I_{DQ})		3360		mA
Drain Current, RF (I_{D_Drive})	See charts page 6, 7, 10, 13, 16			mA
Gate Voltage Typ. Range (V_G)	–1.2 to -2.7			V
Gate Current, RF (I_{G_Drive})	See charts page 6 - 7			mA
Operating Temp. Range, T_{BASE}*	–40	+25	+85	°C

*T_{BASE} is back side of package QPA2966

Electrical specifications are measured at specified test conditions. Specifications are not guaranteed over all recommended operating conditions.

Electrical Specifications

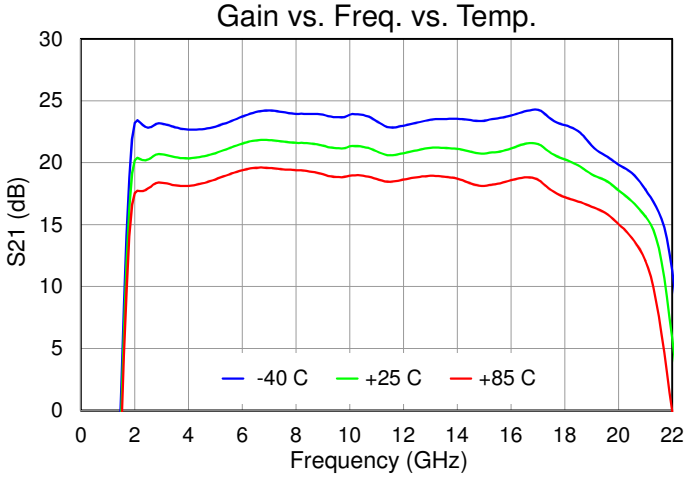
Parameter	Conditions (1) (2)	Min	Typ	Max	Units
Operational Frequency Range		2		18	GHz
Output Power at Saturation, P_{SAT}	P_{IN} = +31 dBm, Frequency = 2 - 16 GHz		43		dBm
	P_{IN} = +31 dBm, Frequency = 17 - 18 GHz		42		
Power Added Efficiency, PAE	P_{IN} = +31 dBm, Frequency = 2 - 16 GHz		22		%
	P_{IN} = +31 dBm, Frequency = 17 - 18 GHz		17		
Small Signal Gain, S21	P_{IN} = -20 dBm		19		dB
Input Return Loss, IRL	P_{IN} = -20 dBm		10		dB
Output Return Loss, ORL	P_{IN} = -20 dBm		10		dB
P_{SAT} Temperature Coefficient	T_{DIFF} = –40°C to +85°C; P_{IN} = +31 dBm		–0.005		dBm/°C
S21 Temperature Coefficient	T_{DIFF} = –40°C to +85°C		–0.04		dB/°C
Gate Leakage	V_D = 10 V, V_G = -3.7 V, no RF	-16.8			mA

Notes:
1. Test conditions unless otherwise noted: CW, V_D = 22 V, I_{DQ} = 3360 mA, adjusting V_G, T_{BASE} = +25 °C, Z_0 = 50 Ω
2. T_{BASE} is back side of package QPA2966

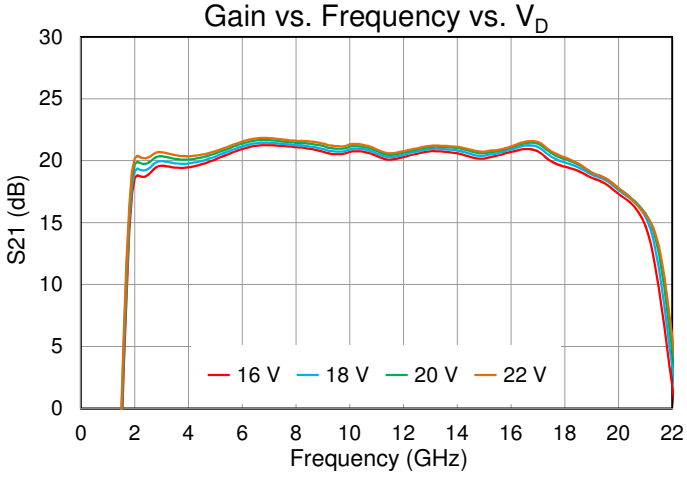
Performance Plots – Small Signal

Test conditions unless otherwise noted: CW, V_D = 22 V, I_{DQ} = 3360 mA, T_{BASE} = +25 °C (T_{BASE} is backside of QPA2966)

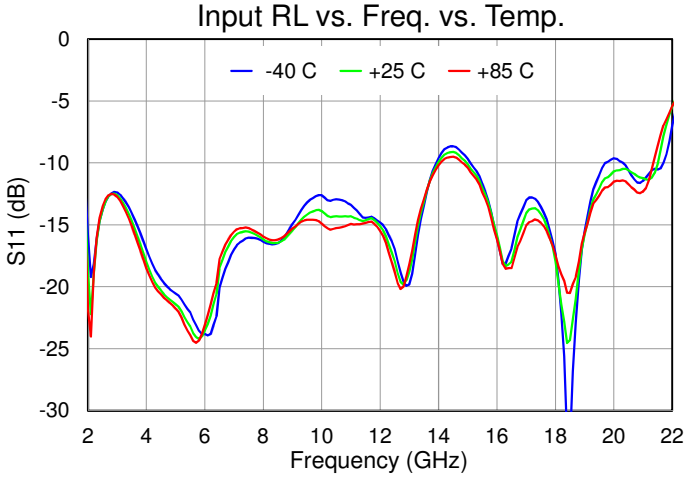
Gain vs. Freq. vs. Temp.



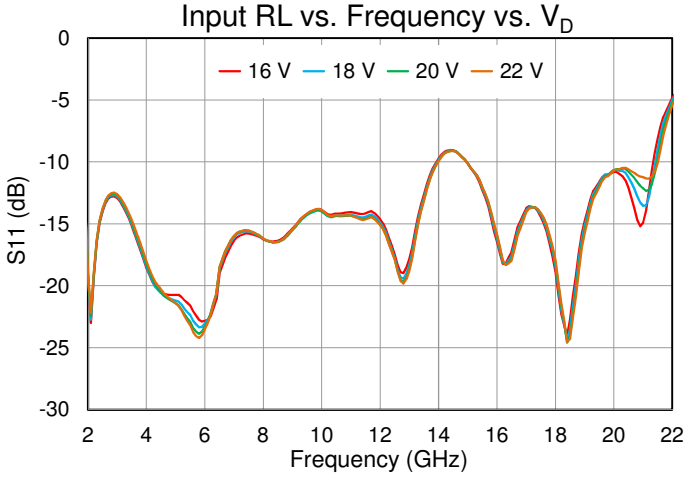
Gain vs. Frequency vs. V_D



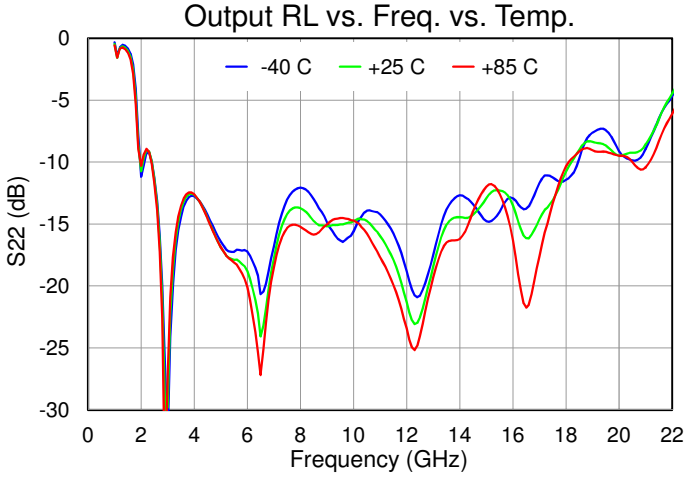
Input RL vs. Freq. vs. Temp.



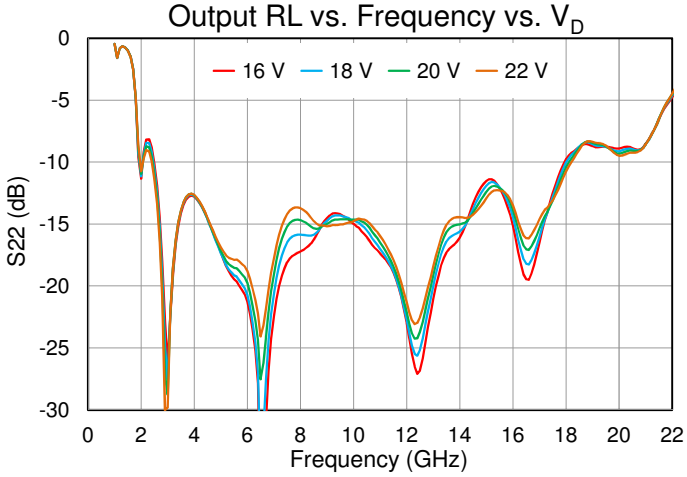
Input RL vs. Frequency vs. V_D



Output RL vs. Freq. vs. Temp.

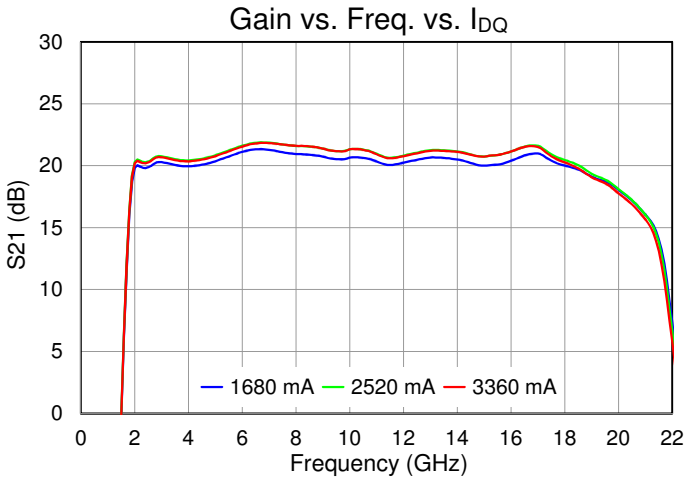


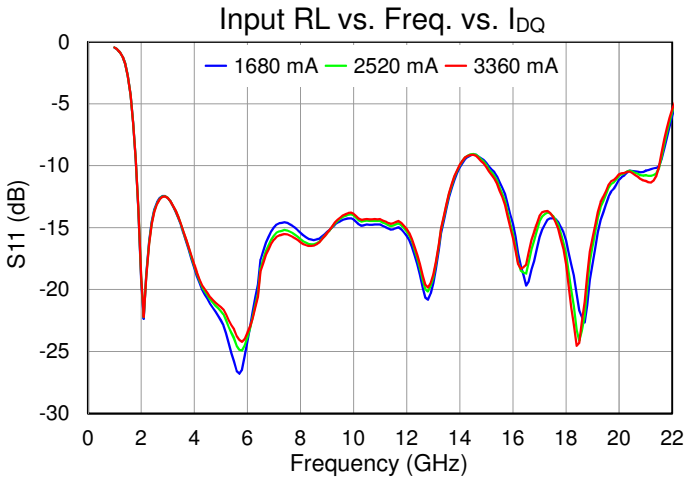
Output RL vs. Frequency vs. V_D

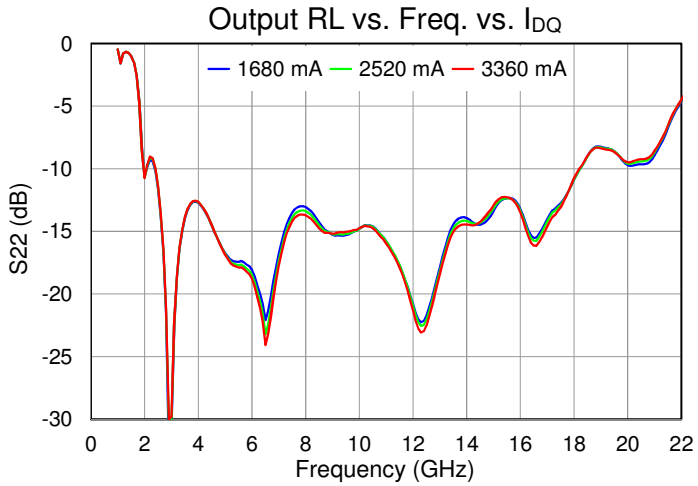


Performance Plots – Small Signal

Test conditions unless otherwise noted: CW, V_D = 22 V, I_{DQ} = 3360 mA, T_{BASE} = +25 °C (T_{BASE} is backside of QPA2966)



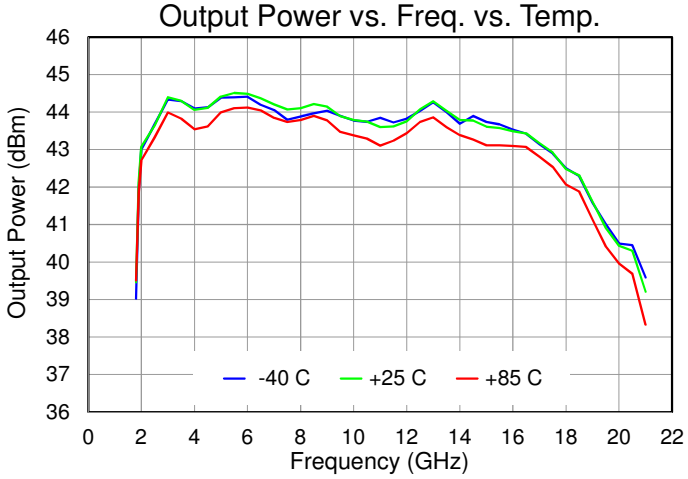




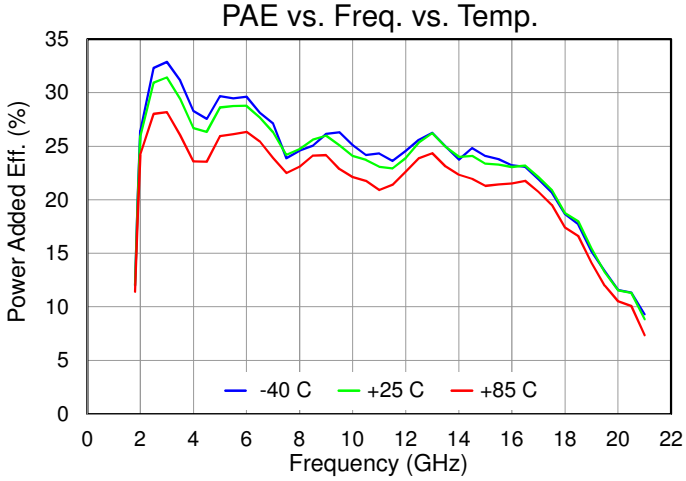
Performance Plots – Large Signal

Test conditions unless otherwise noted: CW, V_D = 22 V, I_{DQ} = 3360 mA, P_{IN} = 31 dBm, T_{BASE} = +25 °C (T_{BASE} is backside of QPA2966)

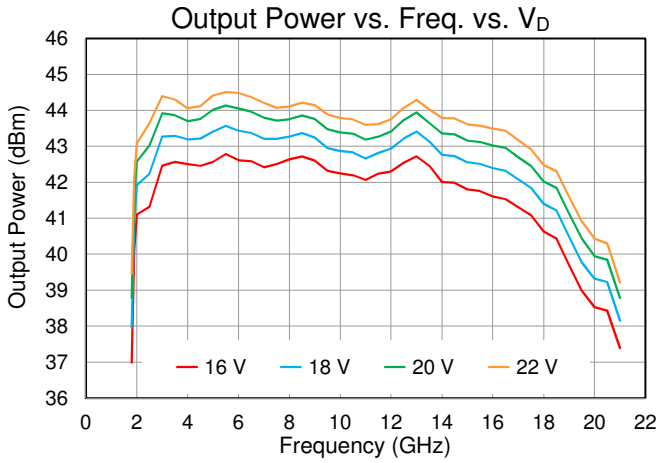
Output Power vs. Freq. vs. Temp.



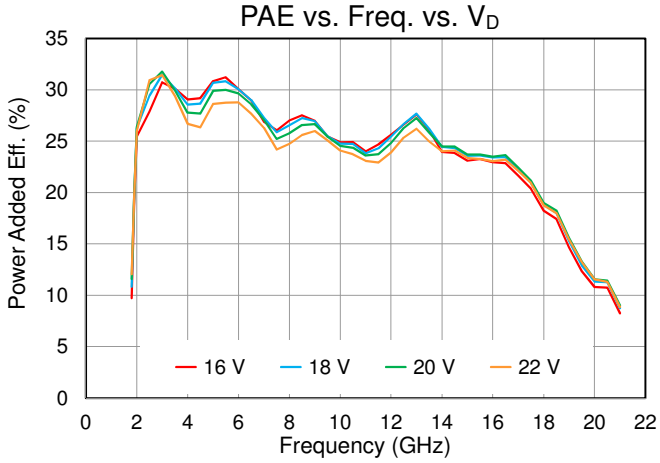
PAE vs. Freq. vs. Temp.



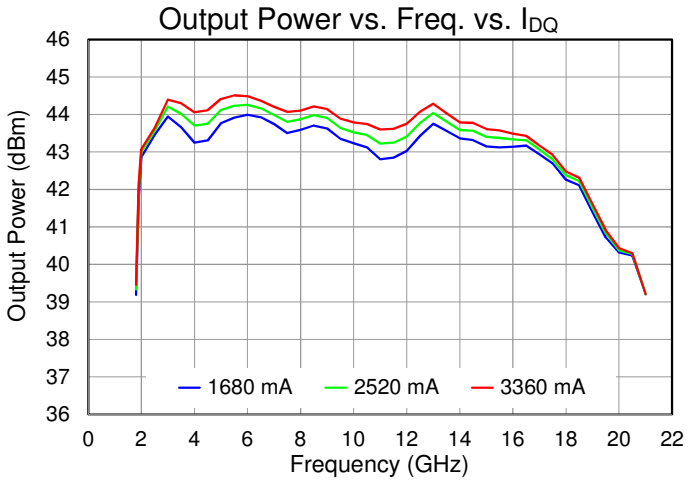
Output Power vs. Freq. vs. V_D



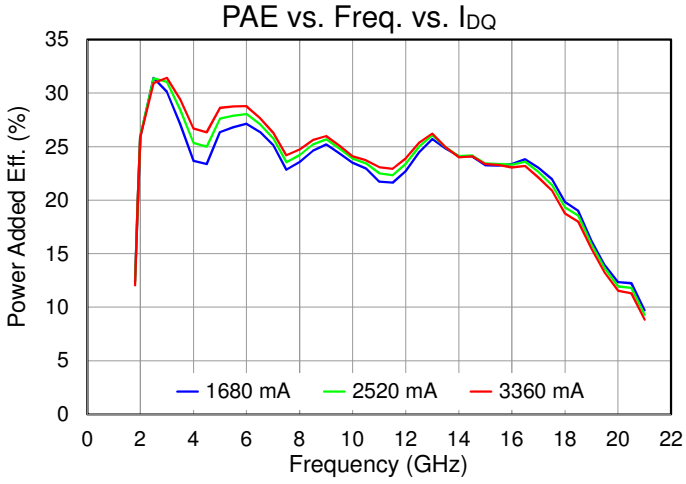
PAE vs. Freq. vs. V_D



Output Power vs. Freq. vs. I_{DQ}



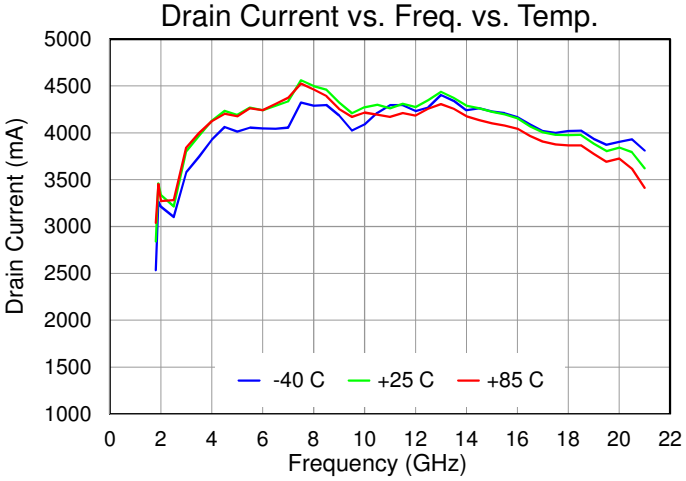
PAE vs. Freq. vs. I_{DQ}



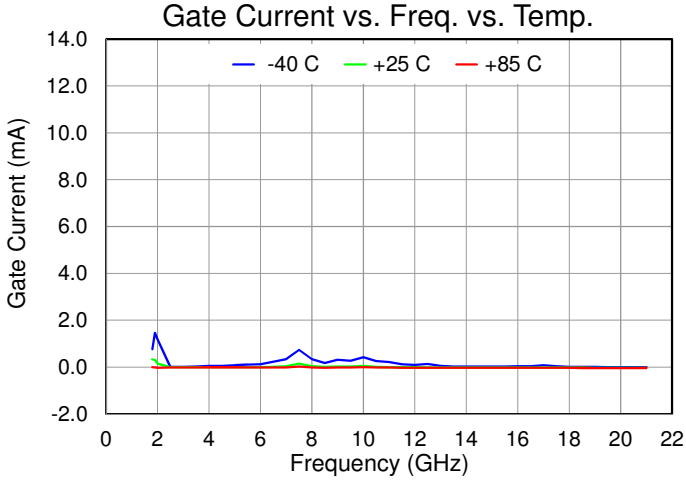
Performance Plots – Large Signal

Test conditions unless otherwise noted: CW, V_D = 22 V, I_{DQ} = 3360 mA, P_{IN} = 31 dBm, T_{BASE} = +25 °C (T_{BASE} is backside of QPA2966)

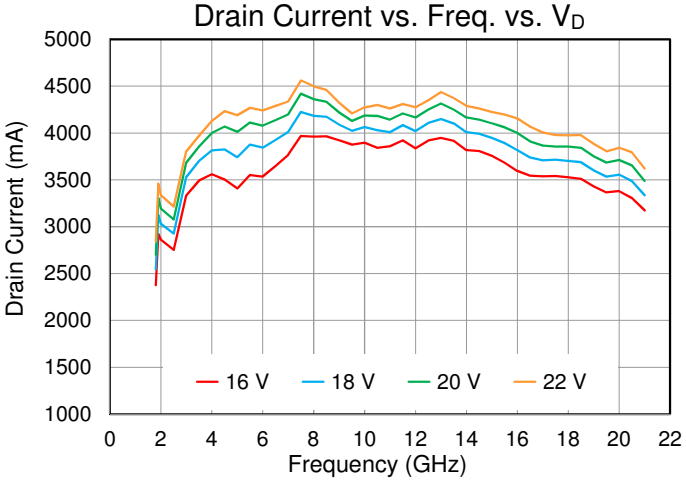
Drain Current vs. Freq. vs. Temp.



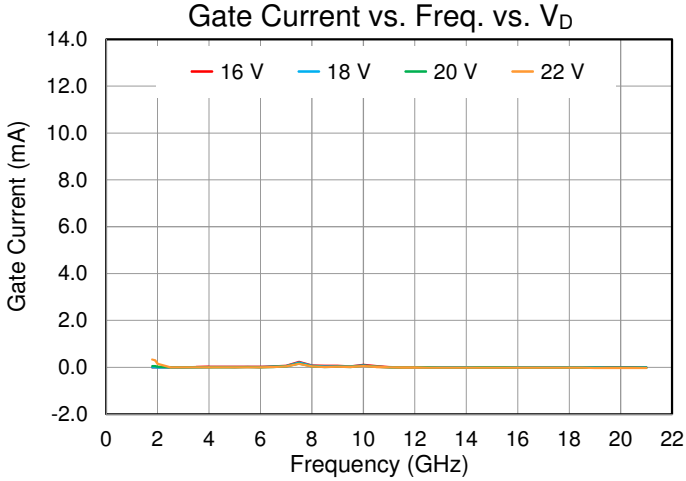
Gate Current vs. Freq. vs. Temp.



Drain Current vs. Freq. vs. V_D



Gate Current vs. Freq. vs. V_D



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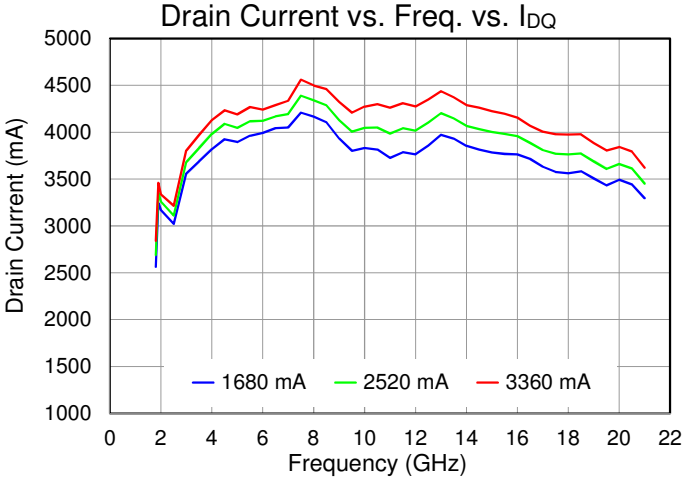

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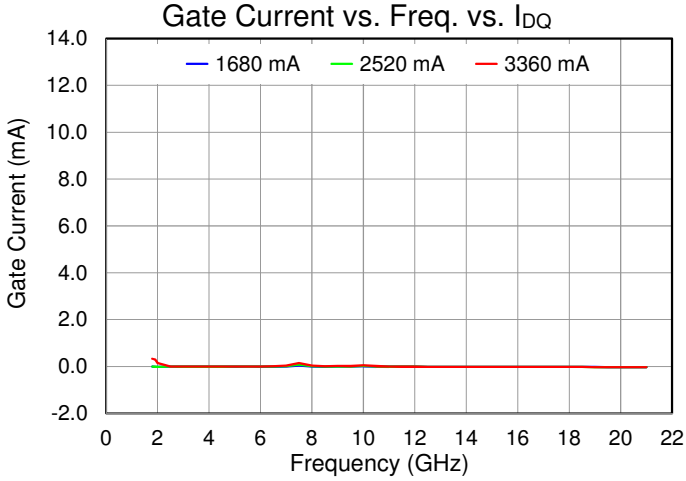

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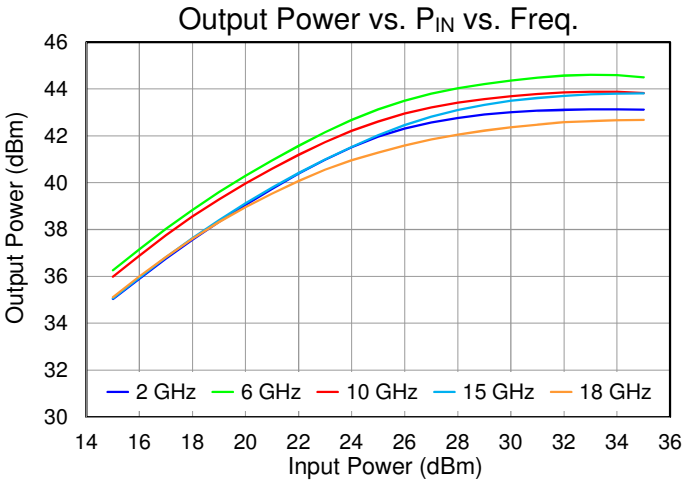

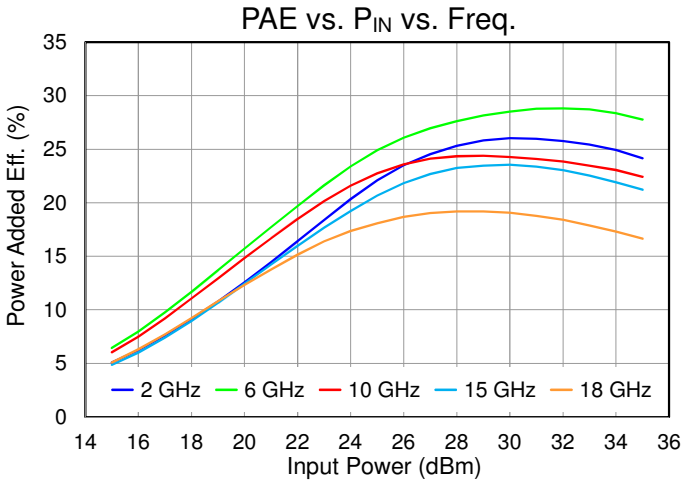

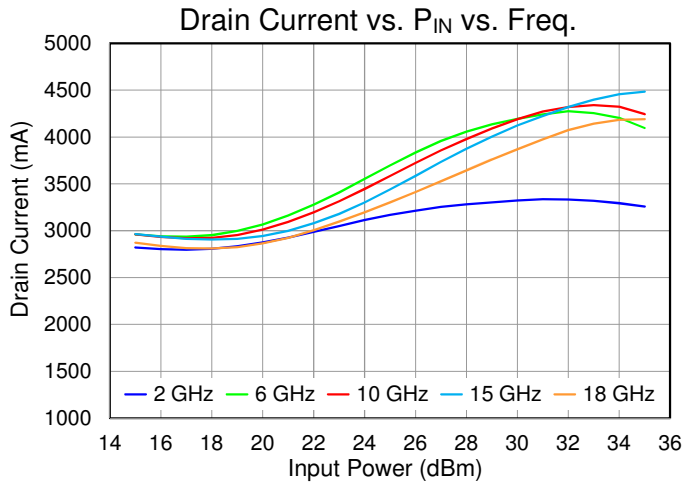

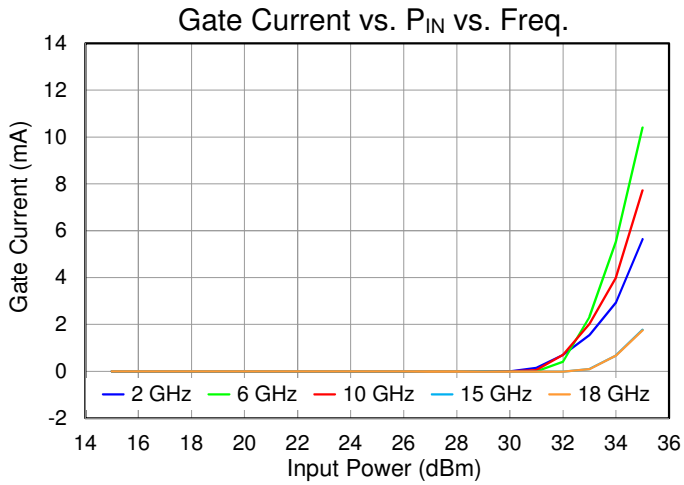

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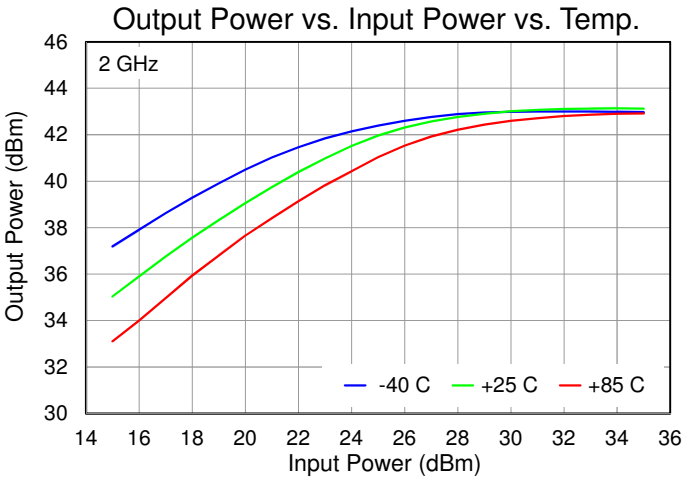

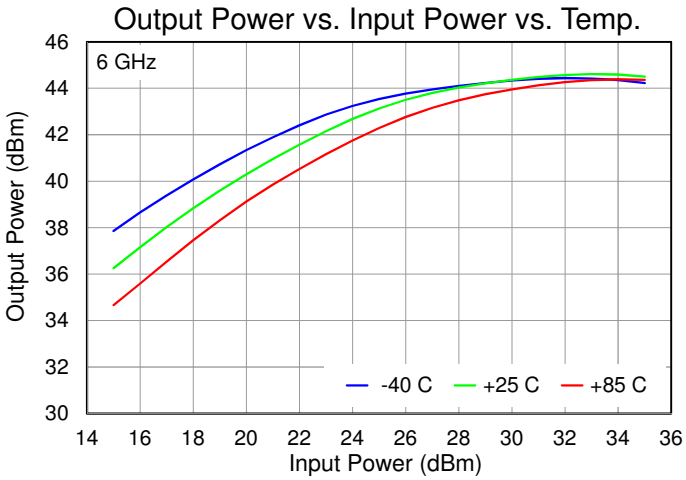

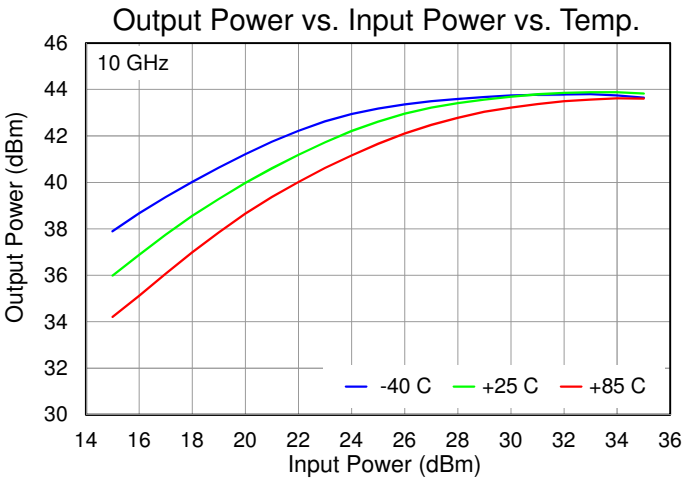

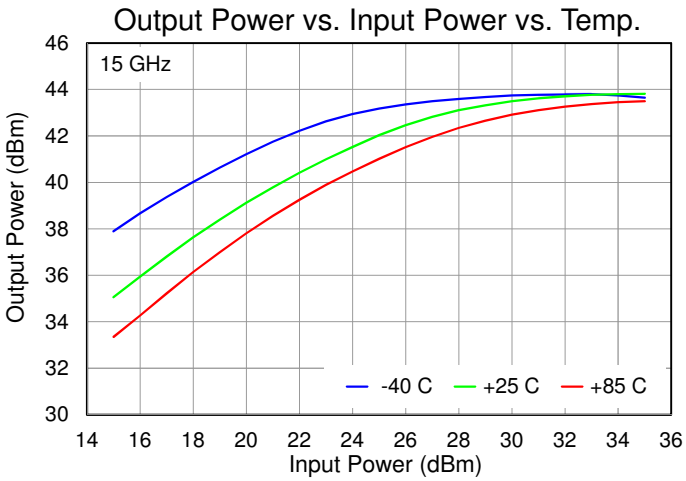

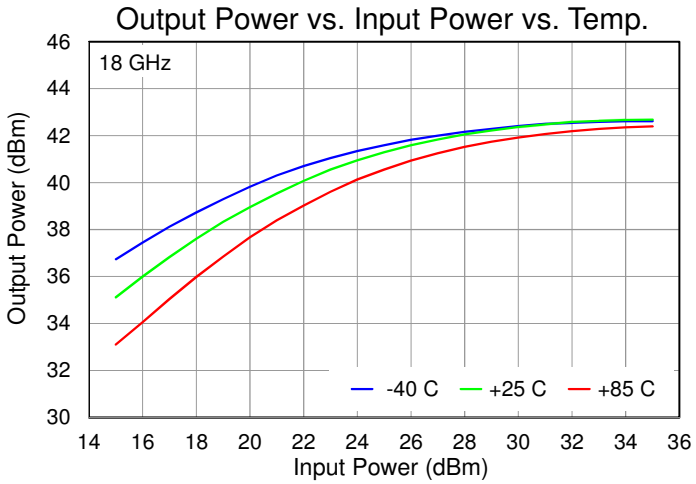

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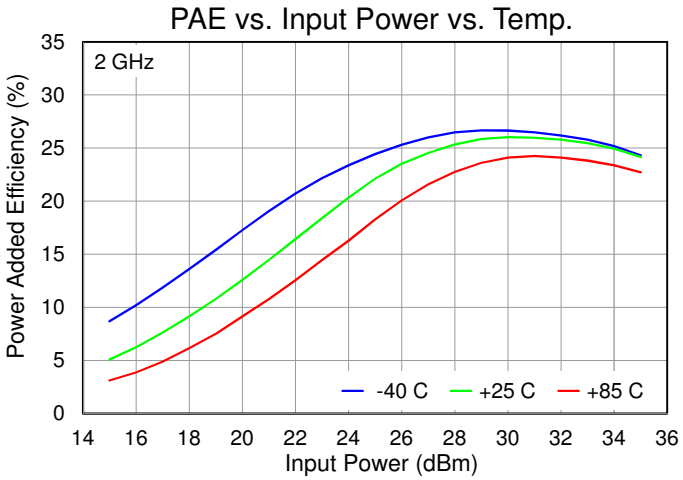

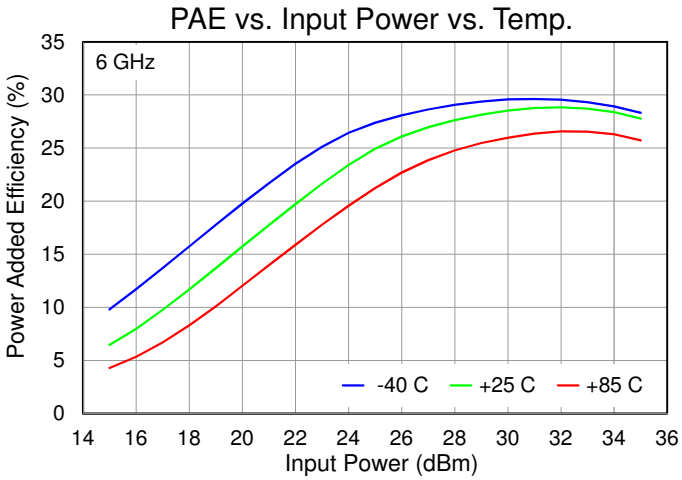

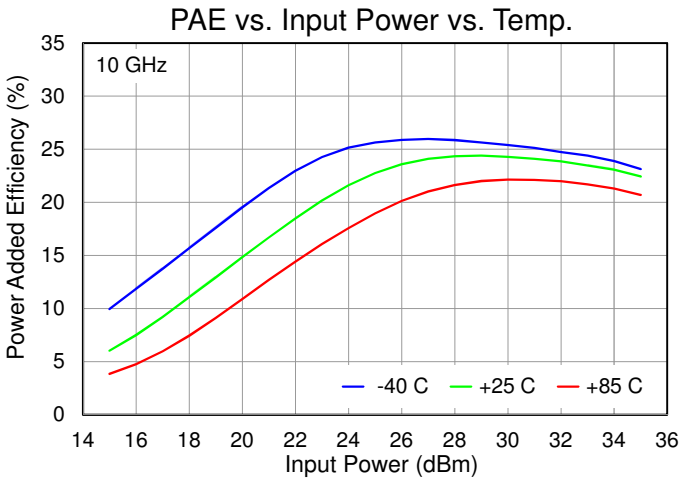

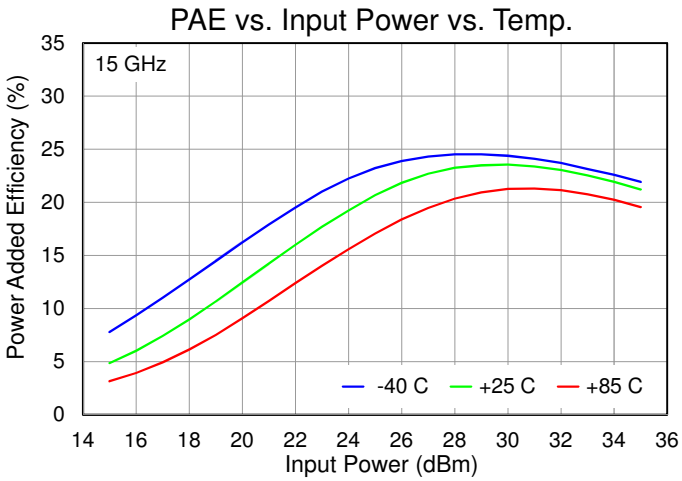

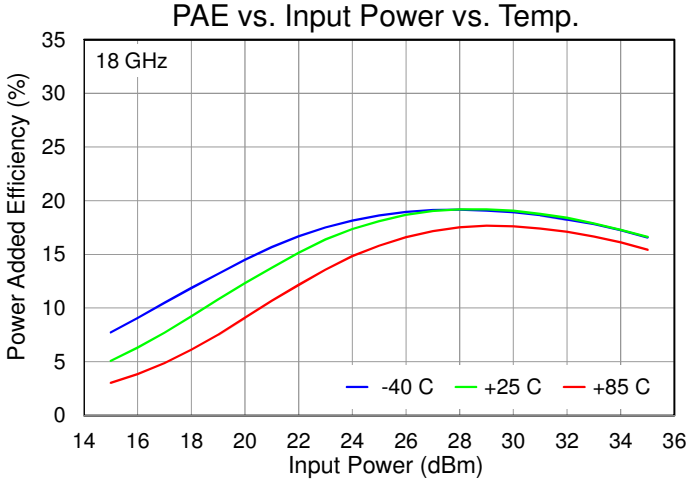

Performance Plots – Large Signal

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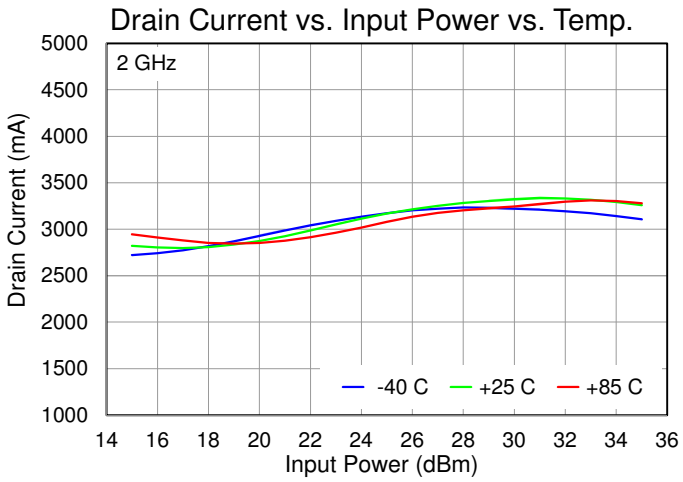
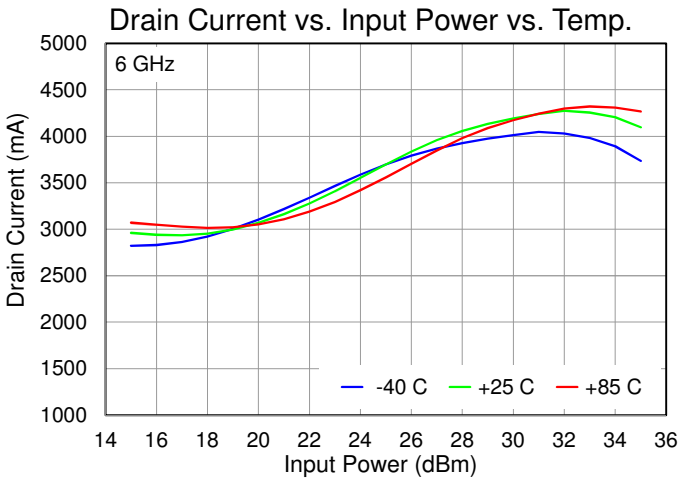
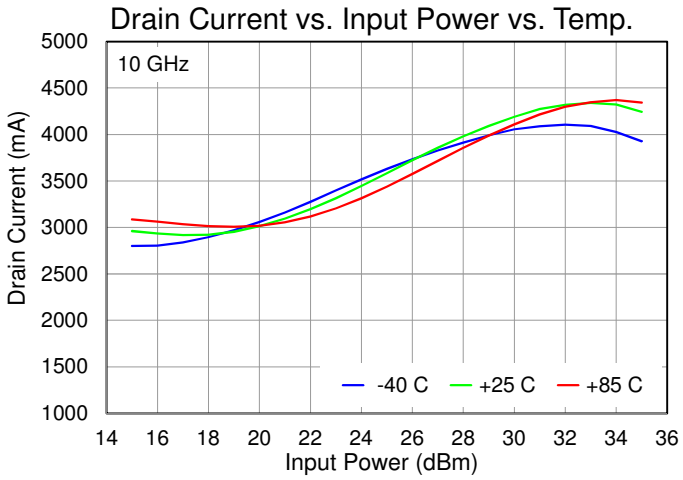
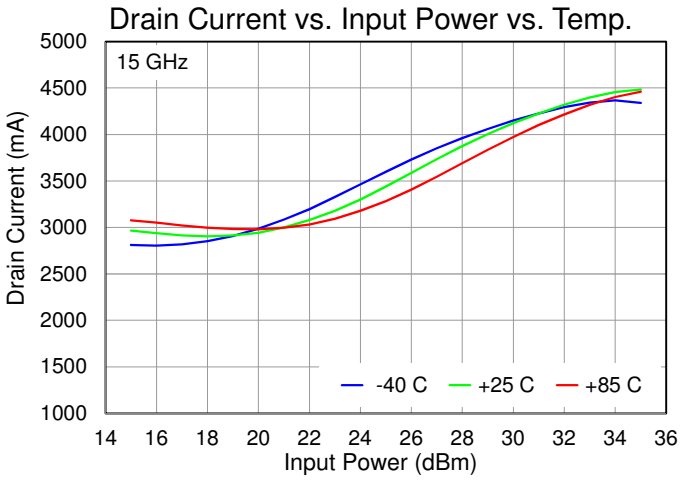
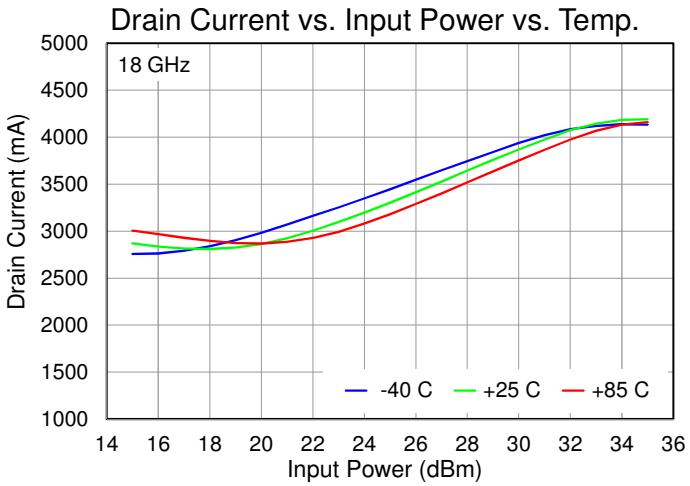




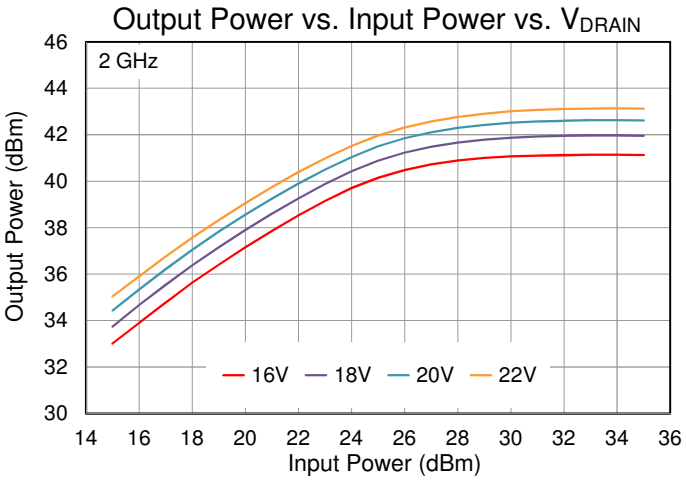


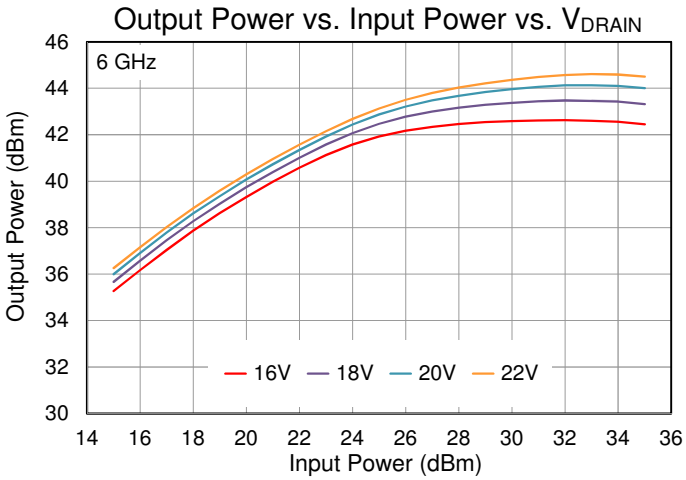


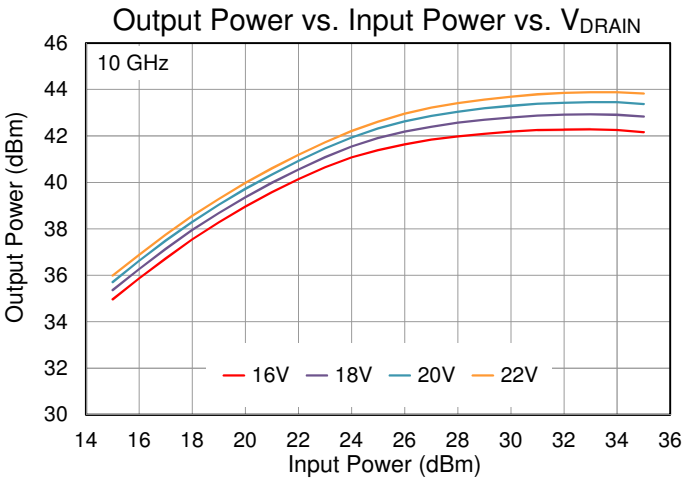


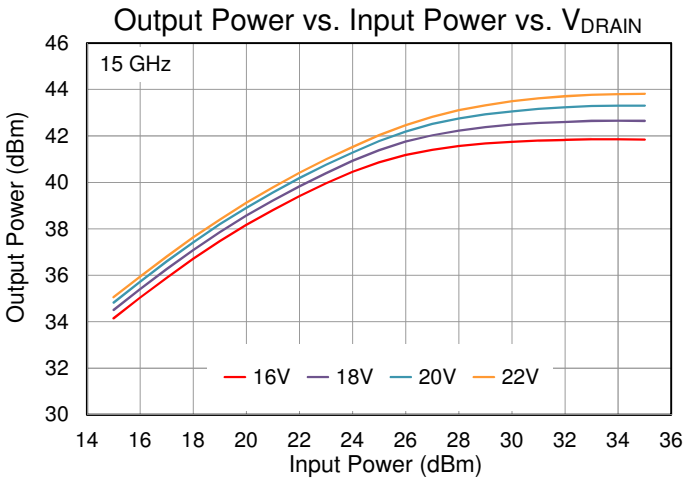
Performance Plots – Large Signal

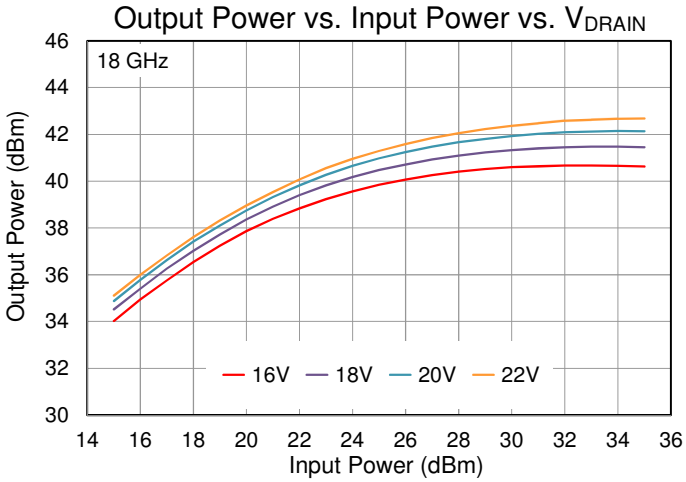
Test conditions unless otherwise noted: CW, V_D = 22 V, I_{DQ} = 3360 mA, P_{IN} = 31 dBm, T_{BASE} = +25 °C (T_{BASE} is backside of QPA2966)





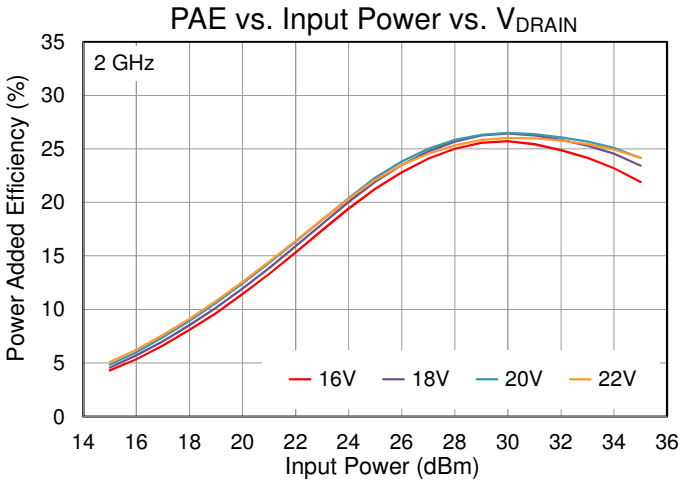


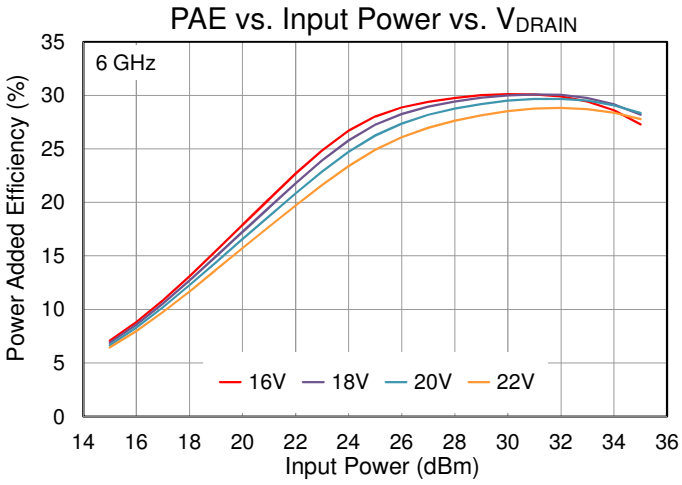


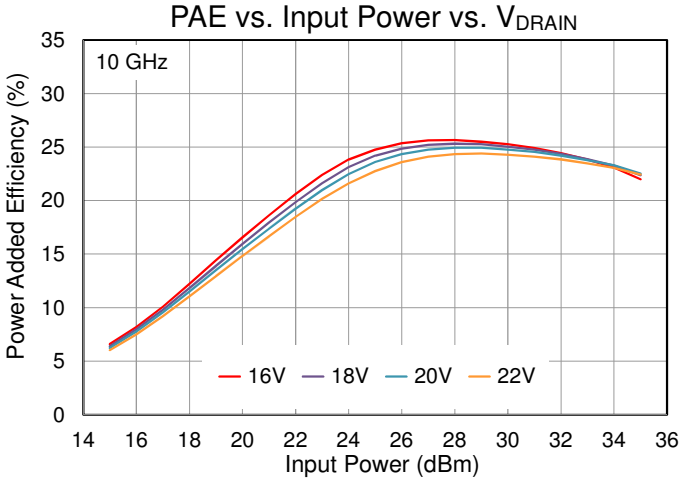


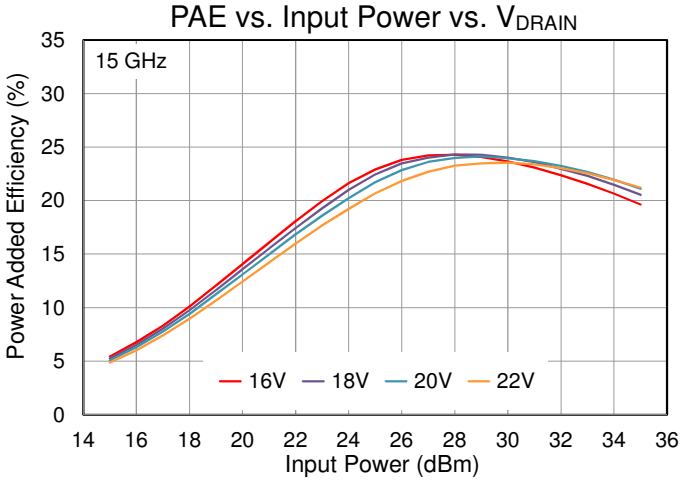
Performance Plots – Large Signal

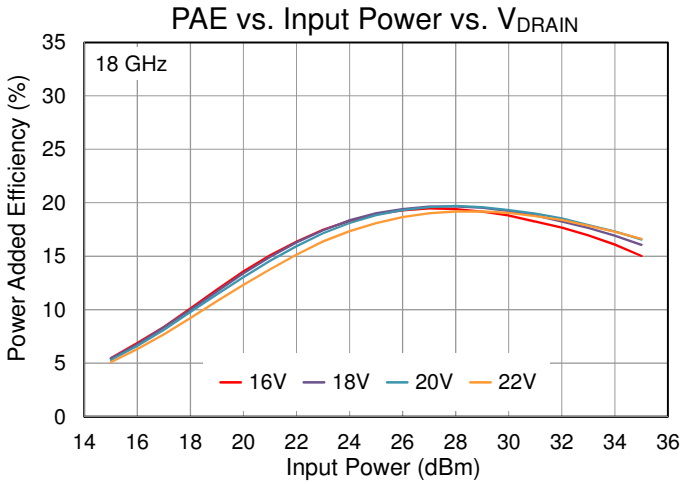
Test conditions unless otherwise noted: CW, V_D = 22 V, I_{DQ} = 3360 mA, P_{IN} = 31 dBm, T_{BASE} = +25 °C (T_{BASE} is backside of QPA2966)





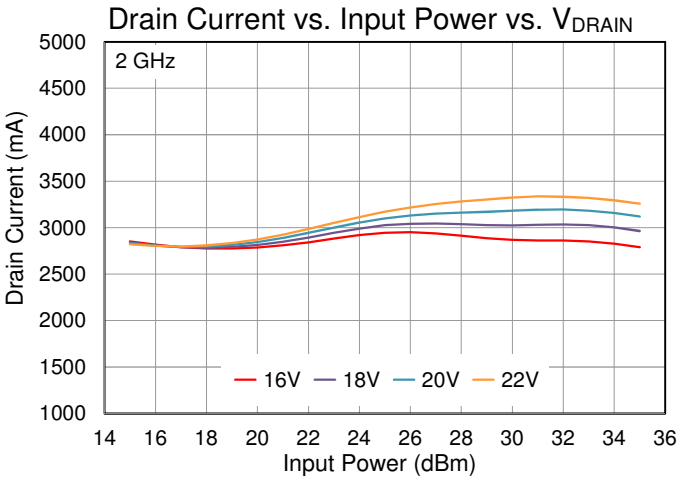


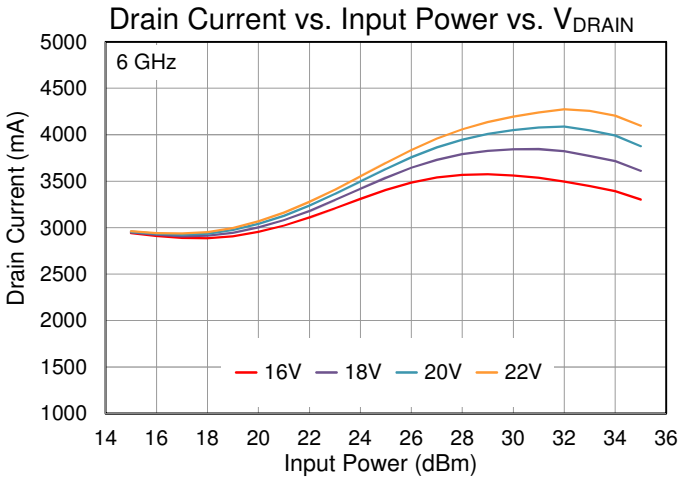


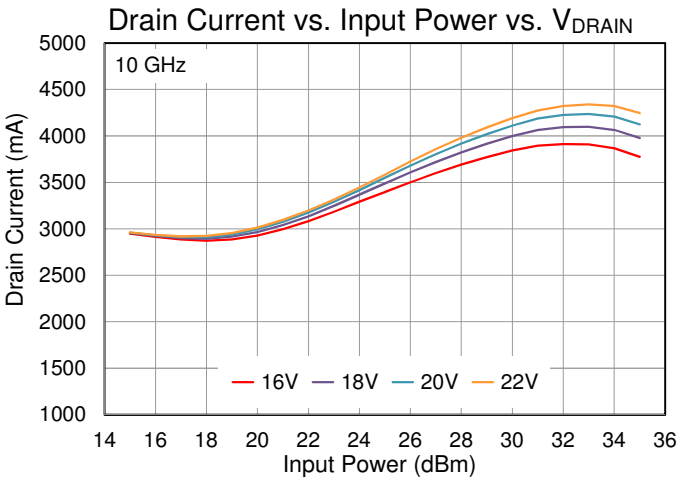


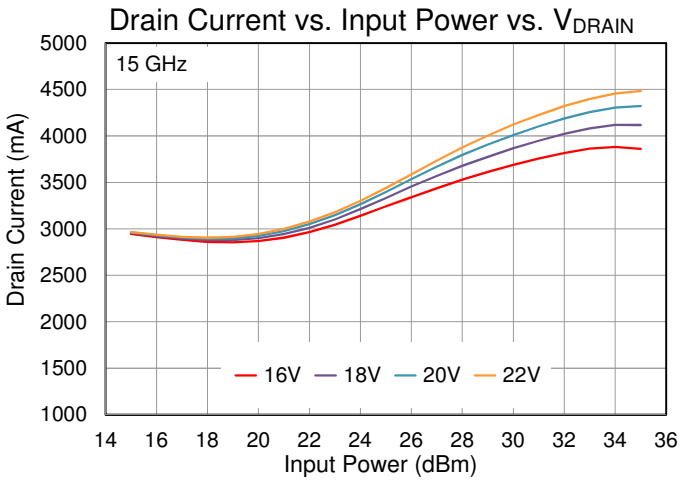
Performance Plots – Large Signal

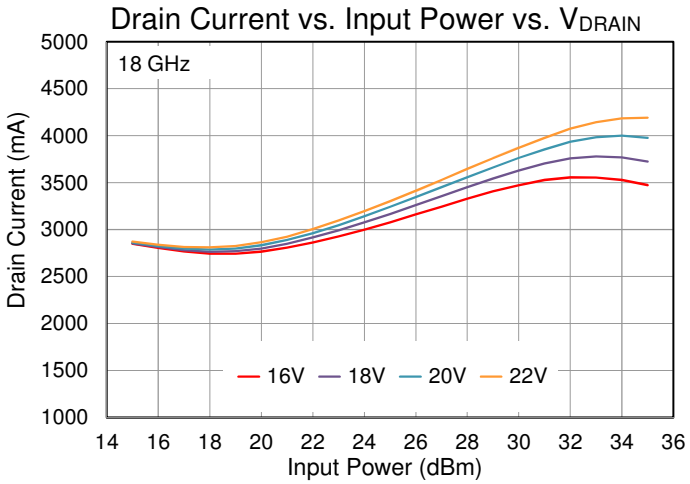
Test conditions unless otherwise noted: CW, V_D = 22 V, I_{DQ} = 3360 mA, P_{IN} = 31 dBm, T_{BASE} = +25 °C (T_{BASE} is backside of QPA2966)





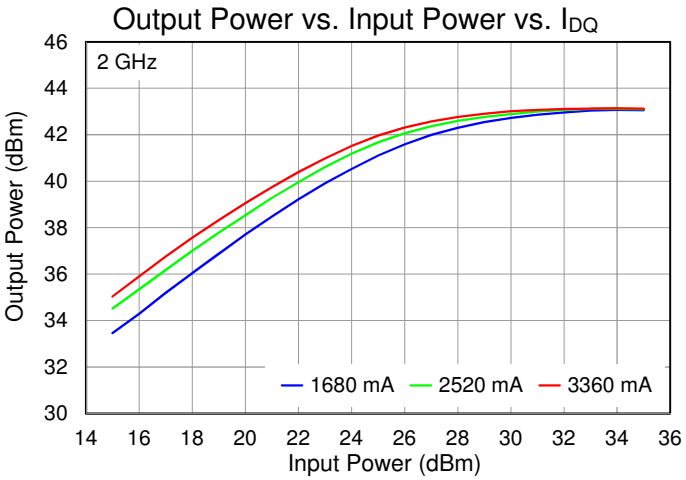


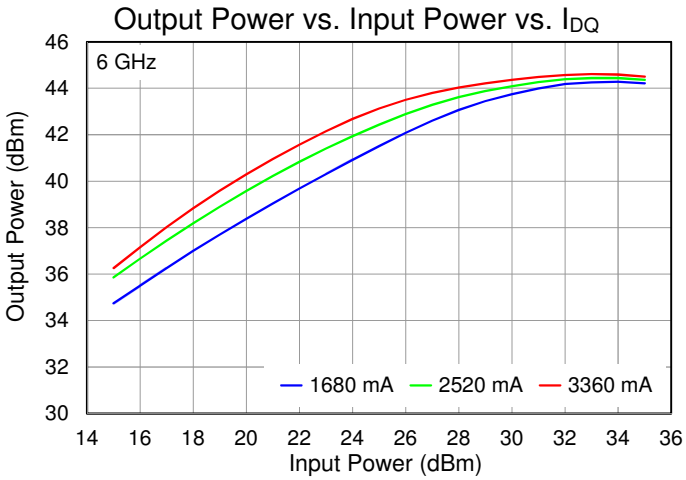


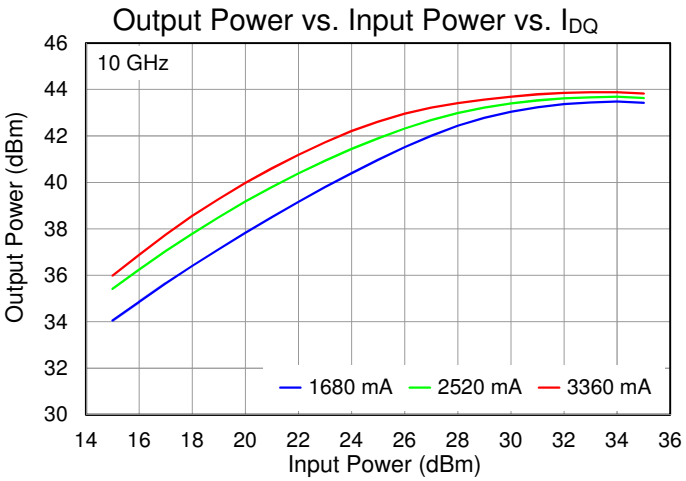


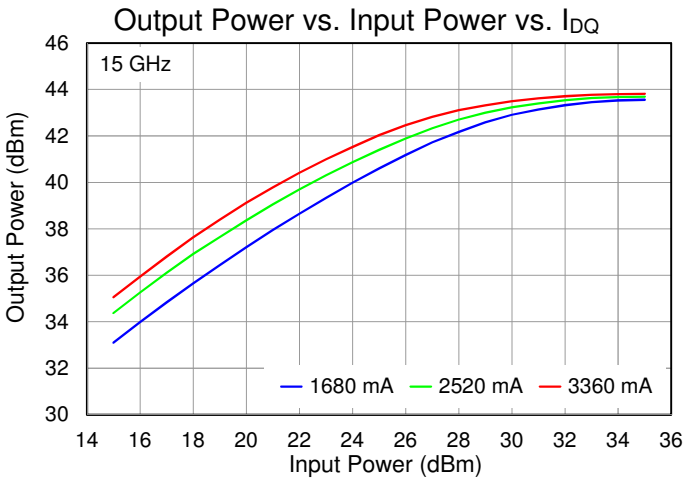
Performance Plots – Large Signal

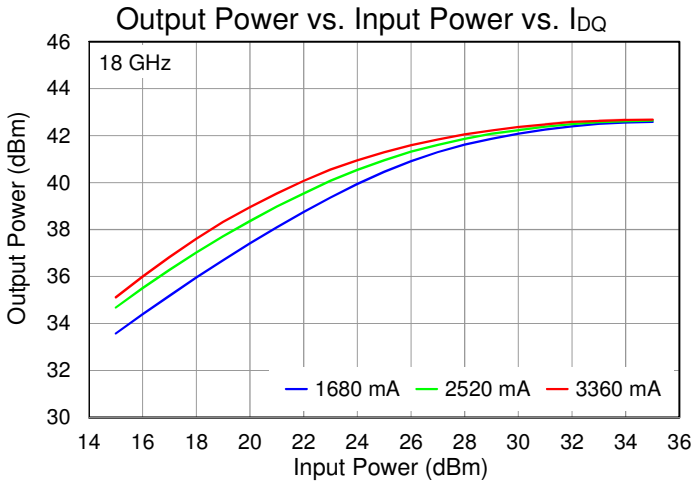
Test conditions unless otherwise noted: CW, V_D = 22 V, I_{DQ} = 3360 mA, P_{IN} = 31 dBm, T_{BASE} = +25 °C (T_{BASE} is backside of QPA2966)







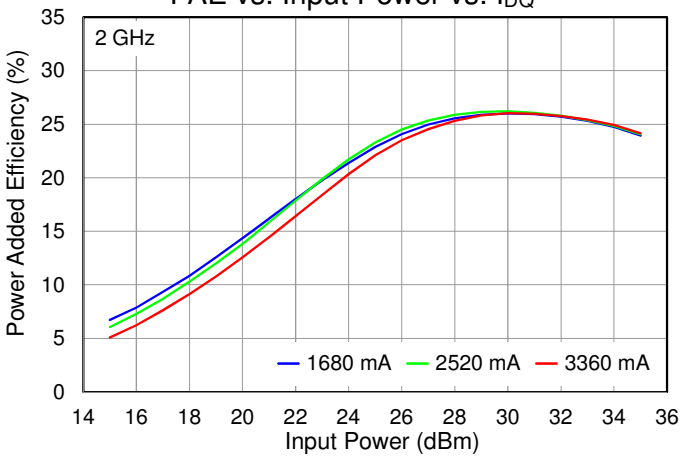




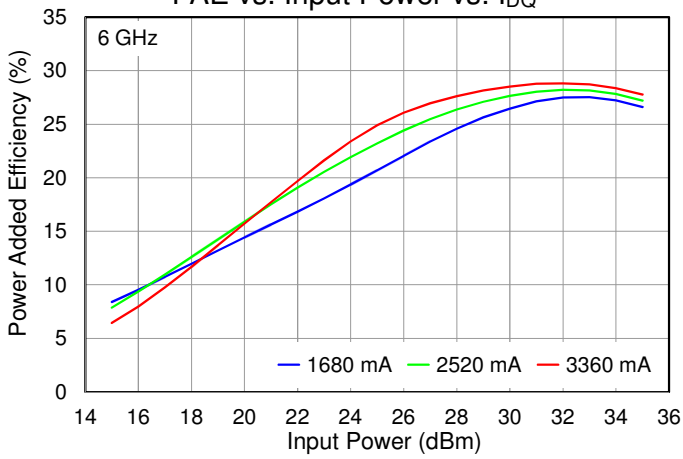
Performance Plots – Large Signal

Test conditions unless otherwise noted: CW, V_D = 22 V, I_{DQ} = 3360 mA, P_{IN} = 31 dBm, T_{BASE} = +25 °C (T_{BASE} is backside of QPA2966)

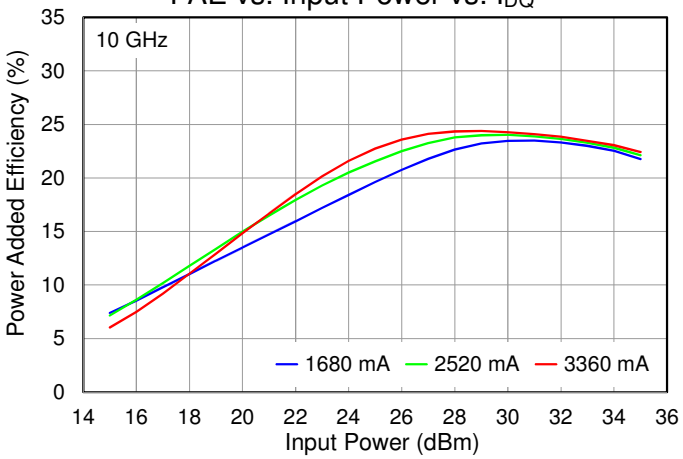
PAE vs. Input Power vs. I_{DQ}



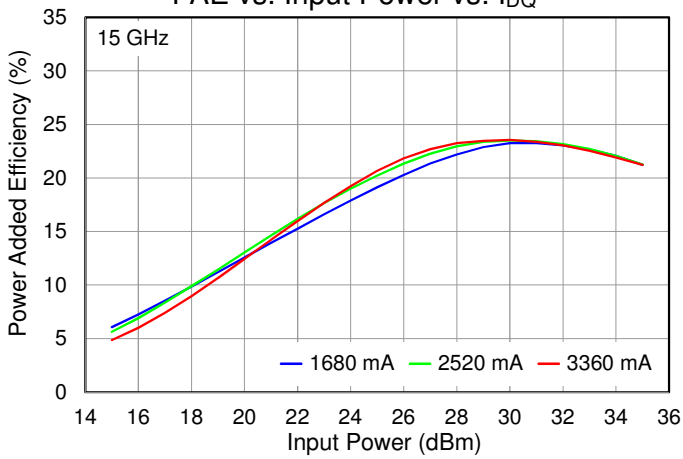
PAE vs. Input Power vs. I_{DQ}



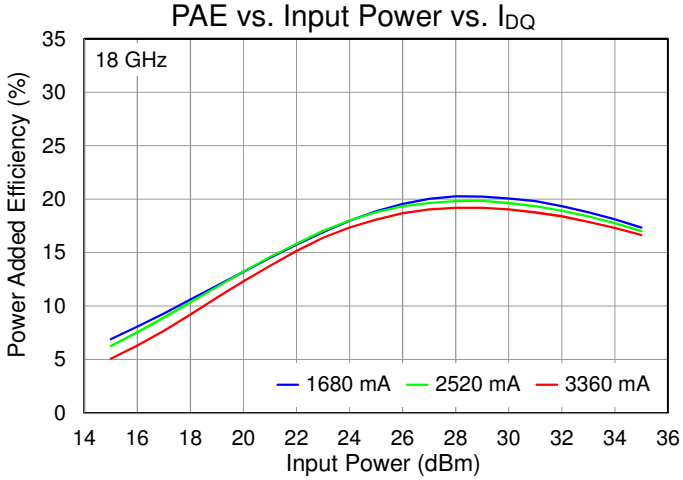
PAE vs. Input Power vs. I_{DQ}



PAE vs. Input Power vs. I_{DQ}

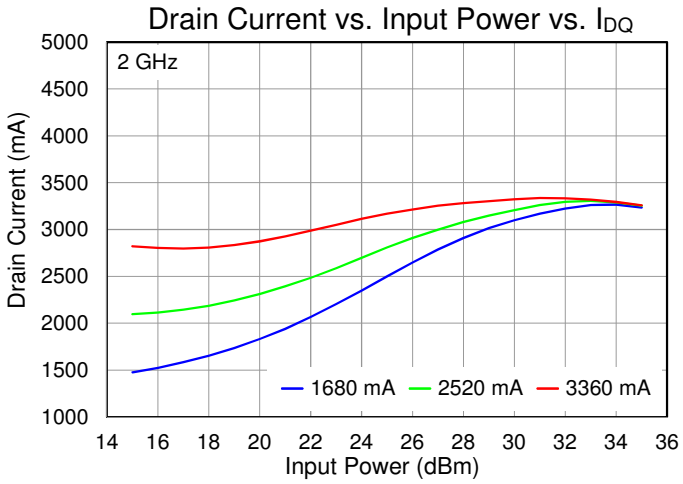


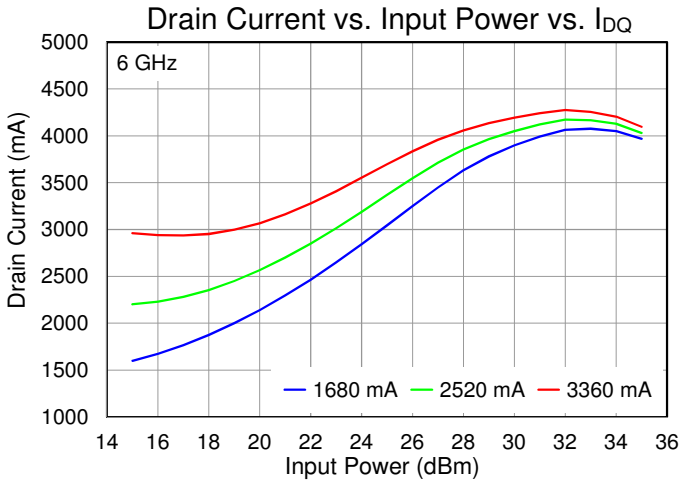
PAE vs. Input Power vs. I_{DQ}

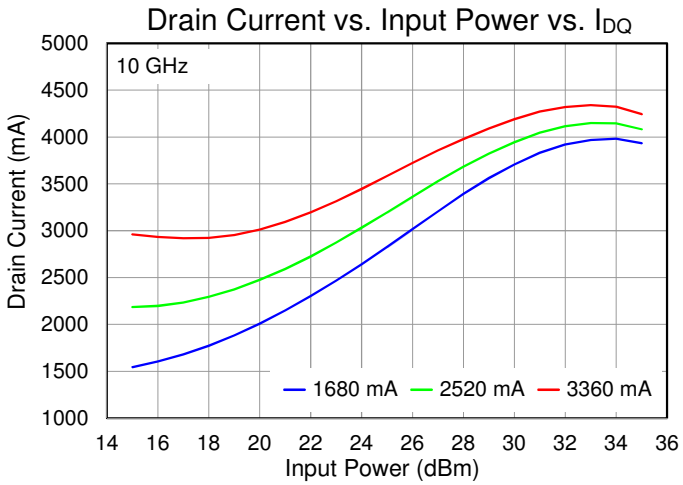


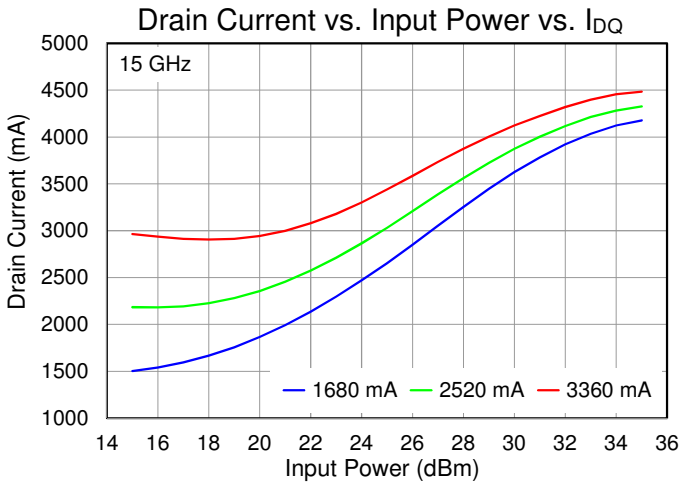
Performance Plots – Large Signal

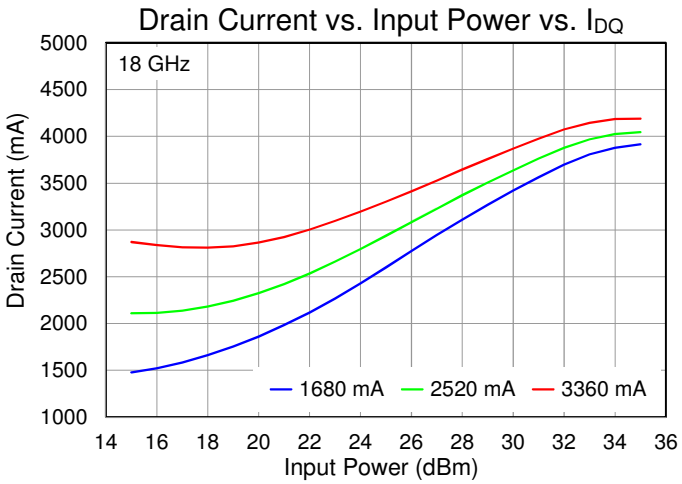
Test conditions unless otherwise noted: CW, V_D = 22 V, I_{DQ} = 3360 mA, P_{IN} = 31 dBm, T_{BASE} = +25 °C (T_{BASE} is backside of QPA2966)





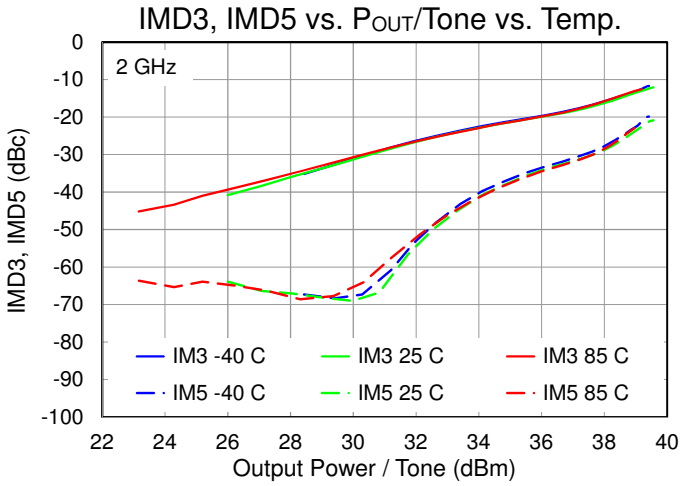


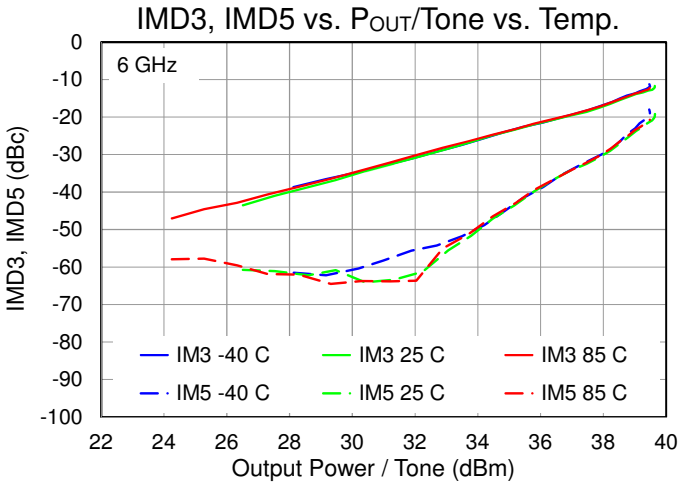


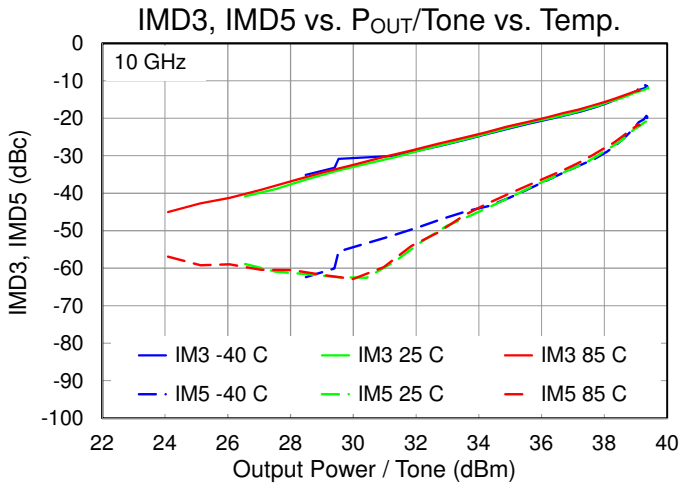


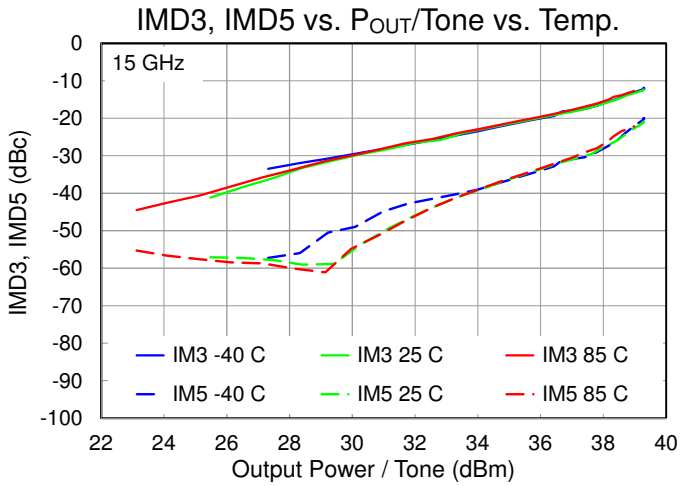
Performance Plots – Linearity

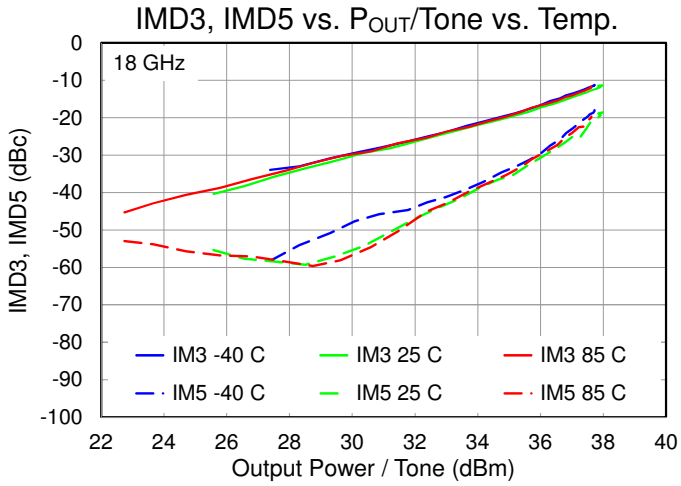
Test conditions unless otherwise noted: CW, V_D = 22 V, I_{DQ} = 3360 mA, Tone Spacing = 100 MHz, T_{BASE} = +25 °C (T_{BASE} is backside of QPA2966)







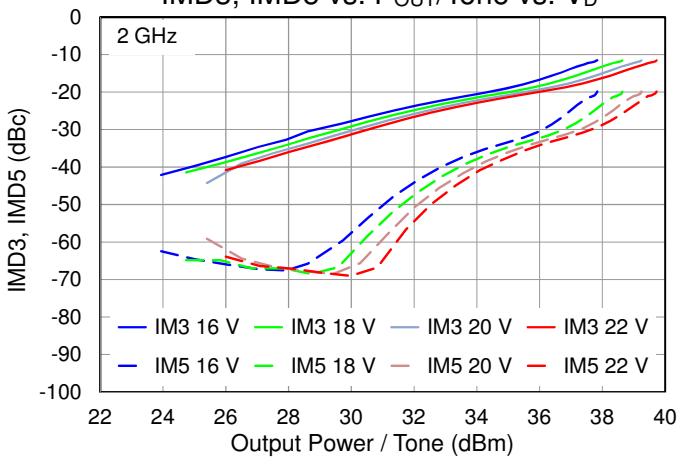




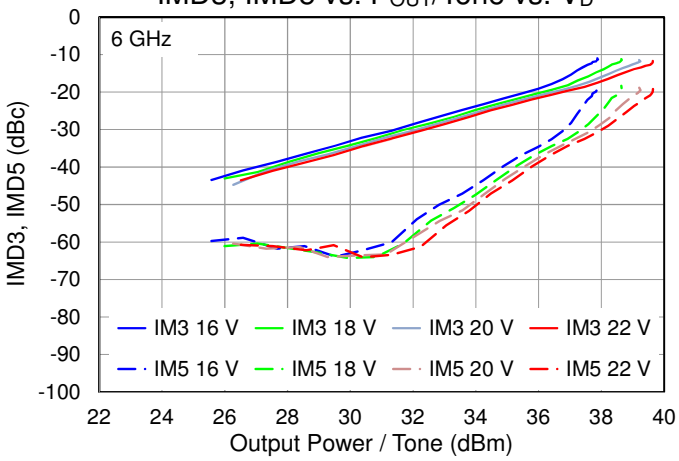
Performance Plots – Linearity

Test conditions unless otherwise noted: CW, V_D = 22 V, I_{DQ} = 3360 mA, Tone Spacing = 100 MHz, T_{BASE} = +25 °C (T_{BASE} is backside of QPA2966)

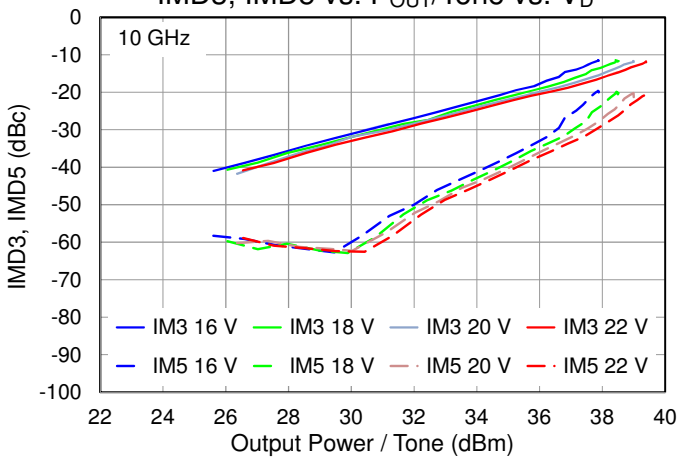
IMD3, IMD5 vs. P_{OUT}/Tone vs. V_D



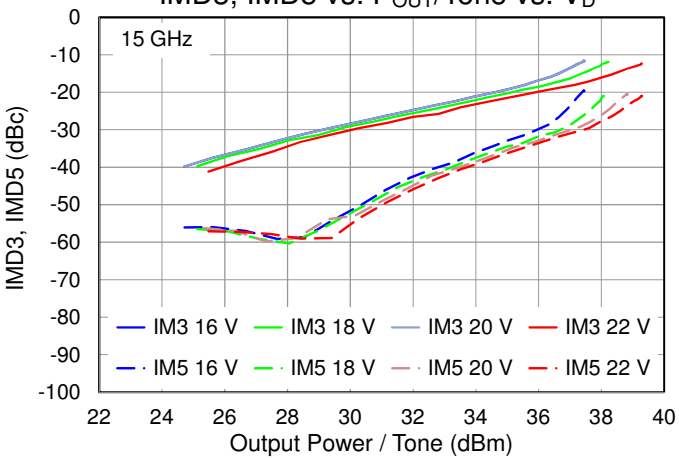
IMD3, IMD5 vs. P_{OUT}/Tone vs. V_D



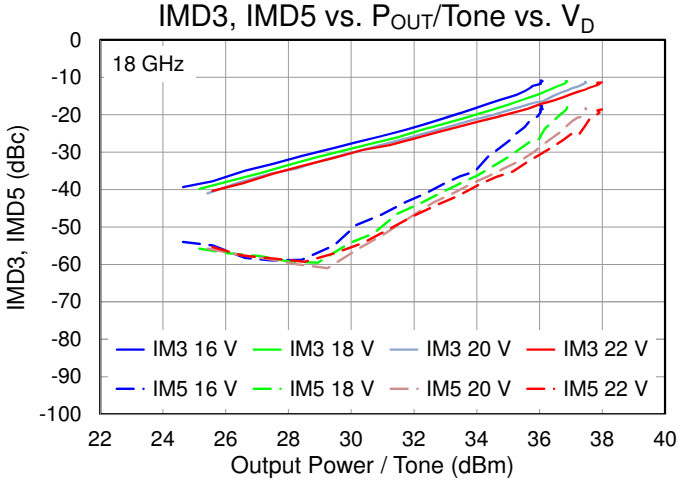
IMD3, IMD5 vs. P_{OUT}/Tone vs. V_D



IMD3, IMD5 vs. P_{OUT}/Tone vs. V_D

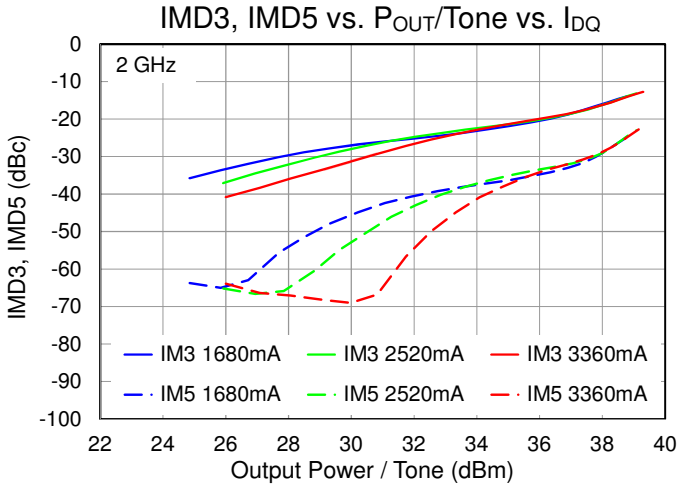


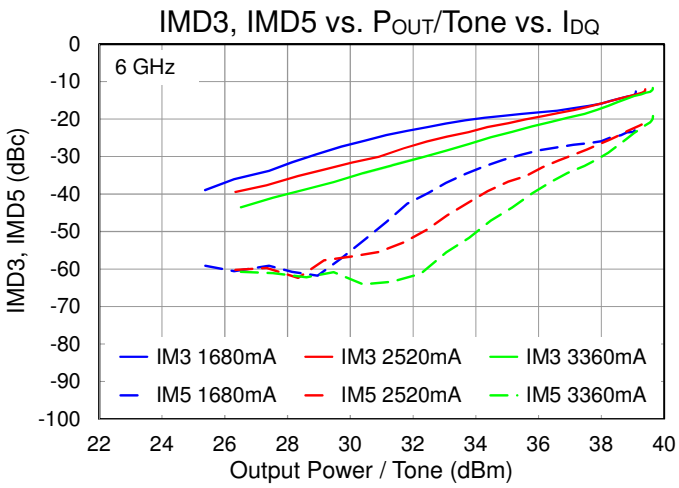
IMD3, IMD5 vs. P_{OUT}/Tone vs. V_D

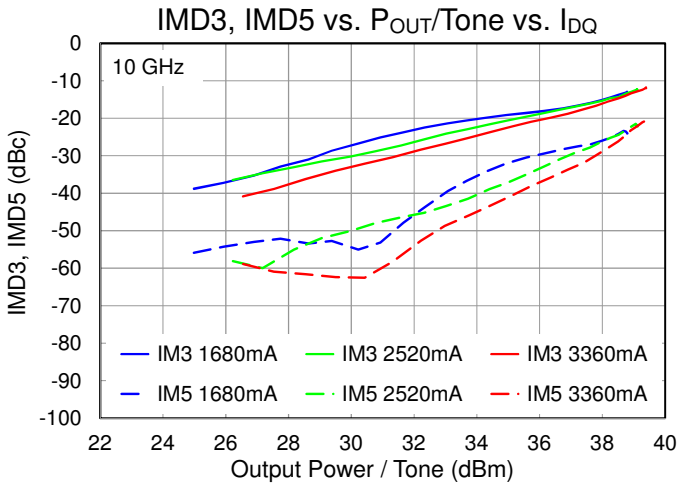


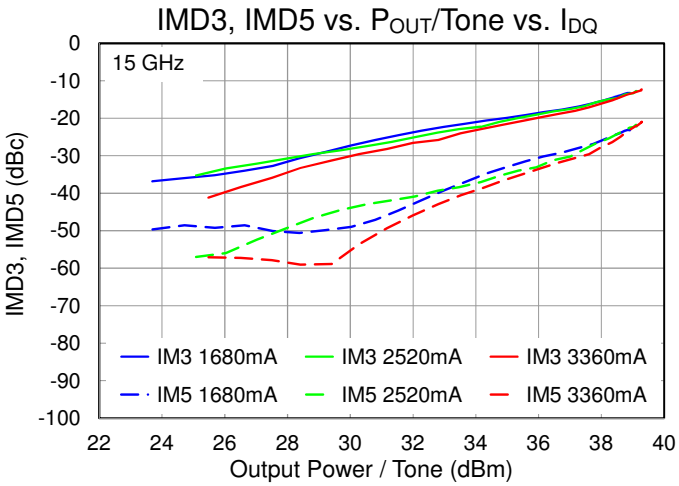
Performance Plots – Linearity

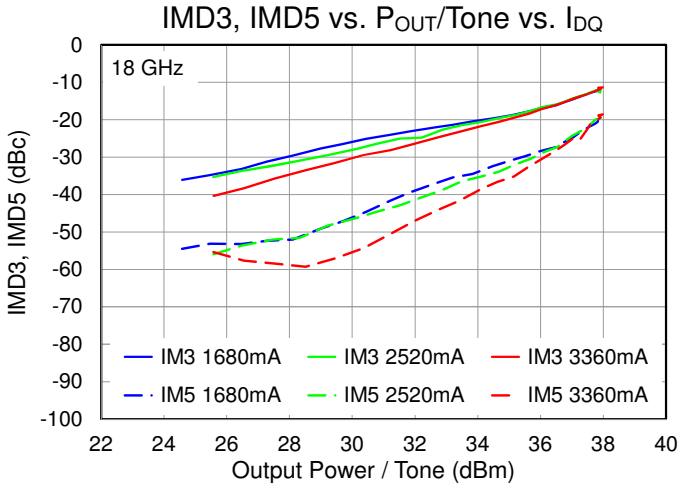
Test conditions unless otherwise noted: CW, V_D = 22 V, I_{DQ} = 3360 mA, Tone Spacing = 100 MHz, T_{BASE} = +25 °C (T_{BASE} is backside of QPA2966)







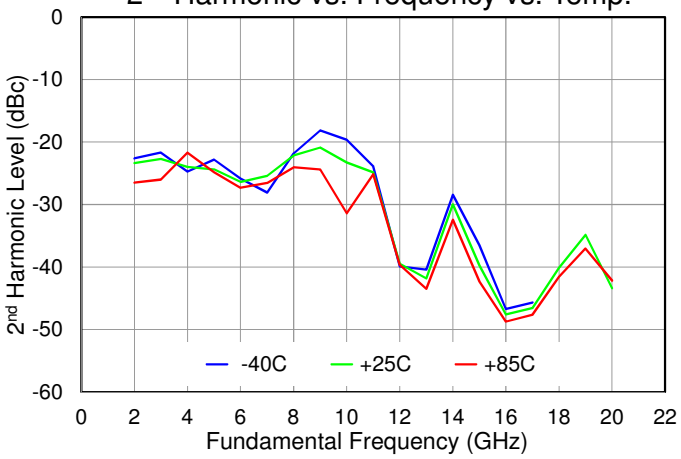




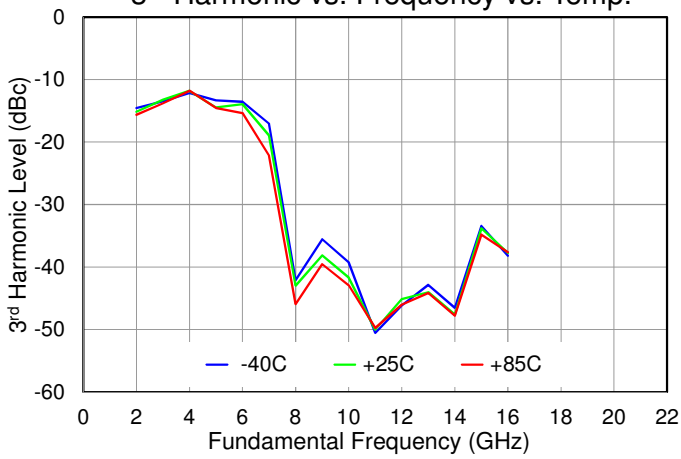
Performance Plots – Harmonics

Test conditions unless otherwise noted: CW, V_D = 22 V, I_{DQ} = 3360 mA, P_{IN} = 31 dBm, T_{BASE} = +25 °C (T_{BASE} is backside of QPA2966)

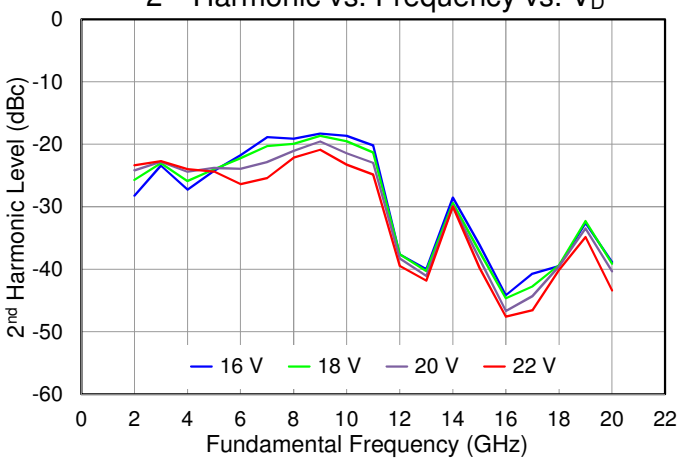
2nd Harmonic vs. Frequency vs. Temp.



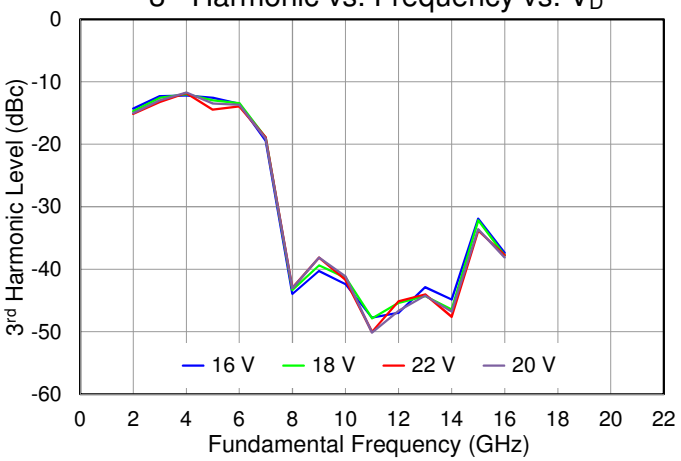
3rd Harmonic vs. Frequency vs. Temp.



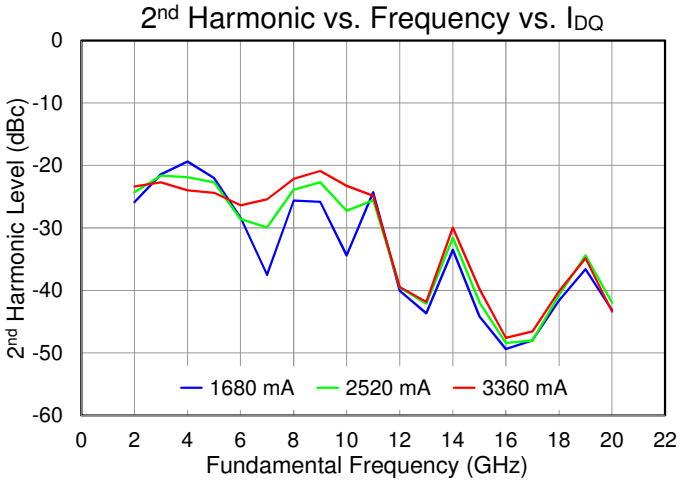
2nd Harmonic vs. Frequency vs. V_D



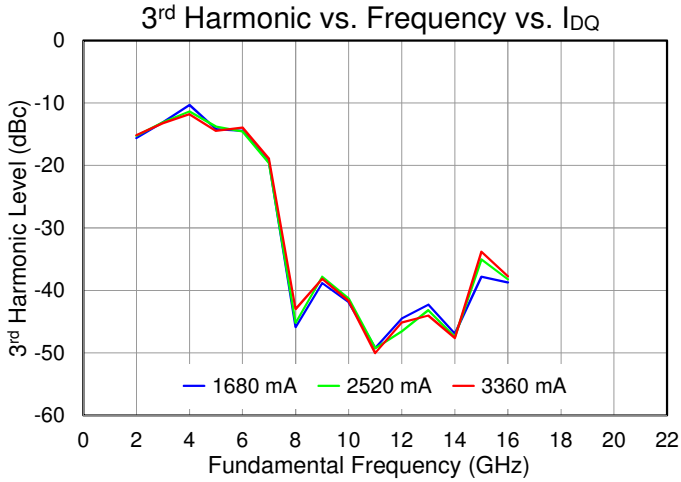
3rd Harmonic vs. Frequency vs. V_D



2nd Harmonic vs. Frequency vs. I_{DQ}



3rd Harmonic vs. Frequency vs. I_{DQ}



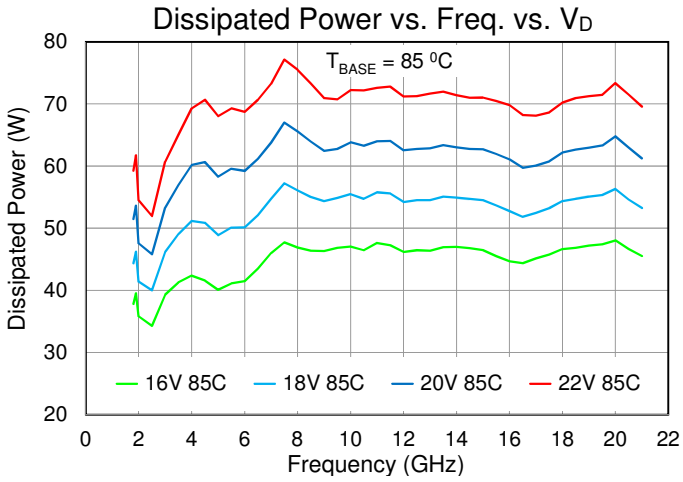
Thermal and Reliability Information

Parameter	Test Conditions	Value	Units
Thermal Resistance (θ_{JC}) (1)	T_{BASE} = 85 °C, V_D = 22 V, I_{DQ} = 3360 mA, No RF (quiescent DC operation) P_{DISS} = 74 W	1.28	ºC/W
Channel Temperature, T_{CH} (Under RF) (2)		180	°C
Thermal Resistance (θ_{JC}) (1)	T_{BASE} = 85 °C, CW, V_D = 22 V, I_{DQ} = 3360 mA, Freq = 7.5 GHz, I_{D_Drive} = 4525 mA, P_{IN} = 31 dBm, P_{OUT} = 43.7 dBm P_{DISS} = 77 W	1.55	ºC/W
Channel Temperature, T_{CH} (Under RF) (2)		204	°C

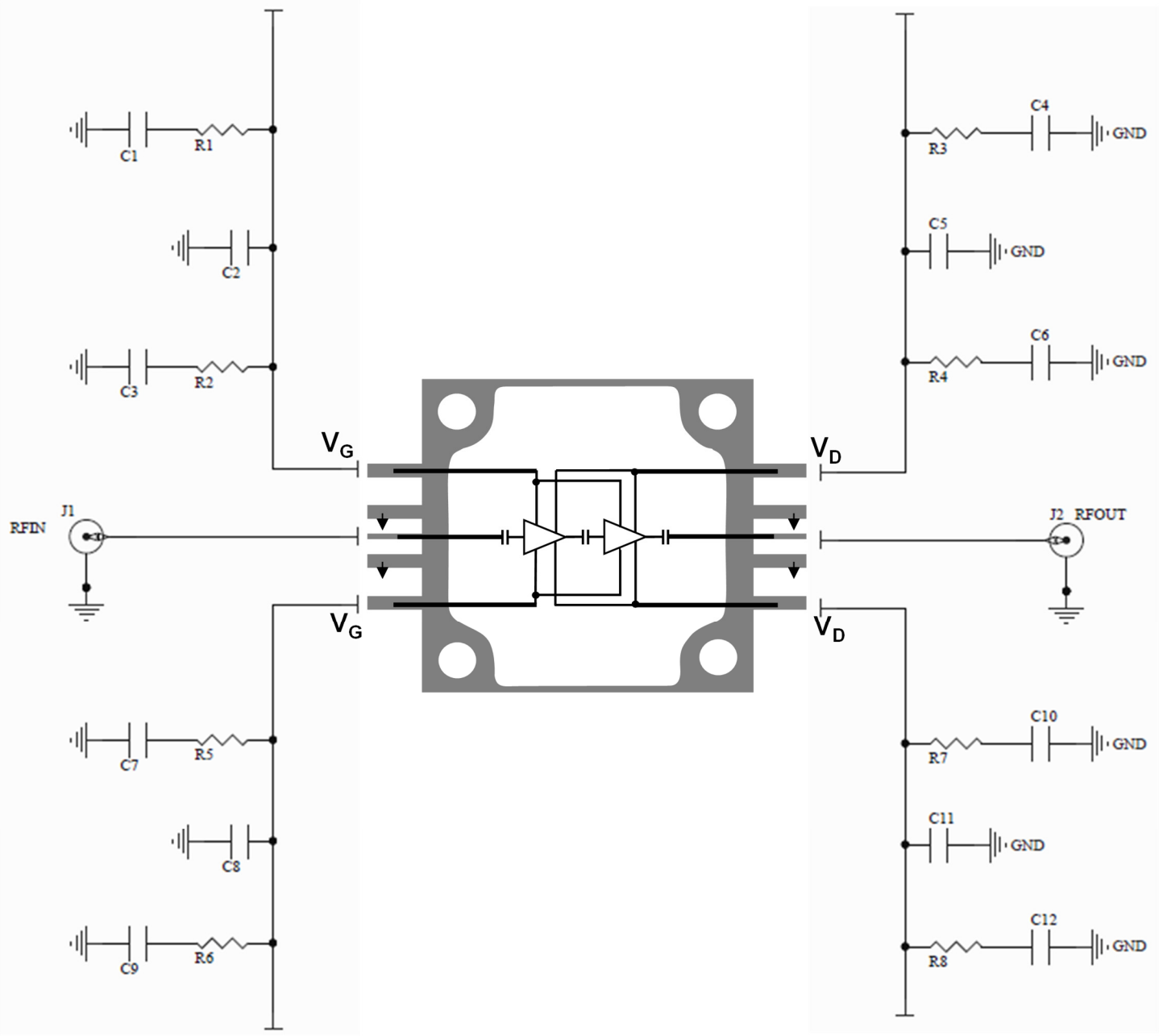
Notes:
1. Thermal resistance determined to the back of package T_{BASE} = 85 °C
2. Channel temperature indicated is an IR scan equivalent temperature. Thermal resistance is calculated using this value. Additional information can be found in the Qorvo Applications Note “GaN Device TCHMAX Theta-JC and Reliability Estimates”, located here https://www.qorvo.com/products/d/da006480

Dissipated Power

Test conditions, unless otherwise noted:
V_D = 22 V, I_{DQ} = 1680 mA, T_{BASE} = 25 °C, P_{IN} = 27 dBm



Applications Circuit



Tie all V_G together, tie all V_D together

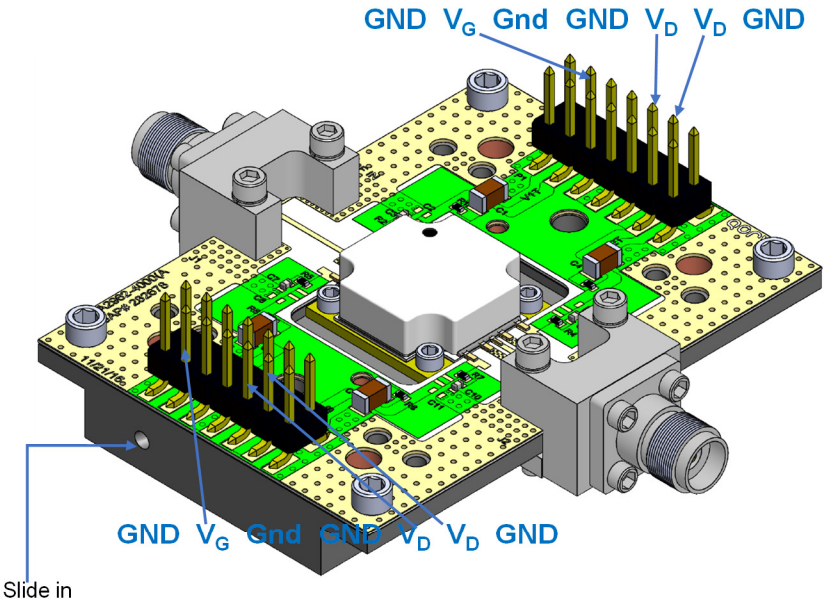
Bias-Up Procedure

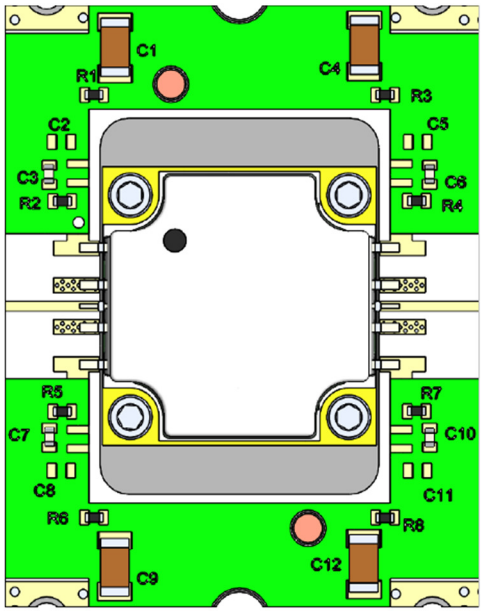
1. Set I_D limit to 5500 mA, I_G limit to 20 mA
2. Set V_G to –4 V
4. Set V_D +22 V
5. Adjust V_G more positive until I_{DQ} = 3360 mA
6. Apply RF signal

Bias-Down Procedure

1. Turn off RF signal
2. Reduce V_G to –4.0 V. Ensure I_{DQ} ~ 0mA
3. Set V_D to 0 V
4. Turn off V_D supply
5. Turn off V_G supply

Application Evaluation Board





Layer Stack Legend (Copper Thickness is Finished Copper Thickness)

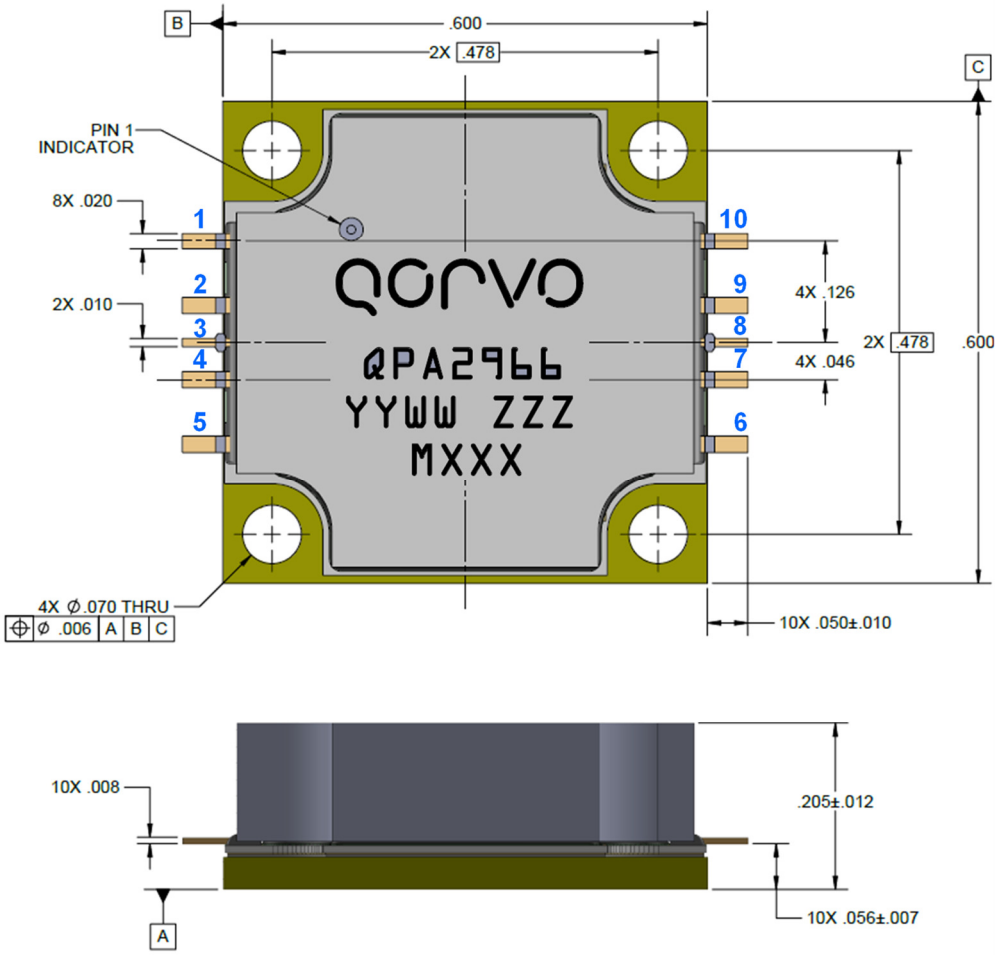
Material	Layer	Thickness	Dielectric Material	Type
	Silkscreen_Top			Legend
Surface Material	Soldermask_Top	0.10mil	Solder Resist	Solder Mask
Copper	Metal1_Top	1.40mil		Signal
Core		10.00mil	ROGERS 6035HTC	Dielectric
Copper	Metal2_Bot	1.40mil		Signal

Total thickness: 12.90mil

Bill of Materials

Reference Des.	Value	Description	Manuf.	Part Number
C3, C6, C7, C10	0.01uF	CAP, 0.01uF, ±10%, 50V, X7R, 0402	Various	
C1, C4, C9, C12	10 uF	CAP, 10uF, ±20%, 50V, X5R, 1206	Various	
R2, R4, R5, R7	0 Ω	RES, 0 OHM, JMPR, 0402	Various	
R1, R3, R6, R8	5.1 Ω	RES, 5.1 OHM, 5%, 50V, 0402	Various	
R5	0 Ω	RES, 0 OHM, 0.1W, 0603	Various	
H1, H2	-	Header, Connector, 2x7, SMD	TE Connectivity	5-146130-6
J1, J2	-	Connector, Female, End Launch, 2.9mm	Southwest Microwave	1092-01A-5
S5 – S8	-	Screw, cap, socket head, 2-56x1/8”	Various	
S1 – S4	-	Screw, cap, socket head, 0-80x3/32”	Various	
PCB	-	Rogers 4035HTC 8 mil dielectric, 1 oz. copper (gold plated), 2 layers; finished thickness 0.013”	Qorvo	Custom
Carrier	-	T-Carrier, Copper C110, 1.594 x 2.200 x 0.275”	Qorvo	Custom
Arctic Silver	-	Chem, Thermal Compound, Silver 5GR	Arctic Silver	AS5-5G
Epoxy	-	Preform, Epoxy 5025E 10 x 12 x 0.003”	Various	
Solder	-	Paste, solder, Sn63/Pb37	Various	

Mechanical and Marking



Notes:

1. **Materials:**
   - Base : Copper
   - Finish: Gold
   - Leads : Alloy 194
   - Lid : FR4
2. **Part is epoxy sealed**
3. **Marking:**
   - QPA2966: Part number
   - YY: Part assembly year
   - WW: Part assembly week
   - ZZZ: Serial number
   - MXXX: Batch ID
4. **Dimensions: inches**
5. **Tolerances:**
   - .XX: ± 0.01
   - .XXX: ± 0.005
   - .XXXX: ± 0.0010
   - Angles: ± 0.5 °

Pin Description

Pin Number	Symbol	Description
1, 5	V_G	Gate voltage, stage 1 and 2. Must be biased on both pins; bypass network required; refer to page 22.
2, 4, 7, 9	Ground	Must be grounded to PCB
3	RF_{IN}	RF input. 50 Ohms. DC blocked.
6, 10	V_D	Drain voltage, stage 1 and 2. Must be biased on both pins; bypass network required; refer to page 22.
8	RF_{OUT}	RF output. 50 Ohms. DC blocked.

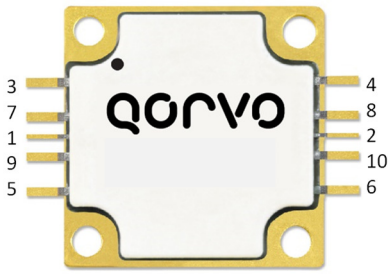
Assembly Notes

1. Carefully clean the PC board, base plate, and package leads with alcohol. Allow it to dry fully.

2. To improve the thermal and RF performance, Qorvo recommends attaching a heat sink to the bottom of the package and apply either a thermal compound (Arctic Silver 5 recommended) or a .004 inch (maximum thickness) Indium shim between the heat sink and the package. Refer to the applications note Application of Arctic Silver 5 Thermal Compound and Indium Shims for Qorvo CP-style Packaged Components for more information.

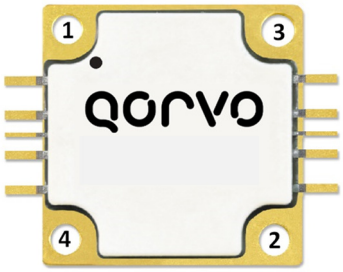
3. The component leads should be manually soldered. Apply a low residue solder alloy meeting J-STD-001 (ROL0, ROL1 or equivalent) with a liquidus temperature below 220 °C to each pin of the TGA/QPA/QPMxxxx. The use of low residue/no-clean flux (ROL0, ROL1) is recommended. The package lead temperature should not exceed 260 deg C. Each solder connection should be completed within 2 to 5 seconds. Adding flux during hand soldering of the component leads with localized spot cleaning is acceptable. Soldering irons meeting the requirements of J-STD-001, Appendix A are acceptable.

4. The leads should be soldered in a staggered or star pattern from side to side, and never solder two adjacent leads. This allows the heat to dissipate on each lead, and not cause the adjacent leads to become de-soldered and damaged or displaced.



5. The packaged part should not be subjected to conventional SMT automated solder reflow processes.

6. (The following is for information only. There are many variables in a second level assembly that Qorvo does not control, so Qorvo does not recommend an absolute torque value.) Use screws to attach the component to the heat sink. A suggested final torque value is 16 in-oz. for a 0-80 screw. Start with screws finger tight, then torque to 8 in-oz., then torque to final value. Use the following tightening pattern:



Handling Precautions

Parameter	Rating	Standard
ESD – Human Body Model (HBM)	1C	ANSI/ESD/JEDEC JS-001
ESD – Charged Device Model (CDM)	C3	ANSI/ESD/JEDEC JS-002
MSL – Moisture Sensitivity Level	N/A	Blank, null, no content

Caution!
ESD-Sensitive Device

Solderability

The component leads should be manually soldered, and the package cannot be subjected to conventional reflow processes. The use of no-clean solder to avoid washing after soldering is recommended.

RoHS Compliance

This product is compliant with the 2011/65/EU RoHS directive (Restrictions on the Use of Certain Hazardous Substances in Electrical and Electronic Equipment), as amended by Directive 2015/863/EU.

This product also has the following attributes:

- Lead Free
- Antimony Free
- TBBP-A ($C_{15}H_{12}Br_40_2$) Free
- SVHC Free
- PFOS Free

Contact Information

For the latest specifications, additional product information, worldwide sales and distribution locations:

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