QPA4246D

37.5 – 42.5 GHz 10 Watt GaN Power Amplifier

Product Overview

Qorvo's QPA4246D is a high power MMIC amplifier fabricated on Qorvo's production 0.15 um GaN on SiC process (QGaN15). It is targeted to the 37.5 - 42.5 GHz Satcom Q-V band. QPA4246D achieves 5 W linear power with 25 dBc third order intermodulation distortion products, and 16 dB small signal gain. It provides 10 W of saturated output power while achieving 17% power-added efficiency.

To simplify system integration, the QPA4246D is fully matched to 50 ohms with integrated DC blocking caps on both I/O ports. Its RF ports are DC coupled to ground for optimum ESD performance.

The QPA4246D is ideal for supporting communications and radar applications in both commercial and military markets.

The QPA4246D is 100% DC and RF tested on-wafer to ensure compliance to electrical specifications.

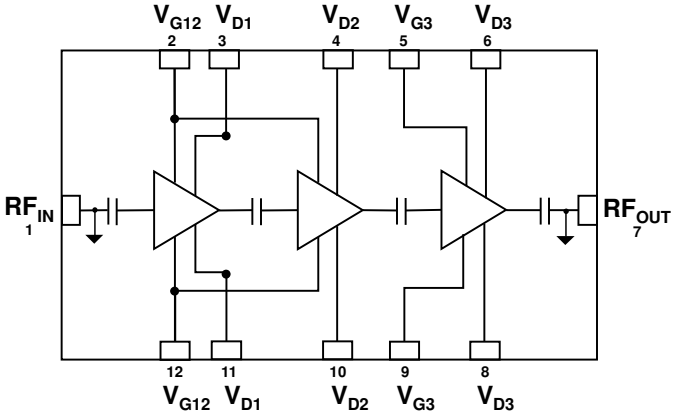
Lead-free and RoHS compliant

Key Features

- Frequency Range: 37.5 – 42.5 GHz
- P_{SAT} (P_{IN} = 29 dBm): 40 dBm
- PAE (P_{IN} = 29 dBm): 17%
- IM3 (P_{OUT}/Tone = 34 dBm): -25 dBc
- Small Signal Gain: 16 dB
- Bias: V_D = 24 V, I_{DQ} = 280 mA, V_G = -2.3 V typ. range
- Die Dimensions: 4.2 x 5.0 x 0.05 mm

Performance is typical across frequency. Please reference electrical specification table and data plots for more details.

Functional Block Diagram



Applications

- Satellite Communications

Ordering Information

Part No.	Description
QPA4246D	10 Watt GaN PA
QPA4246DEVB	Evaluation Board for QPA4246D

Absolute Maximum Ratings

Parameter	Value / Rang
Drain Voltage (V_D)	29.5 V
Gate Voltage Range (V_G)	-4 V to 0 V
Drain Current (I_{D1}), T_{BASE} = 85 °C max	510 mA
Drain Current (I_{D2}), T_{BASE} = 85 °C max	900 mA
Drain Current (I_{D3}), T_{BASE} = 85 °C max	3450 mA
Drain Current Total (I_D), T_{BASE} = 85 °C max	4860 mA
Gate Current (I_G)	See p. 25
Power Dissipation (P_{DISS}), T_{BASE} = 85 °C	70 W
Input Power (P_{IN}), 50 Ω, CW, V_D = 24 V, I_D = 280 mA, T_{BASE} = 85 °C	35 dBm
Input Power (P_{IN}), 3:1 VSWR, CW, V_D = 24 V, I_D = 280 mA, T_{BASE} = 85 °C	35 dBm
Mounting Temperature (30 seconds)	320 ºC
Storage Temperature	-55 to +150 ºC

Operation of this device outside the parameter ranges given above may cause permanent damage. These are stress ratings only, and functional operation of the device at these conditions is not implied.

Recommended Operating Conditions

Parameter	Min	Typ.	Max	Units
Drain Voltage (V_D)	20	24	24	V
Drain Current, Quiescent (I_D)	280	280		mA
Drain Current, RF (I_{D_Drive})	See plot page 4,5,8,11,14			mA
Gate Voltage Typical Range (V_G)	–1.7 to -2.9			V
Gate Current, RF (I_{G_Drive})	See plot page 4,5			mA
Input Power @ Saturation, (P_{IN})(1)	T_{BASE} -40 °C : 29			dBm
	T_{BASE} +25 °C: 29			
	T_{BASE} +85 °C: 31			
Operating Temp. Range (T_{BASE})(2)	–40		+85	ºC

1. See plots page 6
2. T_{BASE} is back side of 0.02” CuMo carrier plate with AuSn solder

Electrical specifications are measured at specified test conditions. Specifications are not guaranteed over all recommended operating conditions.

Electrical Specifications

Parameter	Conditions (1) (2)	Min	Typ.	Max	Units
Operational Frequency Range		37.5		42.5	GHz
Output Power at Saturation, P_{SAT}	P_{IN} = 29 dBm		40		dBm
Power Added Efficiency, PAE	P_{IN} = 29 dBm		17		%
3RD Intermodulation Products, IM3	P_{OUT}/Tone = 34 dBm		-25		dBc
5RD Intermodulation Products, IM5	ΔF = 100 MHz		-30		
Small Signal Gain, S21	P_{IN} = -30 dBm		16		dB
Input Return Loss, IRL			10		
Output Return Loss, ORL			10		
P_{SAT} Temperature Coefficient	T_{DIFF} = 25 ºC to 85 ºC; P_{IN} = 29 dBm		-0.05		dBm/ºC
S21 Temperature Coefficient	T_{DIFF} = 25 ºC to 85 ºC		-0.10		dB/ºC

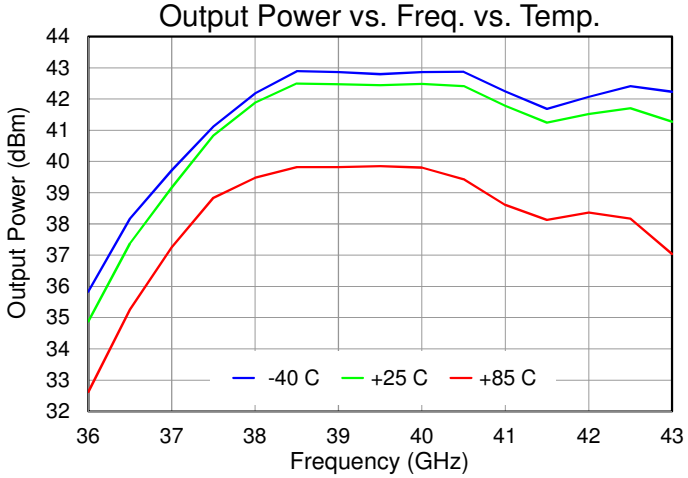
Notes:

1. Test conditions unless otherwise noted: CW, V_D = 24 V, I_D = 280 mA, V_G = -2.3 V +/- 0.6V typical, T_{BASE} = 25ºC, Z_0 = 50 Ω
2. T_{BASE} is back side of 0.02 in CuMo carrier plate with AuSn die attached

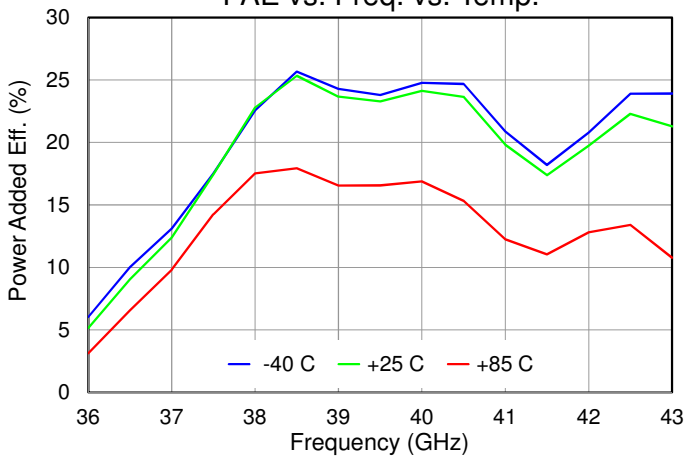
Performance Plots – Large Signal

Test conditions, unless otherwise noted: CW, V_D = 24 V, I_{DQ} = 280 mA, P_{IN} = 29 dBm, T_{BASE} = +25 ºC (T_{BASE} is backside of 0.02 in CuMo carrier plate)

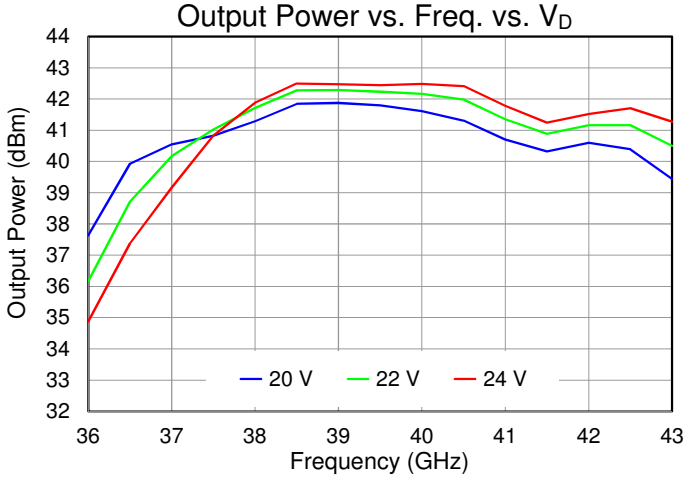
Output Power vs. Freq. vs. Temp.



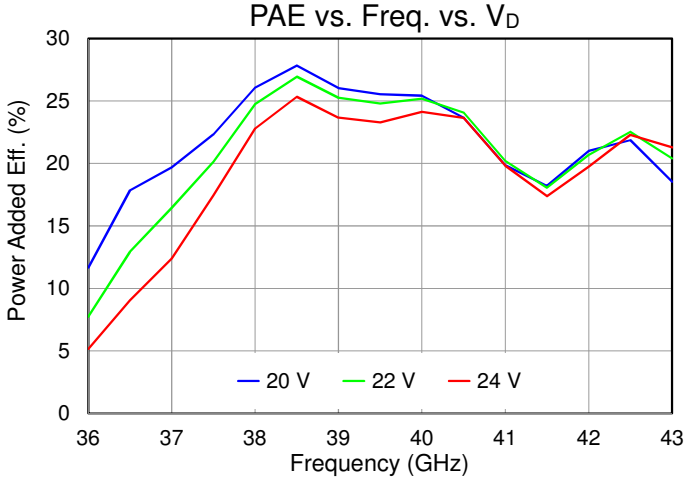
PAE vs. Freq. vs. Temp.



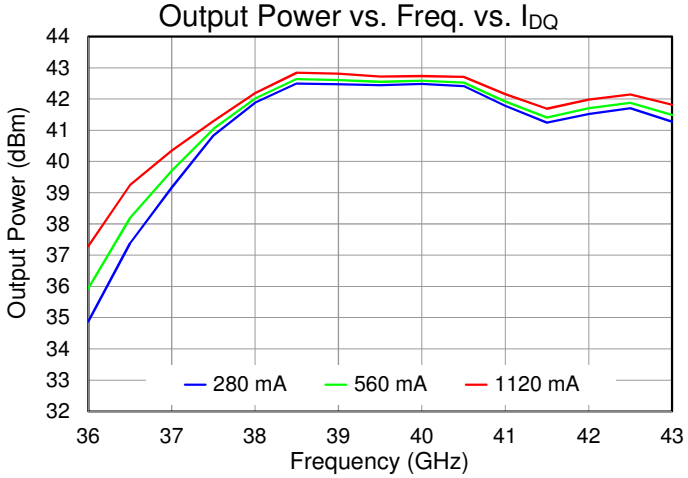
Output Power vs. Freq. vs. V_D



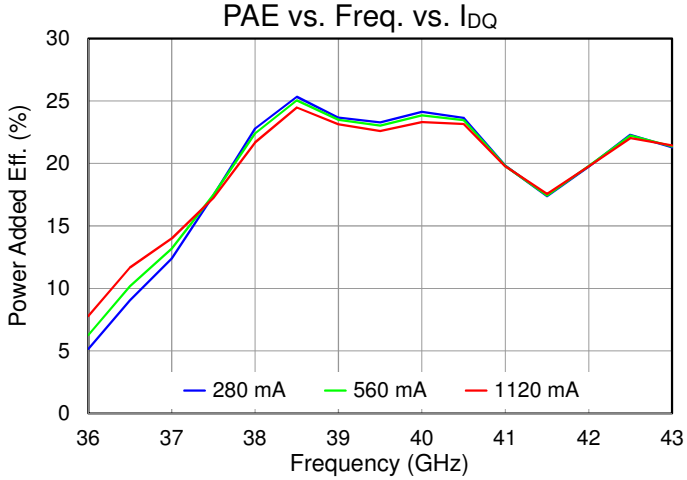
PAE vs. Freq. vs. V_D



Output Power vs. Freq. vs. I_{DQ}



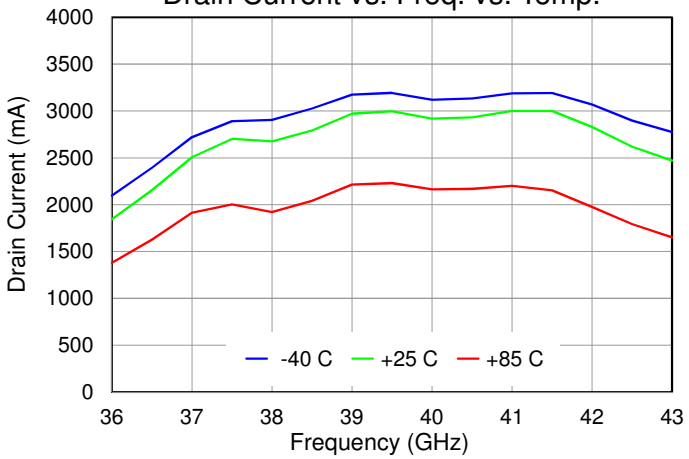
PAE vs. Freq. vs. I_{DQ}



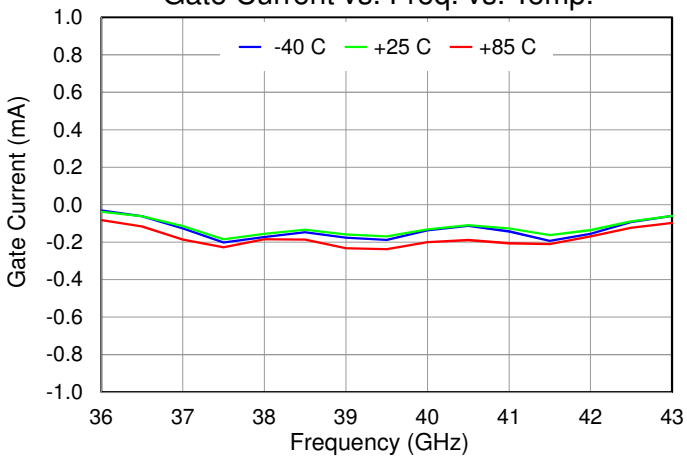
Performance Plots – Large Signal

Test conditions, unless otherwise noted: CW, V_D = 24 V, I_{DQ} = 280 mA, P_{IN} = 29 dBm, T_{BASE} = +25 ºC (T_{BASE} is backside of 0.02 in CuMo carrier plate)

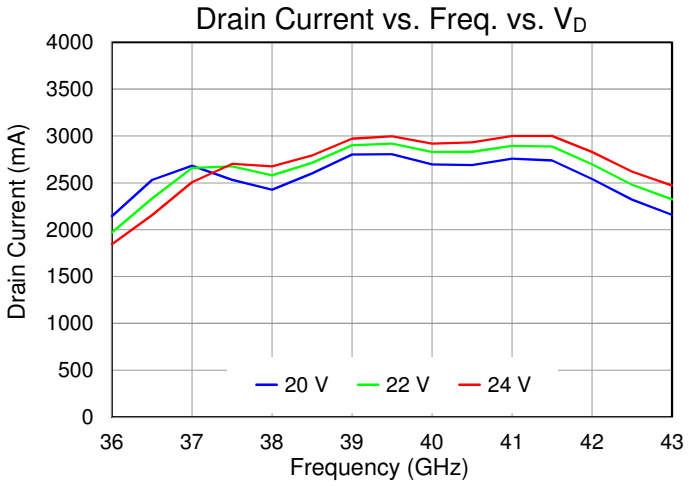
Drain Current vs. Freq. vs. Temp.



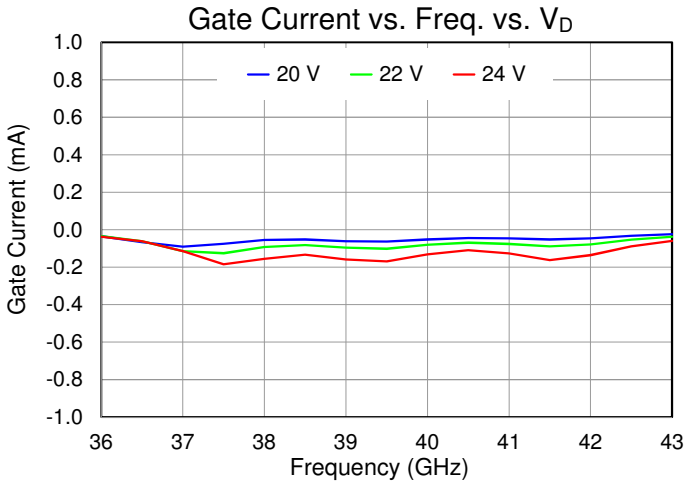
Gate Current vs. Freq. vs. Temp.



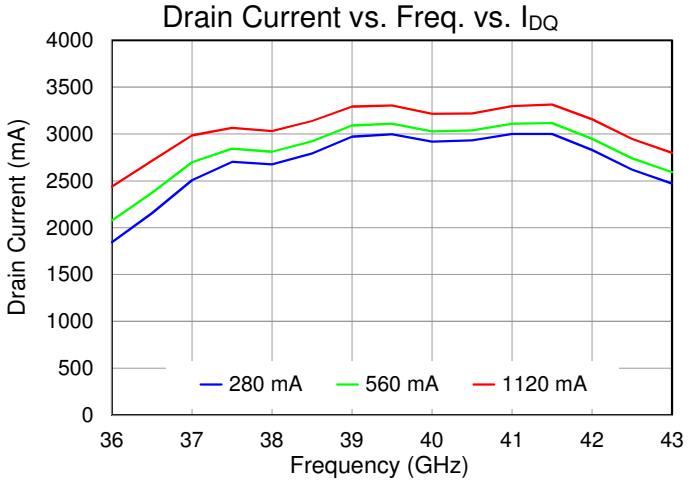
Drain Current vs. Freq. vs. V_D



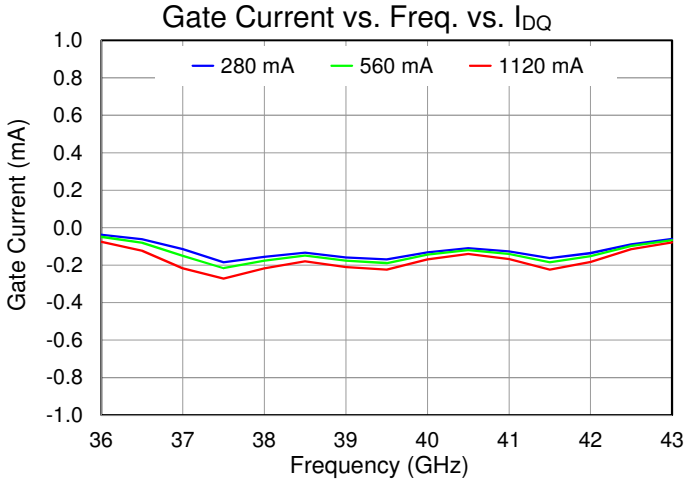
Gate Current vs. Freq. vs. V_D



Drain Current vs. Freq. vs. I_{DQ}



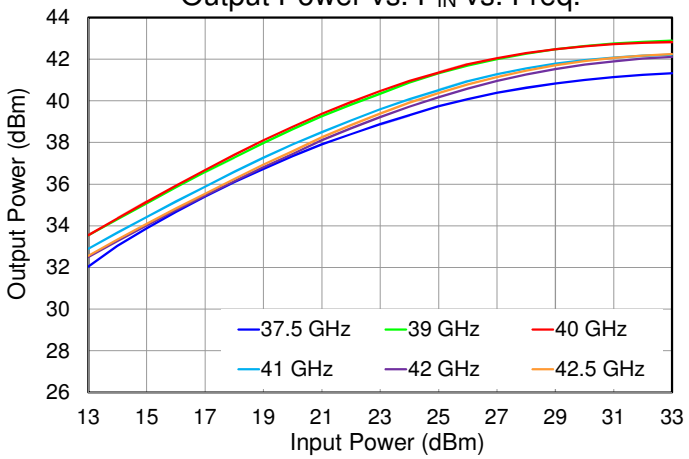
Gate Current vs. Freq. vs. I_{DQ}



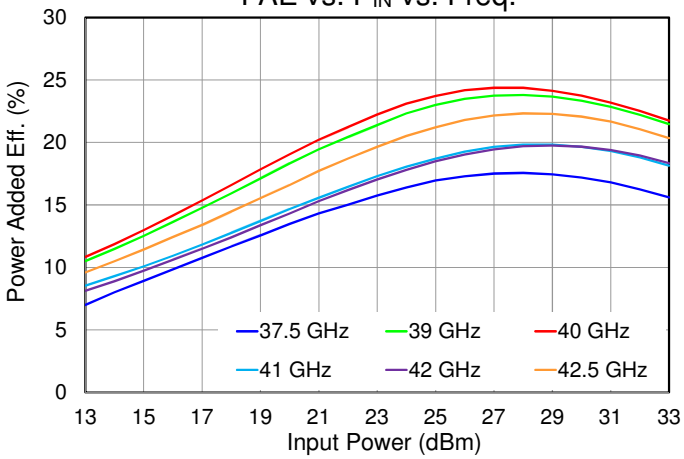
Performance Plots – Large Signal

Test conditions, unless otherwise noted: CW, V_D = 24 V, I_{DQ} = 280 mA, P_{IN} = 29 dBm, T_{BASE} = +25 ºC (T_{BASE} is backside of 0.02 in CuMo carrier plate)

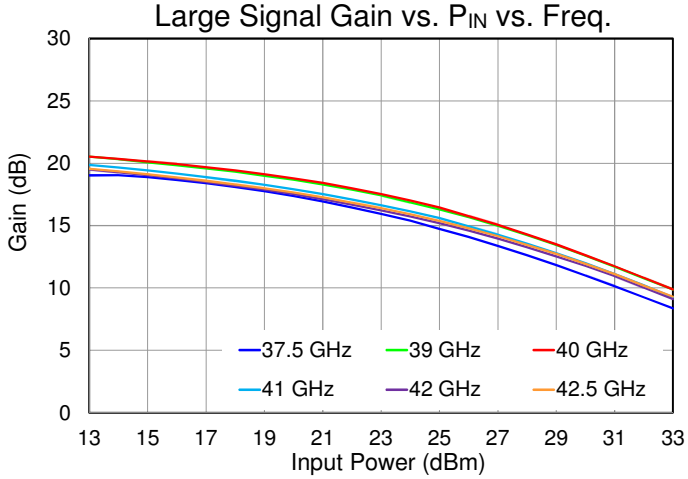
Output Power vs. P_{IN} vs. Freq.



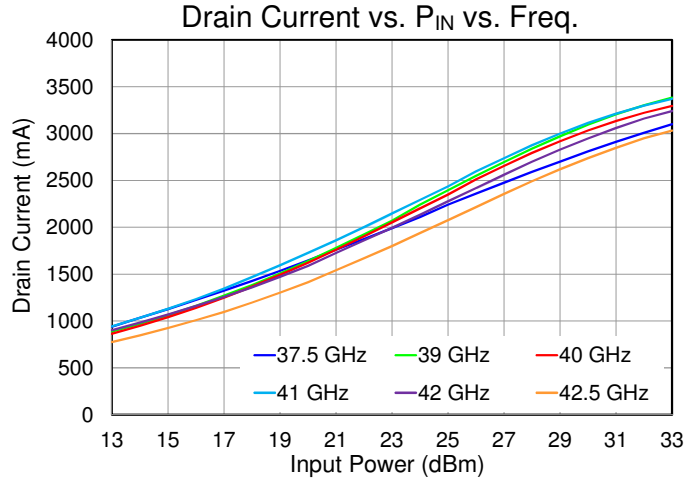
PAE vs. P_{IN} vs. Freq.



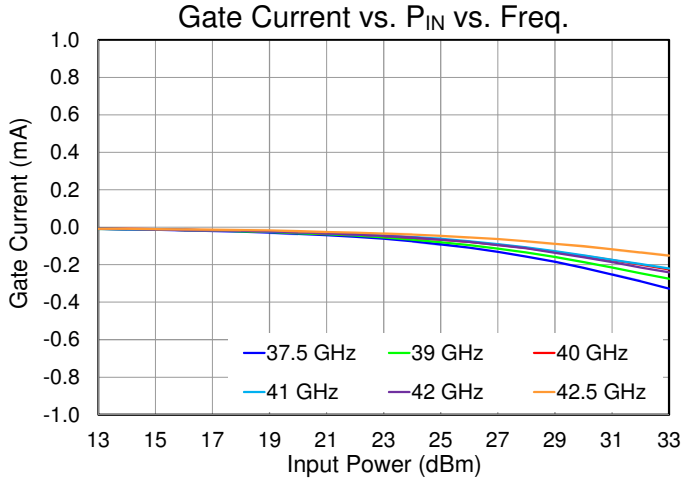
Large Signal Gain vs. P_{IN} vs. Freq.



Drain Current vs. P_{IN} vs. Freq.



Gate Current vs. P_{IN} vs. Freq.



Performance Plots – Large Signal

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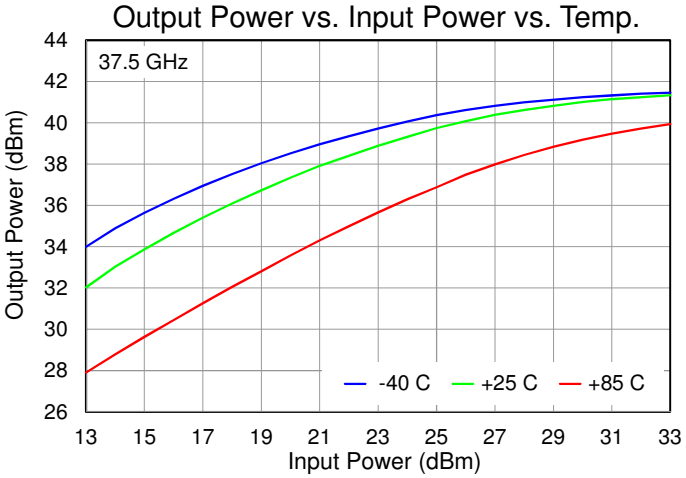
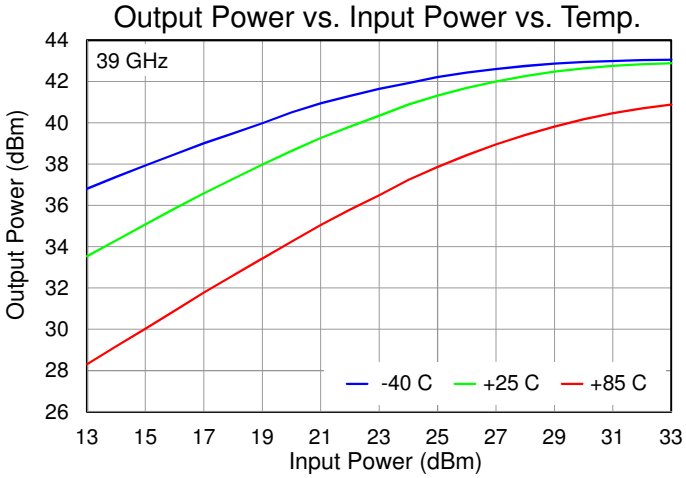
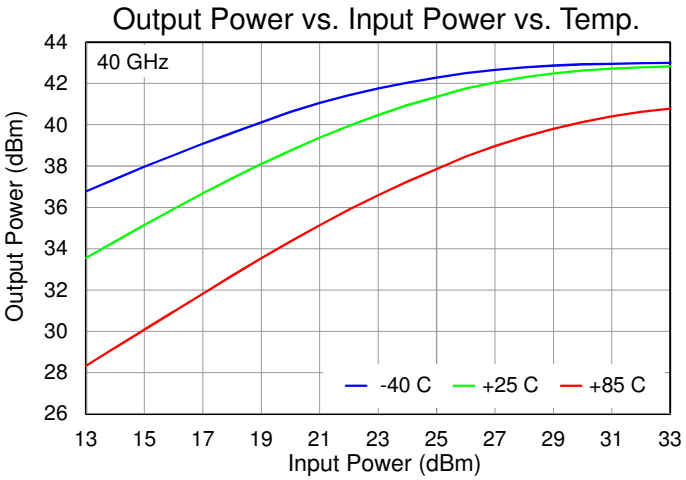
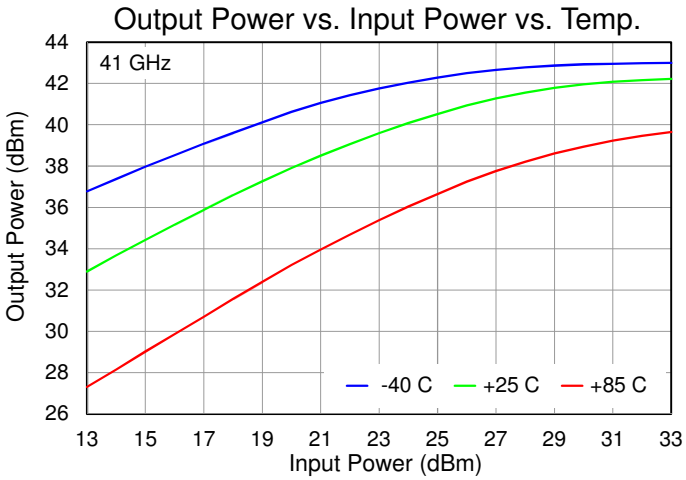
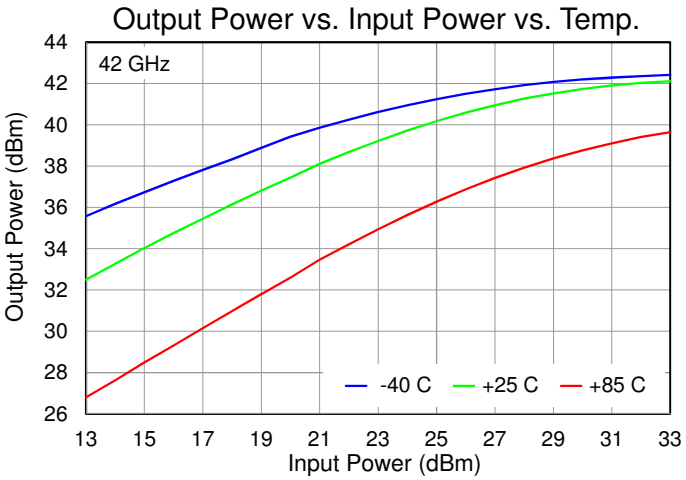
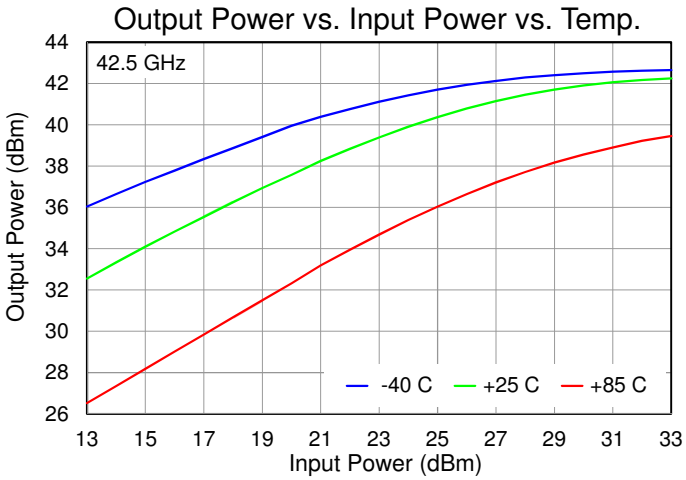






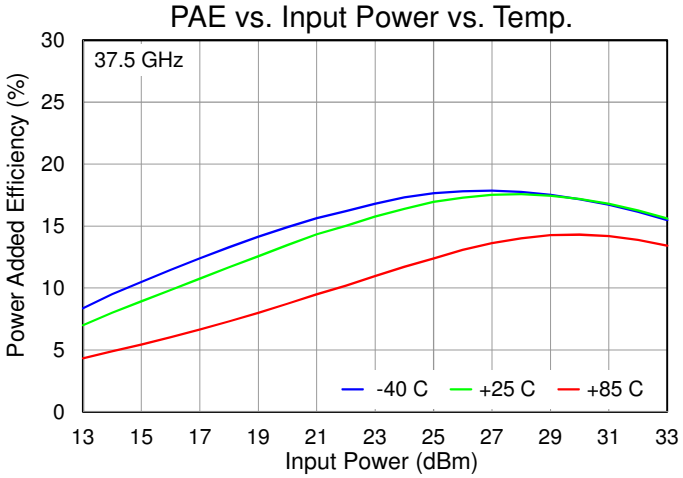


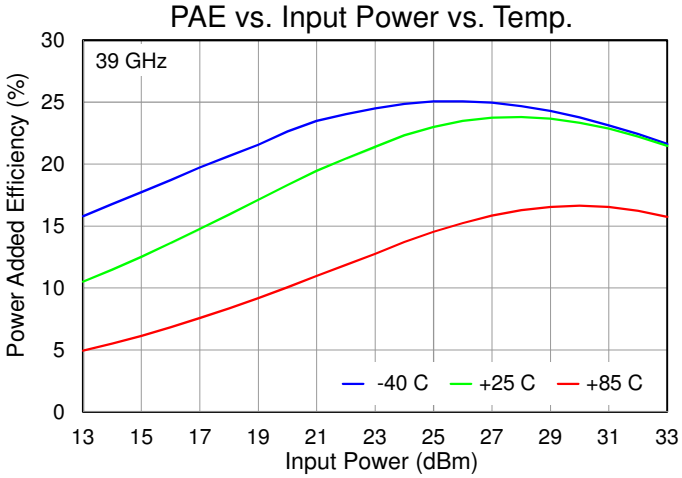


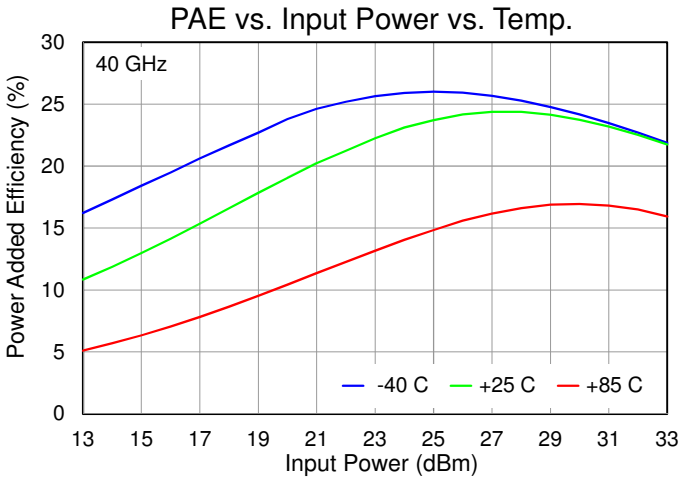


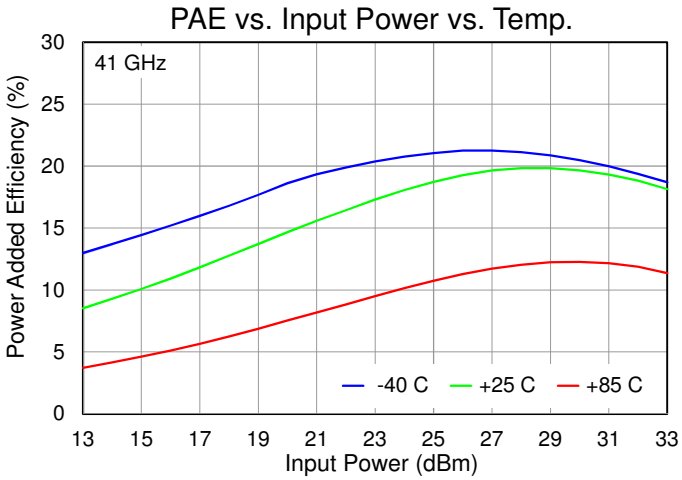
Performance Plots – Large Signal

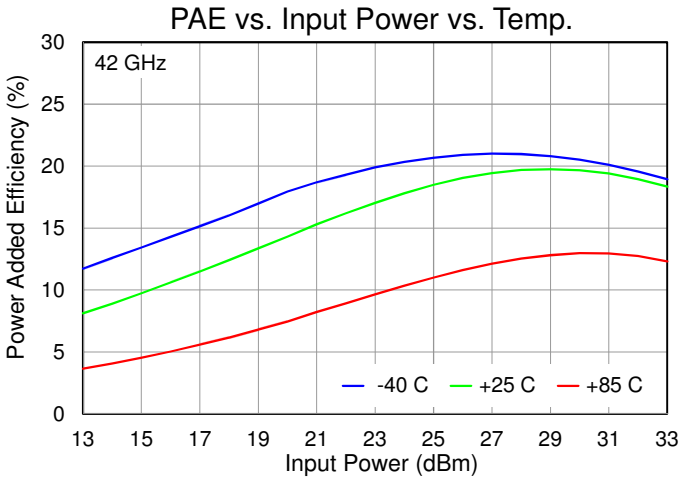
Test conditions, unless otherwise noted: CW, V_D = 24 V, I_{DQ} = 280 mA, P_{IN} = 29 dBm, T_{BASE} = +25 ºC (T_{BASE} is backside of 0.02 in CuMo carrier plate)

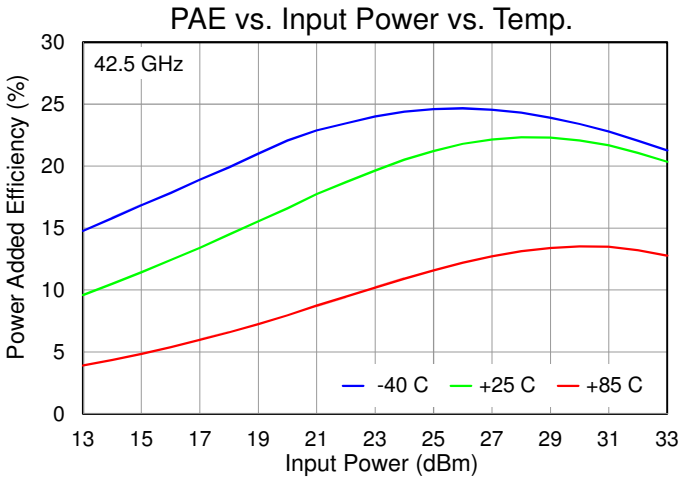






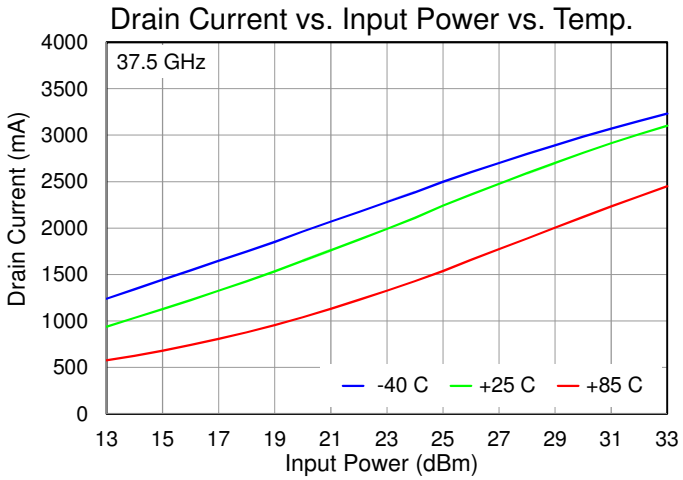


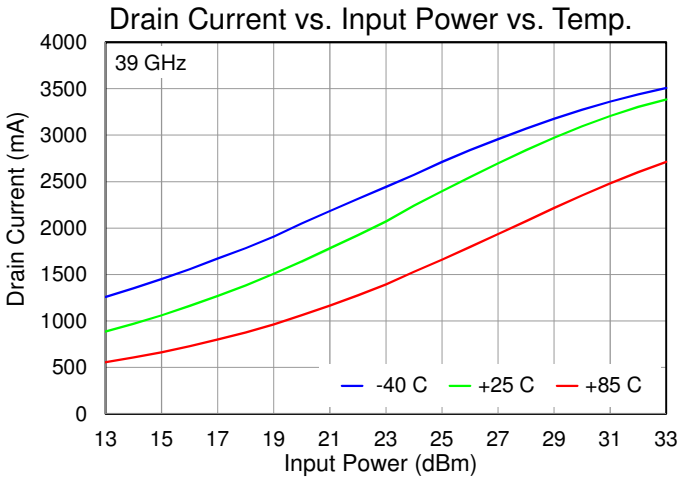


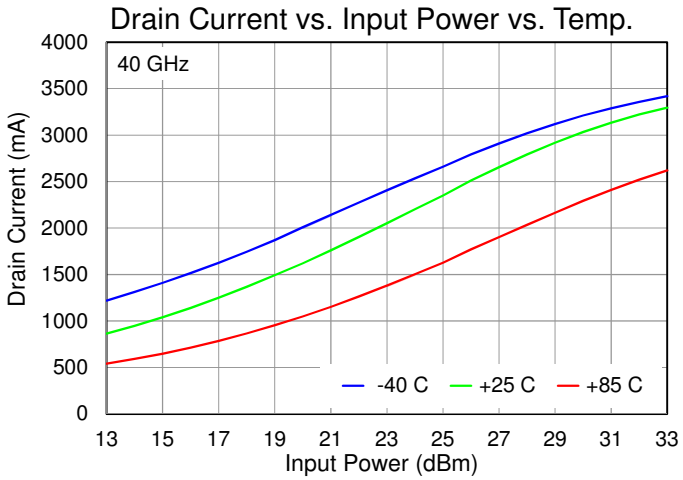


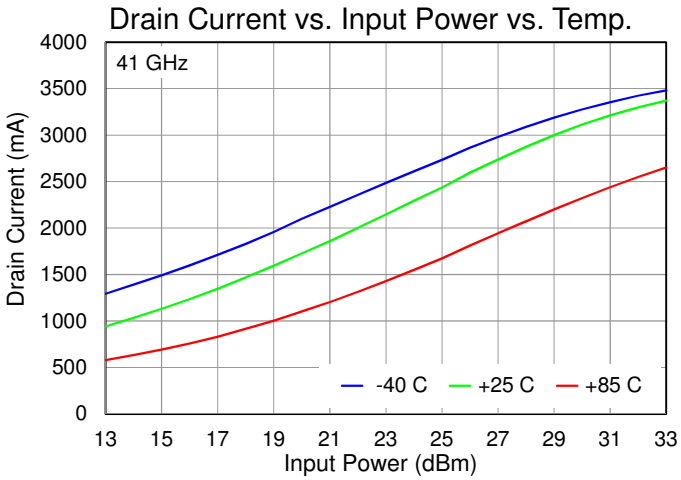
Performance Plots – Large Signal

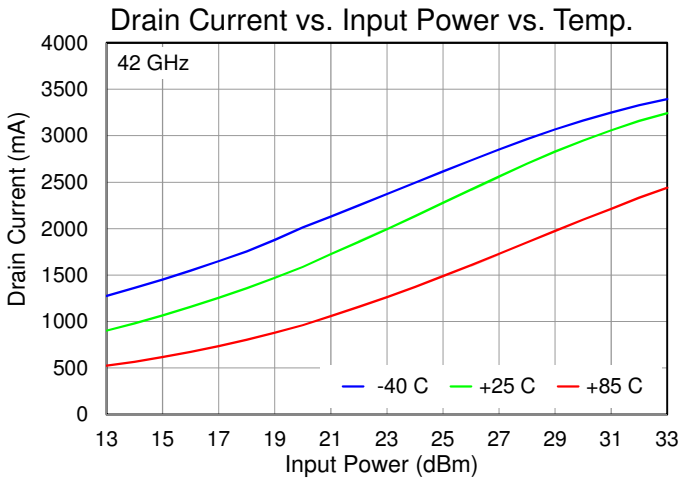
Test conditions, unless otherwise noted: CW, V_D = 24 V, I_{DQ} = 280 mA, P_{IN} = 29 dBm, T_{BASE} = +25 ºC (T_{BASE} is backside of 0.02 in CuMo carrier plate)

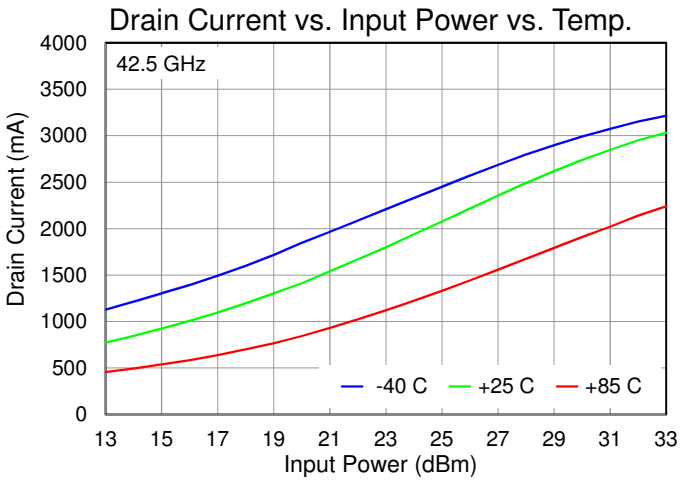






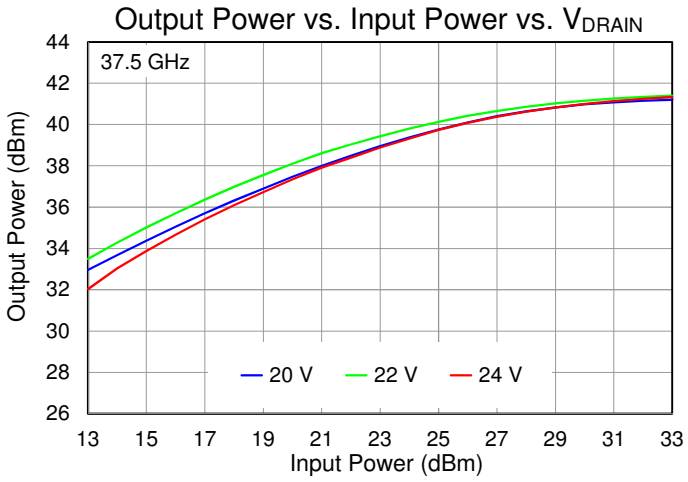


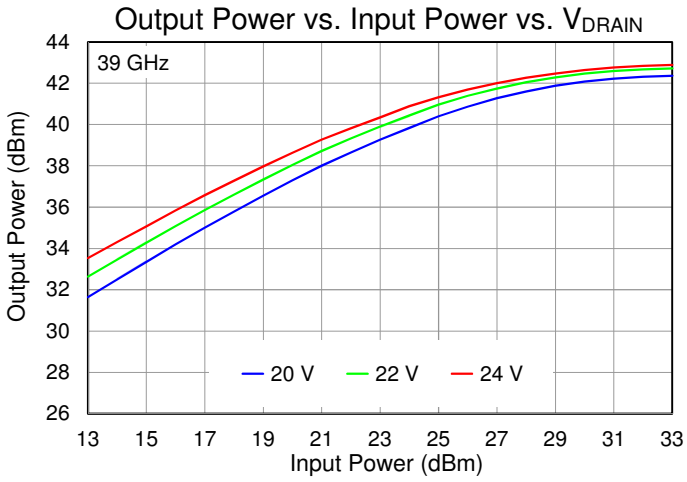


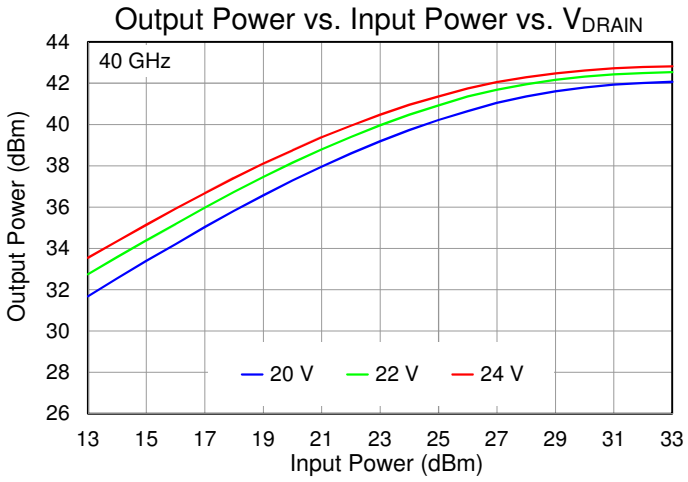


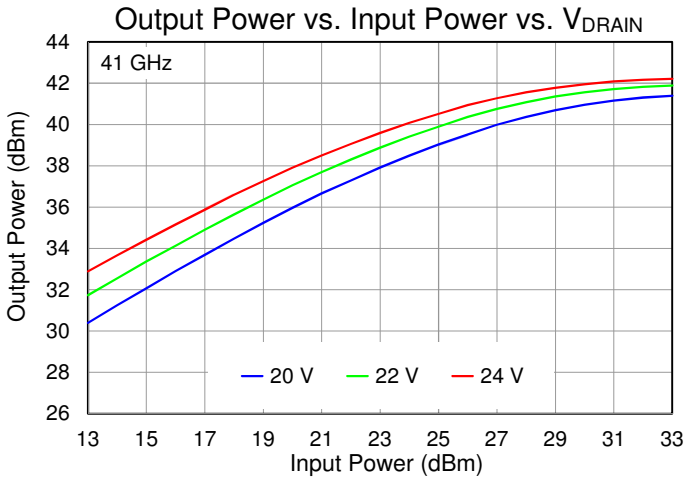
Performance Plots – Large Signal

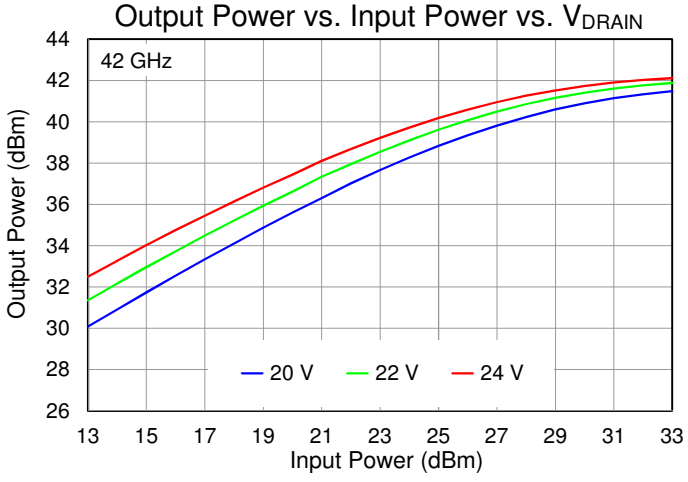
Test conditions, unless otherwise noted: CW, V_D = 24 V, I_{DQ} = 280 mA, P_{IN} = 29 dBm, T_{BASE} = +25 ºC (T_{BASE} is backside of 0.02 in CuMo carrier plate)

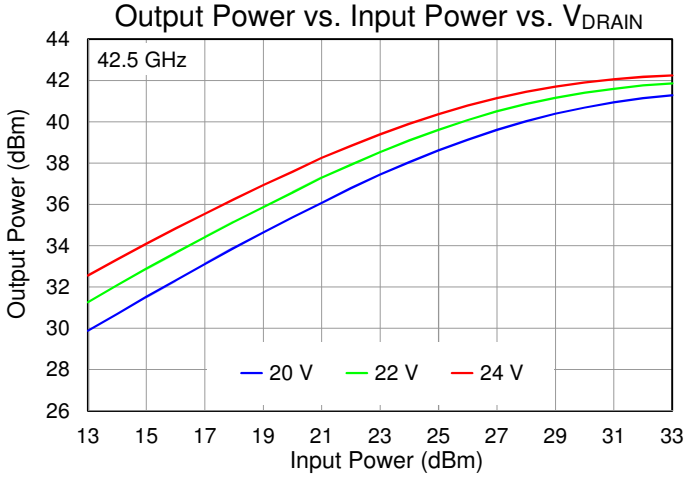






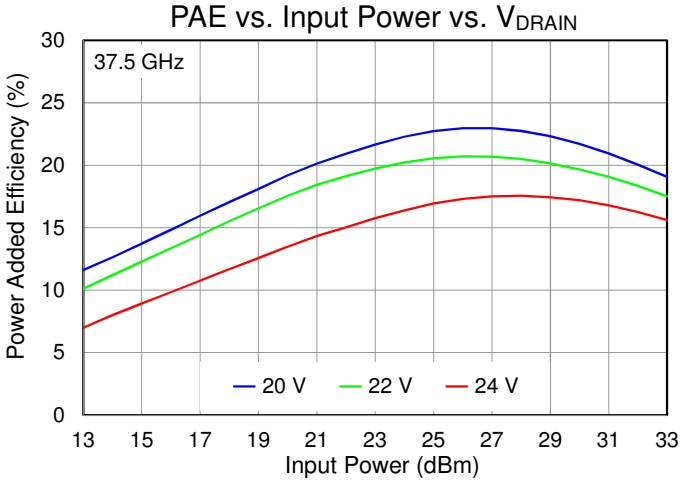


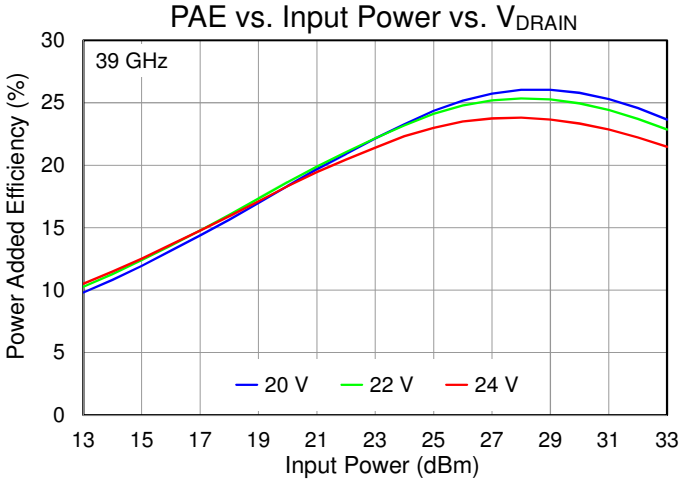


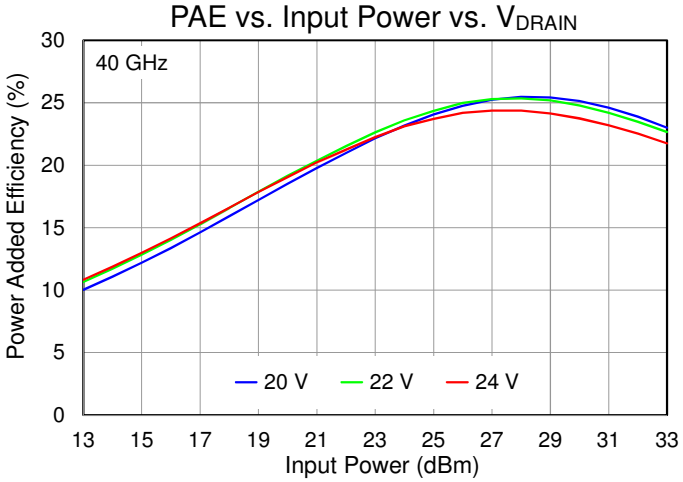


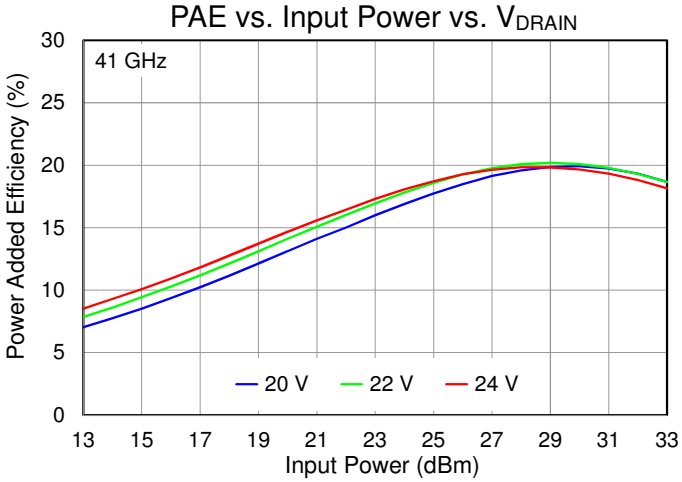
Performance Plots – Large Signal

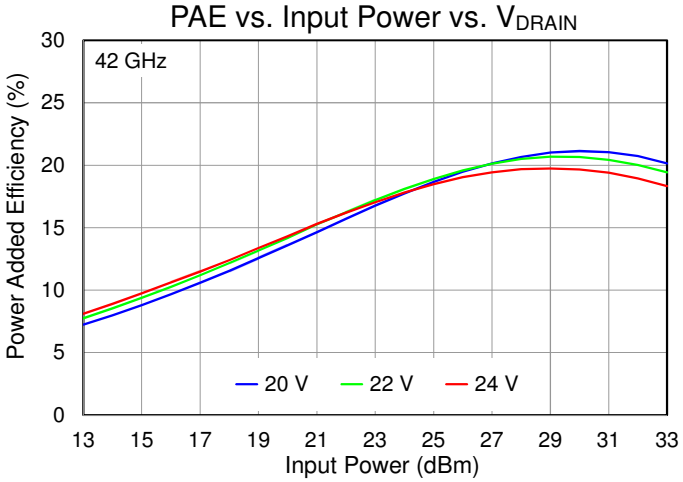
Test conditions, unless otherwise noted: CW, V_D = 24 V, I_{DQ} = 280 mA, P_{IN} = 29 dBm, T_{BASE} = +25 ºC (T_{BASE} is backside of 0.02 in CuMo carrier plate)

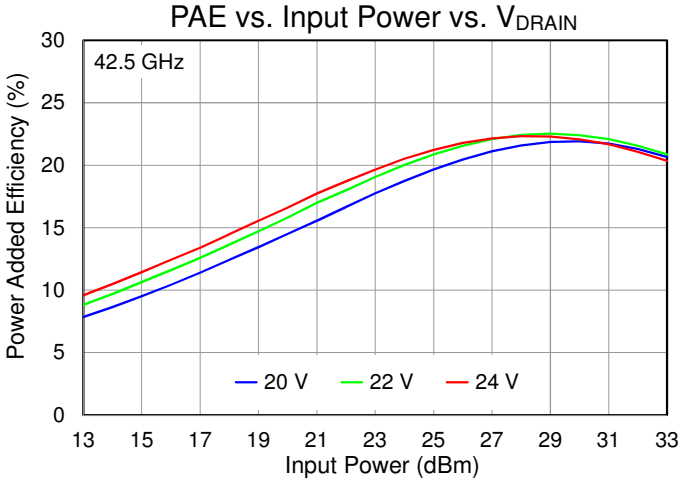






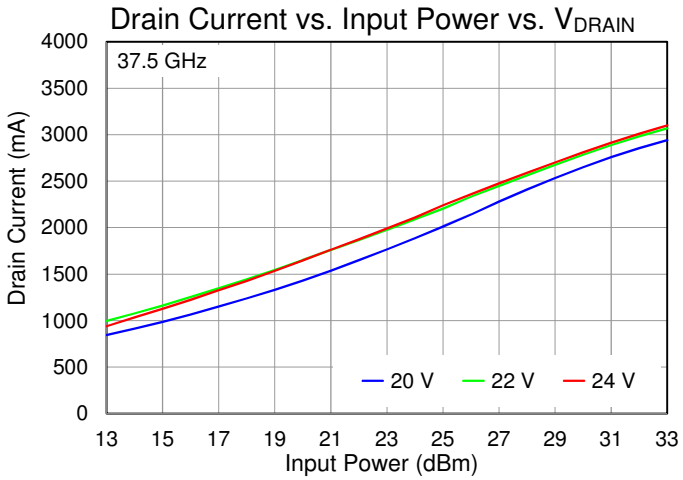


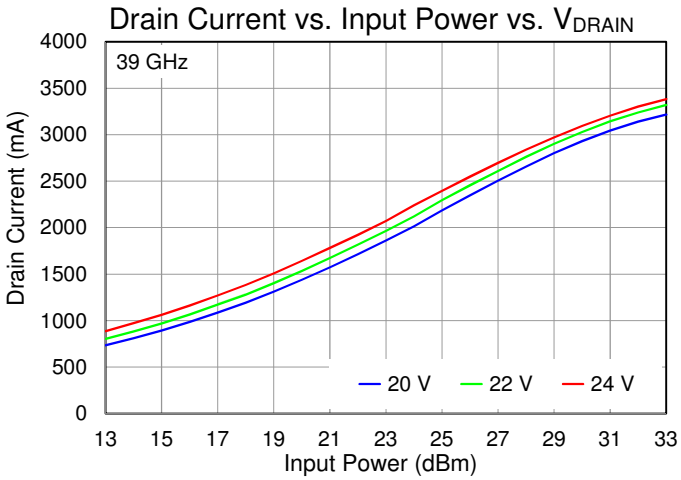


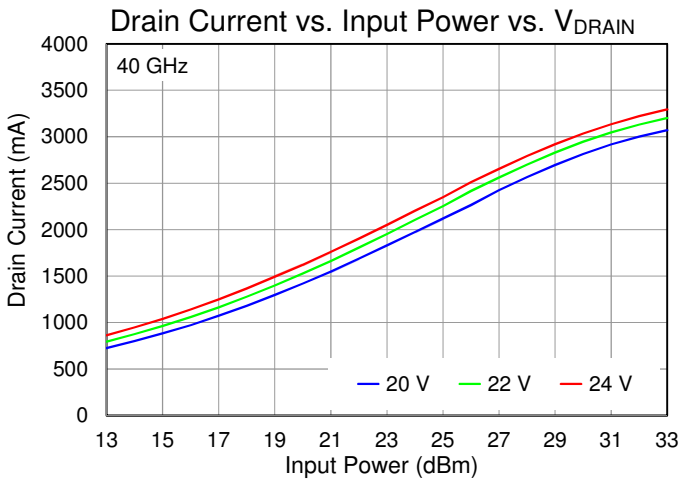


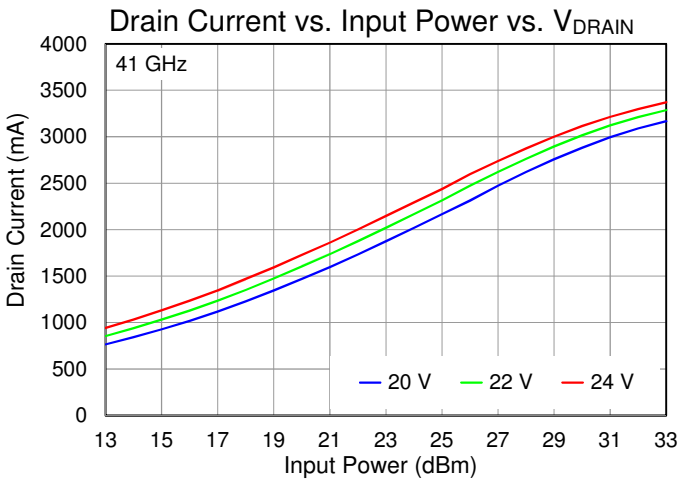
Performance Plots – Large Signal

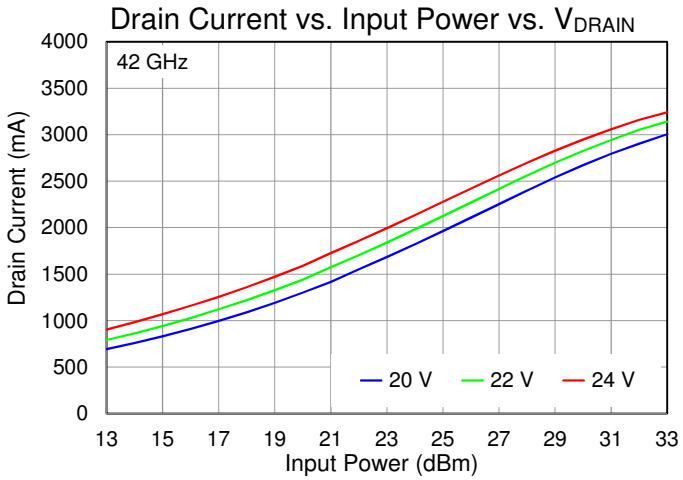
Test conditions, unless otherwise noted: CW, V_D = 24 V, I_{DQ} = 280 mA, P_{IN} = 29 dBm, T_{BASE} = +25 ºC (T_{BASE} is backside of 0.02 in CuMo carrier plate)

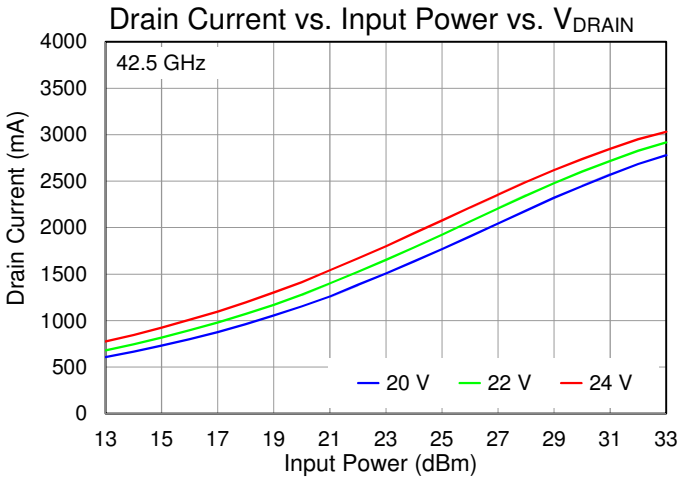






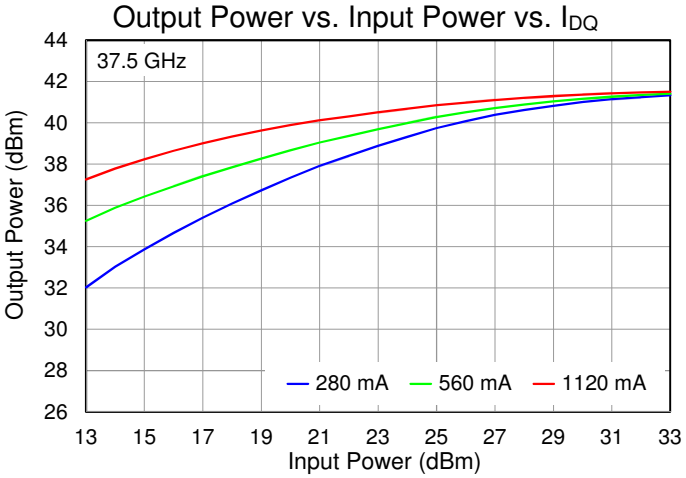


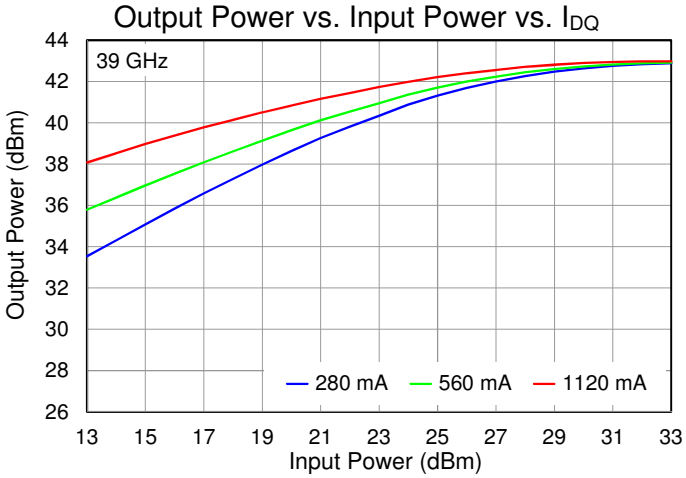


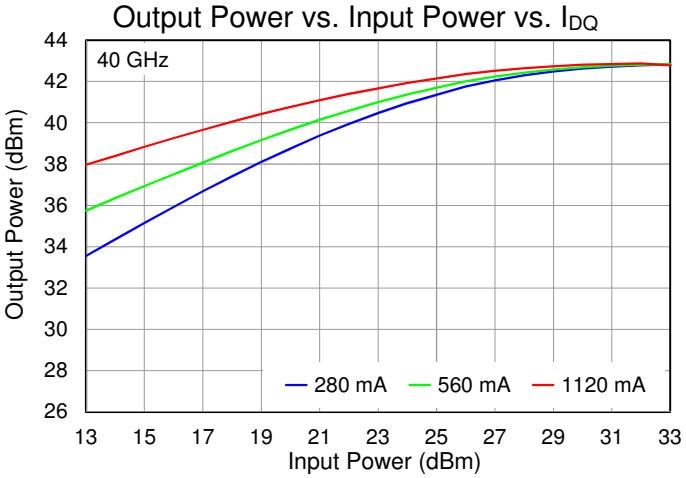


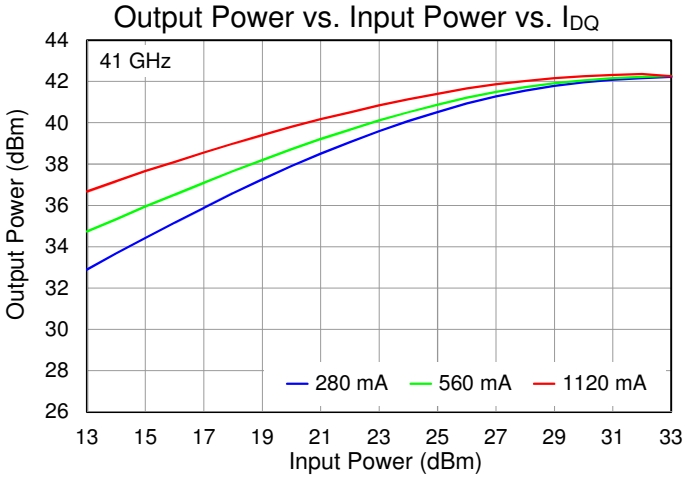
Performance Plots – Large Signal

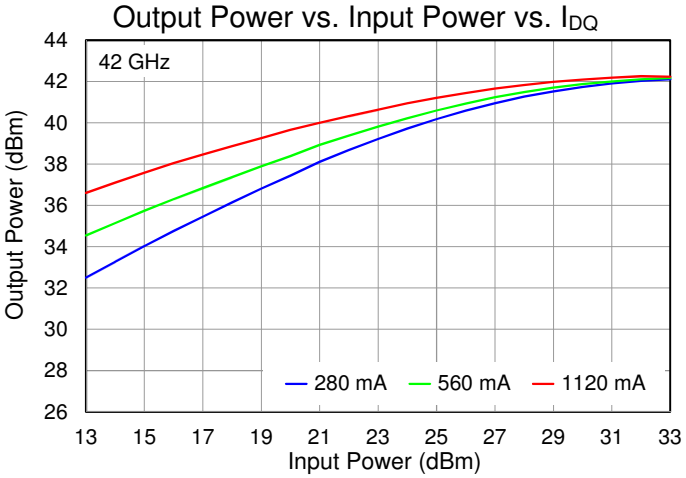
Test conditions, unless otherwise noted: CW, V_D = 24 V, I_{DQ} = 280 mA, P_{IN} = 29 dBm, T_{BASE} = +25 ºC (T_{BASE} is backside of 0.02 in CuMo carrier plate)

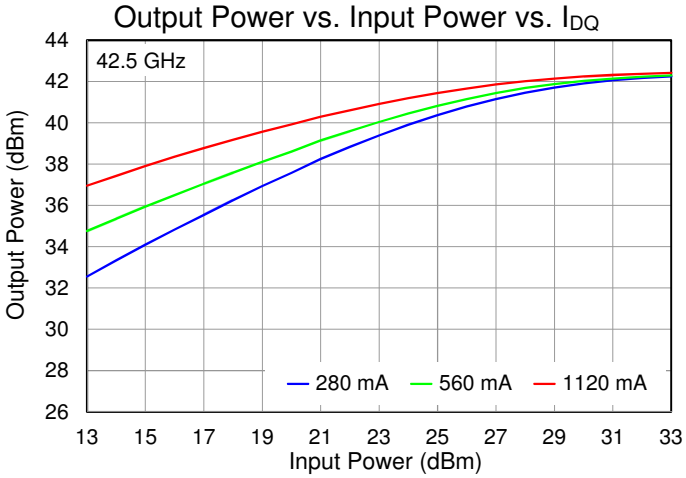






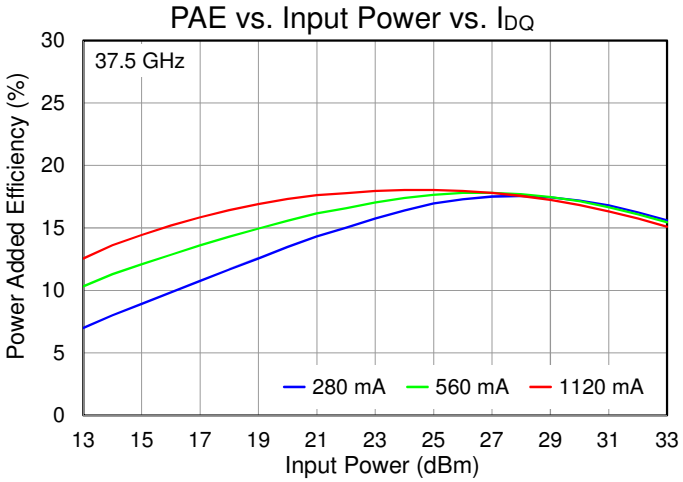


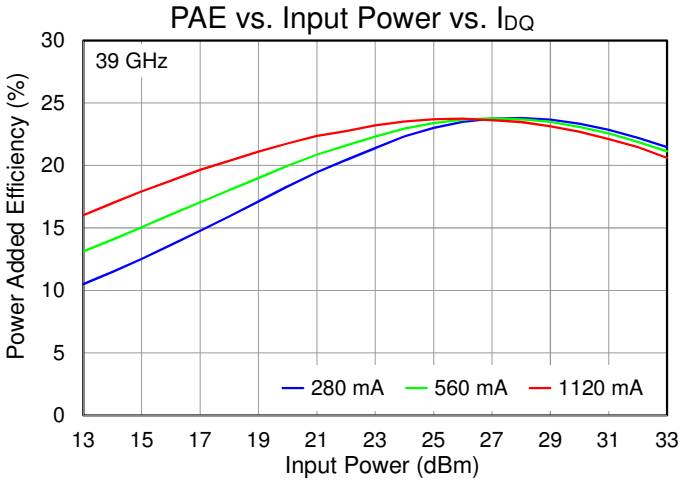


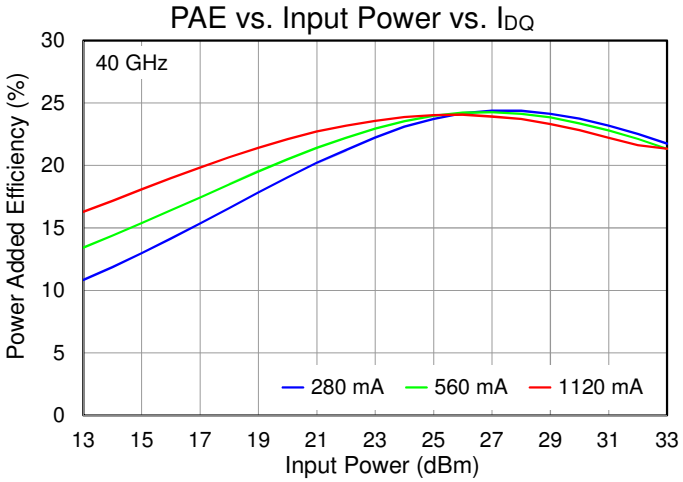


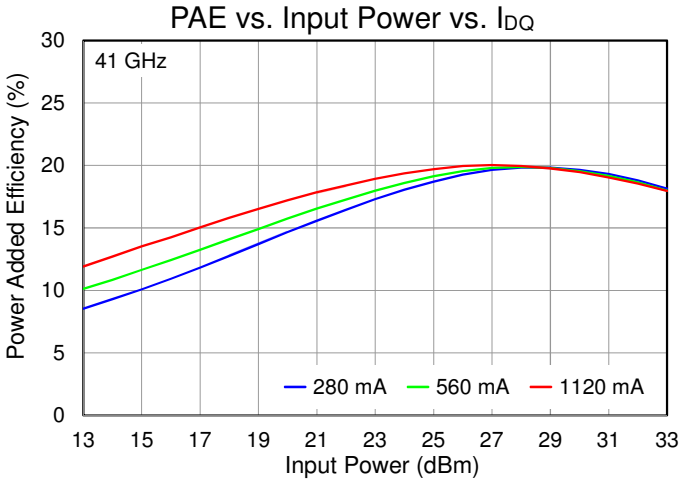
Performance Plots – Large Signal

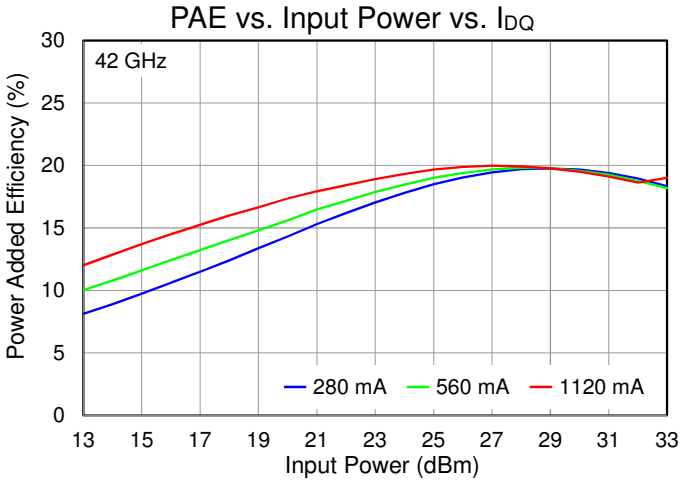
Test conditions, unless otherwise noted: CW, V_D = 24 V, I_{DQ} = 280 mA, P_{IN} = 29 dBm, T_{BASE} = +25 ºC (T_{BASE} is backside of 0.02 in CuMo carrier plate)

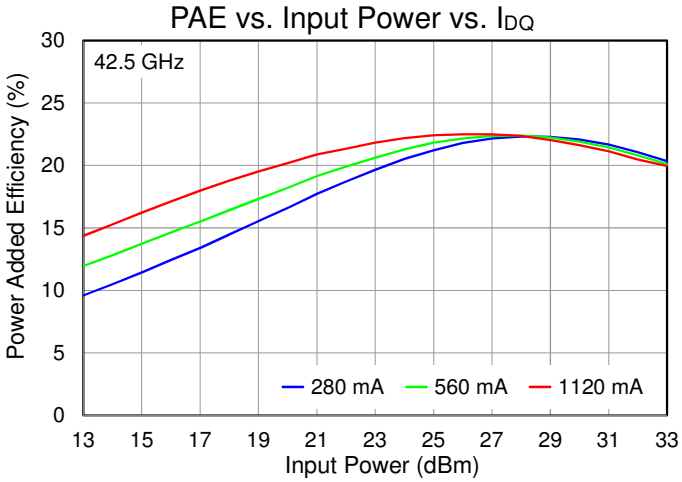






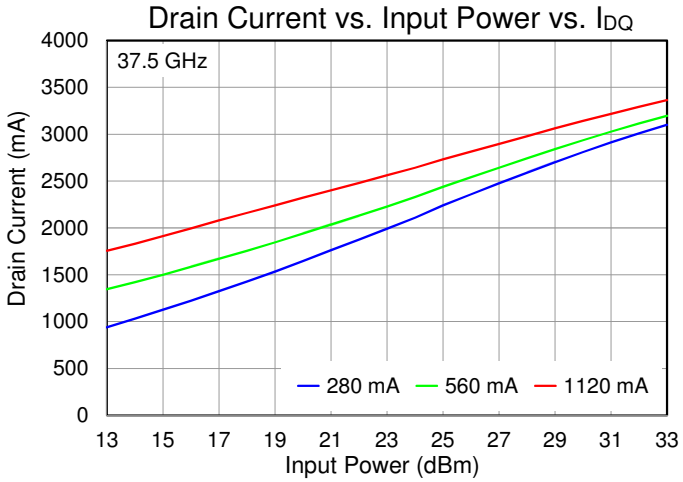


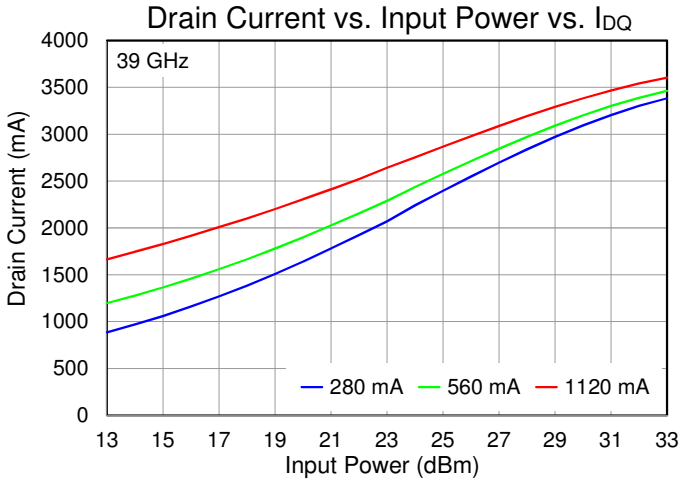


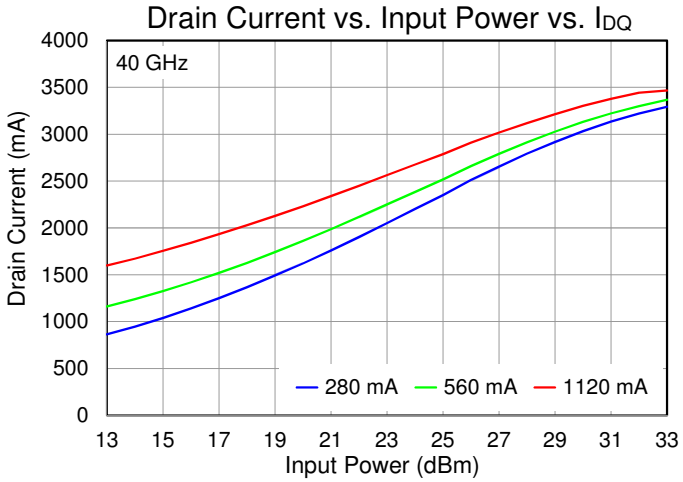


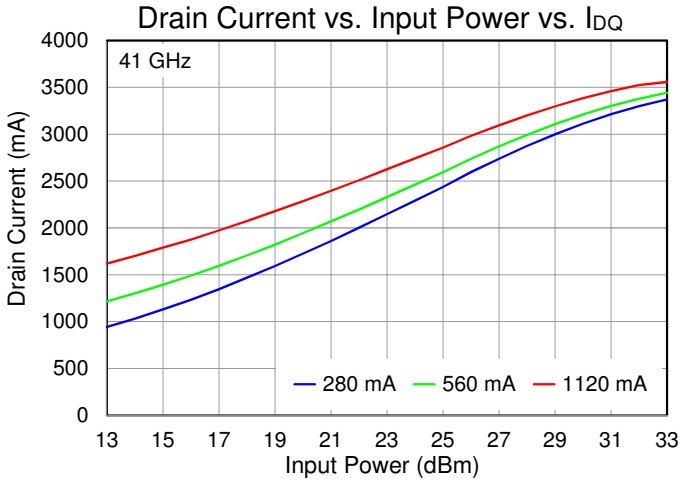
Performance Plots – Large Signal

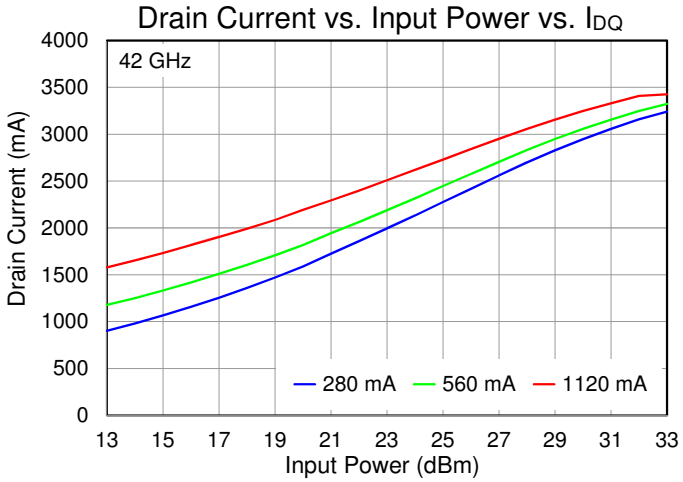
Test conditions, unless otherwise noted: CW, V_D = 24 V, I_{DQ} = 280 mA, P_{IN} = 29 dBm, T_{BASE} = +25 ºC (T_{BASE} is backside of 0.02 in CuMo carrier plate)

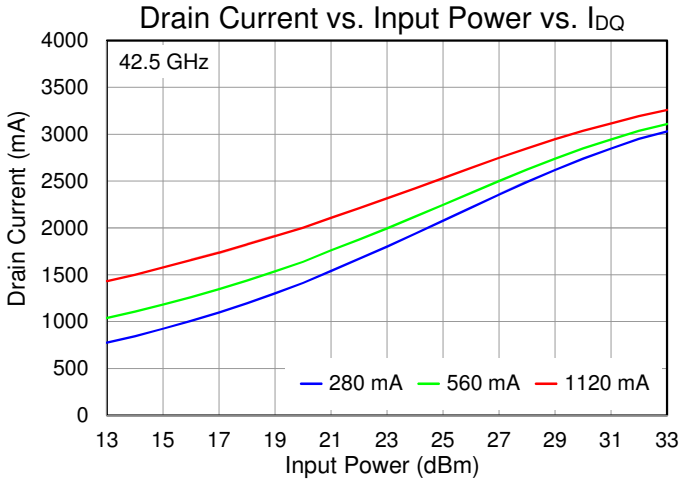






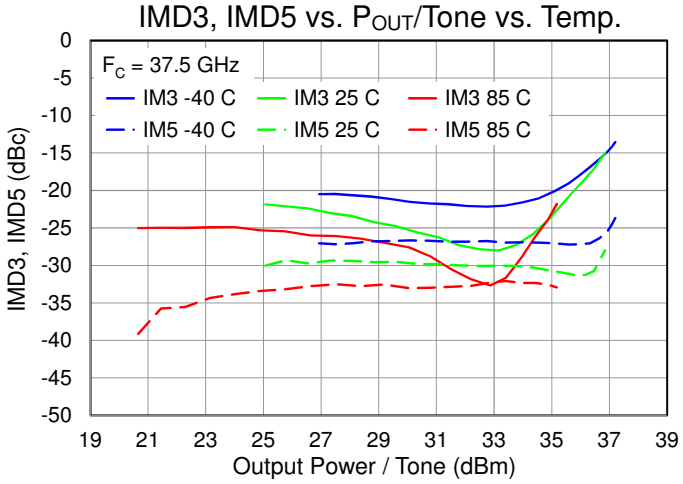


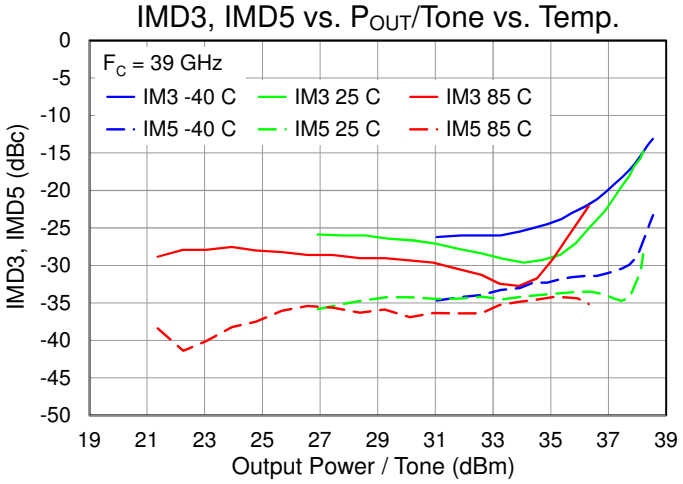


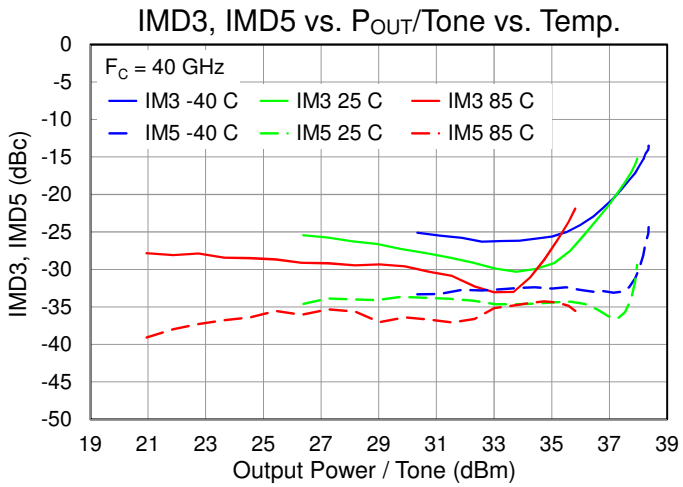


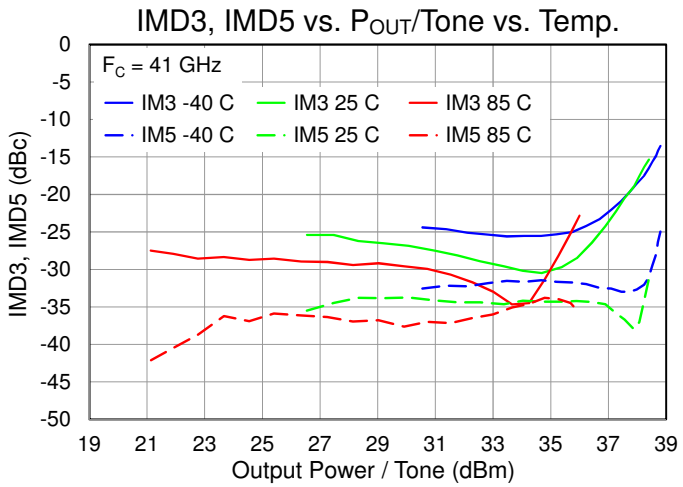
Performance Plots – Linearity

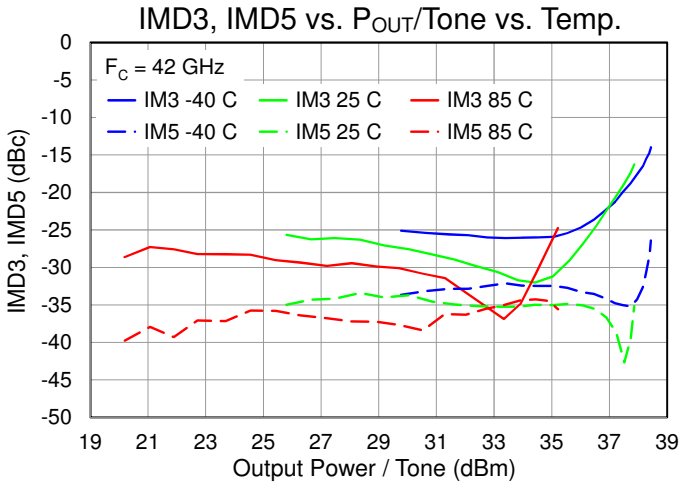
Test conditions, unless otherwise noted: CW, V_D = 24 V, I_{DQ} = 280 mA, Δf = 100 MHz, T_{BASE} = +25 ºC (T_{BASE} is backside of 0.02 in CuMo carrier plate)

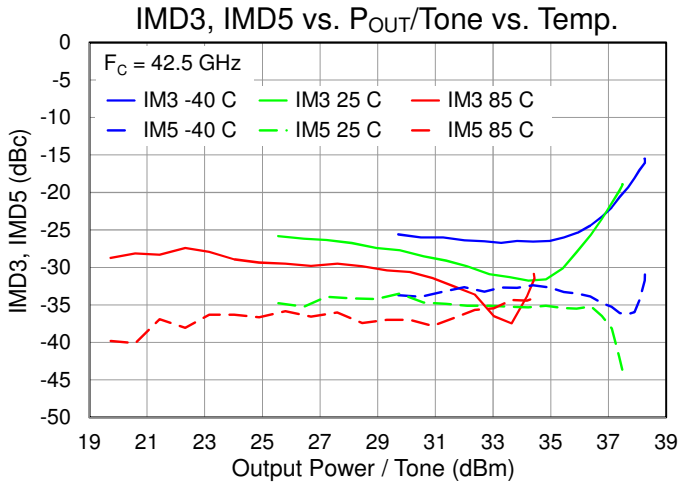








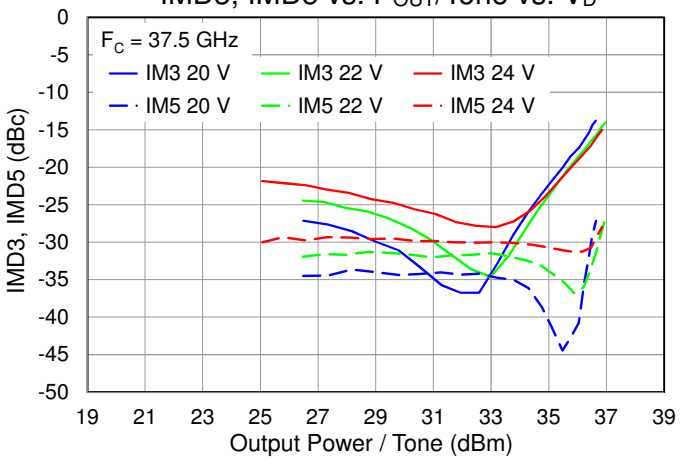




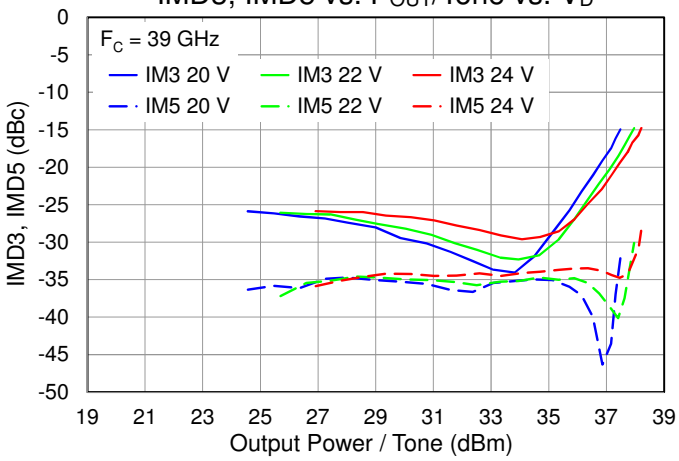
Performance Plots – Linearity

Test conditions, unless otherwise noted: CW, V_D = 24 V, I_{DQ} = 280 mA, Δf = 100 MHz, T_{BASE} = +25 ºC (T_{BASE} is backside of 0.02 in CuMo carrier plate)

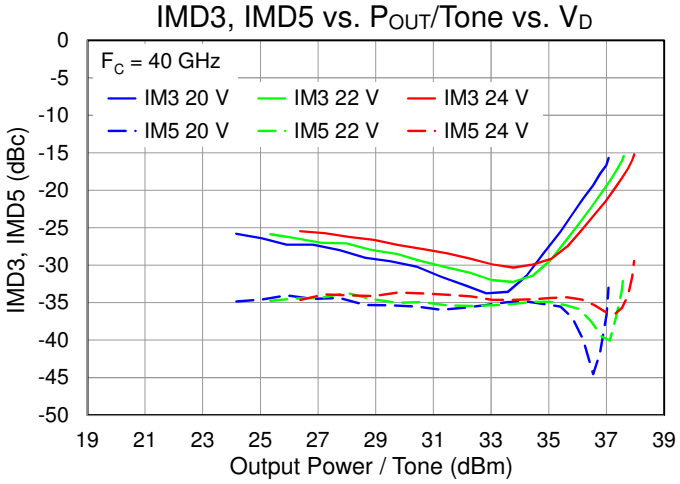
IMD3, IMD5 vs. P_{OUT}/Tone vs. V_D



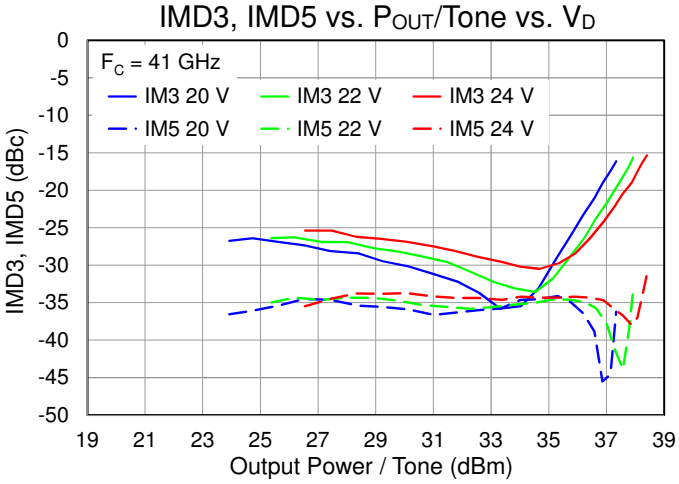
IMD3, IMD5 vs. P_{OUT}/Tone vs. V_D



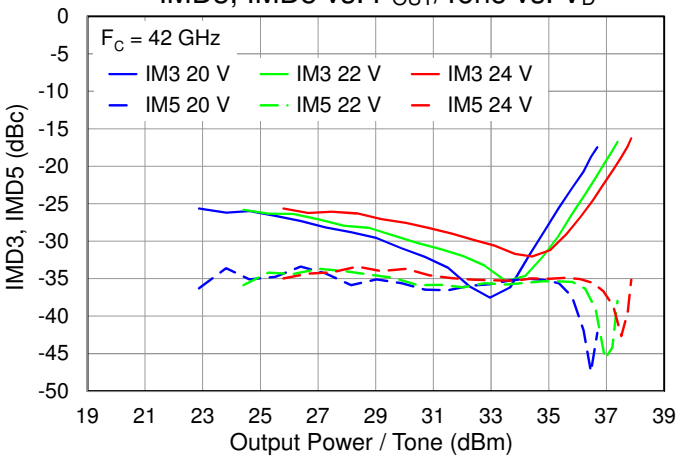
IMD3, IMD5 vs. P_{OUT}/Tone vs. V_D



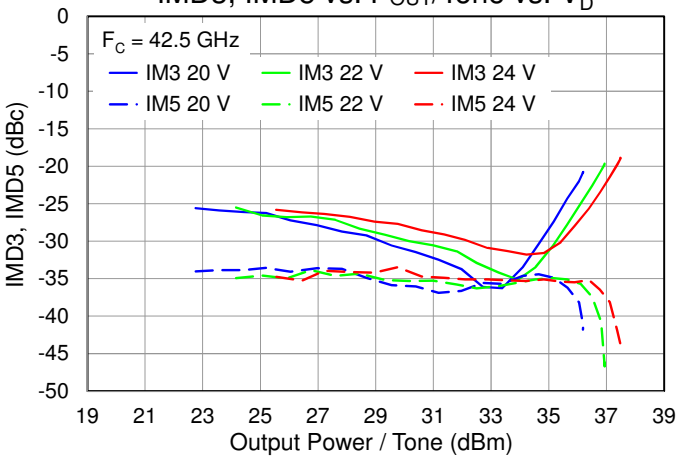
IMD3, IMD5 vs. P_{OUT}/Tone vs. V_D



IMD3, IMD5 vs. P_{OUT}/Tone vs. V_D

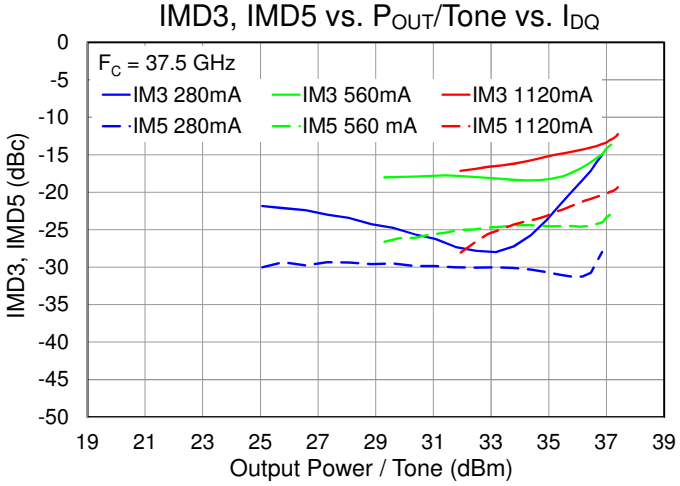


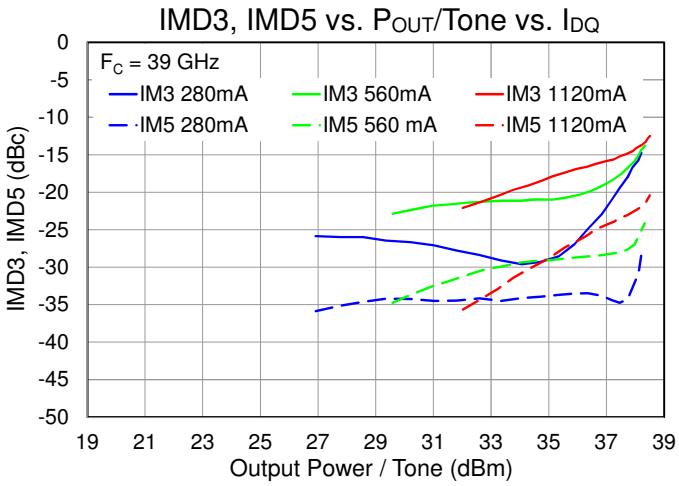
IMD3, IMD5 vs. P_{OUT}/Tone vs. V_D

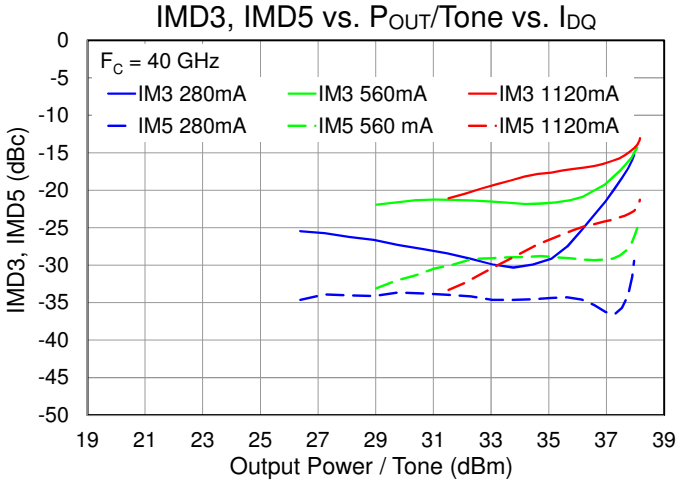


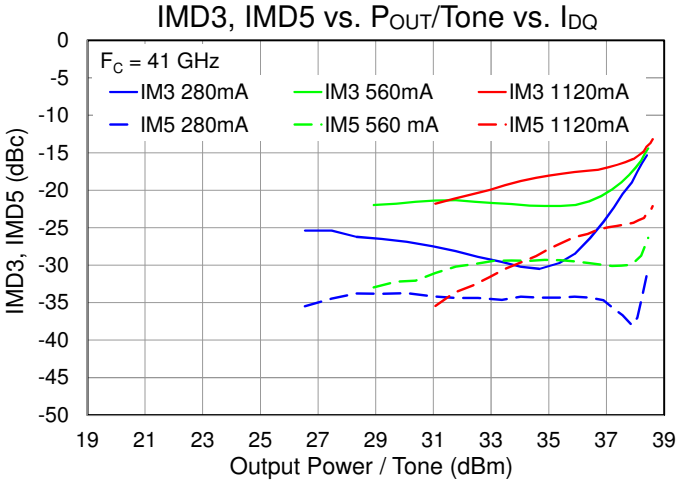
Performance Plots – Linearity

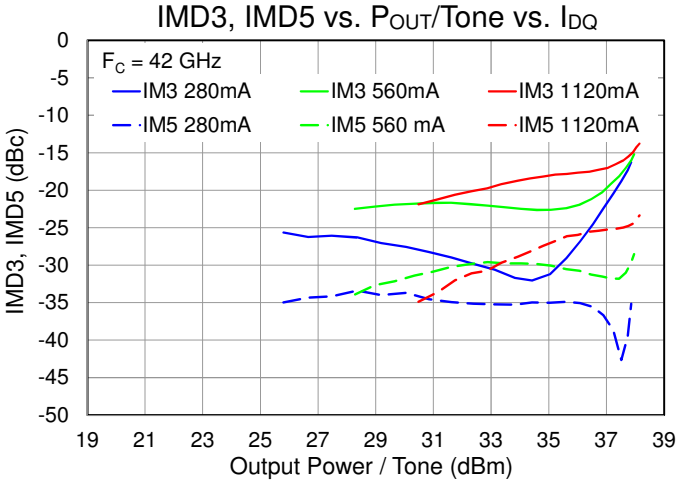
Test conditions, unless otherwise noted: CW, V_D = 24 V, I_{DQ} = 280 mA, Δf = 100 MHz, T_{BASE} = +25 ºC (T_{BASE} is backside of 0.02 in CuMo carrier plate)

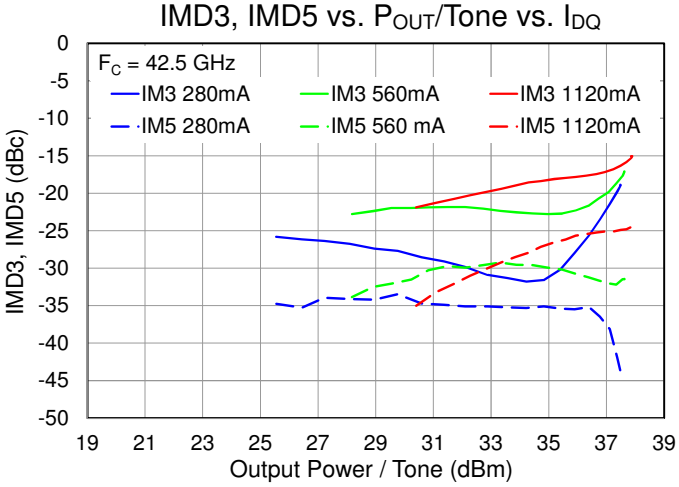








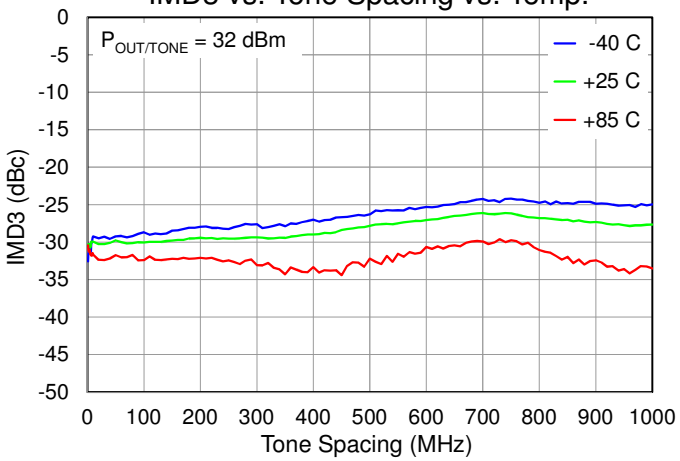




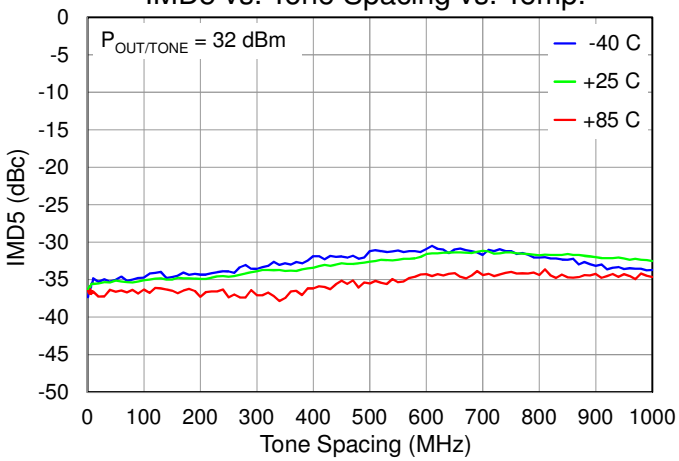
Performance Plots – Linearity

Test conditions, unless otherwise noted: CW, V_D = 24 V, I_{DQ} = 280 mA, F_C = 40 GHz, T_{BASE} = +25 ºC (T_{BASE} is backside of 0.02 in CuMo carrier plate)

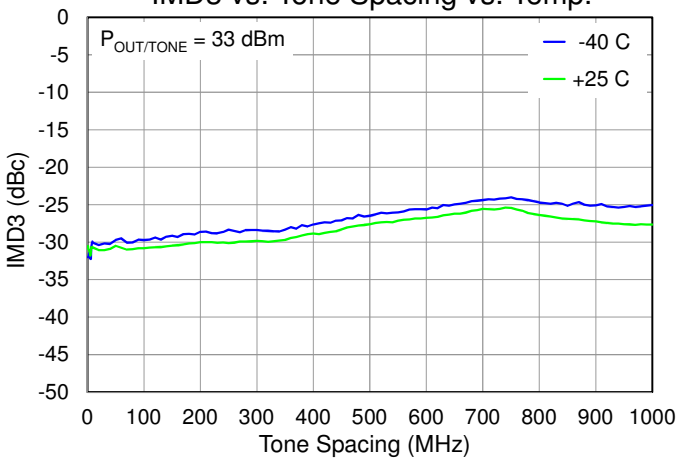
IMD3 vs. Tone Spacing vs. Temp.



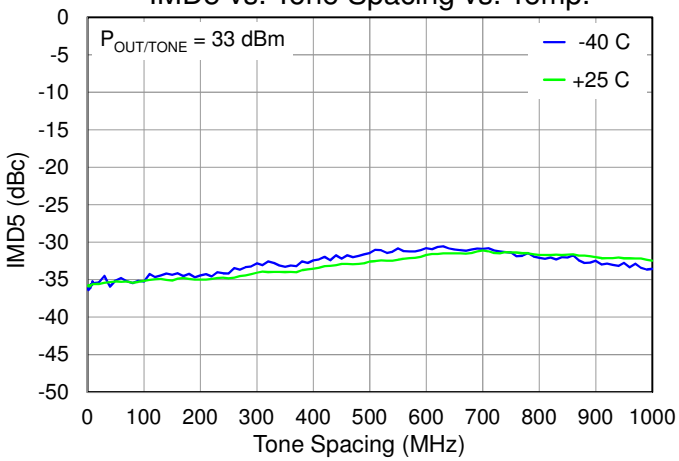
IMD5 vs. Tone Spacing vs. Temp.



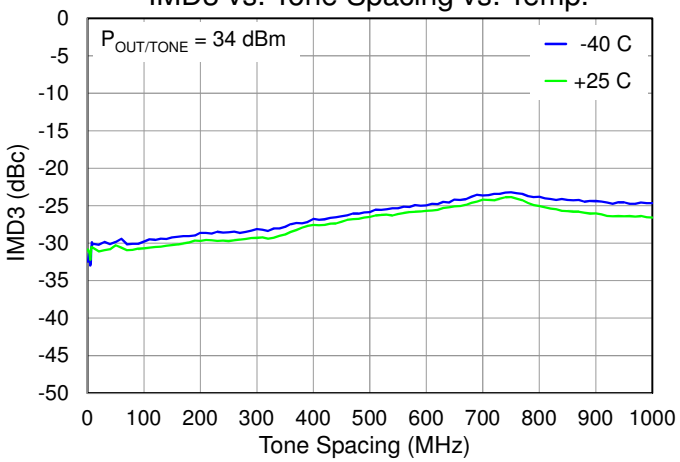
IMD3 vs. Tone Spacing vs. Temp.



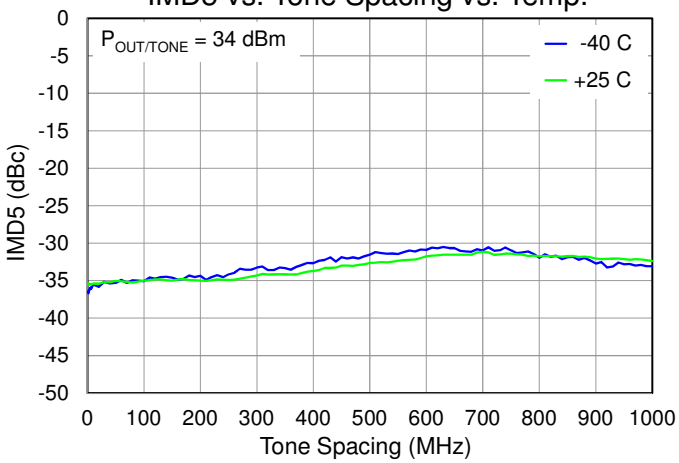
IMD5 vs. Tone Spacing vs. Temp.



IMD3 vs. Tone Spacing vs. Temp.



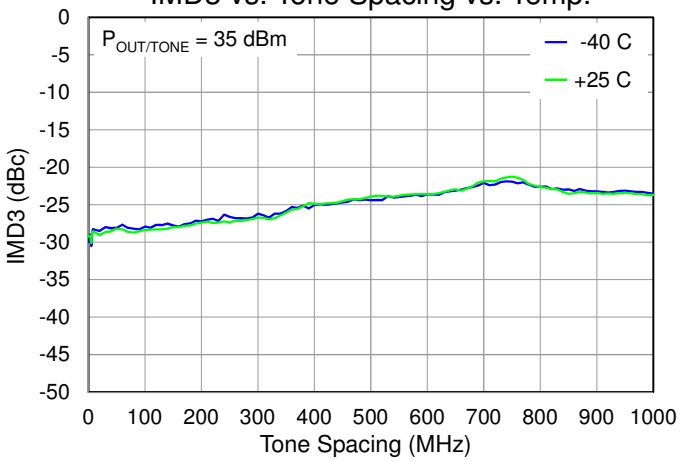
IMD5 vs. Tone Spacing vs. Temp.



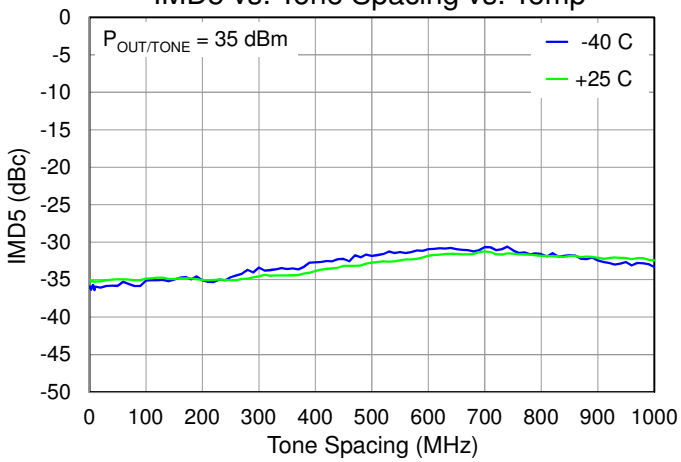
Performance Plots – Linearity

Test conditions, unless otherwise noted: CW, V_D = 24 V, I_{DQ} = 280 mA, F_C = 40 GHz, T_{BASE} = +25 ºC (T_{BASE} is backside of 0.02 in CuMo carrier plate)

IMD3 vs. Tone Spacing vs. Temp.



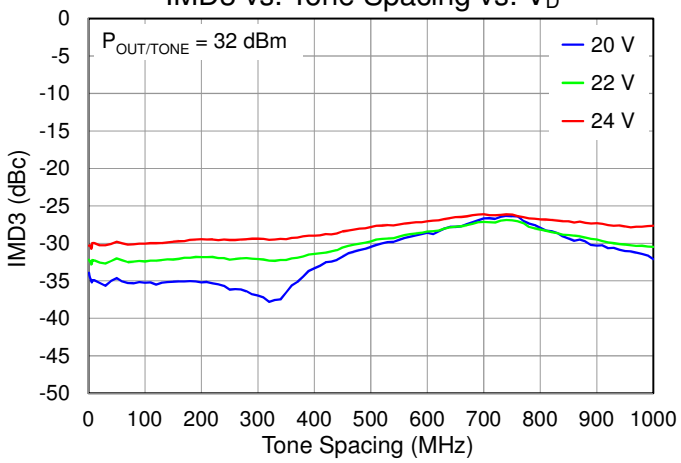
IMD5 vs. Tone Spacing vs. Temp



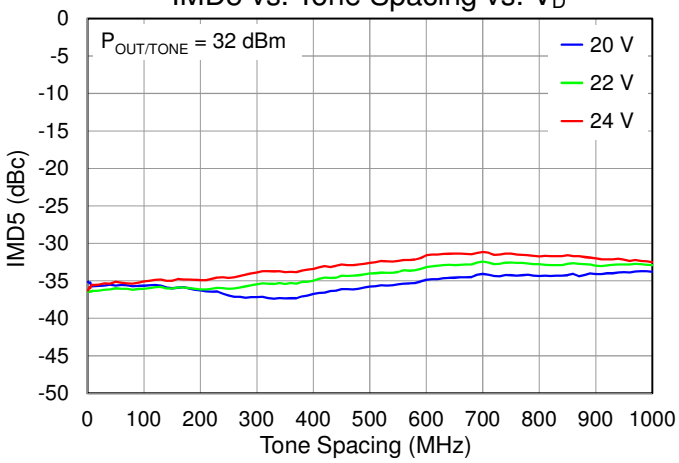
Performance Plots – Linearity

Test conditions, unless otherwise noted: CW, V_D = 24 V, I_{DQ} = 280 mA, F_C = 40 GHz, T_{BASE} = +25 ºC (T_{BASE} is backside of 0.02 in CuMo carrier plate)

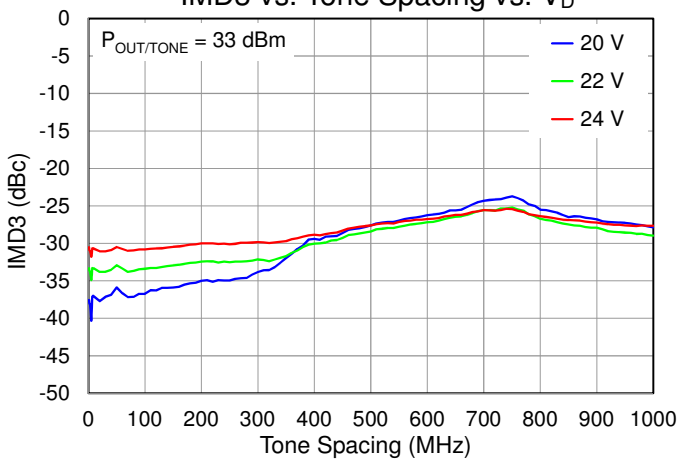
IMD3 vs. Tone Spacing vs. V_D



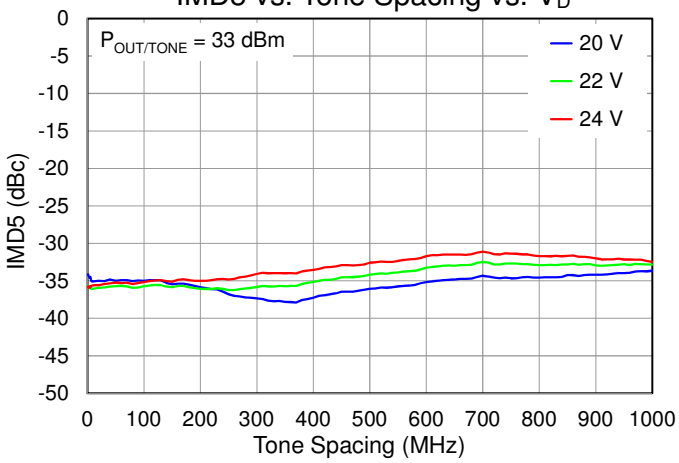
IMD5 vs. Tone Spacing vs. V_D



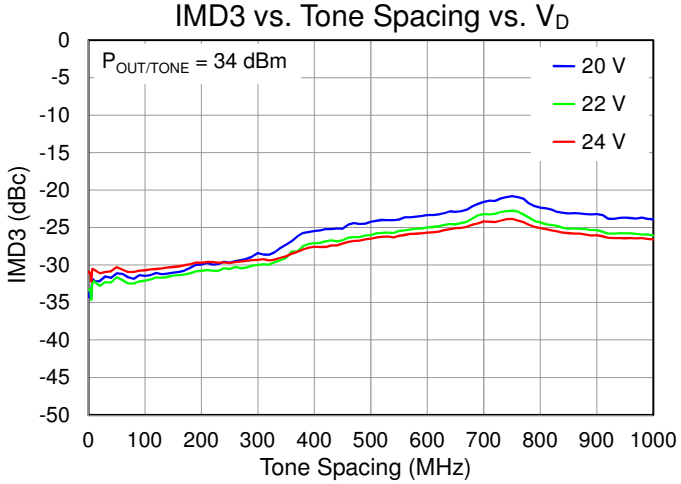
IMD3 vs. Tone Spacing vs. V_D



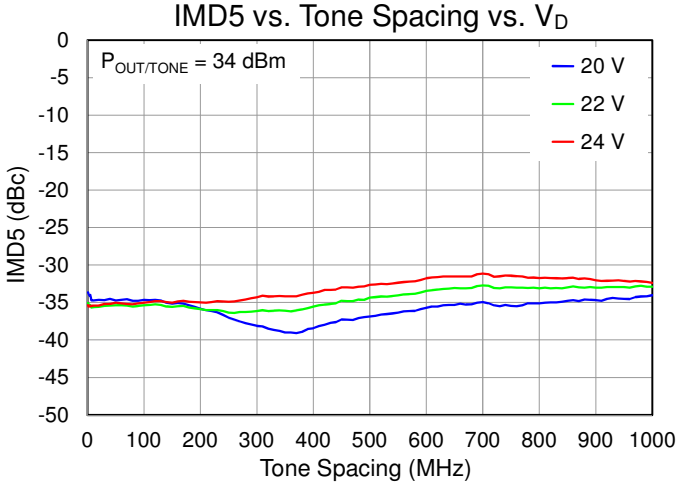
IMD5 vs. Tone Spacing vs. V_D



IMD3 vs. Tone Spacing vs. V_D

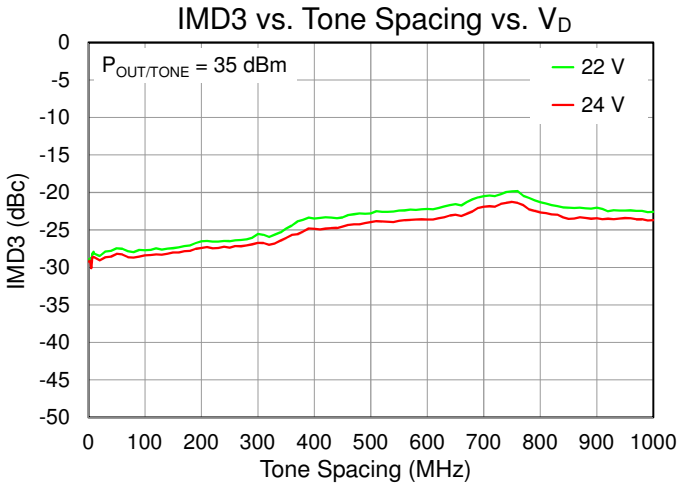


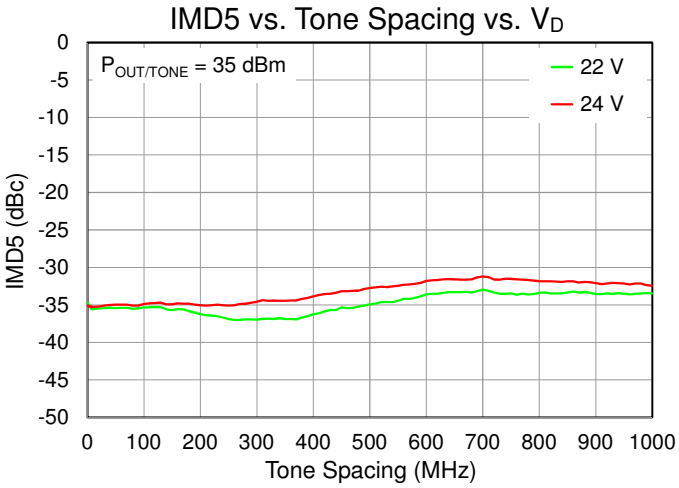
IMD5 vs. Tone Spacing vs. V_D



Performance Plots – Linearity

Test conditions, unless otherwise noted: CW, V_D = 24 V, I_{DQ} = 280 mA, F_C = 40 GHz, T_{BASE} = +25 ºC (T_{BASE} is backside of 0.02 in CuMo carrier plate)

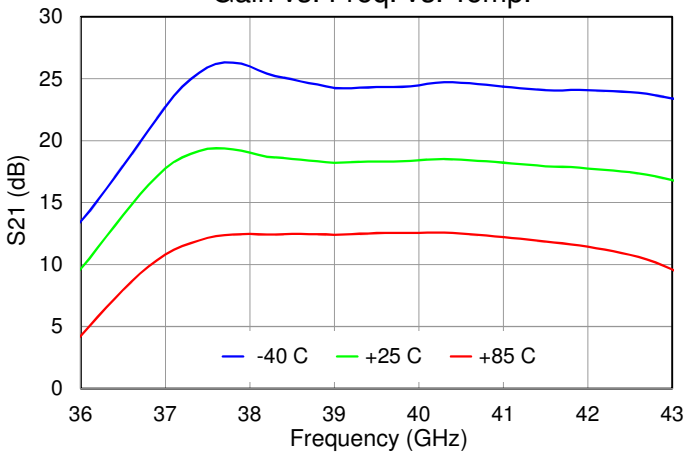




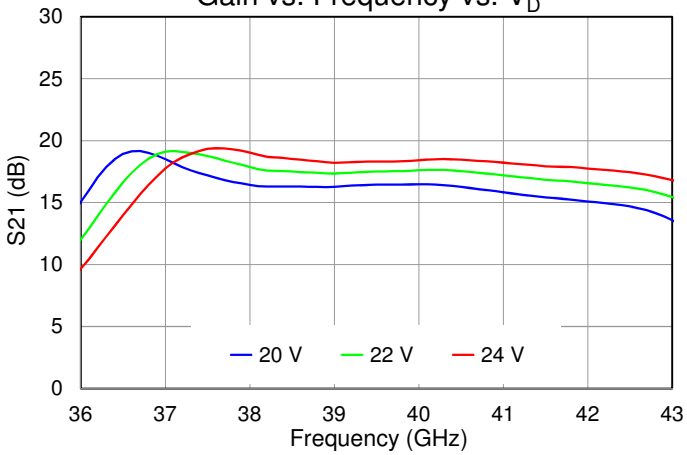
Performance Plots – Small Signal

Test conditions, unless otherwise noted: CW, V_D = 24 V, I_{DQ} = 280 mA, P_{IN} = -30 dBm, T_{BASE} = +25 ºC (T_{BASE} is backside of 0.02 in CuMo carrier plate

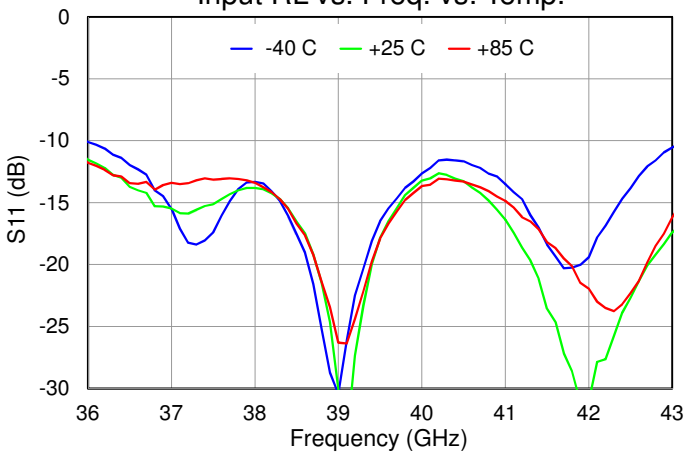
Gain vs. Freq. vs. Temp.



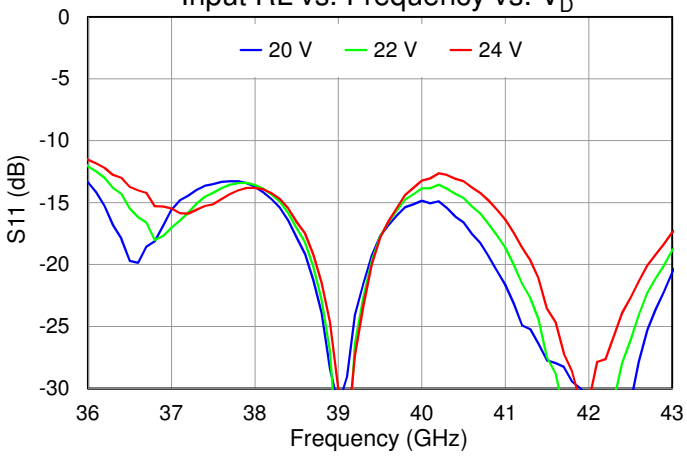
Gain vs. Frequency vs. V_D



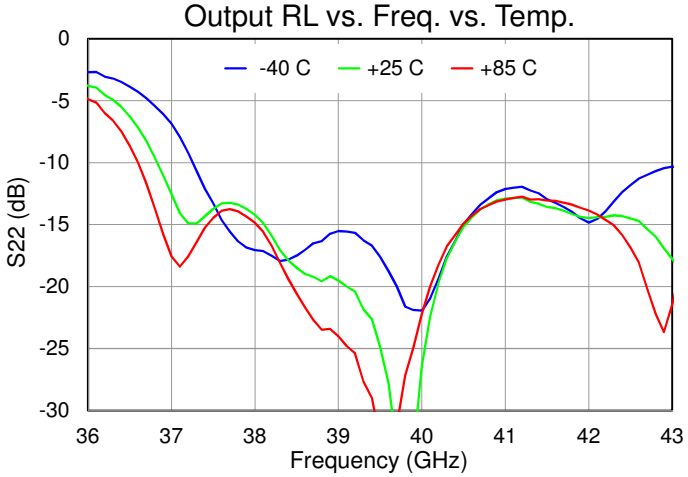
Input RL vs. Freq. vs. Temp.



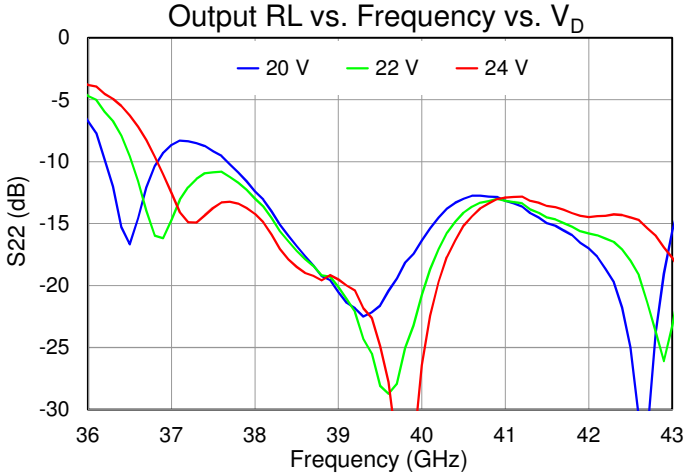
Input RL vs. Frequency vs. V_D



Output RL vs. Freq. vs. Temp.

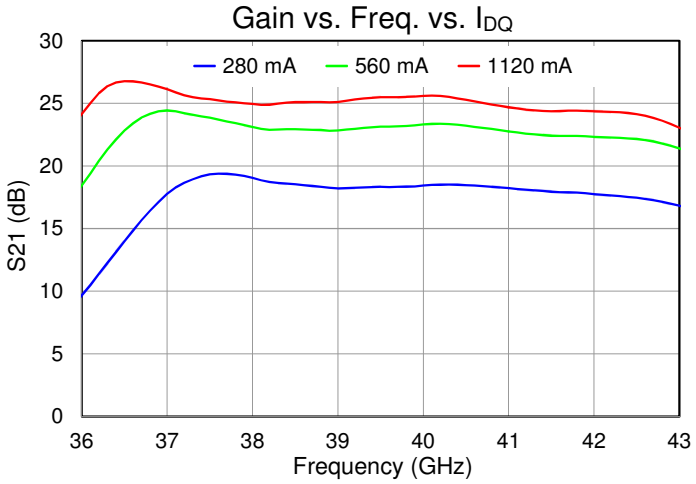


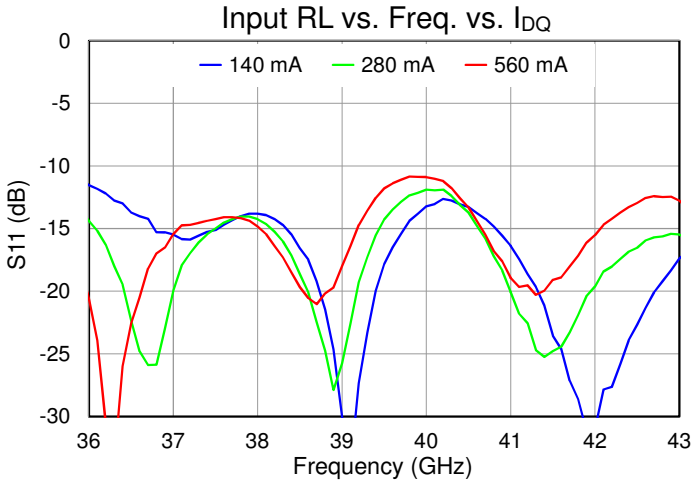
Output RL vs. Frequency vs. V_D

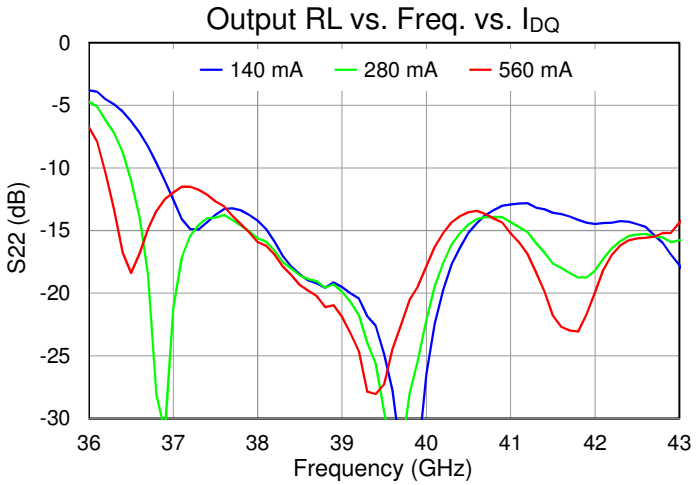


Performance Plots – Small Signal

Test conditions, unless otherwise noted: CW, V_D = 24 V, I_{DQ} = 280 mA, P_{IN} = -30 dBm, T_{BASE} = +25 ºC (T_{BASE} is backside of 0.02 in CuMo carrier plate







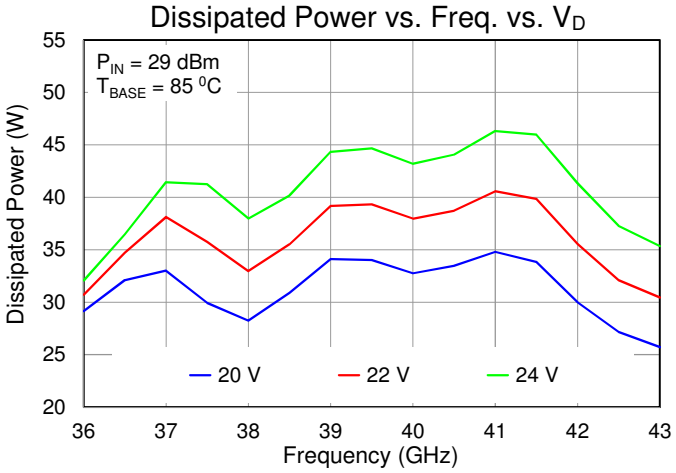
Thermal and Reliability Information

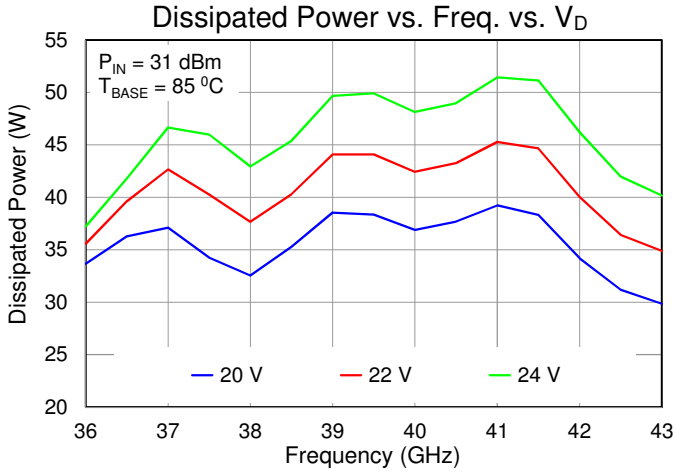
Parameter	Test Conditions	Value	Units
Thermal Resistance, θ_{JC} (1)	Quiescent, no RF T_{BASE} = 85 °C, V_D = 24 V, I_{DQ} = 280 mA, P_{DISS} = 6.72 W	1.3	ºC/W
Channel Temperature, T_{CH} (2)		94	°C
Thermal Resistance, θ_{JC} (1)	P_{IN} = 29 dBm, T_{BASE} = 85 °C, CW, V_D = 24 V, I_{DQ} = 280 mA, Freq = 41 GHz, I_{D_DRIVE} = 2.2 A, P_{OUT} = 38.6 dBm, P_{DISS} = 46.3 W	1.41	ºC/W
Channel Temperature, T_{CH} (2)		150	°C
Thermal Resistance, θ_{JC} (1)	P_{IN} = 31 dBm, T_{BASE} = 85 °C, CW, V_D = 24 V, I_{DQ} = 280 mA, Freq = 41 GHz, I_{D_DRIVE} = 2.44 A, P_{OUT} = 39.2 dBm, P_{DISS} = 51.4 W	1.42	ºC/W
Channel Temperature, T_{CH} (2)		158	°C

Notes:

1. Thermal resistance determined to T_{BASE} (T_{BASE} is backside of 0.02 in carrier plate CuMo with AuSn die attached)
2. Channel temperature indicated is an IR scan equivalent temperature. Thermal resistance is calculated using this value. Additional information can be found in the Qorvo Applications Note “GaN Device TCHMAX Theta-JC and Reliability Estimates,” located here https://www.qorvo.com/products/d/da006480

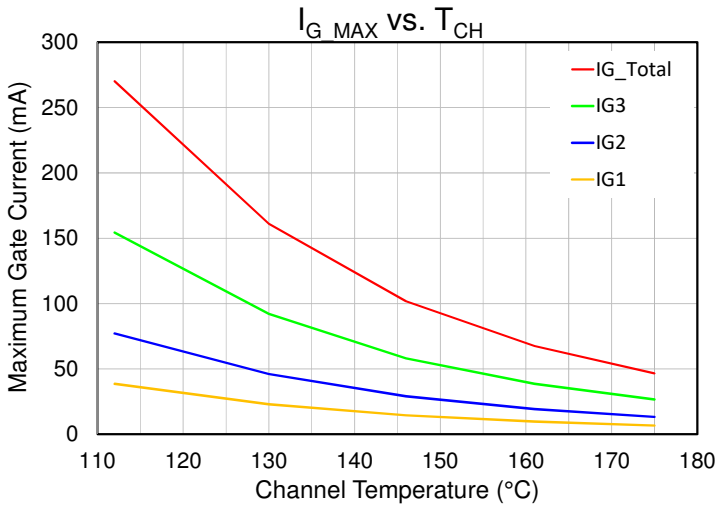
Dissipated Power





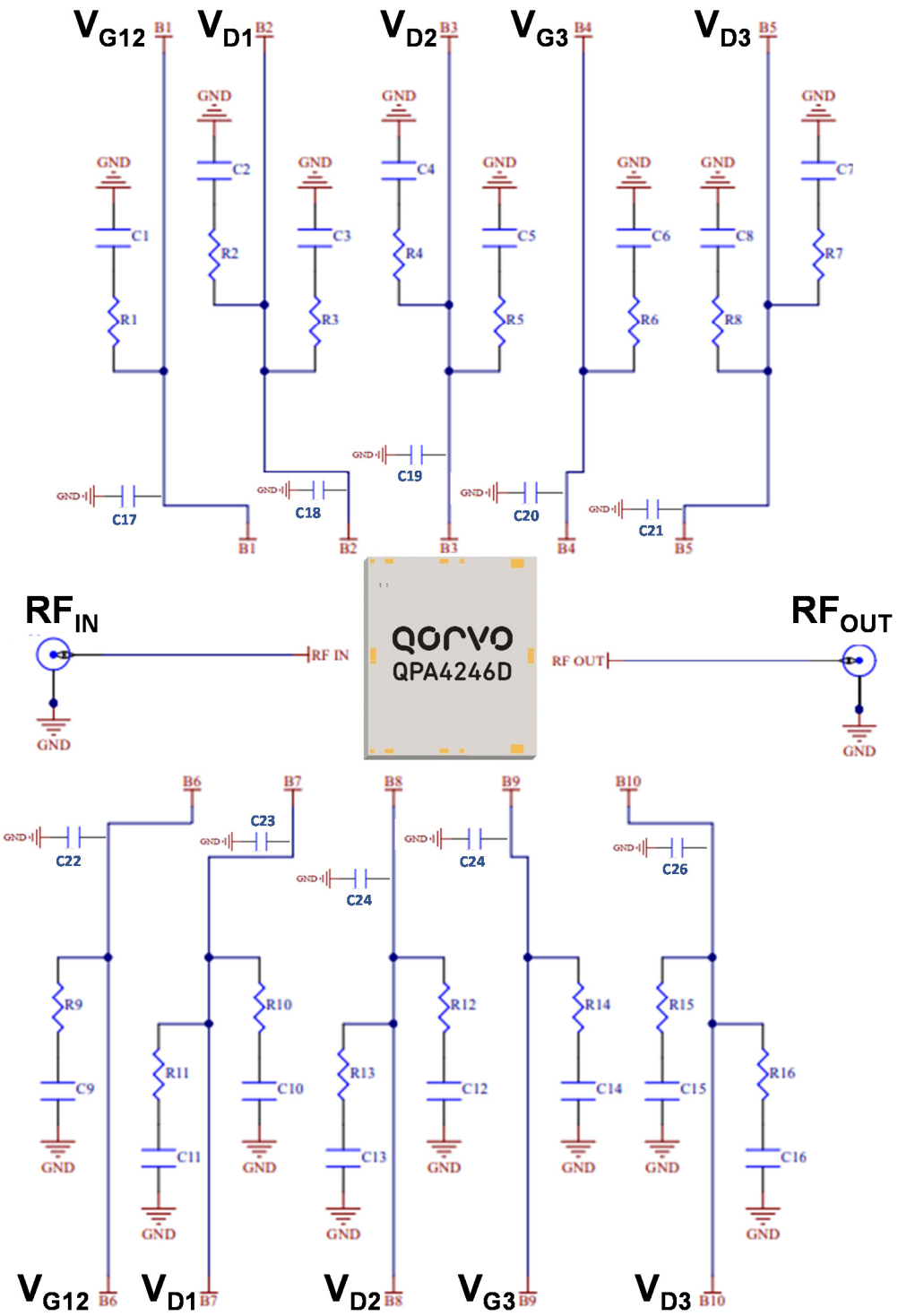
Test conditions, unless otherwise noted: CW, V_D = 24 V, I_{DQ} = 280 mA, T_{BASE} = 85 ºC
T_{BASE} is back side of 0.02 in CuMo carrier plate with AuSn die attached

Maximum Gate Current



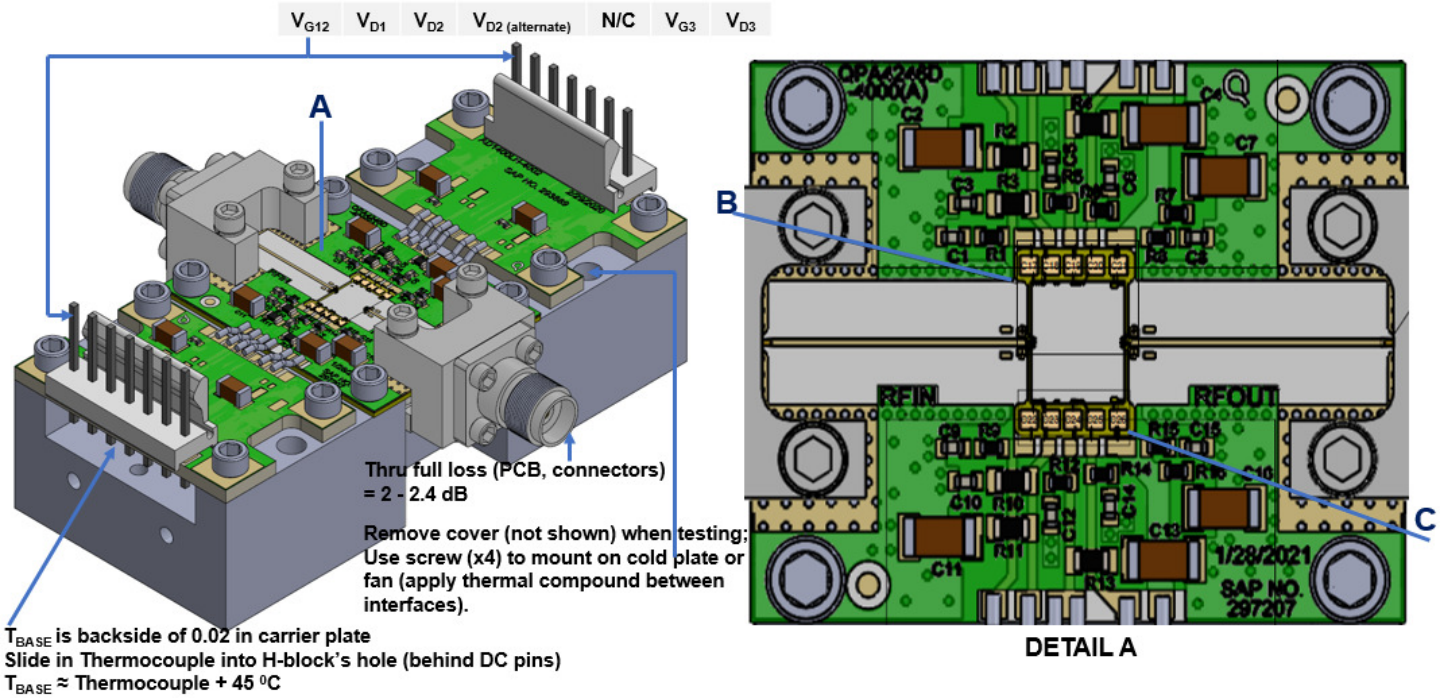
Channel Temperature is an IR scan equivalent

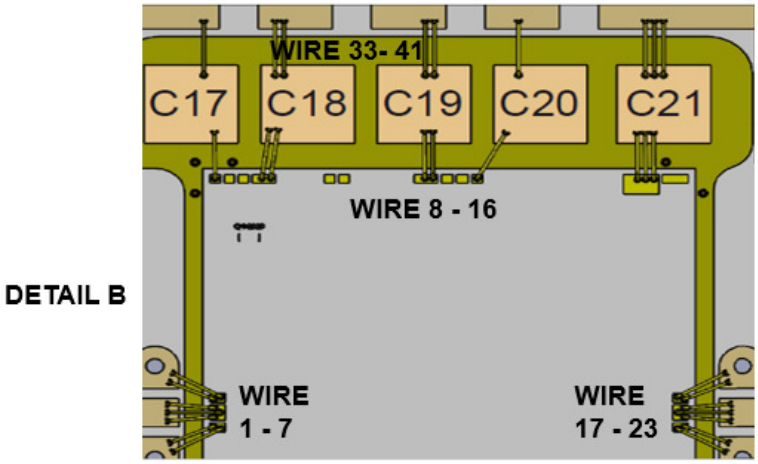
Applications Information

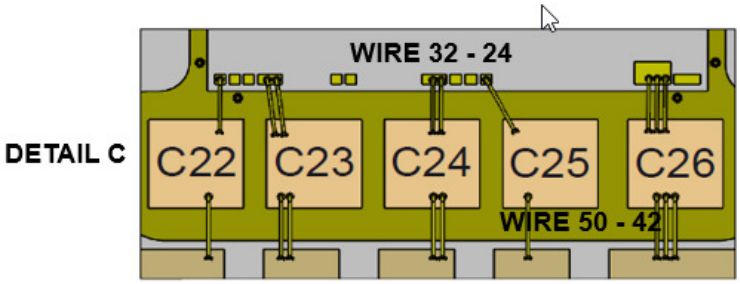


DC must be applied to both sides, top and bottom, of the die
External bypassing required on both sides

Evaluation Board (EVB) Layout







Bill of Materials

Reference Des.	Qty	Value	Description	Part Number
C1, C3, C5, C6, C8, C9, C10, C12, C14, C15	10	0.01 uF	CAP, 0.01uF, ±10%, 50V, X7R, 0402	
C2, C4, C7, C11, C13, C16, C27 – C30	10	10 uF	CAP, 10uF, 20%, 50V, 20%, X5R, 1206	
C17 – C26	10	10 nF	CAP, 10nF, ±15%, 30V, SLC, 0303	
R1, R5 – R9, R12, R14 – R16	10	0 Ω	RES, 0 Ohm, JMPR, 0402	
R2 – R4, R10, R11, R13	6	0 Ω	RES, 0 Ohm, JMPR, 0603	
R17 – R20	4	5.1 Ω	RES, 5.1 Ohm, ±1%, 1/10W, 0402	
PCB_MMIC	1		PCB for MMIC, Taconics TSM-S3B 0.005”, 0.5oz Ni/Pd/Au plating both sides, total thickness 0.009”	Qorvo, Custom
PCB,_Bias	2		PCB for DC Bias	Qorvo, Custom
H1, H2	2		CONN, HDR, Male-vert, 7 PIN, 1 RAW, MTA	TE Connectivity 640456-7 *7 PINS*
J1, J2	2		Connector, RF 2.4mm, F, Pin 0.005, Diel 0.0295	Southwest Microwave 1092-04A-12
CP	1		Carrier Plate, CuMo, 0.9 x 1.15 x 0.02T in	Qorvo, Custom
H-Block	1		H-Block, Copper C110, 1.14 x 2.49 x 0.59T in	Qorvo, Custom
S1 – S4	12		Screw, Cap, Socket Head, 2-56X1/8”	
AuSn			AuSn Solder preform	
Epoxy			Epoxy preform	
Ablebond			Epoxy, Ablebond 84-1LMI	
Solder			Paste, solder, Syntech, Sn63/Pb37	
TC			Thermal Compound, Silver 5GR	Artic Silver 5 AS5-5G

.

Bias-Up Procedure

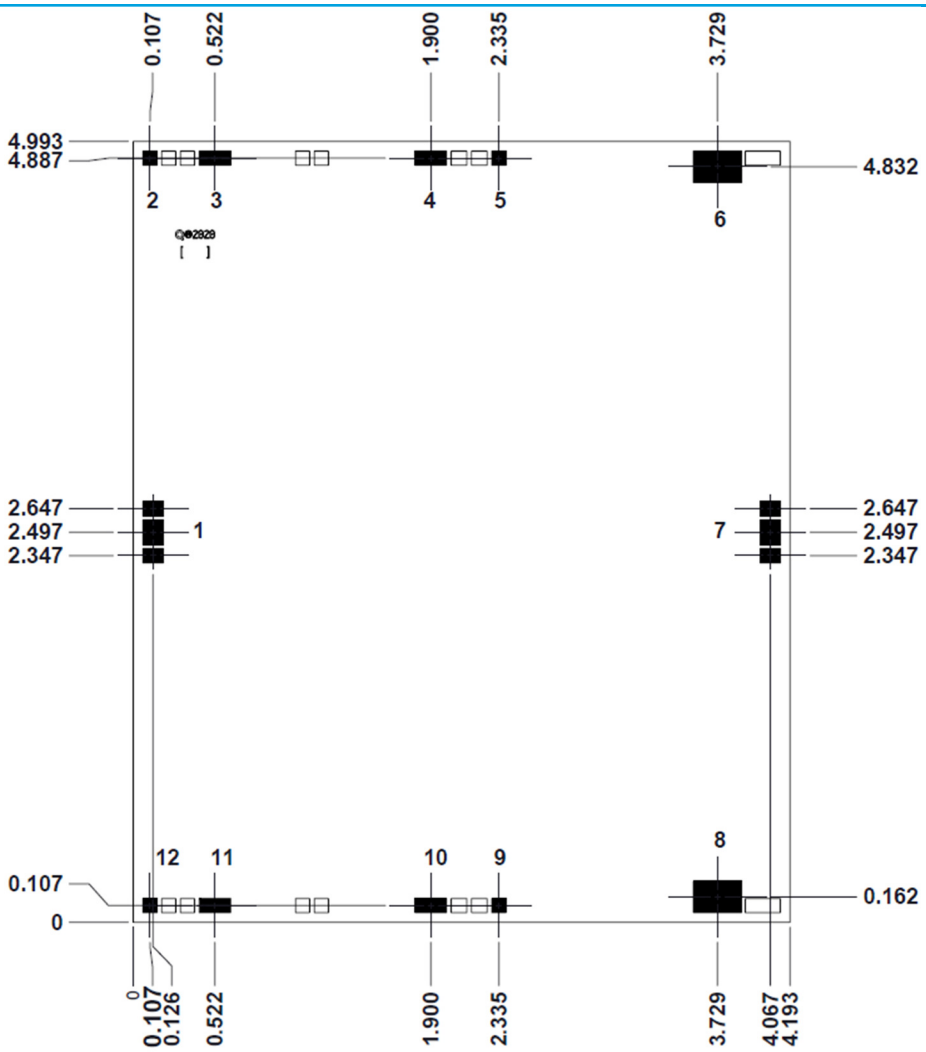
1. Set I_D limit to 4.5 A, I_G limit to 20 mA
2. Set V_G to –3.5 V
3. Set V_D +24 V. Ensure I_{DQ} ~ 0 mA
4. Adjust V_G more positive until I_D = 280 mA; $V_G \approx$ -2.3 V +/- 0.6V typical range
5. Apply RF signal

Bias-Down Procedure

1. Turn off RF signal
2. Reduce V_G to –3.5 V. Ensure I_{DQ} ~ 0 mA
3. Set V_D to 0 V
4. Turn off V_D supply
5. Turn off V_G supply

Combined $V_D = V_{D1} + V_{D2} + V_{D3}$, $V_G = V_{G12} + V_{G3}$
DC must be applied to both sides, top and bottom, of the die

Mechanical Information



Dimensions: mm; Thickness: 0.05 mm; Die x, y size tolerance: ± 0.050; Ground is backside of die

Bond Pad Description

Pad No.	Symbol	Pad Size (mm)	Description
1	RF_{IN}	0.13 x 0.16	RF Input. Matched to 50 Ω, DC blocked, DC shorted to ground
2, 12	V_{G12}	0.09 x 0.09	Gate voltage for stage 1 and 2 (1)
3, 11	V_{D1}	0..20 x 0.09	Drain voltage for stage 1 (1)
4, 10	V_{D2}	0.20 x 0.09	Drain voltage for stage 2 (1)
5, 9	V_{G3}	0.09 x 0.09	Gate voltage for stage 3 (1)
6, 8	V_{D3}	0.30 x 0.20	Drain voltage for stage 3 (1)
7	RF_{OUT}	0.13 x 0.16	RF Output. Matched to 50 Ω, DC blocked, DC shorted to ground

1. External bypassing required; refer to page 26 for recommendation

Assembly Notes

Component placement and adhesive attachment assembly notes:

- Vacuum pencils and/or vacuum collets are the preferred method of pick up.
- Air bridges must be avoided during placement.
- The force impact is critical during auto placement.

Reflow process assembly notes:

- Use AuSn (80/20) solder and limit exposure to temperatures above 300 °C to 3 – 4 minutes, maximum.
- An alloy station or conveyor furnace with reducing atmosphere should be used.
- Do not use any kind of flux.
- Coefficient of thermal expansion matching is critical for long-term reliability.
- Devices must be stored in a dry nitrogen atmosphere.

Interconnect process assembly notes:

- Thermosonic ball bonding is the preferred interconnect technique.
- Force, time, and ultrasonic are critical parameters.
- Aluminum wire should not be used.
- Devices with small pad sizes should be bonded with 0.0007-inch wire.

Handling Precautions

Parameter	Rating	Standard
ESD – Human Body Model (HBM)	2	ANSI/ESD/JEDEC JS-001

Caution!

ESD-Sensitive Device

Solderability

Use only AuSn (80/20) solder, and limit exposure to temperatures above 300 °C to 3 – 4 minutes, maximum.

RoHS Compliance

This part is compliant with 2011/65/EU RoHS directive (Restrictions on the Use of Certain Hazardous Substances in Electrical and Electronic Equipment) as amended by Directive 2015/863/EU.

This product also has the following attributes:

- Lead Free
- Halogen Free (Chlorine, Bromine)
- Antimony Free
- TBBP-A ($C_{15}H_{12}Br_4O_2$) Free
- SVHC Free
- PFOS Free

Contact Information

For the latest specifications, additional product information, worldwide sales and distribution locations:

Web: www.qorvo.com

Tel: 1-844-890-8163

Email: customer.support@qorvo.com

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