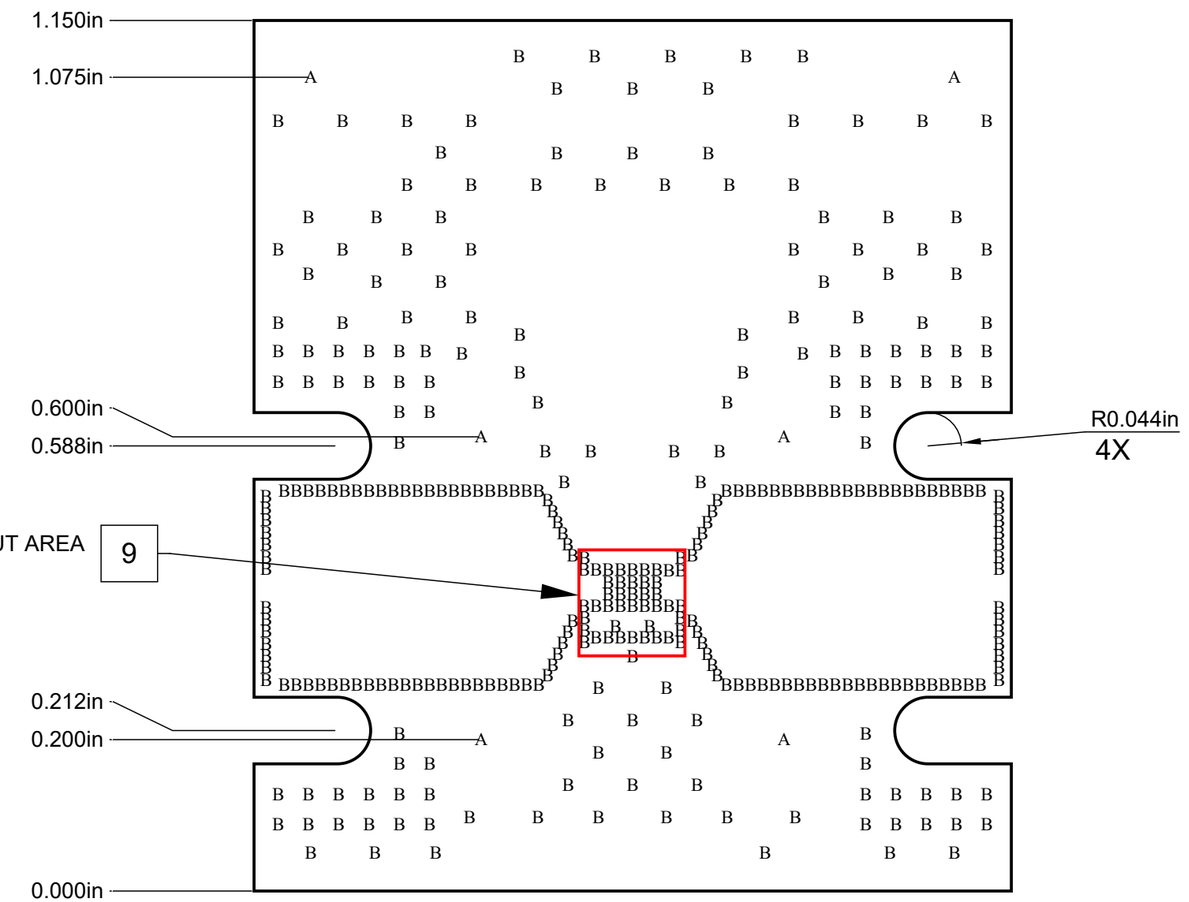
SUPPLIER MUST SEND EMAIL TO EVBHOLD@QORVO.COM IF JOB IS PLACED ON HOLD
SUPPLIER SHALL SEND A COPY OF FINAL WORKING GERBERS TO CEADS@QORVO.COM

NOTES (UNLESS OTHERWISE SPECIFIED):

1. BOARD FABRICATION METHODS MUST COMPLY WITH:
   FABRICATE IN ACCORDANCE WITH IPC-6018B, per IPC-6011, CLASS 2.
2. ARTWORK FORMAT: GERBER 274X
   GERBER DATA SUPPLIED WITH DESIRED FINAL TRACE WIDTHS. PROCESS COMPENSATION TRACE WIDTH ADJUSTMENTS TO BE DONE BY PCB FABRICATOR
3. FINISH PLATING:
   A. METAL 1(TOP) AND METAL 2(BOTTOM):
   ENEPIG (ELECTROLESS NICKEL, ELECTROLESS PALLADIUM, IMMERSION GOLD)
   ENEPIG PLATING POST SOLDERMASK (ONLY ON OPENINGS)
4. STARTING BOARD MATERIAL METAL1 AND METAL2: 0.5oz. COPPER PER LAYER
5. FINISHED BOARD THICKNESS: (SEE LAYER STACKUP) +/- .003in.
6. COPPER IS PULLED BACK PER GERBER DATA FROM EDGE OF BOARD ON METAL 1 (TOP) AND METAL 2 (BOTTOM) EXCEPT IN AREA THAT IS EDGE PLATED PER INSTRUCTIONS ON PAGE 2.
7. TOLERANCE: PC BOARD OUTLINE: ±0.002in.
8. BURRS SHALL NOT EXCEED 0.002in.
9. VIA PLATING/FILLING:
   A. ALL 10 MIL VIAS ARE TO BE COPPER-FILLED, OVER-PLATED AND PLANARIZED. FINISHED COPPER THICKNESS TO BE 0.0018 ±0.0004in.
   B. ALL OTHER PLATED THRU HOLES TO BE PLATED TO 0.0007in. MIN. THICKNESS.
10. METAL 1(TOP) AND METAL2(BOTTOM) AFTER OVERPLATING AND PLANARIZATION SHALL HAVE A MAX ALLOWABLE NEGATIVE FEATURE OF 0.0008in. AND A MAX ALLOWABLE POSITIVE FEATURE OF 0.0003in.
11. CONDUCTOR WIDTHS AND SPACING TO BE WITHIN 0.003in. OF CAD DATABASE.
12. SOLDERMASK IN PLATED-THRU HOLES IS ACCEPTABLE AS LONG AS IT DOES NOT EXIST ON BACKSIDE OF BOARD.
13. ALL HOLES TO BE LOCATED WITHIN ±0.003 OF CAD DATABASE.
14. NO VENDOR MARKING OR SERIALIZATION ALLOWED.
15. DELIVER BOARDS BAGGED AS SINGLES
16. NO ELECTRICAL TEST NEEDED.



REFERENCE NOTE: Uses QPA2598_CAL-4000[1] CAL SAP No. 291855

* FOR MULTIPLE DRILL PROCESS JOBS SEE: *.DRL, *.DR1, *.DR2, etc.

UNLESS OTHERWISE SPECIFIED: DIMENSIONS ARE IN INCHES	SAP MATERIAL NUMBER: 296713		
	APPROVAL AND RELEASE RECORDS MAINTAINED IN PDE		DATE
	DESIGNER	OMARRUFO	12/8/2020
	ENGR.	Z.DU	
INTERPRET DRAWING PER ANSI/ASME Y14.5 - 2009	PDE CONTROLLED		
THIRD ANGLE PROJECTION			
DO NOT SCALE DRAWING			

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TITLE: QPA2225 EVALUATION PCB DESIGN PACKAGE

SIZE	DOCUMENT NUMBER:	PROTOTYPE INSTANCE:	REV.
B	QPA2225-4000	N/A	A

SHEET 1 OF 5	CAD: ALTIUM DESIGNER	SCALE: 2:1

Current Date & Time: 12/14/2020 3:36

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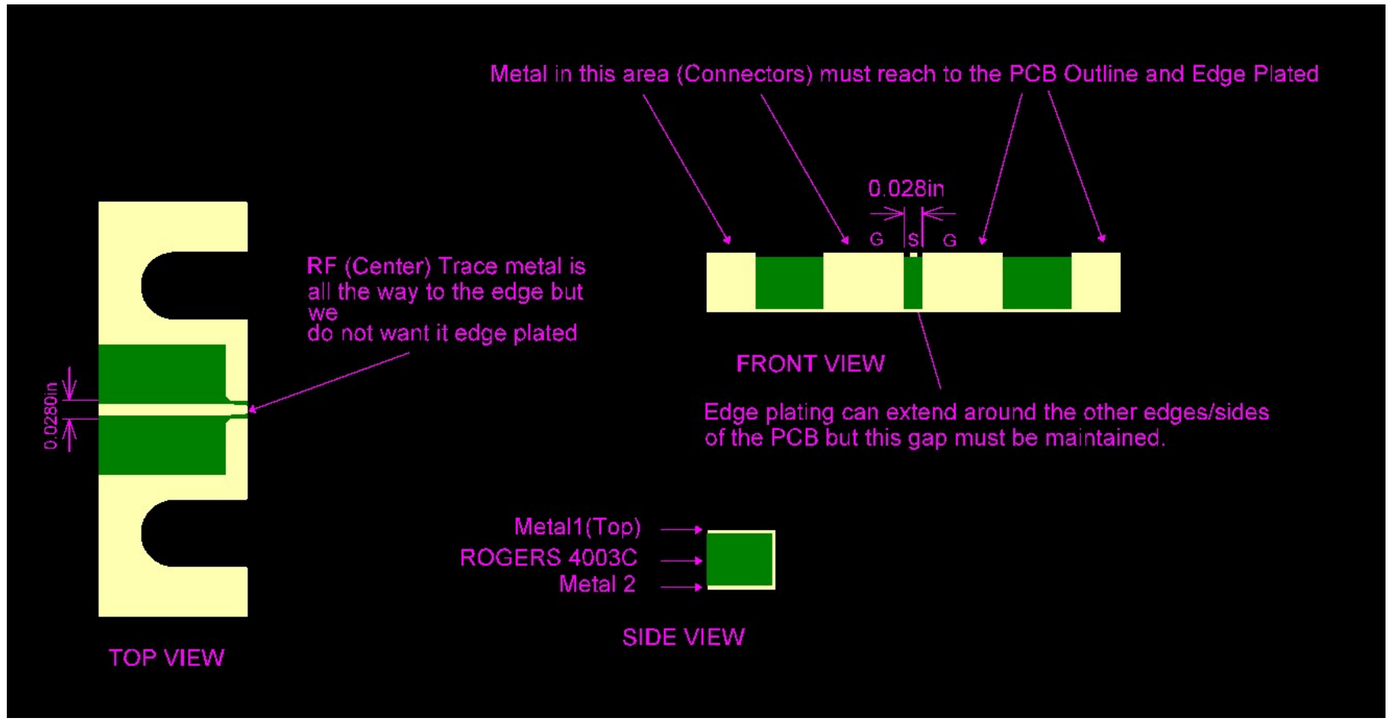
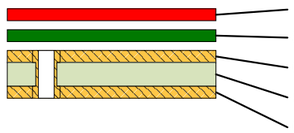


LAYER STACK LEGEND_SEE NOTE 3 FOR MATERIAL (COPPER THICKNESS IS @ FINISHED THICKNESS)



Material	Layer	Thickness	Dielectric Material	Type	Gerber
	SILKSCREEN_TOP			Legend	GTO
Surface Material	SOLDERMASK_TOP	0.0004in	Solder Resist	Solder Mask	GTS
Copper	**METAL1_TOP**	**0.0018in**		**Signal**	**GTL**
Core		*0.0080in*	*ROGERS 4003C*	*Dielectric*	
Copper	**METAL2_BOT**	**0.0018in**		**Signal**	**GBL**

Total thickness: 0.0120in

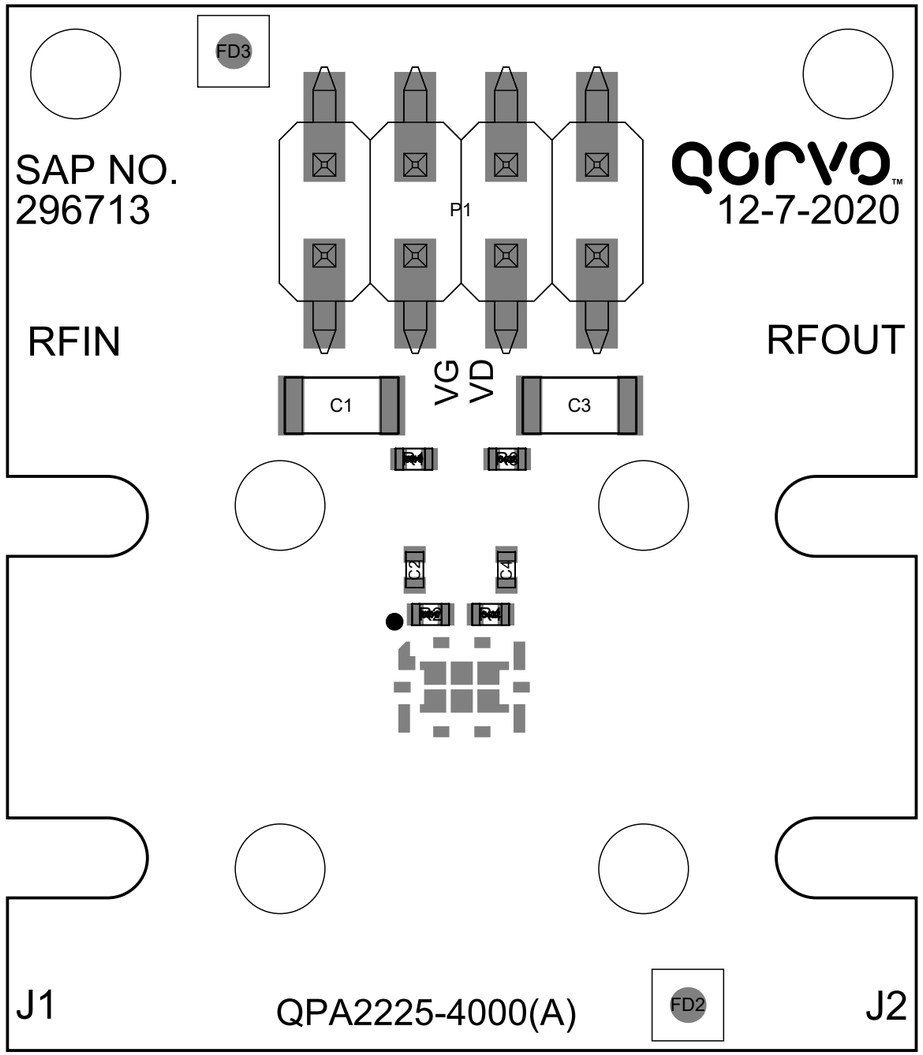
Drill Table (HOLE SIZES ARE DRILLED SIZE)

Symbol	Count	Hole Size	Plated	Drill Layer Pair
B	334	10.00mil(0.25mm)	Plated	METAL1_TOP - METAL2_BOT
A	6	100.00mil(2.54mm)	Plated	METAL1_TOP - METAL2_BOT
	340 Total			

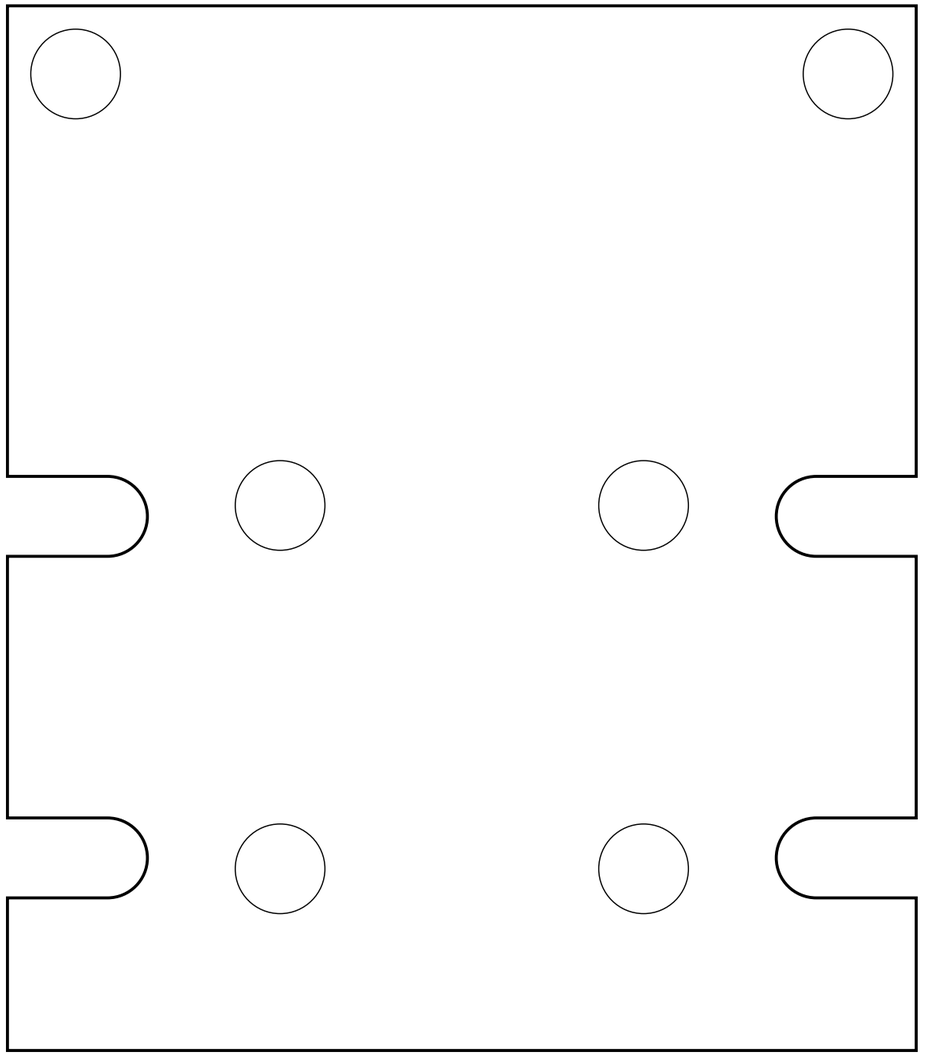
SIZE		DWG. NO.	PROTOTYPE INSTANCE:	REV.
B		QPA2225-4000	N/A	A
SHEET 2 OF 5	CAD: ALTIUM DESIGNER		SCALE: 2:1	

Current Date & Time: 12/14/2020 3:36

TOP ASSEMBLY VIEW



BOTTOM ASSEMBLY VIEW

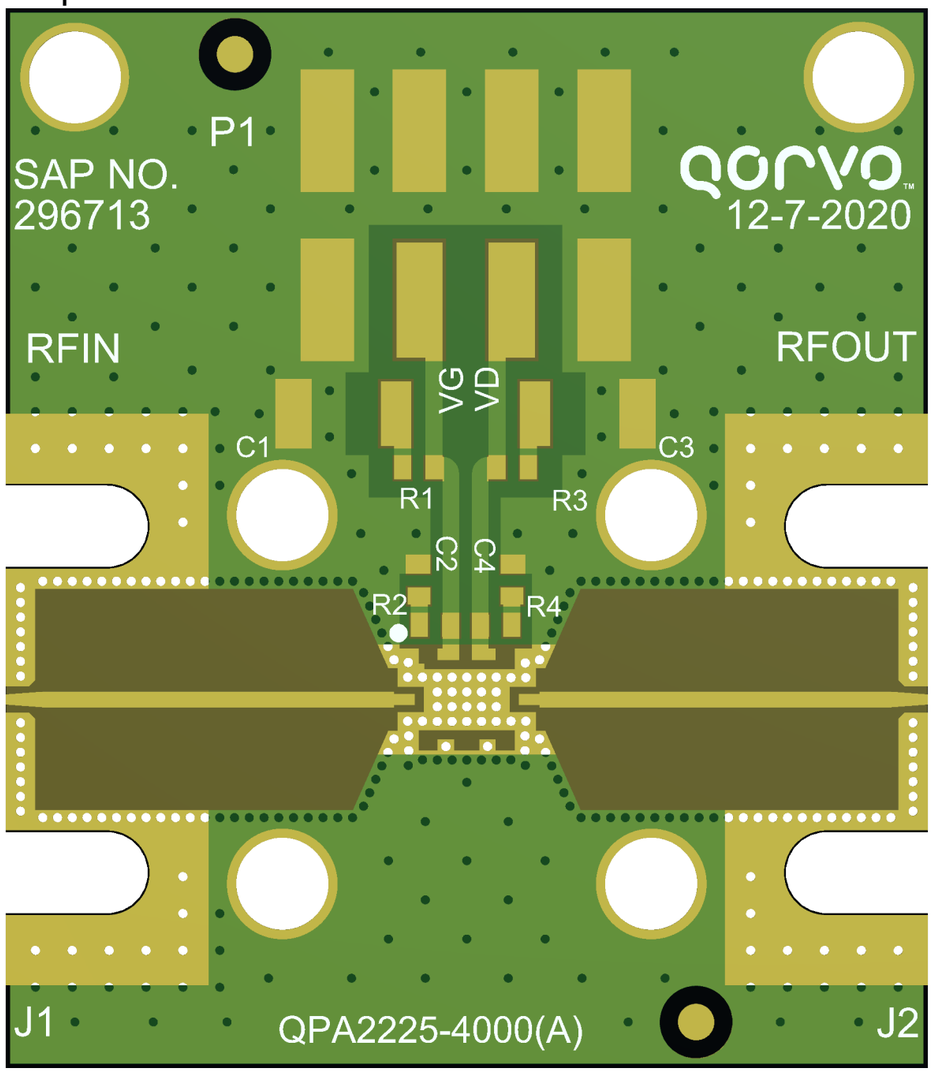


SIZE		DWG. NO.	PROTOTYPE INSTANCE:	REV.
B		QPA2225-4000	N/A	A
SHEET 3 OF 5	CAD: ALTIUM DESIGNER		SCALE:	2:1

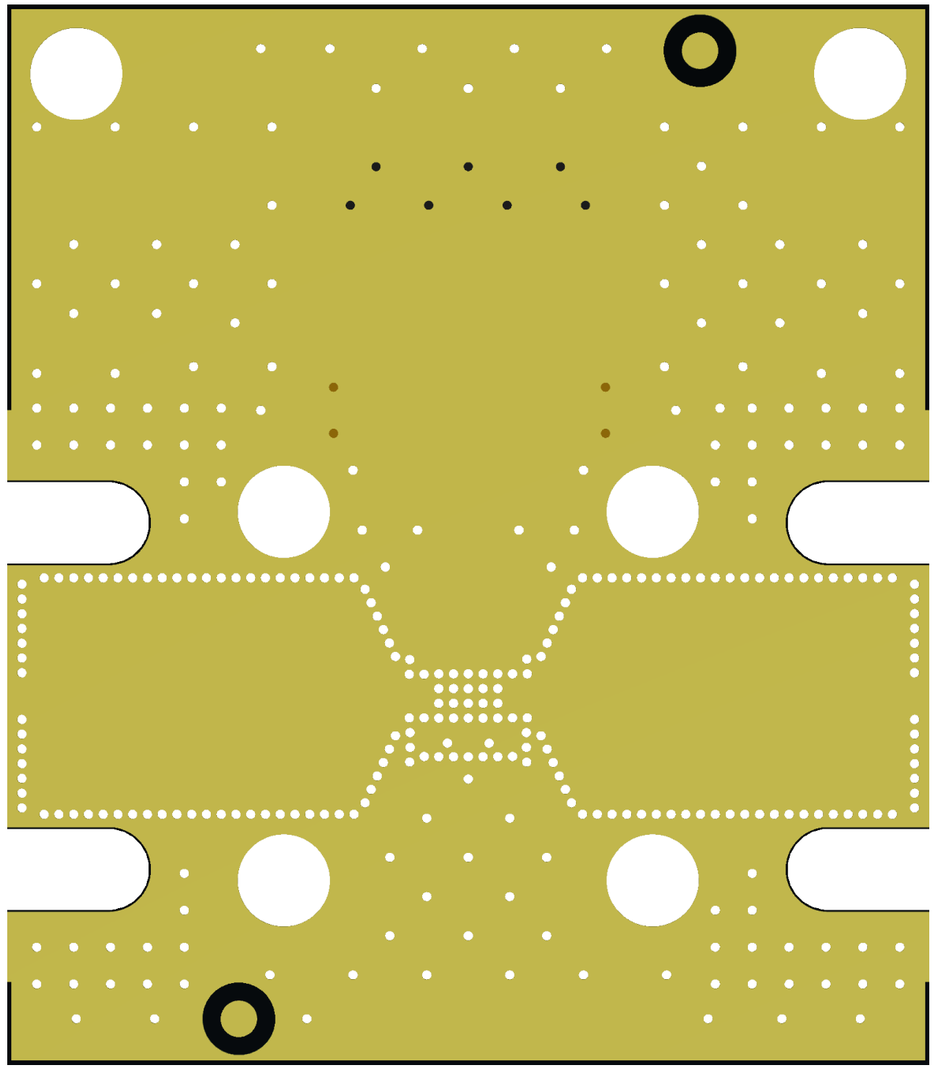
Current Date & Time: 12/14/2020 3:36

FOR-001324 REV D

Top View



Bottom View

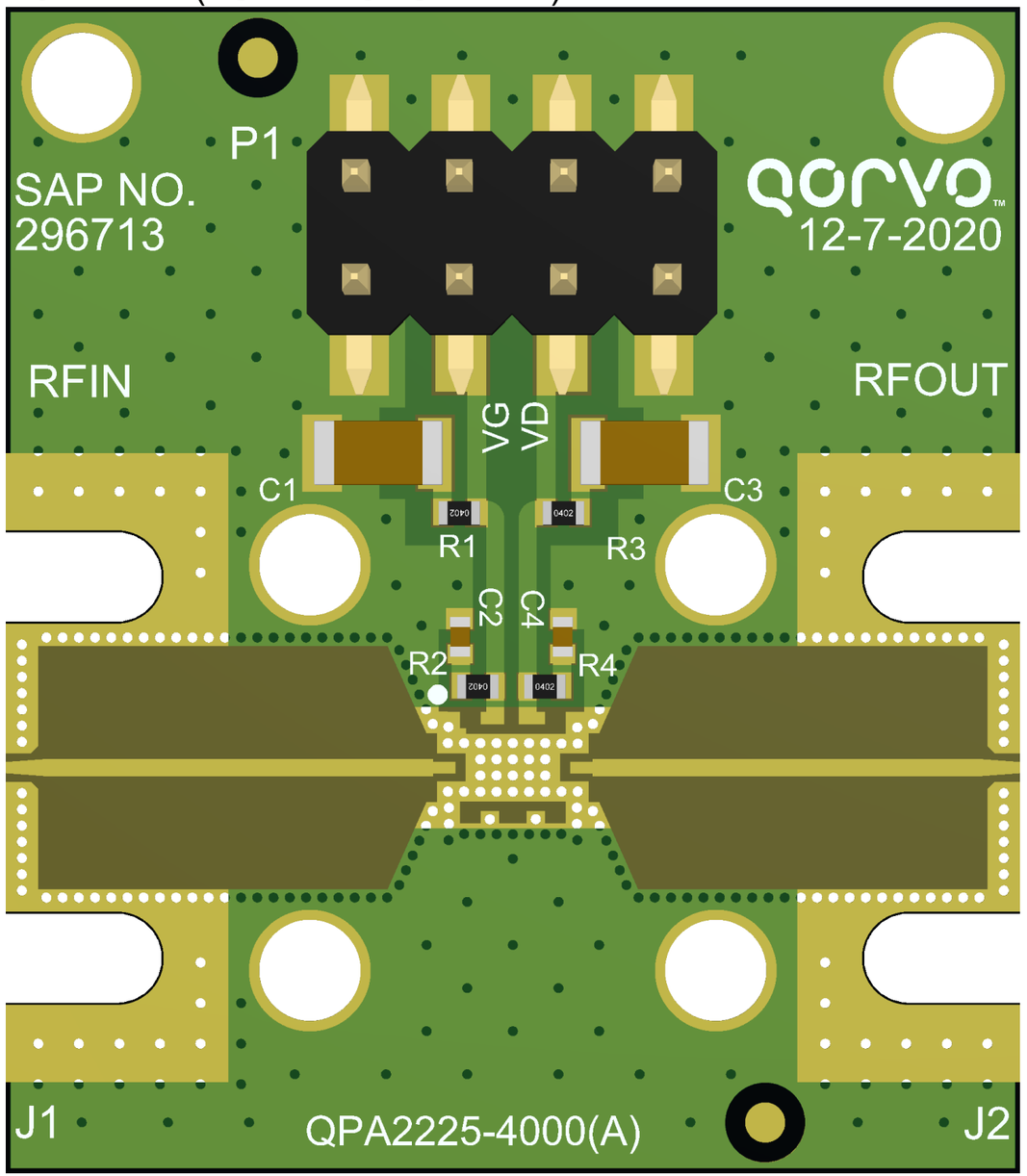


SIZE		DWG. NO.	PROTOTYPE INSTANCE:	REV.
B		QPA2225-4000	N/A	A
SHEET 4 OF 5	CAD: ALTIUM DESIGNER		SCALE:	2:1

Current Date & Time: 12/14/2020 3:36

FOR-001324 REV D

TOP VIEW (FULLY POPULATED)

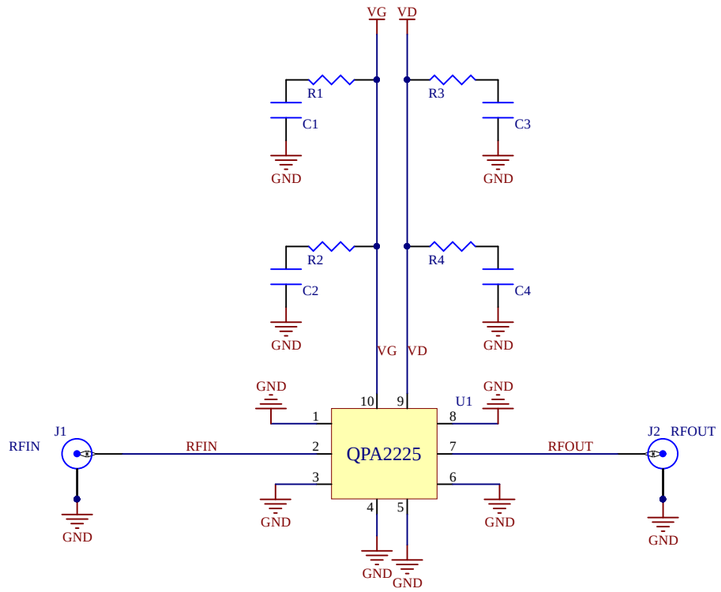


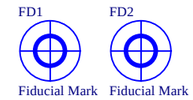
SIZE		DWG. NO.	PROTOTYPE INSTANCE:	REV.
B		QPA2225-4000	N/A	A
SHEET 5 OF 5	CAD: ALTIUM DESIGNER		SCALE: 2:1	

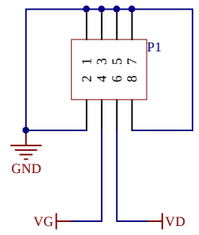
Current Date & Time: 12/14/2020 3:36

FOR-001324 REV D

REVISION HISTORY			
REV	DESCRIPTION	DATE	APPROVAL
A	INITIAL RELEASE	12/7/2020	O.MARRUFO







SAP MATERIAL NUMBER: 296713			
APPROVAL AND RELEASE RECORDS MAINTAINED IN PDE		DATE	
DESIGNER	O.MARRUFO	12/12/2020	
ENGR.	ZHUNMING DU		
PDE CONTROLLED			

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TITLE: QPA2225 EVALUATION PCB DESIGN PACKAGE

SIZE	DOCUMENT NUMBER:	PROTOTYPE INSTANCE:	REV.
B	QPA2225-4000	N/A	A

SCALE: NTS | SHEET 1 OF 1