

ACT88420 Register Definition

Abstract

This application note identifies the ACT88420 internal registers that help make this IC flexible and configurable for many applications. This is the initial released version therefore some registers might be changed in the future.

Introduction

The ACT88420 is an ActivePMU power management unit from Qorvo. It is designed to power a wide range of SSDs, processors, FPGA's, peripherals, and microcontrollers. The ACT88420 core includes Four DC/DC step down converters using integrated power FETs, and Two LDO/LSW. Each of these regulators can be configured for a wide range of output voltages through the I²C interface.

Register Types

The ACT88420 ICs contain the following register types.

Basic Volatile - Customer R/W (Read and Write) and RO (Read only). The customer can modify these register values to change IC functionality. Any changes to these registers are lost when power is recycled. The default values are fixed and cannot be changed.

Basic Non-Volatile - Customer R/W and RO. The customer can modify these register values to change IC functionality. Any changes to these registers are lost when power is recycled. The default values can be modified at the factory to optimize IC functionality for specific applications. Please consult Sales@Qorvo.com for custom options and minimum order quantities.

The ACT88420 contains six major register spaces.

MASTER REGISTERS	0x00h to 0x3Fh
Buck1 Reg	0x40h to 0x5Fh
Buck2 Reg	0x60h to 0x7Fh
Buck3 Reg	0x80h to 0x9Fh
Buck4 Reg	0xA0h to 0xBFh
LDO12 Reg	0xC0h to 0xDFh

Register Map Overview

The following table shows an overview of the ACT88420 register map.

ADDR (HEX)	7	6	5	4	3	2	1	0
Master Registers								
00	ROM_STAT	WDTIMER_ALERT	TWARN	VSYSSTAT	VIN_POK_OV	PBASTAT	VSYSWARN	PBDSTAT
01	ROM_INT_MSK	WD_ALERT_MSK	TMSK	VSYSMSK	VIN_POK_OV_MSK	PBAMSK	VSYSWARN_MSK	PBDMSK
02	RFU	RFU	VSYSWARN_RAW	VSYSDAT	RFU	RFU	RFU	PBDAT
03	GPIO8_STAT	GPIO7_STAT	GPIO6_STAT	GPIO5_STAT	GPIO4_STAT	GPIO3_STAT	GPIO2_STAT	GPIO1_STAT
04	GPIO8_TRIG	GPIO7_TRIG	GPIO6_TRIG	GPIO5_TRIG	GPIO4_TRIG	GPIO3_TRIG	GPIO2_TRIG	GPIO1_TRIG
05	GPIO8_MASK	GPIO7_MASK	GPIO6_MASK	GPIO5_MASK	GPIO4_MASK	GPIO3_MASK	GPIO2_MASK	GPIO1_MASK
06	INTADR							
07	MR	SLEEP	RFU	DPSLP	RFU	POWER_OFF	WDPCEN	WDSREN
09	TRST_DLY[2:0]			PWRCYCTIME[1:0]		PWROFF_TIME[1:0]		DIS_OVUV_SHD
0A	EN_POWERCYCLE	EN_POWEROFF	ROM_EN	VSYSMON[4:0]				
0B	IO1_DLY[2:0]			IO2_DLY[2:0]			RFU	EXTPG_BLANK
0C	IO3_DLY[2:0]			IO4_DLY[2:0]			WDTIME	RETRY_TIME
0D	RFU							
0E	RFU							
0F	RFU							
10	RFU							
11	RFU							
12	RFU							
13	RFU							
14	RFU							
15	POK_OV[2:0]			VSYSWARN[4:0]				
24	GPIO7_CTRL	GPIO6_CTRL	GPIO5_CTRL	GPIO4_CTRL	GPIO3_CTRL	GPIO2_CTRL	GPIO1_CTRL	RFU
25	RFU	AuxinCrtPHLD	RFU		RFU		RFU	
26	RFU		RFU		RFU		RFU	
27	IO5_DLY[2:0]			IO6_DLY[2:0]			RFU	RFU
28	IO7_DLY[2:0]			IO8_DLY[2:0]			LED_EN	RFU
29	LED_DUTY[2:0]			LED_PERIOD[2:0]			RFU[1:0]	
2A	RFU	RFU	RFU	RFU	RFU	RFU	RFU	RFU
2B	RFU		RFU			RFU		
2C	PMIC_ID				CMI_ID			
2E	RFU	EN_RES_PU_I2C	RFU		NLSWENPROVINL	NLSWDISILLPM	LDO2_LPM	LDO1_LPM
ADDR (HEX)	7	6	5	4	3	2	1	0

Buck1 Registers

40	POK	OV	ILIM	ILIM_WARN	UV_FLTMSK	OV_FLTMSK	ILIM_FLTMSK	IWARN_MSK
41	FRCLPMFONT	DISLPMFONT	EN_IPD	DIS_RPD	RFU	ENSKIPLPM	DRV_ADJ[1:0]	
42	RFU	BUCK 1 VSET0 [6:0]						
43	B1_CF_GPIO	BUCK 1 VSET1 [6:0]						
44	ON	PBINEN	QLTCH	SLEEP EN	RFU	DP SLEEP EN	ILIM_SET [1:0]	
45	MODE	RST	RFU			RFU		
46	RFU				SST	DISLPM	RFU	
47	PHASEDLY	PHASE	ON DELAY[2:0]			OFF DELAY[2:0]		

ADDR (HEX)	7	6	5	4	3	2	1	0
Buck2 Registers								
60	POK	OV	ILIM	RFU	UV_FLTMSK	OV_FLTMSK	ILIM_FLTMSK	RFU
61	FRE_SEL[1:0]		ENPD_LOAD	SST [2:0]			DRV_ADJ[1:0]	
62	EN_LPM	BUCK 2 VSET0 [6:0]						
63	DIS_PD	BUCK 2 VSET1 [6:0]						
64	ON	PBINEN	QLTCH	SLEEP EN	RFU	DP SLEEP EN	ILIM_SET	FCCM
65	MODE	RST	RFU			RFU		
66	RFU				IPD_LOAD_B2[1:0]		RFU	
67	IPD_LOAD_B2[3:2]		ON DELAY[2:0]			OFF DELAY[2:0]		
71	IPDLOAD_B1[3:0]				B2_I2C_CF	BUCK2_VSET	B2_CF_GPIO	B2VsetGPBK1_L
74	EN_ULPM	EN_LSilim	EN_ILIM_FB	RFU		EN_ILIM_SD	RFU	

ADDR (HEX)	7	6	5	4	3	2	1	0
Buck3 Registers								
80	POK	OV	ILIM	RFU	UV_FLTMSK	OV_FLTMSK	ILIM_FLTMSK	RFU
81	FRE_SEL[1:0]		ENPD_LOAD	SST [2:0]			DRV_ADJ [1:0]	
82	EN_LPM	BUCK 3 VSET0 [6:0]						
83	DIS_PD	BUCK 3 VSET1 [6:0]						
84	FCCM	BUCK 3 VSET2 [6:0]						
85	B3_CF_GPIO	BUCK 3 VSET3 [6:0]						
86	ON	PBINEN	QLTCH	SLEEP EN	RFU	DP SLEEP EN	ILIM_SET [1:0]	
87	MODE	RST	RFU			RFU		
88	RFU				IPD_LOAD_B3[1:0]		RFU	
89	IPD_LOAD_B3[3:2]		ON_DELAY[2:0]			OFF_DELAY[2:0]		
92	DVS_SET[1:0]		EN_ILIM_SD	RFU		EN_ULPM	EN_LSLIM	EN_ILIM_FB

ADDR (HEX)	7	6	5	4	3	2	1	0
Buck4 Registers								
A0	POK	OV	ILIM	RFU	UV_FLTMSK	OV_FLTMSK	ILIM_FLTMSK	RFU
A1	FRE_SEL[1:0]		ENPD_LOAD	SST[2:0]			DRV_ADJ [1:0]	
A2	EN_LPM	B4_CF_GPIO	BUCK 4 VSET0 [5:0]					
A3	DIS_PD	RFU	BUCK 4 VSET1 [5:0]					
A4	BUCK4_MODE	B4_I2C_CF	BUCK 4 VSET2 [5:0]					
A5	ON	PBINEN	QLTCH	SLEEP EN	RFU	DP SLEEP EN	ILIM_SET	FCCM
A6	MODE	RST	RFU			RFU		
A7	RFU				IPD_LOAD_B4[1:0]		RFU	
A8	IPD_LOAD_B4[3:2]		ON DELAY[2:0]			OFF DELAY[2:0]		
B1	RFU		EN_ILIM_SD	EN_ULPM	EN_LSILIM	EN_ILIM_FB	IOHI_ONDL[1:0]	
B2	RFU		VRANGE	LPM_MODE_LDO	RFU			RFU
B5	ON_LDO	PBINEN_LDO	QLTCH_LDO	SLEEP_EN_LDO	RFU	DPSLP_EN_LDO	ILIM_SCL_LDO	SST_LDO
B6	ON_DLY_LDO[2:0]			OFF_DL_LDO[2:0]			MODE_LDO	RST_LDO
B7	RFU				RFU			RFU

ADDR (HEX)	7	6	5	4	3	2	1	0
LDO1&2 Registers								
C0	PWR_GOOD_LDO1	OV_LDO1	ILIM_LDO1	RFU	UV_FLTMSK_LDO1	OV_FLTMSK_LDO1	ILIM_FLTMSK_LDO1	RFU
C1	SLP_EN_LDO1	DPSLP_EN_LDO1	LDO1 VSET0 [5:0]					
C2	ON_LDO1	PBINEN_LDO1	LDO1 VSET1 [5:0]					
C3	ON DELAY_LDO1[2:0]			OFF DELAY_LDO1[2:0]			MODE LDO1	RST LDO1
C4	RFU				RFU			
C5	RFU			RFU	NLSW1_ILIM_SCL	ILIM_SCL_LDO1	SST_LDO1	QLTCH_LDO1
C6	PWR_GOOD_LDO2	OV_LDO2	ILIM_LDO2	RFU	UV_FLTMSK_LDO2	OV_FLTMSK_LDO2	ILIM_FLTMSK_LDO2	RFU
C7	ILIM_SCL_LDO2	SST_LDO2	LDO2 VSET [5:0]					
C8	ON LDO2	PBINEN_LDO2	RFU	SLEEPP_EN_LDO2	DPSLP_EN_LDO2	RFU		
C9	ON DELAY_LDO2[2:0]			OFF DELAY_LDO2[2:0]			MODE LDO2	RST LDO2
CA	RFU				RFU			

MASTER REGISTERS

MSTR00 - Master Configuration Register

Address = 0x00h	Default = 0x00h	Type = Basic Volatile
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BIT	7	6	5	4	3	2	1	0
Name	ROM_STAT	WDTIMER_ALERT	TWARN	VSYSSTAT	VIN_POK_OV	PBASTAT	VSYSWARN	PBDSTAT
Default	0	0	0	0	0	0	0	0
Access	RO	RO	RO	RO	RO	RO	RO	RO

Name	Description	Notes
ROM_STAT	ROM mode status: 0 – Not in ROM mode. 1 – in ROM mode	If ROM mode is started, this bit goes high and stays latched high until is read. This register is only valid with ICs that use PWREN mode
WDTIMER_ALERT	Watch Dog Timer Alert status: 0 – the timer is not expired 1 – the timer is expired (7.4s)	If watchdog is enabled and watchdog timer times out, this bit goes high and stays latched high until is read.
TWARN	Thermal Interrupt Status: 0: Die temperature is lower than Warning threshold 1: Die temperature is higher than Warning threshold	If die temperature > 135 deg C, this bit goes high. It stays latched high until die temperature < 115 deg C and it is read.
VSYSSTAT	VSYSMON status: 0 – VSYS > VSYS Monitor Threshold 1 – VSYS < VSYS Monitor Threshold	VSYSSTAT is latched to 1 at falling edge of VIN and clear to 0 after read back this byte.
VIN_POK_OV	VIN Over Voltage (interrupt) status: 0 – VIN < VIN_POK_OV 1 – VIN > VIN_POK_OV	Input above VIN_POK_OV threshold VIN_POK_OV=1: If VIN_POK_nMASK=0 it provides real time status of POK_OV If VIN_POK_nMASK=1, POK_OV status is latched until POK_OV is read via I2C.
PBASTAT	Push - Button assert Status: 0 – Push-Button is not assert 1 – Push-Button asserting happens	Push-Button mode only. . When the Push Button is asserted this bit goes high and stays latched high until is read.
VSYSWARN	VSYSWARN status: 0 – VIN > VSYS_WARN 1 – VIN < VSYS_WARN	VSYSWARN is latched to 1 at falling edge of VIN and clear to 0 after read back this byte.
PBDSTAT	Push - Button De-assert Status: 1 – Push-Button de-asserting happen 0 – Push-Button is not de-assert.	Push-Button mode only. When Push Button de-asserting happens, this bit goes high and stays latched high until it is read.

MSTR01 - Master Configuration Register

Address = 0x01h	Default = 0xFFh	Type = Basic Volatile
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BIT	7	6	5	4	3	2	1	0
Name	ROM_INT_MSK	WD_ALERT_MSK	TMSK	VSYSMSK	VIN_POK_OV_MSK	PBAMSK	VSYSWARN_MSK	PBDMSK
Default	1	1	1	1	1	1	1	1
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Name	Description	Notes
ROM_INT_MSK	Mask interrupt when IC is in ROM mode: 0: Not mask interrupt 1: Mask interrupt	Mask the interrupt in ROM mode.
WD_ALERT_MSK	Watch Dog timer Alert Mask: 0: Not mask interrupt 1: Mask interrupt	Mask the interrupt of Watch Dog Timer Expiration.
TMSK	Thermal Interrupt Mask: 0: Not mask interrupt 1: Mask interrupt	Mask the interrupt of Thermal Warning Assert.
VSYS_MSK	SYSMON Interrupt Mask: 0: Not mask interrupt 1: Mask interrupt	Mask the interrupt of VSYSMON Assert.
VIN_POK_OV_MSK	VIN POK OV Interrupt Mask: 0: Not mask interrupt 1: Mask interrupt	Mask the interrupt of VIN POK OV Assert.
PBAMSK	Push - Button Assert Interrupt Mask: 0: Not mask interrupt 1: Mask interrupt	Mask the interrupt of Push - Button Assert. Recommend: should readback REG0x00 to clear all PB status before unmask PBA.
VSYSWARN_MSK	SYSWARN Interrupt Mask: 0: Not mask interrupt 1: Mask interrupt	Mask the interrupt of VSYSWARN Assert.
PBDMSK	Push - Button De-Assert Interrupt Mask: 0: Not mask interrupt 1 – Mask interrupt	Mask the interrupt of Push - Button De-Assert. Recommend: should readback REG0x00 to clear all PB stats before unmask PBD

MSTR02 - Master Configuration Register

Address = 0x02h	Default = 0x00h	Type = Basic Volatile
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BIT	7	6	5	4	3	2	1	0
Name	RFU [1:0]		VSYSWARN_RAW	VSYSDAT	RFU [2:0]			PBDAT
Default	00		0	0	000			0
Access	RO		RO	RO	R/W			RO
Name		Description					Notes	
RFU [1:0]		Reserved for Future Use					Do not change this register value. Changing the register value can affect IC functionality.	
VSYSWARN_RAW		VSYSWARN Raw Data: 0 – VIN is lower than VSYSWARN 1 – VIN is higher than VSYSWARN					Real time status of the AVIN voltage being above or below the SYSWARN threshold	
VSYSDAT		VSYSMON Raw Data: 0 – VIN is lower than VSYSMON 1 – VIN is higher than VSYSMON					Real time status of the AVIN voltage being above or below the SYSMON threshold	
RFU [2:0]		Reserved for Future Use					Do not change this register value. Changing the register value can affect IC functionality.	
PBDAT		Push - Button Raw Data: 0 – Push Button is being asserted 1 – Push Button is de-assert					Real time status of the push button pin. Only valid for ICs with pushbutton functionality	

MSTR03 - Master Configuration Register

Address = 0x03h	Default = 0x00h	Type = Basic Volatile
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BIT	7	6	5	4	3	2	1	0
	GPIO8_STAT	GPIO7_STAT	GPIO6_STAT	GPIO5_STAT	GPIO4_STAT	GPIO3_STAT	GPIO2_STAT	GPIO1_STAT
Default	0	0	0	0	0	0	0	0
Access	RO	RO	RO	RO	RO	RO	RO	RO
Name		Description				Notes		
GPIO8_STAT		0 – GPIO8 input is logic low 1 – GPIO8 input is logic high				Shows the 2-state GPIOx input real-time status when the GPIO is configured as an input.		
GPIO7_STAT		0 – GPIO7 input is logic low 1 – GPIO7 input is logic high						
GPIO6_STAT		0 – GPIO6 input is logic low 1 – GPIO6 input is logic high						
GPIO5_STAT		0 – GPIO5 input is logic low 1 – GPIO5 input is logic high						
GPIO4_STAT		0 – GPIO4 input is logic low 1 – GPIO4 input is logic high						
GPIO3_STAT		0 – GPIO3 input is logic low 1 – GPIO3 input is logic high						
GPIO2_STAT		0 – GPIO2 input is logic low 1 – GPIO2 input is logic high						
GPIO1_STAT		0 – GPIO1 input is logic low 1 – GPIO1 input is logic high						

MSTR04 - Master Configuration Register

Address = 0x04h	Default = 0x00h	Type = Basic Volatile
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BIT	7	6	5	4	3	2	1	0
	GPIO8_TRIG	GPIO7_TRIG	GPIO6_TRIG	GPIO5_TRIG	GPIO4_TRIG	GPIO3_TRIG	GPIO2_TRIG	GPIO1_TRIG
Default	0	0	0	0	0	0	0	0
Access	RO	RO	RO	RO	RO	RO	RO	RO

Name	Description	Notes
GPIO8_TRIG	0 – GPIO8 input logic level has not changed 1 – GPIO8 input logic level has changed	<p>GPIOx toggle detect when GPIOx is configured as an input.</p> <p>Set to 1 when GPIOx change status and latched until read back to clear to 0.</p>
GPIO7_TRIG	0 – GPIO7 input logic level has not changed 1 – GPIO7 input logic level has changed	
GPIO6_TRIG	0 – GPIO6 input logic level has not changed 1 – GPIO6 input logic level has changed	
GPIO5_TRIG	0 – GPIO5 input logic level has not changed 1 – GPIO5 input logic level has changed	
GPIO4_TRIG	0 – GPIO4 input logic level has not changed 1 – GPIO4 input logic level has changed	
GPIO3_TRIG	0 – GPIO3 input logic level has not changed 1 – GPIO3 input logic level has changed	
GPIO2_TRIG	0 – GPIO2 input logic level has not changed 1 – GPIO2 input logic level has changed	
GPIO1_TRIG	0 – GPIO1 input logic level has not changed 1 – GPIO1 input logic level has changed	

MSTR05 - Master Configuration Register

Address = 0x05h	Default = 0xFFh	Type = Basic Volatile
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BIT	7	6	5	4	3	2	1	0
Name	GPIO8_MASK	GPIO7_MASK	GPIO6_MASK	GPIO5_MASK	GPIO4_MASK	GPIO3_MASK	GPIO2_MASK	GPIO1_MASK
Default	1	1	1	1	1	1	1	1
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Name	Description	Notes
GPIO8_MASK	0: trigger the interrupt when GPIO8 Input change status 1: not trigger the interrupt when GPIO8 Input change status	<p>GPIOx can generate interrupt individual when GPIOx config as input, MASK bit NOT set and Toggle event happens.</p> <p>If not masked, a GPIO input logic level status change triggers an interrupt in register 0x04h.</p> <p>GPIOx can generate interrupt individual when GPIOx config as input, MASK bit NOT set and Toggle event happens.</p>
GPIO7_MASK	0: trigger the interrupt when GPIO7 Input change status 1: not trigger the interrupt when GPIO7 Input change status	
GPIO6_MASK	0: trigger the interrupt when GPIO6 Input change status 1: not trigger the interrupt when GPIO6 Input change status	
GPIO5_MASK	0: trigger the interrupt when GPIO5 Input change status 1: not trigger the interrupt when GPIO5 Input change status	
GPIO4_MASK	0: trigger the interrupt when GPIO4 Input change status 1: not trigger the interrupt when GPIO4 Input change status	
GPIO3_MASK	0: trigger the interrupt when GPIO3 Input change status 1: not trigger the interrupt when GPIO3 Input change status	
GPIO2_MASK	0: trigger the interrupt when GPIO2 Input change status 1: not trigger the interrupt when GPIO2 Input change status	
GPIO1_MASK	0: trigger the interrupt when GPIO1 Input change status 1: not trigger the interrupt when GPIO1 Input change status	

MSTR06 - Master Configuration Register

Address = 0x06h	Default = 0x00h	Type = Basic Volatile
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BIT	7	6	5	4	3	2	1	0
Name	INTADR [7:0]							
Default	00000000							
Access	RO							

Name	Description	Notes
INTADR [7:0]	<p>Indicates the interrupt tile address:</p> <p>Value: Tile</p> <p>0x00: MSTR</p> <p>0x01: GPIO</p> <p>0x40: BUCK1</p> <p>0x60: BUCK2</p> <p>0x80: BUCK3</p> <p>0xA0: BUCK4</p> <p>0xC1: LDO1</p> <p>0xC2: LDO2</p>	<p>The value contained in this register identifies the I²C register block that generated the interrupt. This lets the user know what part of the IC generated an interrupt.</p> <p>Real time value of the interrupt address.</p>

MSTR07 - Master Configuration Register

Address = 0x07h	Default = 0x00h	Type = Basic Volatile
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BIT	7	6	5	4	3	2	1	0
Name	MR	SLEEP	RFU	DPSLP	RFU	POWER_OFF	WDPCEN	WDSREN
Default	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Name	Description	Notes
MR	0 – No Manual Reset 1 – Initiate a Manual Reset or Power Cycle by setting this bit by I ² C	Writing a 1 to this bit clears all VM registers, move IC to POWER OFF state, then restarts after 0.5s.
SLEEP	0 – Can make IC exit SLEEP state 1 – Can make IC enter SLEEP state	See datasheet for details on how this bit puts IC into SLEEP state
RFU	Reserved for Future Use	Do not change this register value. Changing the register values can affect IC functionality.
DPSLP	0 – Can make IC exit DPSLP state. 1 – Can make IC enter DPSLP state.	See datasheet for details on how this bit puts IC into DPSLP state
RFU	Reserved for Future Use	Do not change this register value. Changing the register values can affect IC functionality.
POWER_OFF	0 – IC is operating normally 1 – Clear all VM register, IC move to POWER OFF state.	Write from 1 to 0 to move the IC from POWER OFF to POWER ON
WDPCEN	0 – IC does not power cycle if the watchdog timer times out 1 – IC power cycles if the watchdog timer times out(8s),IC will turn off REGs follow sequence, after 0.5s turn-on again.	Note that this is a higher priority than WDSREN
WDSREN	0 – Disables a soft reset if the watchdog timer times out 1 – Enables a soft reset if the watchdog timer times out	

MSTR09 - Master Configuration Register

Address = 0x09h	Default = 0x80h	Type = Basic Non-Volatile
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BIT	7	6	5	4	3	2	1	0
Name	TRST_DLY[2:0]			PWRCYCTIME[1:0]		PWROFF_TIME[1:0]		DIS_OVUV_SHD
Default	100			00		00		0
Access	R/W			R/W		R/W		R/W

Name	Description	Notes
TRST_DLY [2:0]	Setting delay time for nRESET: 000 – 0.5ms 001 – 1ms 010 – 2ms 011 – 4ms 100 – 8ms 101 – 16ms 110 – 32ms 111 – 64ms	
PWRCYCTIME[1:0]	Setting timer for power cycle: 00: 1s<t<4s (trigger at released). 01: 4s<t<8s (trigger at released). 10: 8s, trigger at exact 8s. 11: 12s, trigger at exact 12s.	
PWROFF_TIME[1:0]	Setting timer for power off: 00: 1s<t<4s (trigger at released). 01: 4s<t<8s (trigger at released). 10: 8s, trigger at exact 8s. 11: 12s, trigger at exact 12s.	
DIS_OVUV_SHD	Disable UVOV of REGs: 0 – If an output enters an UV/OV fault condition, the IC enters the OVUV Fault State 1 – If an output enters an UV/OV fault condition, the IC does not enter UVOV Fault State	

MSTR0A - Master Configuration Register

Address = 0x0Ah	Default = 0x80h	Type = Basic Non-Volatile
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BIT	7	6	5	4	3	2	1	0
Name	EN_POWERCYCLE	EN_POWEROFF	ROM_EN	VSYSMON [4:0]				
Default	1	0	0	00000				
Access	R/W	R/W	R/W	R/W				

Name	Description	Notes
EN_POWERCYCLE	0 – Disable Power Cycle by Push-Button 1 – Enable Power Cycle by Push-Button	
EN_POWEROFF	0 – Disable Power OFF by Push-Button 1 – Enable Power OFF by Push-Button	
ROM_EN	0 – Disable ROM mode 1 – Enable ROM mode	
VSYSMON [4:0]	VSYSMON setting (falling, hysteresis =50mV) 00000: 2.725V to 01111: 3.1V, Step size = 25mV 01111 to 11111: 3.1V	

MSTR0B - Master Configuration Register

Address = 0x0Bh	Default = 0x00h	Type = Basic Non-Volatile
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BIT	7	6	5	4	3	2	1	0
Name	IO1_DLY[2:0]			IO2_DLY[2:0]			RFU	EXTPG_BLANK
Default	000			000			0	0
Access	R/W			R/W			R/W	R/W

Name	Description	Notes
IO1_DLY [2:0]	000: 0ms 001: 0.25ms 010: 0.5ms 011: 0.75ms 100: 1ms 101: 2ms 110: 4ms 111: 8ms	Delay setting for both input mode/ output OD mode of GPIO1
IO2_DLY [2:0]	000: 0ms 001: 0.25ms 010: 0.5ms 011: 0.75ms 100: 1ms 101: 2ms 110: 4ms 111: 8ms	Delay setting for both input mode/ output OD mode of GPIO2
RFU	Reserved for Future Use	Do not change this register value. Changing the register values can affect IC functionality.
EXTPG_BLANK	0: 20ms 1: 40ms	External power good blanking time

MSTR0C - Master Configuration Register

Address = 0x0Ch	Default = 0x00h	Type = Basic Non-Volatile
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BIT	7	6	5	4	3	2	1	0
Name	IO3_DLY[2:0]			IO4_DLY[2:0]			WDTIME	RETRY_TIME
Default	000			000			0	0
Access	R/W			R/W			R/W	R/W

Name	Description	Notes
IO3_DLY [2:0]	000: 0ms 001: 0.25ms 010: 0.5ms 011: 0.75ms 100: 1ms 101: 2ms 110: 4ms 111: 8ms	Delay setting for both input mode/ output OD mode of GPIO3
IO4_DLY [2:0]	000: 0ms 001: 0.25ms 010: 0.5ms 011: 0.75ms 100: 1ms 101: 2ms 110: 4ms 111: 8ms	Delay setting for both input mode/ output OD mode of GPIO4
WDTIME	Watch dog timer setting: 0: 7s 1: 20s	
RETRY_TIME	Retry timer setting: 0: 200ms 1: 250ms	

MSTR0D ~ 14 – GPIOs Mode Configuration

Address = 0x0Dh-0x14h	Default = N/A	Type = Basic Non-Volatile
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BIT	7	6	5	4	3	2	1	0
Name	RFU [7:0]							
Default	N/A							
Access	R/W							

Name	Description	Notes
RFU [7:0]	Reserved for Future Use	Do not change these register values. Changing the register values can affect IC functionality.

MSTR15 – Master Configuration Register

Address = 0x15h	Default = 0x00h	Type = Basic Non-Volatile
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BIT	7	6	5	4	3	2	1	0
Name	POK_OV [2:0]			VSYSWARN [4:0]				
Default	000			00000				
Access	R/W			R/W				

Name	Description	Notes
POK_OV [2:0]	VIN_POK_OV setting (rising): 000 – 3.50V 001 – 3.80V 010 – 4.11V 011 – 4.40V 100 – 4.70V 101 – 5.00V 110 – 5.30V 111 – 5.60V	
VSYSWARN [4:0]	VSYSWARN setting (falling): 00000: 2.775V to 01111: 3.15V Step size = 25mV 01111 to 11111: 3.15V	

MSTR24 – Master Configuration Register

Address = 0x24h	Default = 0x00h	Type = Basic Volatile
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BIT	7	6	5	4	3	2	1	0
Name	GPIO7_CTRL	GPIO6_CTRL	GPIO5_CTRL	GPIO4_CTRL	GPIO3_CTRL	GPIO2_CTRL	GPIO1_CTRL	RFU
Default	0	0	0	1	1	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Name	Description	Notes
GPIO7_CTRL	0: HiZ Open drain at GPIO7 1: pull down Open drain at GPIO7	Control GPIO7
GPIO6_CTRL	0: HiZ Open drain at GPIO6 1: pull down Open drain at GPIO6	Control GPIO6
GPIO5_CTRL	0: HiZ Open drain at GPIO5 1: pull down Open drain at GPIO5	Control GPIO5
GPIO4_CTRL	0: HiZ Open drain at GPIO4 1: pull down Open drain at GPIO4	Control GPIO4
GPIO3_CTRL	0: HiZ Open drain at GPIO3 1: pull down Open drain at GPIO3	Control GPIO3
GPIO2_CTRL	0: HiZ Open drain at GPIO2 1: pull down Open drain at GPIO2	Control GPIO2
GPIO1_CTRL	0: HiZ Open drain at GPIO1 1: pull down Open drain at GPIO1	Control GPIO1
RFU	Reserved for Future Use	Do not change this register value. Changing the register value can affect IC functionality.

MSTR25 – Master Configuration Register

Address = 0x25h	Default = 0x6Ah	Type = Basic Non-Volatile
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BIT	7	6	5	4	3	2	1	0
Name	RFU	AuxinCrt PHLD	RFU		RFU		RFU	
Default	0	1	10		10		10	
Access	R/W	R/W	R/W		R/W		R/W	

Name	Description	Notes
RFU	Reserved for Future Use	Do not change these register values. Changing the register values can affect IC functionality.
AuxinCrtPHLD	Advanced factory bits.	Do not change this register value. Changing the register value can affect IC functionality.
RFU	Reserved for Future Use	Do not change these register values. Changing the register values can affect IC functionality.
RFU	Reserved for Future Use	Do not change these register values. Changing the register values can affect IC functionality.
RFU	Reserved for Future Use	Do not change these register values. Changing the register values can affect IC functionality.

MSTR26 – Master Configuration Register

Address = 0x26h	Default = 0xE5h	Type = Basic Non-Volatile
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BIT	7	6	5	4	3	2	1	0
Name	RFU		RFU		RFU		RFU	
Default	11		10		01		01	
Access	R/W		R/W		R/W		R/W	

Name	Description	Notes
RFU	Reserved for Future Use	Do not change these register values. Changing the register values can affect IC functionality.
RFU	Reserved for Future Use	Do not change these register values. Changing the register values can affect IC functionality.
RFU	Reserved for Future Use	Do not change these register values. Changing the register values can affect IC functionality.
RFU	Reserved for Future Use	Do not change these register values. Changing the register values can affect IC functionality.

MSTR27 - Master Configuration Register

Address = 0x27h	Default = 0x00h	Type = Basic Non-Volatile
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BIT	7	6	5	4	3	2	1	0
Name	IO5_DLY[2:0]			IO6_DLY[2:0]			RFU	RFU
Default	000			000			0	0
Access	R/W			R/W			R/W	R/W

Name	Description	Notes
IO5_DLY [2:0]	Delay setting for both input mode/ output OD mode of GPIO5: 000: 0ms 001: 0.25ms 010: 0.5ms 011: 0.75ms 100: 1ms 101: 2ms 110: 4ms 111: 8ms	
IO6_DLY [2:0]	Delay setting for both input mode/ output OD mode of GPIO6: 000: 0ms 001: 0.25ms 010: 0.5ms 011: 0.75ms 100: 1ms 101: 2ms 110: 4ms 111: 8ms	
RFU	Reserved for Future Use	Do not change this register value. Changing the register value can affect IC functionality.
RFU	Reserved for Future Use	Do not change this register value. Changing the register value can affect IC functionality.

MSTR28 - Master Configuration Register

Address = 0x28h	Default = 0x00h	Type = Basic Non-Volatile
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BIT	7	6	5	4	3	2	1	0
Name	IO7_DLY[2:0]			IO8_DLY[2:0]			LED_EN	RFU
Default	000			000			0	0
Access	R/W			R/W			R/W	R/W

Name	Description	Notes
IO7_DLY [2:0]	Delay setting for both input mode/ output OD mode of GPIO7: 000: 0ms 001: 0.25ms 010: 0.5ms 011: 0.75ms 100: 1ms 101: 2ms 110: 4ms 111: 8ms	
IO8_DLY [2:0]	Delay setting for both input mode/ output OD mode of GPIO8: 000: 0ms 001: 0.25ms 010: 0.5ms 011: 0.75ms 100: 1ms 101: 2ms 110: 4ms 111: 8ms	
LED_EN	0: disable LED current of GPIO8 and release CLK to save IQ current 1: enable LED for GPIO8	
RFU	Reserved for Future Use	Do not change this register value. Changing the register value can affect IC functionality.

MSTR29 - Master Configuration Register

Address = 0x29h	Default = 0x00h	Type = Basic Non-Volatile
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BIT	7	6	5	4	3	2	1	0
Name	LED_DUTY[2:0]			LED_PERIOD[2:0]			RFU[1:0]	
Default	000			000			0	
Access	R/W			R/W			R/W	

Name	Description	Notes
LED_DUTY[2:0]	Select LED duty option: 000: 12.5% 001: 25% 010: 37.5% 011: 50% 100: 62.5% 101: 75% 110: 87.5% 111: 100%	
LED_PERIOD[2:0]	Select period f for LED lighting: 000: 0.466s 001: 0.932s 010: 1.864s 011: 2.796s 100: 3.728s 101: 5.590s 110: 7.450s 111: 11.184ms	
RFU	Reserved for Future Use	Do not change this register value. Changing the register value can affect IC functionality.

MSTR2A - RFU

Address = 0x2Ah	Default = N/A	Type = Basic Non-Volatile
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BIT	7	6	5	4	3	2	1	0
Name	RFU [7:0]							
Default	N/A							
Access	R/W							

Name	Description	Notes
RFU [7:0]	Reserved for Future Use	Do not change these register values. Changing the register values can affect IC functionality.

MSTR2B – Master Configuration Register

Address = 0x2Bh	Default = N/A	Type = Basic Non-Volatile
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BIT	7	6	5	4	3	2	1	0
Name	RFU		RFU			RFU		
Default	N/A		N/A			N/A		
Access	R/W		R/W			R/W		

Name	Description	Notes
RFU	Reserved for Future Use	Do not change these register values. Changing the register values can affect IC functionality.

MSTR2C – Master Configuration Register

Address = 0x2Ch	Default = 0x00h	Type = Basic Non-Volatile
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BIT	7	6	5	4	3	2	1	0
Name	PMIC_ID[3:0]				CMI_ID[3:0]			
Default					0000			
Access	R/W				R/W			

Name	Description	Notes
PMIC_ID[3:0]	PMIC ID	
CMI_ID[3:0]	CMI ID	

MSTR2E – Master Configuration Register

Address = 0x2Eh	Default = 0x20h	Type = Basic Non-Volatile
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BIT	7	6	5	4	3	2	1	0
Name	RFU	EN_RES_PU_I2C	RFU		NLSWENPROVINL	NLSWDISILLPM	LDO2_LPM	LDO1_LPM
Default	0	0	1		1	0	0	0
Access	R/W	R/W	R/W		R/W	R/W	R/W	R/W

Name	Description	Notes
RFU	Reserved for Future Use	Do not change this register value. Changing the register value can affect IC functionality.
EN_RES_PU_I2C	0: not enable 5k resistor pull up for SDA & SCL 1: enable 5k resistor pull up for SDA & SCL	
L1_TRILOWDL[1:0]	Reserved for Future Use	Do not change this register value. Changing the register value can affect IC functionality.
NLSWENPROVINL	Enable current protection for NLSW when VINL is low: 0: Disable 1: Enable	
NLSWDISILLPM	Disable ILIM protection in LPM of NLSW: 0: Enable ILIM 1: Disable ILIM	
LDO2_LPM	Low power mode for LDO2: 0: Normal mode 1: Force the LDO in LPM, no ILIM, no OV	
LDO1_LPM	Low power mode for LDO1: 0: Normal mode 1: Force the LDO in LPM, no ILIM, no OV	

BUCK1 REGULATORS REGISTERS

B1_REG00 – Buck1 Configuration Register

Address = 0x40h	Default = 0x0Fh	Type = Basic Volatile
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BIT	7	6	5	4	3	2	1	0
Name	POK	OV	ILIM	ILIM_WARN	UV_FLTMSK	OV_FLTMSK	ILIM_FLTMSK	IWARN_MSK
Default	0	0	0	0	1	1	1	1
Access	RO	RO	RO	RO	R/W	R/W	R/W	R/W

Name	Description	Notes
POK	POK status: 0 – Buck1 voltage is below the power good threshold 1 – Buck1 voltage is above the power good threshold	Provides real-time power good status
OV	OV status: 0 – Buck1 voltage is below the overvoltage threshold 1 – Buck1 voltage is above the overvoltage threshold	When output voltage > OV, this bit goes high. It is latched high until output voltage < OV and the bit is read.
ILIM	ILIM status: 0: Output ILIM is not triggered 1: Output ILIM is triggered	If the peak switch current reaches 122% of ILIMSET threshold, this bit goes high. It is latched high until peak switch current < 122% of ILIMSET and this bit is read.
ILIM_WARN	ILIM Warning status. 0: Output ILIM warning is not triggered 1: Output ILIM warning is triggered	If the peak switch current reaches the ILIMSET threshold for 16 consecutive switching cycles, this bit goes high. It is latched high until peak switch current < ILIMSET and this bit is read.
UV_FLTMSK	Mask VOUT UV interrupt: 0: Unmask Vout UV interrupt 1: Default mask Vout UV interrupt	When 1, the Buck1 POK signal is masked and does not go to the master controller. This prevents Buck1 from asserting the nIRQ pin when it is disabled or drops out of regulation. POK still provides real-time power good status.
OV_FLTMSK	Mask Vout OV interrupt: 0: Unmask Vout OV interrupt 1: Default mask Vout OV interrupt	When 1, the Buck1 OV signal is masked and does not go to the master controller. This prevents Buck1 from asserting the nIRQ pin when it is above regulation limits. OV still provides OV status.
ILIM_FLTMSK	Mask ILIM interrupt: 0: Unmask ILM interrupt	When 1, the Buck1 ILIM signal is masked and does not go to the master controller. This prevents Buck1 from asserting the nIRQ pin when it is above regulation limits. ILIM still provides current limit status.

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	1: Default mask ILIM interrupt	
IWARN_MSK	Mask ILIM warning interrupt: 0: Unmask ILM warning interrupt 1: Default mask ILIM warning interrupt	When 1, the Buck1 ILIM_WARN bit is masked and does not go to the master controller. This prevents Buck1 from asserting the nIRQ pin when it is above regulation limits. ILIM_WARN still provides current limit warning status.

B1_REG01 – Buck1 Configuration Register

Address = 0x41h	Default = 0x40h	Type = Basic Non-Volatile
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BIT	7	6	5	4	3	2	1	0
Name	FRCLPMFONT	DISLPMFONT	EN_IPD	DIS_RPD	RFU	ENSKIPLPM	DRV_ADJ[1:0]	
Default	0	1	0	0	1	1	00	
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	

Name	Description	Notes
FORCELPMFONT	0 – Does not force Buck1 to operate in ULPM mode. 1 – Force Buck1 to operate in ULPM mode	This bit only have effect when DISLPMFONT=0.
DISLPMFONT	1: Disable LPM FONT 0: Enable LPM FONT	
EN_IPD	0 – Disable Buck1 pulldown load function 1 – Enable Buck1 pulldown load function	Bit option to enable pull-down load current at VOUT when Buck1 is enabled. There are 4 bits @ Registers 0x71[7:4] are used to config the threshold pull-down current.
DIS_RPD	0: Discharge VOUT when turn-off BUCK by 50hm 1: Don't discharge VOUT when turn-off BUCK	Bit option to disable PullDown Resistor when BUCK is turned-off.
RFU	Reserved for Future Use	Do not change this register value. Changing the register value can affect IC functionality.
ENSKIPLPM	0: Cannot skip when in BURST Mode at high Duty 1: Allow skip when in BURST Mode at high Duty	Using combine this bit with EN_MINPK bit. This bit only have effect when EN_MINPK=1
DRV_ADJ [1:0]	Adjust Gate Driver (Rising and Falling SW): 00 – Slowest 11 – Fastest	

B1_VSET0 – Buck1 Voltage Set0 Register

Address = 0x42h	Default = 0x4Ch	Type = Basic Non-Volatile
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BIT	7	6	5	4	3	2	1	0
Name	RFU	VSET0 [6:0]						
Default	0	1001100						
Access	R/W	R/W						

Name	Description	Notes
RFU	Reserved for Future Use	Do not change this register value. Changing the register value can affect IC functionality.
VSET0 [6:0]	Buck1 output voltage setting 0.6V to 3.775V in 25mV steps	The output voltage is equal to VSET [6:0] * 0.025 + 0.6V.

B1_VSET1 – Buck1 Voltage SET1 Register

Address = 0x43h	Default = 0xDCh	Type = Basic Non-Volatile
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BIT	7	6	5	4	3	2	1	0
Name	B1_CF_GPIO	VSET1 [6:0]						
Default	1	1011100						
Access	R/W	R/W						

Name	Description	Notes
B1_CF_GPIO	0: Disable 1: Enable	Enable configure VSET/LSW mode by GPIO
VSET1 [6:0]	Buck1 output voltage setting 0.6V to 3.775V in 25mV steps	The output voltage setting is the same as the B1_VSET0 register.

B1_REG03 – Buck1 Configuration Register

Address = 0x44h	Default = 0x92h	Type = Basic Non-Volatile
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BIT	7	6	5	4	3	2	1	0
Name	ON	PBINEN	QLTCH	SLEEP_EN	RFU	DPSLP_EN	ILIM_SET[1:0]	
Default	1	0	0	1	0	0	10	
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	

Name	Description	Notes
ON	0 – Not enable Buck 1 – Enable Buck	This functionality is dependent on the overall IC configuration. Consult the factory for details.
PBINEN	0 - Not enable turn on by Push Button 1 – Enable turn on by Push Button	This functionality is dependent on the overall IC configuration. Consult the factory for details.
QLTCH	0 – Buck1 shuts down when its sequenced input shuts down 1 – Buck1 stays on when its sequenced input shuts down	
SLEEP_EN	0 – Buck1 stays on when the IC enters Sleep mode 1 – Buck1 turns off when the IC enters Sleep mode	
RFU	Reserved for Future Use	Do not change this register value. Changing the register value can affect IC functionality.
DPSLP_EN	0 – Buck1 stays on when the IC enters Deep Sleep mode 1 – Buck1 turns off when the IC enters Deep Sleep mode	
ILIM_SET[1:0]	00: LSILIM/HSILIM = 5A/4A 01: LSILIM/HSILIM = 6.2A/5A 10: LSILIM/HSILIM = 7.8A/6.2A 11: LSILIM/HSILIM = 10A/7.8A	

B1_REG04 – Buck1 Configuration Register

Address = 0x45h	Default = 0x8Ah	Type = Basic Non-Volatile
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BIT	7	6	5	4	3	2	1	0
Name	MODE	RST	RFU			RFU		
Default	1	0	001			010		
Access	R/W	R/W	R/W			R/W		

Name	Description	Notes
MODE	Determines startup sequencing from the CMI code	This is a factory expert bit that should not be changed. Modifying this bit may result in unexpected IC behavior.
RST	0 – Buck1 does not affect nRESET output 1 – Buck1 affects nRESET output	
RFU	Reserved for Future Use	Do not change this register value. Changing the register value can affect IC functionality.
RFU	Reserved for Future Use	Do not change this register value. Changing the register value can affect IC functionality.

B1_REG05 – Buck1 Configuration Register

Address = 0x46h	Default = 0x08h	Type = Basic Non-Volatile
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BIT	7	6	5	4	3	2	1	0
Name	RFU				SST	DISLPM	RFU	
Default	0000				1	0	00	
Access	R/W				R/W	R/W	R/W	

Name	Description	Notes
RFU	RFU	Do not change this register value. Changing the register value can affect IC functionality.
SST	Soft-start time option: 0 – 500us 1 – 250us	
DISLPM	0 – Enable LPM mode 1 – Disable LPM mode	Disable Low Power Mode. Will work in DCM or CCM depend on the output load
RFU	Reserved for Future Use	Do not change this register value. Changing the register value can affect IC functionality.

B1_REG06 – Buck1 Configuration Register

Address = 0x47h	Default = 0x28h	Type = Basic Non-Volatile
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BIT	7	6	5	4	3	2	1	0
Name	PHASE_DELAY	PHASE	ON_DELAY [2:0]			OFF_DELAY [2:0]		
Default	0	0	101			000		
Access	R/W	R/W	R/W			R/W		

Name	Description	Notes
PHASE_DELAY	0 – Aligns converter switching to the main clock edge 1 – Delays converter switching 100ns from the main clock edge	
PHASE	0 – Aligns converter switching to the main clock rising edge 1 – Aligns converter switching to the main clock falling edge	
ON_DELAY [2:0]	000 – minimum 001 – 0.25ms 010 – 0.5ms 011 – 0.75ms 100 – 1ms 101 – 2ms 110 – 4ms 111 – 8ms	Sets the delay time between the Buck1 enable input to when it turns on.
OFF_DELAY [2:0]	000 – minimum 001 – 0.25ms 010 – 0.5ms 011 – 0.75ms 100 – 1ms 101 – 2ms 110 – 4ms 111 – 8ms	Sets the delay time between the Buck1 disable input to when it turns off.

BUCK2 REGULATOR REGISTERS

B2_REG00 – Buck2 Configuration Register

Address = 0x60h	Default = 0x0Eh	Type = Basic Volatile
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BIT	7	6	5	4	3	2	1	0
Name	POK	OV	ILIM	RFU	UV_FLTMSK	OV_FLTMSK	ILIM_FLTMSK	RFU
Default	0	0	0	0	1	1	1	0
Access	RO	RO	RO	RO	R/W	R/W	R/W	RO

Name	Description	Notes
POK	POK status: 0 – Buck2 voltage is below the power good threshold 1 – Buck2 voltage is above the power good threshold	Provides real-time power good status
OV	OV status: 0 – Buck2 voltage is below the overvoltage threshold 1 – Buck2 voltage is above the overvoltage threshold	When output voltage > OV, this bit goes high. It is latched high until output voltage < OV and this bit is read.
ILIM	ILIM status: 0: Output ILIM is not triggered 1: Output ILIM is triggered	If the peak switch current reaches the ILIMSET threshold for 16 consecutive switching cycles, this bit goes high. It is latched high until peak switch current < ILIMSET and this bit is read.
RFU	Reserved for Future Use	Do not change this register value. Changing the register value can affect IC functionality.
UV_FLTMSK	Mask VOUT UV interrupt: 0: Unmask Vout UV interrupt 1: Default mask Vout UV interrupt	When 1, the Buck2 POK signal is masked and does not go to the master controller. This prevents Buck2 from asserting the nIRQ pin when it is disabled or drops out of regulation. Buck2 POK still provides real-time power good status.
OV_FLTMSK	Mask Vout OV interrupt: 0: Unmask Vout OV interrupt 1: Default mask Vout OV interrupt	When 1, the Buck2 OV signal is masked and does not go to the master controller. This prevents Buck2 from asserting the nIRQ pin when it is above regulation limits. Buck2 OV still provides OV status.
ILIM_FLTMSK	Mask ILIM interrupt: 0: Unmask ILM interrupt 1: Default mask ILIM interrupt	When 1, the Buck2 ILIM signal is masked and does not go to the master controller. This prevents Buck2 from asserting the nIRQ pin when it is above regulation limits. Buck2 ILIM still provides current limit status.
RFU	Reserved for Future Use	Do not change this register value. Changing the register value can affect IC functionality.

B2_REG01 – Buck2 Configuration Register

Address = 0x61h	Default = 0x54h	Type = Basic Non-Volatile
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BIT	7	6	5	4	3	2	1	0
Name	FREQ_SEL[1:0]		ENPD_LOAD		SST[2:0]		DRV_ADJ [1:0]	
Default	01		0		101		00	
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Name	Description	Notes
FREQ_SEL[1:0]	Select Frequency setting: 00 – 1.5MHz 01 – 2.0MHz 10 – 2.5MHz 11 – 3.3MHz	
ENPD_LOAD	0 – Disable Buck2 pulldown load current function 1 – Enable Buck2 pulldown load current function	Bit option to enable pull-down load current at VOUT when Buck2 is enabled. There are 4 bits @ registers 0x66[3:2] and 0x67[7:6] are used to config the threshold pull-down current.
SST[2:0]	Soft start time setting: 000: 50us 001: 75us 010: 100us 011: 150us 100: 200us 101: 250us 110: 500us 111: 350us	
DRV_ADJ [1:0]	Adjust Gate Driver (Rising and Falling SW): 00 – Slowest 11 – Fastest	

B2_VSET0 – Buck2 Voltage Set0 Register

Address = 0x62h	Default = 0xBCCh	Type = Basic Non-Volatile
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BIT	7	6	5	4	3	2	1	0
Name	EN_LPM	VSET0 [6:0]						
Default	1	0111100						
Access	R/W	R/W						

Name	Description	Notes
EN_LPM	0 – I _q = 250uA 1 – I _q = 45uA	This bit is only effective when EN_ULPM[] = 0
VSET0 [6:0]	Buck2 output voltage setting 0.6V to 1.87V in 10mV steps	The output voltage is equal to VSET [6:0] * 0.01 + 0.6V.

B2_VSET1 – Buck2 Voltage Set1 Register

Address = 0x63h	Default = 0x78h	Type = Basic Non-Volatile
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BIT	7	6	5	4	3	2	1	0
Name	DIS_PD	VSET1 [6:0]						
Default	0	1111000						
Access	R/W	R/W						

Name	Description	Notes
DIS_PD	0 – Discharge V _{OUT} when turn-off BUCK by 9.4Ohm 1 – Don't discharge V _{OUT} when turn-off BUCK	Option to disable Pull-Down Resistor when BUCK is turned-off.
VSET1 [6:0]	Buck2 output voltage setting 0.6V to 1.87V in 10mV steps	The output voltage is equal to VSET [6:0] * 0.01 + 0.6V.

B2_REG03 – Buck2 Configuration Register

Address = 0x64h	Default = 0x92h	Type = Basic Non-Volatile
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BIT	7	6	5	4	3	2	1	0
Name	ON	PBINEN	QLTCH	SLEEP_EN	RFU	DPSLP_EN	ILIM_SET	FCCM
Default	1	0	0	1	0	0	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Name	Description	Notes
ON	0 – Not enable Buck 1 – Enable Buck	This functionality is dependent on the overall IC configuration. Consult the factory for details.
PBINEN	0 – Not enable turn on by Push Button 1 – Enable turn on by Push Button	This functionality is dependent on the overall IC configuration. Consult the factory for details.
QLTCH	0 – Buck2 shuts down when its sequenced input shuts down 1 – Buck2 stays on when its sequenced input shuts down	
SLEEP_EN	0 – Buck2 stays on when the IC enters Sleep mode 1 – Buck2 turns off when the IC enters Sleep mode	
RFU	Reserved for Future Use	Do not change this register value. Changing the register value can affect IC functionality.
DPSLP_EN	0 – Buck2 stays on when the IC enters Deep Sleep mode 1 – Buck2 turns off when the IC enters Deep Sleep mode	
ILIM_SET	Setting for current limit: 0: LSILIM/HSILIM = 3A/2.5A 1: LSILIM/HSILIM = 4.8A/4.0A	
FCCM	0 – Allows Buck2 to operate in both continuous conduction mode and LPM mode 1 – Force Buck2 to operate in continuous conduction mode.	

B2_REG04 – Buck2 Configuration Register

Address = 0x65h	Default = 0x90h	Type = Basic Non-Volatile
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BIT	7	6	5	4	3	2	1	0
Name	MODE	RST	RFU			RFU		
Default	1	0	010			000		
Access	R/W	R/W	R/W			R/W		

Name	Description	Notes
MODE	Determines startup sequencing from the CMI code	This is a factory expert bit that should not be changed. Modifying this bit may result in unexpected IC behavior.
RST	0 – Buck2 does not affect nRESET output 1 – Buck2 affects nRESET output	
RFU	Reserved for Future Use	Do not change this register value. Changing the register value can affect IC functionality.
RFU	Reserved for Future Use	Do not change this register value. Changing the register value can affect IC functionality.

B2_REG05 – Buck2 Configuration Register

Address = 0x66h	Default = 0x00h	Type = Basic Non-Volatile
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BIT	7	6	5	4	3	2	1	0
Name	RFU				IPDLOAD_B2[1:0]		RFU	
Default	0000				00		00	
Access	R/W				R/W		R/W	

Name	Description	Notes
RFU	Reserved for Future Use	Do not change this register value. Changing the register value can affect IC functionality.
IPDLOAD_B2[1:0]	0000: 10mA 0001: 13mA 0010: 17mA 0011: 20mA 0100: 24mA 0101: 27mA 0110: 30mA 0111: 34mA 1000: 37mA 1001: 40mA 1010: 44mA 1011: 47mA 1100: 50mA 1101: 54mA 1110: 57mA 1111: 60mA	Combine with two bits REG0x67[7:6] to setting the PD Load current at VOUT_B2
RFU	Reserved for Future Use	Do not change this register value. Changing the register value can affect IC functionality.

B2_REG06 – Buck2 Configuration Register

Address = 0x67h	Default = 0x10h	Type = Basic Non-Volatile
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BIT	7	6	5	4	3	2	1	0
Name	IPD_LOAD_B2[3:2]		ON_DLY [2:0]			OFF_DELAY [2:0]		
Default	00		010			000		
Access	R/W		R/W			R/W		

Name	Description	Notes
IPD_LOAD_B2[3:2]	Sets Buck2 pulldown load	See register 0x66h for details
ON_DELAY [2:0]	Sets the delay time between the Buck2 enable input to when it turns on: 000 – minimum 001 – 0.25ms 010 – 0.5ms 011 – 0.75ms 100 – 1ms 101 – 2ms 110 – 4ms 111 – 8ms	
OFF_DELAY [2:0]	Sets the delay time between the Buck2 disable input to when it turns off: 000 – minimum 001 – 0.25ms 010 – 0.5ms 011 – 0.75ms 100 – 1ms 101 – 2ms 110 – 4ms 111 – 8ms	

B2_REG07 – Buck 1 & 2 Configuration Register

Address = 0x71h	Default = 0x08h	Type = Basic Non-Volatile
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BIT	7	6	5	4	3	2	1	0
Name	IPDLOAD_B1[3:0]				B2_I2C_CF	BUCK2_VSET	B2_CF_GPIO	B2VSETGPBK1_L
Default	0000				1	0	0	0
Access	R/W				R/W	R/W	R/W	R/W

Name	Description	Notes
IPDLOAD_B1[3:0]	Setting the PD Load current at VOUT_B1: 0000: 10mA 0001: 13mA 0010: 17mA 0011: 20mA 0100: 24mA 0101: 27mA 0110: 30mA 0111: 34mA 1000: 37mA 1001: 40mA 1010: 44mA 1011: 47mA 1100: 50mA 1101: 54mA 1110: 57mA 1111: 60mA	
B2_I2C_CF	0: Disable 1: Enable	Enable configure VSET by I2C Need to set "B2_CF_GPIO"=0 to let this bit effective.
BUCK2_VSET	0: VSET0 1: VSET1	Select BUCK2 VSET when enable configure VSSET by I2C
B2_CF_GPIO	0: Disable 1: Enable	Enable configure VSET by GPIO. Once this bit is 1, it will override bit B2_I2C_CF
B2VSETGPBK1_L	0: VSET0 1: VSET1	When GPIO config for Buck1 LOW then VSET of BUCK2 will be selected by this bit.

B2_REG08 – Buck2 Configuration Register

Address = 0x74h	Default = 0xF4h	Type = Basic Non-Volatile
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BIT	7	6	5	4	3	2	1	0
Name	EN_ULPM	EN_LSILIM	EN_ILIM_FB	RFU[1:0]		EN_ILIM_SD	RFU	
Default	1	1	1	10		1	00	
Access	R/W	R/W	R/W	R/W		R/W	R/W	

Name	Description	Notes
EN_ULPM	The bit is used to enable/disable Ultra Low Power Mode 0: Disable Ultra-LPM 1: Enable Ultra-LPM, the supply current is 11uA @ Noload, no switching	
EN_LSILIM	Enable Low-Side ILIM Protection: 0: Disable 1: Enable. Only allow new High-Side cycle if the inductor current less than LSILIM	This bit is used to protect current run way when the ONTIME calculation less than 150ns.
EN_ILIM_FB	Bit option to enable ILIM Foldback Function: 0: Disable 1: Enable	
RFU	Reserved for Future Use	Do not change this register value. Changing the register value can affect IC functionality.
EN_ILIM_SD	Enable regulator shut down: 0: Disable 1: Enable	
RFU	Reserved for Future Use	Do not change this register value. Changing the register values can affect IC functionality.

BUCK3 REGULATOR REGISTERS

B3_REG00 – Buck3 Configuration Register

Address = 0x80h	Default = 0x0Eh	Type = Basic Volatile
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BIT	7	6	5	4	3	2	1	0
Name	POK	OV	ILIM	RFU	UV_FLTMSK	OV_FLTMSK	ILIM_FLTMSK	RFU
Default	0	0	0	0	1	1	1	0
Access	RO	RO	RO	RO	R/W	R/W	R/W	RO

Name	Description	Notes
POK	POK status: 0 – Buck3 voltage is below the power good threshold 1 – Buck3 voltage is above the power good threshold	Provides real-time power good status
OV	OV status: 0 – Buck3 voltage is below the overvoltage threshold 1 – Buck3 voltage is above the overvoltage threshold	When output voltage > OV, this bit goes high. It is latched high until output voltage < OV and this bit is read.
ILIM	ILIM status: 0: Output ILIM is not triggered 1: Output ILIM is triggered	If the peak switch current reaches the ILIMSET threshold for 16 consecutive switching cycles, this bit goes high. It is latched high until peak switch current < ILIMSET and this bit is read.
RFU	Reserved for Future Use	Do not change this register value. Changing the register value can affect IC functionality.
UV_FLTMSK	Mask VOUT UV interrupt 0: Unmask Vout UV interrupt 1: Default mask Vout UV interrupt	When 1, the Buck3 POK signal is masked and does not go to the master controller. This prevents Buck3 from asserting the nIRQ pin when it is disabled or drops out of regulation. Buck3 POK still provides real-time power good status.
OV_FLTMSK	Mask Vout OV interrupt: 0: Unmask Vout OV interrupt 1: Default mask Vout OV interrupt	When 1, the Buck3 OV signal is masked and does not go to the master controller. This prevents Buck3 from asserting the nIRQ pin when it is above regulation limits. Buck3 OV still provides OV status.
ILIM_FLTMSK	Mask ILIM interrupt: 0: Unmask ILM interrupt 1: Default mask ILIM interrupt	When 1, the Buck3 ILIM signal is and does not go to the master controller. This prevents Buck3 from asserting the nIRQ pin when it is above regulation limits. ILIM still provides current limit status.
RFU	Reserved for Future Use	Do not change this register value. Changing the register value can affect IC functionality.

B3_REG01 – Buck3 Configuration Register

Address = 0x81h	Default = 0x54h	Type = Basic Non-Volatile
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BIT	7	6	5	4	3	2	1	0
Name	FREQ_SEL[1:0]		ENPD_LOAD		SST[2:0]		DRV_ADJ [1:0]	
Default	01		0		101		00	
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Name	Description	Notes
FREQ_SEL[1:0]	Select Frequency setting: 00 – 1.5MHz 01 – 2.0MHz 10 – 2.5MHz 11 – 3.3MHz	
ENPD_LOAD	0 – Disable Buck3 pulldown load current function 1 – Enable Buck3 pulldown load current function	Enable Buck3 pull-down load current when Buck3 is enabled. There are 4 bits @ registers 0x88[3:2] and 0x89[7:6] config the pull-down current load.
SST[2:0]	Soft start time setting: 000: 50us 001: 75us 010: 100us 011: 150us 100: 200us 101: 250us 110: 500us 111: 350us	
DRV_ADJ [1:0]	Adjust Gate Driver (Rising and Falling SW): 00 – Slowest 11 – Fastest	

B3_VSET0 – Buck3 Voltage Set0 Register

Address = 0x82h	Default = 0x9Eh	Type = Basic Non-Volatile
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BIT	7	6	5	4	3	2	1	0
Name	EN_LPM	VSET0 [6:0]						
Default	1	0011110						
Access	R/W	R/W						

Name	Description	Notes
EN_LPM	0 – I _q = 250uA 1 – I _q = 45uA	This bit is only effective when EN_ULPM[] = 0
VSET0 [6:0]	Buck3 output voltage setting : 0.5V to 1.77V in 10mV steps	Controls the Buck3 output voltage. B3_VSET0 is used in ACTIVE mode. The output voltage is equal to VSET [6:0] * 0.01 + 0.5V.

B3_VSET1 – Buck3 Voltage Set1 Register

Address = 0x83h	Default = 0x1Fh	Type = Basic Non-Volatile
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BIT	7	6	5	4	3	2	1	0
Name	DIS_PD	VSET1 [6:0]						
Default	0	0011111						
Access	R/W	R/W						

Name	Description	Notes
DIS_PD	0 – Discharge V _{OUT} when turn-off BUCK by 9.4Ohm. 1 – Don't discharge V _{OUT} when turn-off BUCK	Option to disable Pull-Down Resistor when BUCK is turned-off
VSET1 [6:0]	Buck3 output voltage setting 0.5V to 1.77V in 10mV steps	The output voltage is equal to VSET [6:0] * 0.01 + 0.5V.

B3_VSET2 – Buck3 Voltage Set2 Register

Address = 0x84h	Default = 0x23h	Type = Basic Non-Volatile
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BIT	7	6	5	4	3	2	1	0
Name	FCCM	VSET2 [6:0]						
Default	0	0100011						
Access	R/W	R/W						

Name	Description	Notes
FCCM	0 – Allows Buck3 to operate in both continuous conduction mode and LPM mode 1 – Force Buck3 to operate in continuous conduction mode.	
VSET2 [6:0]	Buck3 output voltage setting 0.5V to 1.77V in 10mV steps	The output voltage is equal to VSET [6:0] * 0.01 + 0.5V.

B3_VSET3 – Buck3 Voltage Set3 Register

Address = 0x85h	Default = 0x9Fh	Type = Basic Non-Volatile
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BIT	7	6	5	4	3	2	1	0
Name	B3_CF_GPIO	VSET3 [6:0]						
Default	1	0011111						
Access	R/W	R/W						

Name	Description	Notes
B3_CF_GPIO	0: disable 1: enable	Enable configure VSET by GPIO
VSET3 [6:0]	Buck3 output voltage setting 0.5V to 1.77V in 10mV steps	The output voltage is equal to VSET [6:0] * 0.01 + 0.5V.

B3_REG03 – Buck3 Configuration Register

Address = 0x86h	Default = 0x82h	Type = Basic Non-Volatile
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BIT	7	6	5	4	3	2	1	0
Name	ON	PBINEN	QLTCH	SLEEP_EN	RFU	DPSLP_EN	ILIM_SET[1:0]	
Default	1	0	0	0	0	0	10	
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	

Name	Description	Notes
ON	0 – Not enable Buck 1 – Enable Buck	This functionality is dependent on the overall IC configuration. Consult the factory for details.
PBINEN	0 - Not enable turn on by Push Button 1 – Enable turn on by Push Button	This functionality is dependent on the overall IC configuration. Consult the factory for details.
QLTCH	0 – Buck3 shuts down when its sequenced input shuts down 1 – Buck3 stays on when its sequenced input shuts down	
SLEEP_EN	0 – Buck3 stays on when the IC enters Sleep mode 1 – Buck3 turns off when the IC enters Sleep mode	
RFU	Reserved for Future Use	Do not change this register value. Changing the register value can affect IC functionality.
DPSLP_EN	0 – Buck3 stays on when the IC enters Deep Sleep mode 1 – Buck3 turns off when the IC enters Deep Sleep mode	
ILIM_SET[1:0]	Buck3 ILIM setting: 00: LSILIM/HSILIM = 5A/4A 01: LSILIM/HSILIM = 6.2A/5A 10: LSILIM/HSILIM = 7.8A/6.2A 11: LSILIM/HSILIM = 10A/7.8A	

B3_REG04 – Buck3 Configuration Register

Address = 0x87h	Default = 0xC1h	Type = Basic Non-Volatile
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BIT	7	6	5	4	3	2	1	0
Name	MODE	RST	RFU			RFU		
Default	1	1	000			001		
Access	R/W	R/W	R/W			R/W		

Name	Description	Notes
MODE	Determines startup sequencing from the CMI code	This is a factory expert bit that should not be changed. Modifying this bit may result in unexpected IC behavior.
RST	0 – Buck3 does not affect nRESET output 1 – Buck3 affects nRESET output	
RFU	Reserved for Future Use	Do not change this register value. Changing the register value can affect IC functionality.
RFU	Reserved for Future Use	Do not change this register value. Changing the register value can affect IC functionality.

B3_REG05 – Buck3 Configuration Register

Address = 0x88h	Default = 0x00h	Type = Basic Non-Volatile
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BIT	7	6	5	4	3	2	1	0
Name	RFU				IPDLOAD_B3[1:0]		RFU	
Default	0000				00		00	
Access	R/W				R/W		R/W	

Name	Description	Notes
RFU	Reserved for Future Use	Do not change this register value. Changing the register value can affect IC functionality.
IPDLOAD_B3[1:0]	0000: 10mA 0001: 13mA 0010: 17mA 0011: 20mA 0100: 24mA 0101: 27mA 0110: 30mA 0111: 34mA 1000: 37mA 1001: 40mA 1010: 44mA 1011: 47mA 1100: 50mA 1101: 54mA 1110: 57mA 1111: 60mA	Combine with two bits REG0x89[7:6] to setting the PD Load current at VOUT_B3
RFU	Reserved for Future Use	Do not change this register value. Changing the register value can affect IC functionality.

B3_REG06 – Buck3 Configuration Register

Address = 0x89h	Default = 0x18h	Type = Basic Non-Volatile
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BIT	7	6	5	4	3	2	1	0
Name	IPDLOAD_B3[3:2]		ON_DELAY [2:0]			OFF_DELAY [2:0]		
Default	00		011			000		
Access	R/W		R/W			R/W		

Name	Description	Notes
IPDLOAD_B3[3:2]	Sets Buck3 pulldown load current.	See register 0x88h for details
ON_DELAY [2:0]	Sets the delay time between the Buck3 enable input to when it turns on: 000 – minimum 001 – 0.25ms 010 – 0.5ms 011 – 0.75ms 100 – 1ms 101 – 2ms 110 – 4ms 111 – 8ms	
OFF_DELAY [2:0]	Sets the delay time between the Buck3 disable input to when it turns off: 000 – minimum 001 – 0.25ms 010 – 0.5ms 011 – 0.75ms 100 – 1ms 101 – 2ms 110 – 4ms 111 – 8ms	

B3_REG07 – Buck3 Configuration Register

Address = 0x92h	Default = 0xA7h	Type = Basic Non-Volatile
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BIT	7	6	5	4	3	2	1	0
Name	DVS_SET[1:0]		EN_ILIM_SD		RFU[1:0]		EN_ULPM	EN_LSILIM
Default	10		1		00		1	1
Access	R/W		R/W		R/W		R/W	R/W

Name	Description	Notes
DVS_SET[1:0]	Buck3 DVS slew rate setting: 00: 22.5mV/us 01: 11.25mV/us 10: 5.625mV/us 11: 2.8125mV/us	
EN_ILIM_SD	Enable regulator shut down: 0: Disable 1: Enable	
RFU[1:0]	Reserved for Future Use	Do not change this register value. Changing the register value can affect IC functionality.
EN_ULPM	The bit is used to enable/disable Ultra Low Power Mode: 0: Disable Ultra-LPM 1: Enable Ultra-LPM, the supply current is 11uA @ Noload, no switching	
EN_LSILIM	Enable Low-Side ILIM Protection: 0: Disable 1: Enable. Only allow new High-Side cycle if the inductor current less than LSILIM	This bit is used to protect current run way when the ONTIME calculation less than 150ns
EN_ILIM_FB	Bit option to enable ILIM Foldback Function: 0: Disable 1: Enable	

BUCK4 REGULATOR REGISTERS

B4_REG00 – Buck4 Configuration Register

Address = 0xA0h	Default = 0x0Eh	Type = Basic Volatile
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BIT	7	6	5	4	3	2	1	0
Name	POK	OV	ILIM	RFU	UV_FLTMSK	OV_FLTMSK	ILIM_FLTMSK	RFU
Default	0	0	0	0	1	1	1	0
Access	RO	RO	RO	RO	R/W	R/W	R/W	RO

Name	Description	Notes
POK	POK status: 0 – Buck4 voltage is below the power good threshold 1 – Buck4 voltage is above the power good threshold	Provides real-time power good status
OV	OV status: 0 – Buck4 voltage is below the overvoltage threshold 1 – Buck4 voltage is above the overvoltage threshold	When output voltage > OV, this bit goes high. It is latched high until output voltage < OV and this bit is read.
ILIM	ILIM status: 0: Output ILIM is not triggered 1: Output ILIM is triggered	If the peak switch current reaches the ILIMSET threshold for 16 consecutive switching cycles, this bit goes high. It is latched high until peak switch current < ILIMSET and this bit is read.
RFU	Reserved for Future Use	Do not change this register value. Changing the register value can affect IC functionality.
UV_FLTMSK	Mask VOUT UV interrupt: 0: Unmask Vout UV interrupt 1: Default mask Vout UV interrupt	When 1, the Buck4 POK signal is masked and does not go to the master controller. This prevents Buck4 from asserting the nIRQ pin when it is disabled or drops out of regulation. Buck4 POK still provides real-time power good status.
OV_FLTMSK	Mask Vout OV interrupt 0: Unmask Vout OV interrupt 1: Default mask Vout OV interrupt	When 1, the Buck4 OV signal is masked and does not go to the master controller. This prevents Buck4 from asserting the nIRQ pin when it is above regulation limits. Buck4 OV still provides OV status.
ILIM_FLTMSK	Mask ILIM interrupt: 0: Unmask ILM interrupt 1: Default mask ILIM interrupt	When 1, the Buck4 ILIM signal is masked and does not go to the master controller. This prevents Buck4 from asserting the nIRQ pin when it is above regulation limits. ILIM still provides current limit status.
RFU	Reserved for Future Use	Do not change this register value. Changing the register value can affect IC functionality.

B4_REG01 – Buck4 Configuration Register

Address = 0xA1h	Default = 0x54h	Type = Basic Non-Volatile
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BIT	7	6	5	4	3	2	1	0
Name	FREQ_SEL[1:0]		ENPD_LOAD	SST[2:0]			DRV_ADJ [1:0]	
Default	01		0	101			00	
Access	R/W	R/W	R/W	R/W			R/W	

Name	Description	Notes
FREQ_SEL[1:0]	Select Frequency setting: 00 – 1.5MHz 01 – 2.0MHz 10 – 2.5MHz 11 – 3.3MHz	
ENPD_LOAD	0 – Disable Buck4 pulldown load current function 1 – Enable Buck4 pulldown load current function	Enable Buck4 pull-down load current when Buck4 is enabled. There are 4 bits @ registers 0xA7[3:2] and 0xA8[7:6] config the pull-down current load.
SST[2:0]	Soft start time setting: 000: 50us 001: 75us 010: 100us 011: 150us 100: 200us 101: 250us 110: 500us 111: 350us	
DRV_ADJ [1:0]	Adjust Gate Driver (Rising and Falling SW): 00 – Slowest 11 – Fastest	

B4_VSET0 – Buck4 Voltage Set0 Register

Address = 0xA2h	Default = 0x8Ch	Type = Basic Non-Volatile
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BIT	7	6	5	4	3	2	1	0
Name	EN_LPM	B4_CF_GPIO	VSET0 [5:0]					
Default	1	0	001100					
Access	R/W	R/W	R/W					

Name	Description	Notes
EN_LPM	0 – I _q = 250uA 1 – I _q = 45uA	This bit is only effective when EN_ULPM[0]=0
B4_CF_GPIO	1: enable 0: disable	Enable configure VSET by GPIO
VSET0 [5:0]	Buck4 output voltage setting. 0.6V to 3.75V in 50mV steps 0.6V to 1.23V in 10mV steps	The output voltage is equal to: VSET0 [5:0] * 0.01 + 0.6V if VRANGE=0, VSET0 [5:0] * 0.05 + 0.6V if VRANGE=1.

B4_VSET1 – Buck4 Voltage Set1 Register

Address = 0xA3h	Default = 0x18h	Type = Basic Non-Volatile
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BIT	7	6	5	4	3	2	1	0
Name	DIS_PD	RFU	VSET1 [5:0]					
Default	1	0	011000					
Access	R/W	R/W	R/W					

Name	Description	Notes
DIS_PD	0 – Discharge VOUT when turn-off BUCK by 9.4Ohm 1 – Don't discharge VOUT when turn-off BUCK	Option disable Pull-Down Resistor when BUCK is turned-off
RFU	Reserved for Future Use	Do not change this register value. Changing the register value can affect IC functionality.
VSET1 [5:0]	Buck4 output voltage setting 0.6V to 3.75V in 50mV steps 0.6V to 1.23V in 10mV steps	Controls the Buck4 output voltage. The output voltage is equal to: VSET1 [5:0] * 0.01 + 0.6V if VRANGE=0, VSET1 [5:0] * 0.05 + 0.6V if VRANGE=1.

B4_VSET2 – Buck4 Voltage Set1 Register

Address = 0xA4h	Default = 0x58h	Type = Basic Non-Volatile
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BIT	7	6	5	4	3	2	1	0
Name	BUCK4_MODE	B4_I2C_CF	VSET2 [5:0]					
Default	0	1	011000					
Access	R/W	R/W	R/W					

Name	Description	Notes
BUCK4_MODE	0: REG4 work in LDO mode 1: REG4 work as BUCK mode.	Set Buck4 between Buck and LDO mode. Do not change this bit when Buck4 is enabled.
B4_I2C_CF	0: disable 1: enable	Enable configure VSET by I2C Need to set "B4_CF_GPIO"=0 to let this bit effective.
VSET2 [5:0]	Buck4 LDO output voltage setting 0.6V to 3.75V in 50mV steps	Controls the Buck4 LDO mode output voltage. The output voltage is equal to VSET2[5:0] * 0.05 + 0.6V.

B4_REG03 – Buck4 Configuration Register

Address = 0xA5h	Default = 0x80h	Type = Basic Non-Volatile
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BIT	7	6	5	4	3	2	1	0
Name	ON	PBINEN	QLTCH	SLEEP_EN	RFU	DPSLP_EN	ILIM_SET	FCCM
Default	1	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Name	Description	Notes
ON	0 – Not enable Buck 1 – Enable Buck	This functionality is dependent on the overall IC configuration. Consult the factory for details.
PBINEN	0 - Not enable turn on by Push Button 1 – Enable turn on by Push Button	This is a factory expert bit that should not be changed. Modifying this bit may result in unexpected IC behavior.
QLTCH	0 – Buck4 shuts down when its sequenced input shuts down 1 – Buck4 stays on when its sequenced input shuts down	
SLEEP_EN	0 – Buck4 stays on when the IC enters Sleep mode 1 – Buck4 turns off when the IC enters Sleep mode	
RFU	Reserved for Future Use	Do not change this register value. Changing the register value can affect IC functionality.
DPSLP_EN	0 – Buck4 stays on when the IC enters Deep Sleep mode 1 – Buck4 turns off when the IC enters Deep Sleep mode	
ILIM_SET	Setting for current limit: 0: LSILIM/HSILIM = 2.4A/2A 1: LSILIM/HSILIM = 4.25A/3.5A	
FCCM	0 – Allows Buck4 to operate in both continuous conduction mode and LPM mode 1 – Force Buck4 to operate in continuous conduction mode.	

B4_REG04 – Buck4 Configuration Register

Address = 0xA6h	Default = 0x80h	Type = Basic Non-Volatile
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BIT	7	6	5	4	3	2	1	0
Name	MODE	RST	RFU			RFU		
Default	1	0	000			000		
Access	R/W	R/W	R/W			R/W		

Name	Description	Notes
MODE	Determines startup sequencing from the CMI code	This is a factory expert bit that should not be changed. Modifying this bit may result in unexpected IC behavior.
RST	0 – Buck4 does not affect nRESET output 1 – Buck4 affects nRESET output	
RFU	Reserved for Future Use	Reserved for Future Use
RFU	Reserved for Future Use	Reserved for Future Use

B4_REG05 – Buck4 Configuration Register

Address = 0xA7h	Default = 0x00h	Type = Basic Non-Volatile
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BIT	7	6	5	4	3	2	1	0
Name	RFU				IPDLOAD_B4[1:0]		RFU	
Default	0000				00		00	
Access	R/W				R/W		R/W	

Name	Description	Notes
RFU	Reserved for Future Use	Do not change this register value. Changing the register value can affect IC functionality.
IPDLOAD_B4[1:0]	0000: 10mA 0001: 13mA 0010: 17mA 0011: 20mA 0100: 24mA 0101: 27mA 0110: 30mA 0111: 34mA 1000: 37mA 1001: 40mA 1010: 44mA 1011: 47mA 1100: 50mA 1101: 54mA 1110: 57mA 1111: 60mA	Combine with two bits REG0xA8[7:6] to setting the PD Load current at VOUT_B4
RFU	Reserved for Future Use	Do not change this register value. Changing the register value can affect IC functionality.

B4_REG06 – Buck4 Configuration Register

Address = 0xA8h	Default = 0x00h	Type = Basic Non-Volatile
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BIT	7	6	5	4	3	2	1	0
Name	IPD_LOAD_B4[3:2]		ON_DELAY [2:0]			OFF_DELAY [2:0]		
Default	00		000			000		
Access	R/W		R/W			R/W		

Name	Description	Notes
IPD_LOAD_B4[3:2]	Sets Buck4 pulldown load	See register 0xA7h for details
ON_DELAY [2:0]	<p>Sets the delay time between the Buck4 enable input to when it turns on:</p> <p>000 – minimum</p> <p>001 – 0.25ms</p> <p>010 – 0.5ms</p> <p>011 – 0.75ms</p> <p>100 – 1ms</p> <p>101 – 2ms</p> <p>110 – 4ms</p> <p>111 – 8ms</p>	
OFF_DELAY [2:0]	<p>Sets the delay time between the Buck4 disable input to when it turns off:</p> <p>000 – minimum</p> <p>001 – 0.25ms</p> <p>010 – 0.5ms</p> <p>011 – 0.75ms</p> <p>100 – 1ms</p> <p>101 – 2ms</p> <p>110 – 4ms</p> <p>111 – 8ms</p>	

B4_REG07 – Buck4 Configuration Register

Address = 0xB1h	Default = 0xBFh	Type = Basic Non-Volatile
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BIT	7	6	5	4	3	2	1	0
Name	RFU		EN_ILIM_SD	EN_ULPM	EN_LSILIM	EN_ILIM_FB	IOHI_ONDL[1:0]	
Default	10		1	1	1	1	11	
Access	R/W		R/W	R/W	R/W	R/W	R/W	

Name	Description	Notes
RFU	Reserved for future use	Do not change this register value. Changing the register value can affect IC functionality.
EN_ILIM_SD	Enable regulator shut down: 0: Disable 1: Enable	
EN_ULPM	The bit is used to enable/disable Ultra Low Power Mode: 0: Disable Ultra-LPM 1: Enable Ultra-LPM, the supply current is 11uA @ Noload, no switching	
EN_LSILIM	Enable Low-Side ILIM Protection: 0: Disable 1: Enable. Only allow new High-Side cycle if the inductor current less than LSILIM	This bit is used to protect current run way when the ONTIME calculation less than 150ns
EN_ILIM_FB	Bit option to enable ILIM Foldback Function: 0: Disable 1: Enable	
IOHI_ONDL[1:0]	Setting on delay when turn-on controlled by GPIO Hi level: 00: 0ms 01: 0.75ms 10: 1.5ms 11: 2.25ms	

B4_REG08 – Buck4 LDO Mode Configuration Register

Address = 0xB2h	Default = 0x20h	Type = Basic Non-Volatile
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BIT	7	6	5	4	3	2	1	0
Name	RFU		VRANGE	LPM_MODE_LDO	RFU			RFU
Default	00		1	0	000			0
Access	R/W		R/W	R/W	R/W			R/W

Name	Description	Notes
RFU	Reserved for Future Use	Do not change this register value. Changing the register value can affect IC functionality.
VRANGE	Select output voltage range for buck mode: 1: 0.6V-3.75V (step 50mV) 0: 0.6V - 1.23V (step 10mV)	
LPM_MODE_LDO	Enable Buck4 LDO mode LPM mode: 0: disable 1: enable	
RFU	Reserved for Future Use	Do not change this register value. Changing the register value can affect IC functionality.
RFU	Reserved for Future Use	Do not change this register value. Changing the register value can affect IC functionality.

B4_REG09 – Buck4 LDO Mode Configuration Register

Address = 0xB5h	Default = 0x82h	Type = Basic Non-Volatile
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BIT	7	6	5	4	3	2	1	0
Name	ON_LDO	PBIN_EN_LDO	QLTCH_LDO	SLEEP_EN_LDO	RFU	DPSLP_EN_LDO	ILIM_SCL_LDO	SST_LDO
Default	1	0	0	0	0	0	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Name	Description	Notes
ON_LDO	0 – Not enable Buck4 LDO 1 – Enable Buck4 LDO	This functionality is dependent on the overall IC configuration. Consult the factory for details.
PBIN_EN_LDO	0 - Not enable Buck4 LDO turn on by Push Button 1 – Enable Buck4 LDO turn on by Push Button	This functionality is dependent on the overall IC configuration. Consult the factory for details.
QLTCH_LDO	0 – Buck4 LDO mode shuts down when its sequenced input shuts down 1 – Buck4 LDO mode stays on when its sequenced input shuts down	
SLEEP_EN_LDO	0 – Buck4 LDO mode stays on when the IC enters Sleep mode 1 – Buck4 LDO mode turns off when the IC enters Sleep mode	
RFU	Reserved for Future Use	Do not change this register value. Changing the register value can affect IC functionality.
DPSLP_EN_LDO	0 – Buck4 LDO mode stays on when the IC enters Deep Sleep mode 1 – Buck4 LDO mode turns off when the IC enters Deep Sleep mode	
ILIM_SCL_LDO	Current limit setting for LDO/PLSW mode: 0: 400mA 1: 500mA	
SST_LDO	Buck4 LDO mode soft start time: 0: 140us 1: 280us.	

B4_REG0A – Buck4 LDO Mode Configuration Register

Address = 0xB6h	Default = 0x02h	Type = Basic Non-Volatile
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BIT	7	6	5	4	3	2	1	0
Name	ON_DLY_LDO[2:0]			OFF_DLY_LDO[2:0]			MODE_LDO	RST_LDO
Default	000			000			1	0
Access	R/W			R/W				

Name	Description	Notes
ON_DLY_LDO[2:0]	Sets the delay time between the Buck4 LDO mode enable input to when it turns on: 000 – minimum 001 – 0.25ms 010 – 0.5ms 011 – 0.75ms 100 – 1ms 101 – 2ms 110 – 4ms 111 – 8ms	
OFF_DLY_LDO[2:0]	Sets the delay time between the Buck4 LDO mode disable input to when it turns off: 000 – minimum 001 – 0.25ms 010 – 0.5ms 011 – 0.75ms 100 – 1ms 101 – 2ms 110 – 4ms 111 – 8ms	
MODE_LDO	Determines startup sequencing from the CMI code	This is a factory expert bit that should not be changed. Modifying this bit may result in unexpected IC behavior.
RST_LDO	0 – Buck4 LDO mode does not affect nRESET output 1 – Buck4 LDO mode affects nRESET output	

B4_REG0B – Buck4 LDO Mode Configuration Register

Address = 0xB7h	Default = 0x00h	Type = Basic Non-Volatile
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BIT	7	6	5	4	3	2	1	0
Name	RFU				RFU			RFU
Default	0000				00			00
Access	R/W				R/W			R/W

Name	Description	Notes
RFU	Reserved for Future Use	Do not change this register value. Changing the register value can affect IC functionality.
RFU	Reserved for Future Use	Do not change this register value. Changing the register value can affect IC functionality.
RFU	Reserved for Future Use	Do not change this register value. Changing the register value can affect IC functionality.

LDO REGISTERS

LDO12_REG00 – LDO1 Configuration Register

Address = 0xC0h	Default = 0x0Eh	Type = Basic Volatile
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BIT	7	6	5	4	3	2	1	0
Name	PWR_GOOD_LDO1	OV_LDO1	ILIM_LDO1	RFU	UV_FLTMSK_LDO1	OV_FLTMSK_LDO1	ILIM_FLTMSK_LDO1	RFU
Default	0	0	0	0	1	1	1	0
Access	RO	RO	RO	RO	R/W	R/W	R/W	RO

Name	Description	Notes
PWR_GOOD_LDO1	POK status: 0 – LDO1 voltage is below the power good threshold 1 – LDO1 voltage is above the power good threshold	Provides real-time power good status
OV_LDO1	OV status: 0 – LDO1 voltage is below the overvoltage threshold 1 – LDO1 voltage is above the overvoltage threshold	When output voltage > OV, this bit goes high. It is latched high until output voltage < OV and this bit is read.
ILIM_LDO1	ILIM status: 0: Output ILIM is not triggered 1: Output ILIM is triggered	When output current reached ILIM setting, this bit goes high. It is latched high until output current < ILIM and this bit is read.
RFU	Reserved for Future Use	Do not change this register value. Changing the register value can affect IC functionality.
UV_FLTMSK_LDO1	Mask LDO1 VOUT UV interrupt: 0: Unmask Vout UV interrupt 1: Default mask Vout UV interrupt	When 1, the LDO1 PG signal is masked and does not go to the master controller. This prevents LDO1 from asserting the nIRQ pin when it is disabled or drops out of regulation. LDO1 PG still provides real-time status.
OV_FLTMSK_LDO1	Mask LDO1 Vout OV interrupt: 0: Unmask Vout OV interrupt 1: Default mask Vout OV interrupt	When 1, the OV_LDO1 signal is masked and does not go to the master controller. This prevents LDO1 from asserting the nIRQ pin when it is above regulation limits. OV_LDO1 still provides overvoltage status.
ILIM_FLTMSK_LDO1	Mask ILIM interrupt: 0 - Unmasks the LDO1 ILIM interrupt 1 - Masks the LDO1 ILIM interrupt	When 1, the LDO1 ILIM signal is masked and does not go to the master controller. This prevents LDO1 from asserting the nIRQ pin when it is above regulation limits. ILIM still provides current limit status.
RFU	Reserved for Future Use	Do not change this register value. Changing the register value can affect IC functionality.

LDO12_VSET0 – LDO1 Voltage Set0 Register

Address = 0xC1h	Default = 0x26h	Type = Basic Non-Volatile
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BIT	7	6	5	4	3	2	1	0
Name	SLP_EN_LDO1	DPSLP_EN_LDO1	LDO1_VSET0 [5:0]					
Default	0	0	100110					
Access	R/W	R/W	R/W					

Name	Description	Notes
SLP_EN_LDO1	Enable LDO1 SLEEP mode: 0 – LDO1 stays on when the IC enters Sleep mode 1 – LDO1 turns off when the IC enters Sleep mode	
DPSLP_EN_LDO1	Enable LDO1 Deep SLEEP mode: 0 – LDO1 stays on when the IC enters Deep Sleep mode 1 – LDO1 turns off when the IC enters Deep Sleep mode	
LDO1_VSET0 [5:0]	LDO1 output voltage setting. 0.6V to 3.75V in 50mV steps	The LDO output voltage is equal to $LDO1_VSET [5:0] * 0.05 + 0.6V$

LDO12_VSET1 – LDO1 Voltage Set1 Register

Address = 0xC2h	Default = 0x98h	Type = Basic Non-Volatile
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BIT	7	6	5	4	3	2	1	0
Name	ON_LDO1	PBIN_EN_LDO1	LDO1_VSET1 [5:0]					
Default	1	0	011000					
Access	R/W	R/W	R/W					

Name	Description	Notes
ON_LDO1	0 – Not enable LDO1 1 – Enable LDO1	This functionality is dependent on the overall IC configuration. Consult the factory for details.
PBIN_EN_LDO1	0 - Not enable turn on by Push Button 1 – Enable turn on by Push Button	This functionality is dependent on the overall IC configuration. Consult the factory for details..
LDO1_VSET1 [5:0]	LDO1 output voltage setting. 0.6V to 3.75V in 50mV steps	The LDO output voltage is equal to $LDO1_VSET [5:0] * 0.05 + 0.6V$

LDO12_REG01 – LDO1 Configuration Register

Address = 0xC3h	Default = 0x02h	Type = Basic Non-Volatile
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BIT	7	6	5	4	3	2	1	0
Name	ONDELAY_LDO1 [2:0]			OFFDELAY_LDO1 [2:0]			MODE_LDO1	RST_LDO1
Default	000			000			1	0
Access	R/W			R/W				

Name	Description	Notes
ONDELAY_LDO1 [2:0]	Sets the delay time between the LDO1 enable input to when it turns on: 000 – minimum 001 – 0.25ms 010 – 0.5ms 011 – 0.75ms 100 – 1ms 101 – 2ms 110 – 4ms 111 – 8ms	
OFFDELAY_LDO1 [2:0]	Sets the delay time between the LDO1 disable input to when it turns off: 000 – minimum 001 – 0.25ms 010 – 0.5ms 011 – 0.75ms 100 – 1ms 101 – 2ms 110 – 4ms 111 – 8ms	
MODE_LDO1	Determines startup sequencing from the CMI code	This is a factory expert bit that should not be changed. Modifying this bit may result in unexpected IC behavior.
RST_LDO1	0 – LDO1 does not affect nRESET output 1 – LDO1 affects nRESET output	

LDO12_REG02 – LDO1 Configuration Register

Address = 0xC4h	Default = 0x00h	Type = Basic Non-Volatile
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BIT	7	6	5	4	3	2	1	0
Name	RFU				RFU			
Default	0000				0000			
Access	R/W				R/W			

Name	Description	Notes
RFU	Reserved for Future Use	Do not change this register value. Changing the register value can affect IC functionality.
RFU	Reserved for Future Use	Do not change this register value. Changing the register value can affect IC functionality.

LDO12_REG03 – LDO1 Configuration Register

Address = 0xC5h	Default = 0x0Ch	Type n/a = Basic Non-Volatile
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BIT	7	6	5	4	3	2	1	0
Name	RFU			RFU	NLSW_ILIM_SCL	ILIM_SCL_LDO1	SST_LDO1	QLTCH_LDO1
Default	0			0	1	1	0	0
Access	R/W			R/W	R/W	R/W	R/W	R/W

Name	Description	Notes
RFU	Reserved for Future Use	Do not change this register value. Changing the register value can affect IC functionality.
RFU	Reserved for Future Use	Do not change this register value. Changing the register value can affect IC functionality.
NLSW1_ILIM_SCL	Current limit setting for NLSW mode: 0 – 650mA 1 – 1110mA	
ILIM_SCL_LDO1	Current limit setting for LDO/PLSW mode: 0 – 400mA 1 – 500mA	
SST_LDO1	LDO1 soft-start time: 0 – 140us 1 – 280us	
QLTCH_LDO1	0 – LDO1 shuts down when its sequenced input shuts down 1 – LDO1 stays on when its sequenced input shuts down	

LDO12_REG04 – LDO2 Configuration Register

Address = 0xC6h	Default = 0x0Eh	Type = Basic Volatile
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BIT	7	6	5	4	3	2	1	0
Name	PWR_GOOD_LDO2	OV_LDO2	ILIM_LDO2	RFU	UV_FLTMSK_LDO2	OV_FLTMSK_LDO2	ILIM_FLTMSK_LDO2	RFU
Default	0	0	0	0	1	1	1	0
Access	RO	RO	RO	RO	RW	R/W	R/W	RO

Name	Description	Notes
PWR_GOOD_LDO2	POK status: 0 – LDO2 voltage is below the power good threshold 1 – LDO2 voltage is above the power good threshold	Provides real-time power good status
OV_LDO2	OV status: 0 – LDO2 voltage is below the overvoltage threshold 1 – LDO2 voltage is above the overvoltage threshold	When output voltage > OV, this bit goes high. It is latched high until output voltage < OV and this bit is read.
ILIM_LDO2	ILIM status: 0: Output ILIM is not triggered 1: Output ILIM is triggered	When output current reached ILIM setting, this bit goes high. It is latched high until output current < ILIM and this bit is read.
RFU	Reserved for Future Use	Do not change this register value. Changing the register value can affect IC functionality.
UV_FLTMSK_LDO2	Mask LDO2 VOUT UV interrupt 0: Unmask Vout UV interrupt 1: Default mask Vout UV interrupt	When 1, the LDO2 PG signal is masked and does not go to the master controller. This prevents LDO2 from asserting the nIRQ pin when it is disabled or drops out of regulation. LDO2 PG still provides real-time status.
OV_FLTMSK_LDO2	Mask LDO2 Vout OV interrupt: 1: Default mask Vout OV interrupt 0: Unmask Vout OV interrupt	When 1, the OV_LDO2 signal is masked and does not go to the master controller. This prevents LDO2 from asserting the nIRQ pin when it is above regulation limits. OV_LDO2 still provides real-time overvoltage status.
ILIM_FLTMSK_LDO2	Mask LDO2 ILIM interrupt: 1: Default mask ILIM interrupt 0: Unmask ILM interrupt	When 1, the LDO2 ILIM signal is masked and does not go to the master controller. This prevents LDO2 from asserting the nIRQ pin when it is above regulation limits. ILIM_LDO2 still provides real-time current limit status.
RFU	Reserved for Future Use	Do not change this register value. Changing the register value can affect IC functionality.

LDO12_VSET – LDO2 Voltage Set Register

Address = 0xC7h	Default = 0x18h	Type = Basic Non-Volatile
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BIT	7	6	5	4	3	2	1	0
Name	ILIM_SCL_LDO2	SST_LDO2	LDO2_VSET [5:0]					
Default	0	0	011000					
Access	R/W	R/W	R/W					

Name	Description	Notes
ILIM_SCL_LDO2	Current limit setting for LDO/PLSW mode: 0 – 400mA 1 – 500mA	
SST_LDO2	LDO2 soft-start time: 0 – 140us 1 – 280us	
LDO2_VSET [5:0]	LDO2 output voltage setting. 0.6V to 3.75V in 50mV steps	The LDO output voltage is equal to $LDO2_VSET [5:0] * 0.05 + 0.6V$

LDO12_REG05 – LDO2 Configuration Register

Address = 0xC8h	Default = 0x80h	Type = Factory Non-Volatile
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BIT	7	6	5	4	3	2	1	0
Name	ON_LDO2	PBIN_EN_LDO2	RFU	SLEEP_EN_LDO2	DPSLP_EN_LDO2	RFU		
Default	1	0	0	0	0	000		
Access	R/W	R/W	R/W	R/W	R/W	R/W		

Name	Description	Notes
ON_LDO2	0 – Not enable LDO2 1 – Enable LDO2	This functionality is dependent on the overall IC configuration. Consult the factory for details.
PBIN_EN_LDO2	0 - Not enable LDO2 turn on by Push Button 1 – Enable LDO2 turn on by Push Button	This is a factory expert bit that should not be changed. Modifying this bit may result in unexpected IC behavior.
RFU	Reserved for Future Use	Do not change this register value. Changing the register value can affect IC functionality.
SLEEP_EN_LDO2	0 – LDO2 stays on when the IC enters Sleep mode 1 – LDO2 turns off when the IC enters Sleep mode	
DPSLP_EN_LDO2	0 – LDO2 stays on when the IC enters Deep Sleep mode 1 – LDO2 turns off when the IC enters Deep Sleep mode	
RFU	Reserved for Future Use	Do not change this register value. Changing the register value can affect IC functionality.

LDO12_REG06 – LDO2 Configuration Register

Address = 0xC9h	Default = 0xA2h	Type = Basic Non-Volatile
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BIT	7	6	5	4	3	2	1	0
Name	ON_DELAY_LDO2 [2:0]			OFF_DELAY_LDO2 [2:0]			MODE_LDO2	RST_LDO2
Default	101			000			1	0
Access	R/W			R/W			R/W	R/W

Name	Description	Notes
ON_DELAY_LDO2 [2:0]	Sets the delay time between the LDO2 enable input to when it turns on: 000 – minimum 001 – 0.25ms 010 – 0.5ms 011 – 0.75ms 100 – 1ms 101 – 2ms 110 – 4ms 111 – 8ms	
OFF_DELAY_LDO2 [2:0]	Sets the delay time between the LDO2 disable input to when it turns off: 000 – minimum 001 – 0.25ms 010 – 0.5ms 011 – 0.75ms 100 – 1ms 101 – 2ms 110 – 4ms 111 – 8ms	
MODE_LDO2	Determines startup sequencing from the CMI code	This is a factory expert bit that should not be changed. Modifying this bit may result in unexpected IC behavior.
RST_LDO2	0 – LDO2 does not affect nRESET output 1 – LDO2 affects nRESET output	

LDO12_REG0A – LDO2 Configuration Register

Address = 0xCAh	Default = 0x00h	Type = Basic Non-Volatile
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BIT	7	6	5	4	3	2	1	0
Name	RFU				RFU			
Default	0000				0000			
Access	R/W				R/W			

Name	Description	Notes
RFU	Reserved for Future Use	Do not change this register value. Changing the register value can affect IC functionality.
RFU	Reserved for Future Use	Do not change this register value. Changing the register value can affect IC functionality.

Referenced Documents

The reference documents below take precedence over the contents of this application note and should always be consulted for the latest information.

ACT88420 Data Sheet

Contact Information

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