APPLICATION NOTE AN135

NXP iMX6UL/iMX6ULL Power Solution Using the ACT88430 PMIC

Abstract

This application note shows Qorvo's ACT88430 integrated PMIC power solution for the iMX6UL/iMX6ULL processor. It also shows how to convert an existing ACT8847 based design to an ACT88430 based design.

Introduction

The ACT88430 PMIC is an integrated power management integrated circuit. It powers a wide range of processors, including computer vision, solidstate disk drives, video processors, FPGA's, and microcontrollers. It is highly flexible and can be reconfigured via I^2C for multiple applications without the need for PCB changes. The low external component count and high configurability significantly speeds time to market. The core of the device includes 4 DC/DC step down converters using integrated power FETs and 3 low-dropout regulators (LDOs). Buck1 and LDO1 can be configured as a load switch.

Qorvo has optimized the ACT88430QJ120 and the ACT88430QJ123 to support the NXP iMX6UL/iMX6ULL microprocessor sequencing and voltage requirements. The ACT88430 solutions provide a smaller, more optimized solution than Qorvo's existing ACT8847 power solution. The ACT88430 is designed in a newer, more advanced silicon process, and provides better performance in a smaller package than the ACT8847. The ACT88430 offers more configurability, higher output current. The ACT88430 has a smaller output inductor, capacitor, and package, which provides for more compact designs.

Table 1. ACT88430 and ACT8847 Key Differences

ACT88430		ACT8847	
Input voltage range	Vin = 2.7V to 5.5V	Input voltage range	Vin = 2.5V to 5.5V
Power rails	7 (4 Bucks + 3 LDOs)	Power rails	13 (4 Bucks + 9 LDOs)
Buck1	4A	REG1_Buck	1.5A
Buck2	2.5A	REG2_Buck	2.8A
Buck3	2.5A	REG3_Buck	2.8A
Buck4	2.5A	REG4_Buck	1.5A
LDO1	800mA	REG5_LDO	150mA
LDO2	200mA	REG6_LDO	150mA
LDO3	200mA	REG7_LDO	350mA
-	-	REG8_LDO	350mA
-	-	REG9_LDO	350mA
-	-	REG10_LDO	150mA
-	-	REG11_LDO	350mA
-	-	REG12_LDO	350mA
-	-	REG13_LDO	50mA
Operating Junction Temperature	-40 to 125°C	Operating Junction Temperature	-40 to 125°C
Package	5 x 5 mm 40 pin FCQFN	Package	6×6 mm TQFN66-48

Replacing the ACT8847 with the ACT88430

Replacing the existing ACT8847 solution with the upgraded ACT88430 requires a few simple steps. The device packages and pinouts are quite different, so this change requires a new PCB layout; however, the outputs and features are similar. The user just needs to match the ACT88430 outputs to the iMX6UL/iMX6ULL power inputs per Figure 1.

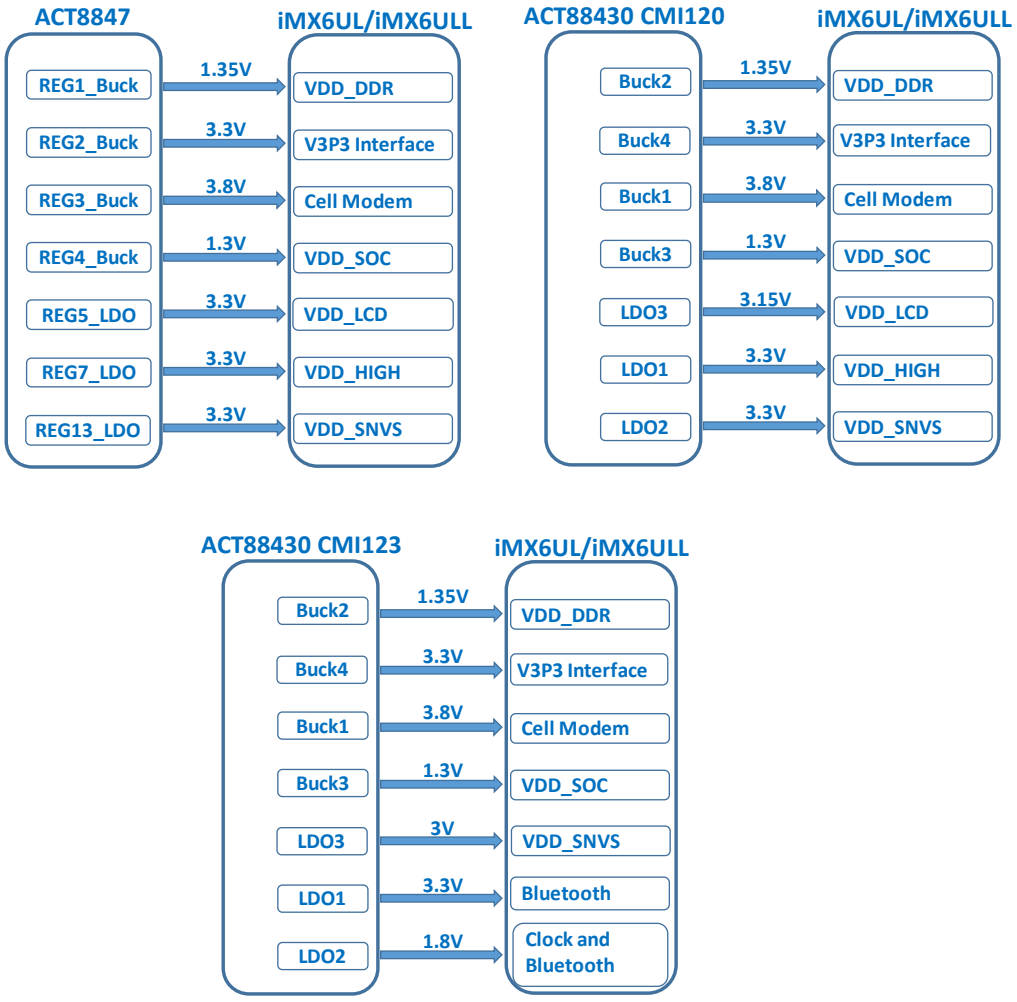


Figure 1. ACT8847 and ACT88430 Power Connections to the NXP iMX6UL/iMX6ULL

ACT88430QJ120 Output Voltages and Sequencing

ACT88430QJ120 is specifically optimized to power the NXP iMX6UL/iMX6ULL. The output voltages and sequencing are directly compatible with the iMX6UL/iMX6ULL processor. The solution is configured for a 5V input voltage.

The following table shows the ACT88430 output voltages, current limit, and switching frequencies.

Table 2. ACT88430QJ120 Voltage and Currents

Rail	VSET0-Active Mode Voltage (V)	VSET1- DVS Voltage (V)	Current Limit Setting(A)	Fsw (kHz)
Buck1	3.8	3.3	5.3	2250
Buck2	1.35	1.35	2	2250
Buck3	1.3	1.3	2	2250
Buck4	3.3	3.3	4	2250
LDO1	3.3	n/a	0.35	n/a
LDO2	3.3	n/a	0.315	n/a
LDO3	3.15	n/a	0.39	n/a
EXT_EN	n/a	n/a	n/a	n/a

Table 3. ACT88430QJ120 Startup and Sequencing

Rail	Sequence Order	Sequencing Input Trigger	StartUp Delay (us)	Soft-Start (us)
LDO2	1	VIN_UVLO	313	220
LDO1	2	EXT_PG	213	570
Buck2	3	LDO1	513	485
Buck3	4	Buck2	513	485
Buck4	5	Buck3	513	204
LDO3	6	Buck4	313	126
Buck1	7	GPIO	313	485

Table 3 and Figure 2 shows the startup and sequencing, which is meets NXP's iMX6UL/iMX6ULL sequencing requirements.

CMI 120 Startup

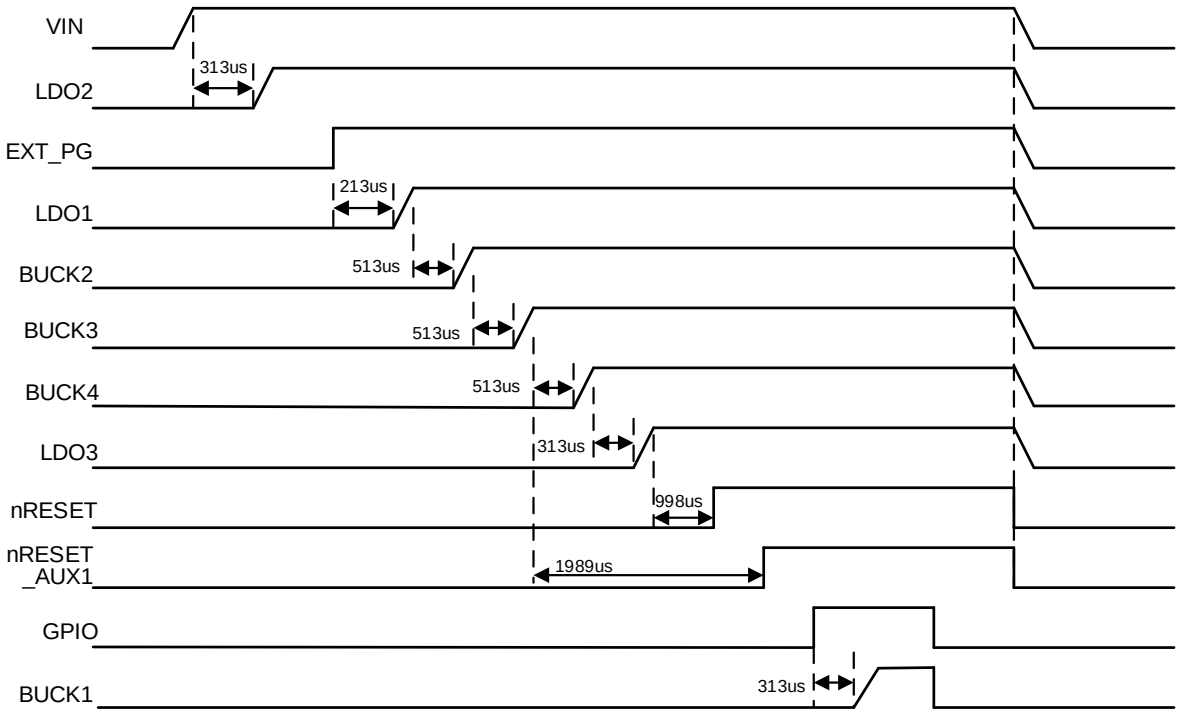


Figure 2. ACT88430QJ120 Startup

PIN Functions

The ACT88430 input and output pins are configurable via CMI configurations. Refer to the ACT88430 datasheet for more details about the available functionality. The ACT88430QJ120 pins, which are designed to support the IMX6UL/IMX6ULL, support the following functions.

PWREN (pin F6)

The PWREN pin is not functional with CMI 120. Pull up to VCC.

EXT_PG (pin F5)

EXT_PG is configured as an external input to turn on LDO1 and start the turn on sequencing. When EXT_PG is L, LDO1 is disabled. When EXT_PG is H, LDO1 is enabled.

EXT_EN (pin E5)

The EXT_EN pin is not used and can be left open or pulled to GND.

MODE (pin F3)

The MODE pin configures Buck1 into either bypass or switcher mode. MODE must be connected to AGND to configure Buck1 into switcher mode.

GPIO (pin F4)

GPIO is configured as an input to turn on Buck1. GPIO H = Buck1 on. GPIO L = Buck1 off.

POK (pin C3)

The POK pin is not used and can be left open or pulled to GND.

PG (pin E4)

The PG pin is not used and can be left open or pulled to GND.

IRQ (pin C4)

The IRQ pin is not used and can be left open or pulled to GND.

nRESET (pin D5)

The nRESET is triggered by all outputs. It goes high 998us after the last regulator, LDO3, goes into regulation.

nRESET_AUX1 (pin C6)

The nRESET_AUX1 is triggered from Buck4. It goes high 1989us after Buck4 goes into regulation.

nRESET_AUX2 (pin C5)

The nRESET_AUX2 pin is not used and can be left open or pulled to GND.

Device ID

The CMI 120 Device ID (register 0x7Dh) = 0x20h

I2C Address

The CMI 120 7-bit I2C address is 0x53h. This results in 0xA6h for a write address and 0xA7h for a read address.

ACT88430QJ120 Reference Schematic

The following schematic shows the general ACT88430 schematic. Note that all functions are integrated, and that the user only needs to add the power supply's external capacitors and inductors.

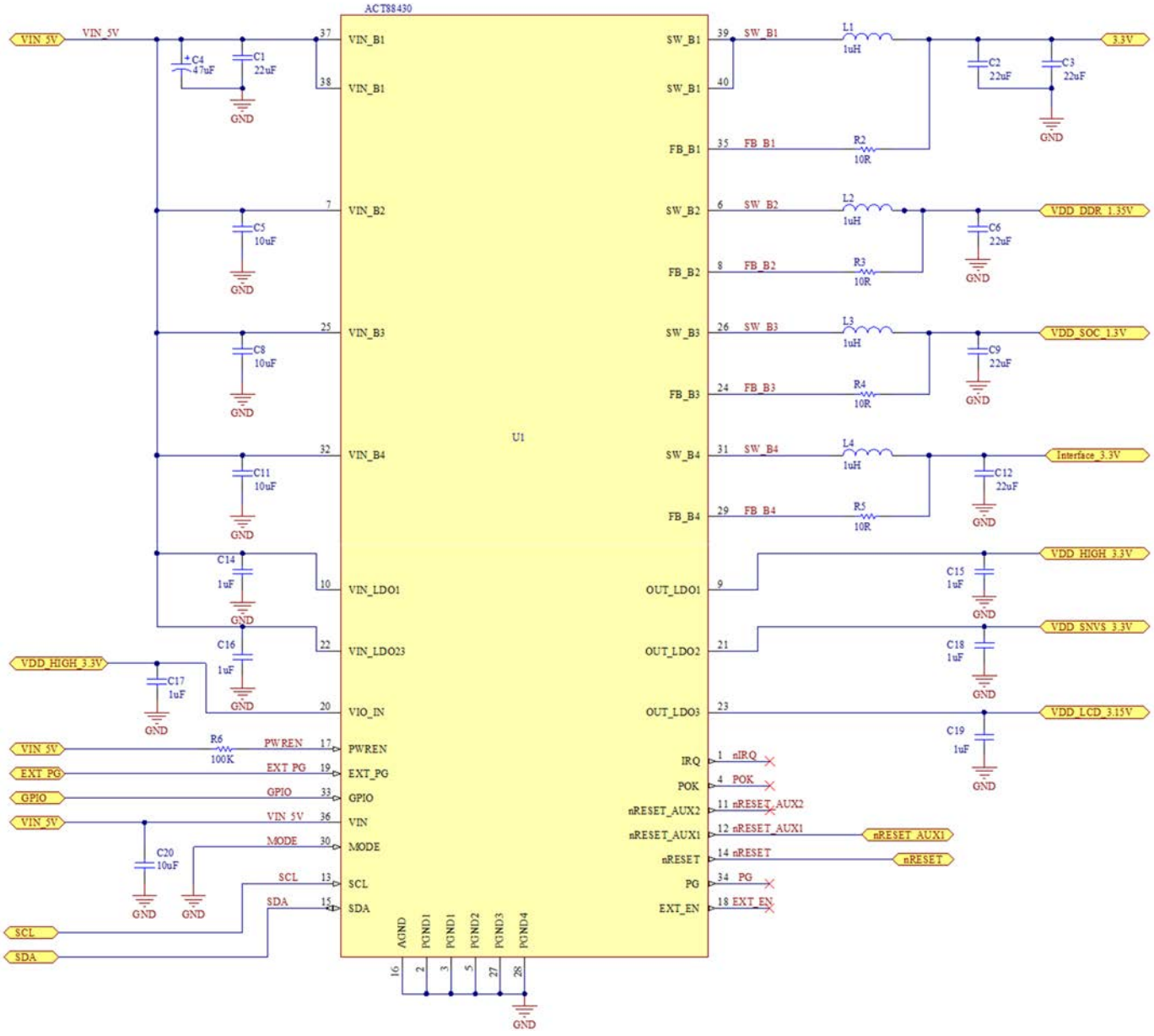


Figure 3. ACT88430 Reference Schematic

Referenced Documents

ACT88430QJ123 is specifically optimized to power the NXP iMX6UL/iMX6ULL. The output voltages and sequencing are directly compatible with the iMX6UL/iMX6ULL processor. The solution is configured for a 5V input voltage.

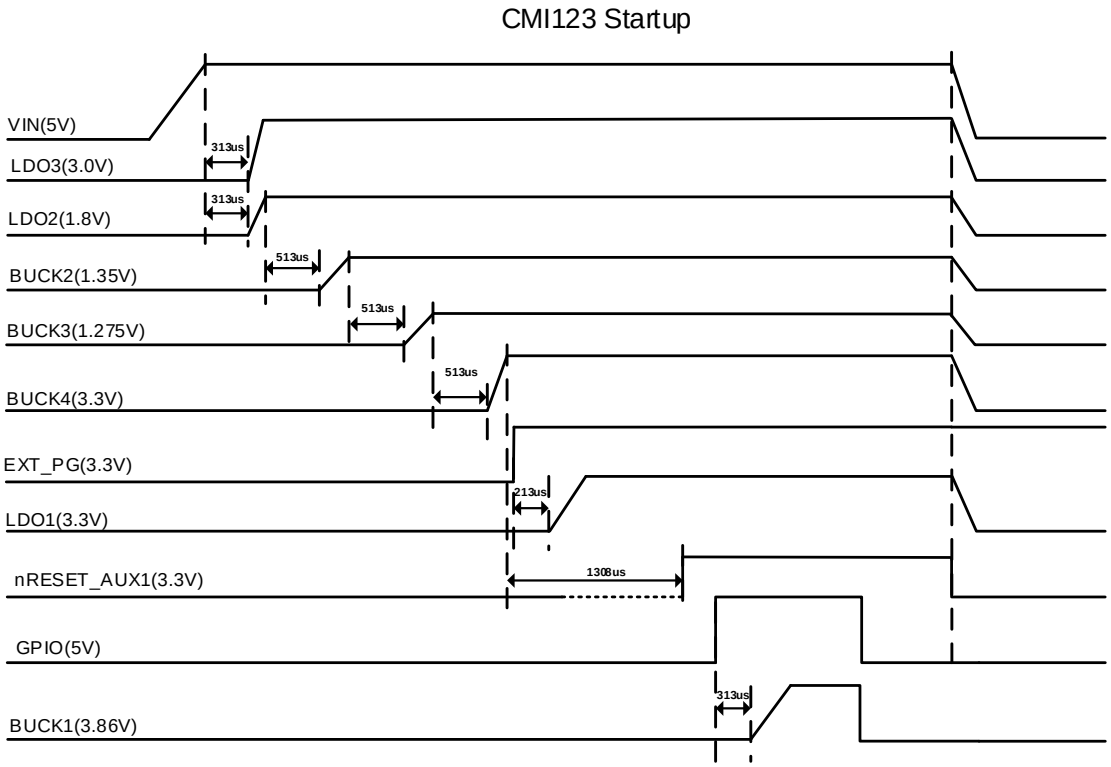
The following table shows the ACT88430 output voltages, current limit, and switching frequencies.

Table 4. ACT88430QJ123 Voltage and Currents

Rail	Active Mode Voltage VSET0 (V)	DVS Voltage VSET1 (V)	DVS Voltage Trigger	Sleep Mode Voltage (V)	Current Limit (A)	Fsw (kHz)
Buck1	3.86	3.86	n/a	0	5.3	2250
Buck2	1.35	1.35	n/a	0	2	2250
Buck3	1.275	1.275	n/a	0	2	2250
Buck4	3.3	3.3	n/a	0	4	2250
LDO1	3.3	n/a	n/a	0	0.5	n/a
LDO2	1.8	n/a	n/a	1.8	0.315	n/a
LDO3	3.0	n/a	n/a	3.0	0.39	n/a
EXT_EN	n/a	n/a	n/a	n/a	n/a	n/a

Table 5. ACT88430QJ123 Startup and Sequencing

Rail	Sequence Order	Sequencing Input Trigger	StartUp Delay (us)	Soft-Start (us)
LDO3	1	UVLO	313	126
LDO2	1	UVLO	313	220
Buck2	2	LDO2	513	485
Buck3	3	Buck2	513	485
Buck4	4	Buck3	513	204
LDO1	5	EXT_PG	213	570
Buck1	6	GPIO	313	485



SLEEP Mode

SLEEP mode is not enabled. Pull PWREN to VCC.

DVS Mode

This CMI does not support DVS functionality.

POK Thresholds

POK_UV = 4.2V

POK_OV = 5.7V

PG

The PG pin is not used and can be left open or pulled to GND.

POK

The POK pin is not used and can be left open or pulled to GND.

EXT_EN

The EXT_EN pin is not used and can be left open or pulled to GND.

IRQ

IRQ pin is not used and can be left open or pulled to GND.

nRESET

The nRESET pin is programmed as an open drain output. The nRESET pin is not used and should be pulled to GND.

nRESET_AUX1

The nRESET_AUX1 pin is programmed as an open drain output. It goes high 1308us after Buck4 goes into regulation.

nRESET_AUX2

The nRESET pin is not used and should be pulled to GND.

EXT_PG

EXT_PG is configured as an external input to turn on LDO1 to start the turn on sequence. LDO1 turn on is gated by the AND of the internal Buck4 POK signal and the external EXT_PG input signa.

MODE

The MODE pin configures Buck1 into either bypass or switcher mode. MODE must be connected to AGND to configure Buck1 into switcher mode.

GPIO

GPIO is configured as an input to turn on Buck1. When GPIO is H, Buck1 is enabled. When GPIO is H, Buck1 is disabled.

PWREN

PWREN is not used and must be connected to VCC.

Buck1/2/3/4 Voltage Setting

Buck1/2/3/4 reference voltage is 0.8V. This sets the programmable voltage range between 0.8V to 3.998V in 12.5mV steps.

LDO1/2/3 Voltage Setting

The LDO1/2/3 reference voltage is 0.8V.

Device ID

The CMI 123 Device ID (register 0x7Dh) = 0x23h

I2C Address

The CMI 123 7-bit I2C address is 0x53h. This results in 0xA6h for a write address and 0xA7h for a read address.

Referenced Documents

The reference documents below take precedence over the contents of this application note and should always be consulted for the latest information.

ACT88430 Data Sheet

Contact Information

For the latest specifications, additional product information, worldwide sales and distribution locations:

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