QM33120W Datasheet

UWB Low-Power Transceiver

Product Overview

The QM33120W is a single-chip Ultra-Wideband (UWB) low-power low-cost transceiver device compliant to IEEE Std. 802.15.4-2020 and IEEE Std. 802.15.4z-2020 (BPRF mode). The device can be used in TWR, TDoA, and AoA systems to locate assets to an accuracy of 10 cm. They also provide a precision location and data transfer simultaneously.

WLCSP 52 3.1 mm x 3.5 mm

Key Features

- IEEE 802.15.4-2020 UWB IEEE 802.15.4z-2020 (BPRF mode)
- Supports channels 5 & 9 (6489.6 MHz & 7987.2 MHz)
- Supports 2-way ranging, TDoA and AoA location schemes
- Low external component count
- Supports enhanced Time-of-Flight security modes
- Integrated HW AES 256
- Low power consumption
- Data rates of 850 kbps, 6.8 Mbps
- Packet length from zero to 1023 bytes
- Custom modes to support ultra-short frame lengths
- Integrated MAC support features
- SPI interface to host MCU supports rates up to 32 MHz
- Supports Japan and Korea regulatory compliance

Key Benefits

- Asset location to an accuracy of 10 cm
- High multipath fading immunity
- Secure ranging/distance measurement using STS (Scrambled-Timestamp)
- Supports high tag densities in real-time location systems (RTLS)
- Low-cost precision location
- Suitable for coin cell applications

Applications

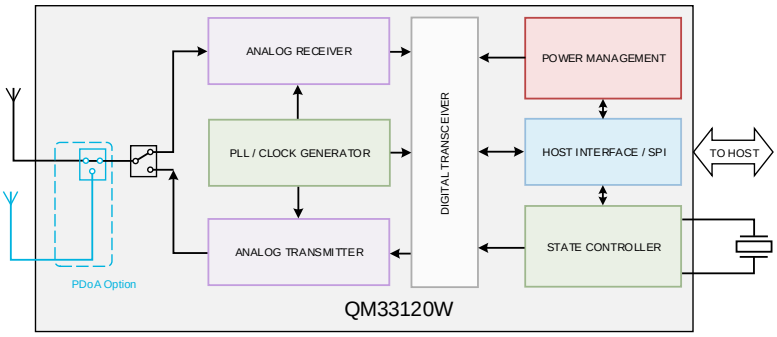
- Precision real-time location systems (RTLS) using TWR, TDoA, or AoA schemes in a variety of mobile, consumer, and industrial applications
- Location-aware wireless sensor networks
- Geo-fencing safety
- Secure access/payments
- Low latency wireless data comms
- Location-aware controls

Ordering Information

Part No.	Description	Quantity
QM33120WSR	UWB Transceiver WLCSP dual RF port	100pc
QM33120WTR13	UWB Transceiver WLCSP dual RF port	3000pc

fira | The Power to Be Precise

Functional Block Diagram



High-Level Block Diagram

Table of Contents

List of Figures

List of Tables

IC Description

The QM33120W IC is a fully integrated low-power, single chip CMOS RF 6.5 GHz-8 GHz IR-UWB transceiver device compliant with the IEEE 802.15.4-2020 (HRP UWB PHY), IEEE 802.15.4z–2020, and IEEE 802.15.8 standards.

QM33120W device consist of an analog front-end containing a receiver and a transmitter and a digital backend that interfaces to an off-chip host processor. A TX/RX switch is used to connect the receiver or transmitter to the antenna port. Temperature and voltage monitors are provided on-chip.

The receiver consists of an RF front-end which amplifies the received signal in a low-noise amplifier before down-converting it directly to the baseband. The receiver is optimized for wide bandwidth, linearity, and noise figure. This allows each of the supported UWB channels to be down-converted with minimum additional noise and distortion. The baseband signal is demodulated, and the resulting received data is made available to the host controller via SPI.

The transmit pulse train is generated by applying digitally encoded transmit data to the analog pulse generator. The pulse train is up-converted to a carrier generated by the synthesizer and centered on one of the permitted UWB channels. The modulated RF waveform is amplified before transmission from the external antenna.

The device has two RF antenna ports and can be used for Angle of Arrival (AoA) applications. In this case, the receiver switches between antenna ports to enable a PDoA measurement.

The QM33120W has an on-chip One-Time Programmable (OTP) memory. This memory can be used to store calibration data such as TX power level and crystal initial frequency error adjustment. These adjustment values can be automatically retrieved when needed.

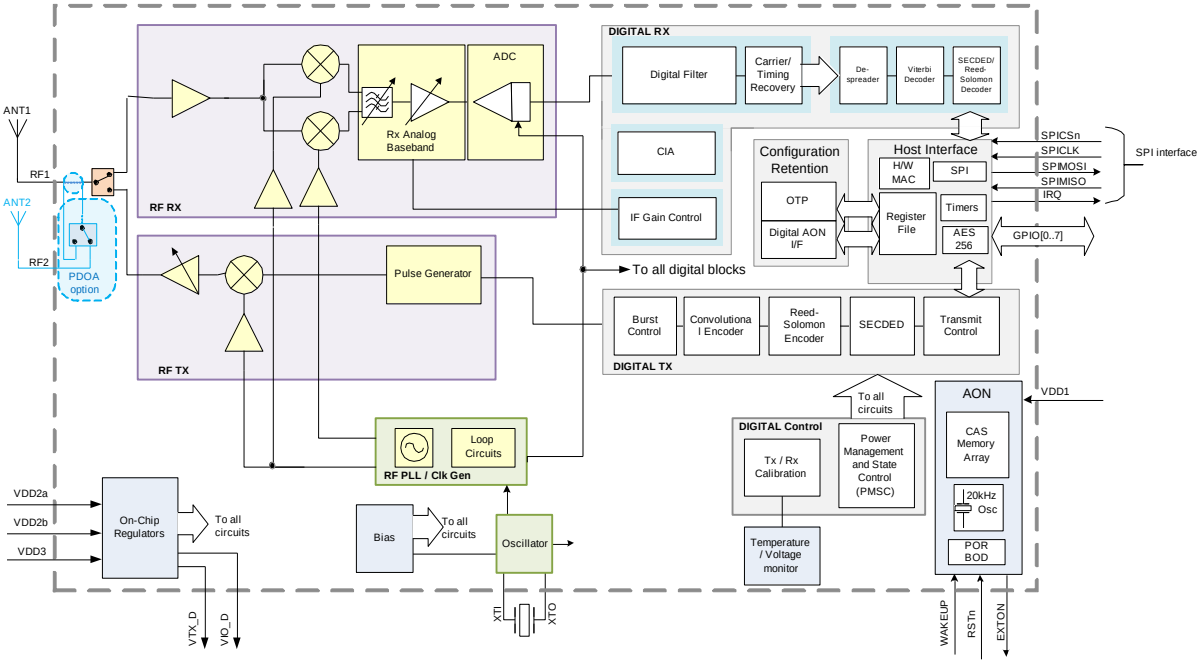


Figure 1: QM33120W Block Diagram

The Always-On (AON) memory is 256 bytes and can be used to retain QM33120W configuration data during the lowest power operational states. The AON can operate directly from the battery. This data is downloaded during crystal startup automatically.

The QM33120W contains a phase-locked-loop (PLL) with integrated loop filters. This PLL provides the RF local oscillator signals for the Rx Mixer and the Tx RF frequency carrier to the Tx mixer. The channel information signal defines the output channel frequency as follows; channel 5 = 6489.6 MHz, channel 9 = 7987.2 MHz.

The QM33120W has various debug and test options (RF loopback, event counters, test modes, and more) and gives access to internal signals for on-the-bench debugging and to simplify production tests.

The QM33120W incorporates timestamp system security features to prevent all known hacking-type attacks such as ‘imposter’, ‘cicada’, ‘parasite’ ‘record & replay’ attacks, etc. MAC features implemented include CRC generation, CRC checking, and receive frame filtering.

1.1 Backward Compatibility with DW1000 and DW3000

The QM33120W can be configured to be backward compatible over-the-air with DW1000 on channel 5 and for data rates of 6.8 Mbps and 850 kbps. It is also compatible with the DW3000 product line with some differences primarily related to GPIO functionality, the SPI boot mode cannot be configured by GPIO states at power on, the OTP method can still be used.

2 Pin Configuration and Descriptions

The QM33120W is supplied in WLSCP (52 balls) package. The pin assignments are illustrated below and the description is given in the table below.

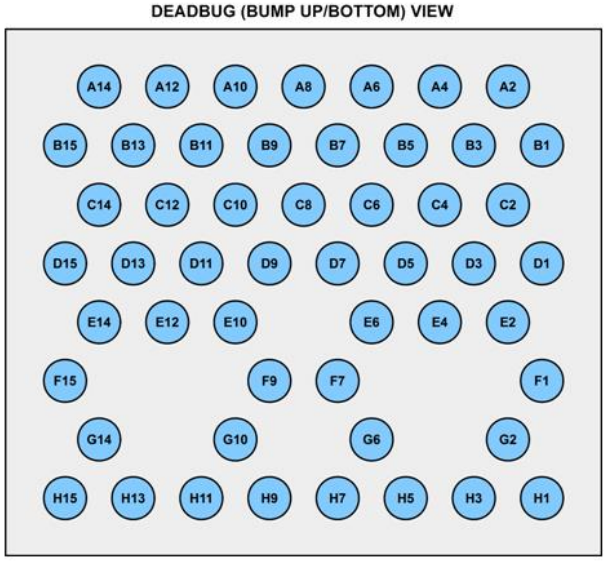


Figure 2: WLSCP Ball Configuration

Table 1: QM33120W Pin functions

CSP Ball #	Signal Name	I/O Type (Default)	Description
B1	IRQ/GPIO8	DIO (O-L)	Interrupt Request output from the QM33120W to the host processor. By default, IRQ is an active-high output but may be configured to be active-low if required. For correct operation in SLEEP and DEEPSLEEP modes, it should be configured for active-high operation. This pin will float in SLEEP and DEEPSLEEP states and may cause spurious interrupts unless pulled low. When the IRQ functionality is not being used the pin may be reconfigured as a general purpose I/O line, GPIO8.
C4	GPIO6 /EXTSWRX/ PDoA_SW2	DIO (I)	General purpose I/O pin. After power-up, the pin will default to a General Purpose I/O pin. It may be configured EXTSWRX, the pin will go high at the start of RX. When it's configured as PDoA_SW2, the pin will go high when the device is receiving or transmitting from RF port 1, used for AoA switching (within a frame), switches within 1us STS gap.
C2	RESV/ RXOKLED/ GPIO0	DIO(I)	General purpose I/O pin. After power-up, the software should change its function to the desired user mode. It may be configured for use as an RXOKLED driving pin can be used to indicate the reception of a good frame.

CSP Ball #	Signal Name	I/O Type (Default)	Description
D3	RESV/ SFDLED/ GPIO1	DIO (O-L)	General purpose I/O pin. After power-up, the software should change its function to the desired user mode. It may be configured for use as an SFDLED driving pin that can be used to indicate when SFD (Start Frame Delimiter) is found by the receiver. It can also be configured as a GPIO.
D1	GPIO5/COEX OUT/ EXTRXE (PDoA_SW1)	DIO (I)	General purpose I/O pin, after power-up, the pin will default to a General Purpose I/O pin. It may be configured for use as COEX_OUT, an output flag that can be configured via software to indicate an RX, TX, or both. It can also be configured as PDoA_SW1, in this mode, it will go high 100ns before the start of RX.
E4	RESV/ RXLED/ GPIO2	DIO (I)	General purpose I/O pin. After power-up, the software should change its function to the desired user mode. It may be configured for use as an RXLED driving pin that can be used to indicate receive mode. It can also be configured as a GPIO.
E2	RESV/ TXLED/ GPIO3	DIO (I)	General purpose I/O pin. After power-up, the software should change its function to the desired user mode. It may be configured for use as a TXLED driving pin that can be used to indicate a transmission. It can also be configured as a GPIO.
F1	GPIO4/ COEXIN/ EXTTXE (PDoA_SW0)	DIO (I)	General purpose I/O pin, after power-up, the pin will default to a General Purpose I/O pin. It may be configured for use as COEXIN, an input used to abort any ongoing TX or RX RF operations. Can be SW configured for TX, RX, or both. It may be configured PDoA_SW0, it will stay on during TX frame, turning on approx. 10us before the first TX pulse.
G2	SYNC/GPIO7 /PDoA_SW3	DIO (I)	The SYNC input pin is used for external synchronization. When the SYNC input functionality is not being used this pin may be reconfigured as a general purpose I/O pin, GPIO7. When it's configured as PDoA_SW3, the pin will go high when the device is receiving or transmitting from RF port 2. Used for AoA switching (within a frame), switches within 1us STS gap.
E6 E10 E12 F7	GND	G	RF ground pin *.
H5	RF2	AIO	RF port for antenna 2 (50 Ω single-ended RF connection). When in use for PDoA variant, a 2 pF is required on the pin. When not in use for PDoA variant, a 2pF is required on the pin with 50 Ω termination. In non PDoA chip variants, the 2 pF is not required, but the pin should be grounded with 50 Ω.
F9 G6 G10 H1 H3	GND	G	RF ground pin *.
H11	RF1	AIO	RF port for antenna 1 (50 Ω single-ended connection). A 2 pF is required on the pin.
H7 H9 H13	GND	G	RF ground pin *.
H15	XTI	AI	Reference crystal input or external reference overdrive pin.
G14	XTO	AI	Reference crystal output.

CSP Ball #	Signal Name	I/O Type (Default)	Description
F15	VDD2a	P	Voltage Supply (2.4 V to 3.6 V) * A ferrite bead must be placed between B15 and F15 for isolation.
B15	VDD2b	P	Voltage Supply (2.4 V to 3.6 V) * A ferrite bead must be placed between B15 and F15 for isolation.
D11 E14	VSS2	G	Ground return for VDD2.
C12 D13	VSS3	G	Ground return for VDD3.
D15	VDD3	P	Voltage Supply (1.5 V to 3.6 V).
C14	VTX_D	PD	TX supply decoupling. Requires external capacitor to ground *.
B13	VDD1	P	Main power supply (1.62V – 3.6V). Should be Always ON *. The following I/Os are supplied by this pin: WAKEUP, EXTON, RSTn, SPICLK, SPICSn, SPICDI, and SPICDO.
A14 B11 C8 C10 D9	VSS1	G	Ground return for VDD1, also PSUB (substrate) connection.
A12	EXTON	DO (O-L)	External device enable. Asserted during the wake-up process and held active until the device enters sleep mode. Can be used to control external DC-DC converters or other circuits that are not required when the device is in sleep mode to minimize power consumption.
B9	RESV/ WAKEUP	DI	When asserted into its active high state, the WAKEUP pin brings the QM33120W out of SLEEP or DEEPSLEEP states into operational mode. This should be connected to the ground if not used. When this pin is pulled low, the D3 pin will drive as an output.
A10	RSTn	DIO (O-H)	Reset pin. Active-Low Output. May be pulled low by the external open-drain driver to reset the QM33120W. Must not be pulled high by the external source.
A8	SPICLK	DI	SPI peripheral clock input.
B7	SPICDO (SPIMOSI)	DI	SPI peripheral data input (Controller data output).
A6	SPICDI (SPIMISO)	D0 (O-L)	SPI peripheral data output (Controller data input).
B5	SPICSn	DI	SPI chip select. This is an active-low enable input. The high-to-low transition on SPICSn signals the start of a new SPI transaction. SPICSn can also act as a wake-up signal to bring QM33120W out of either SLEEP or DEEPSLEEP states.
A4	VIO_D	PD	IO supply decoupling. Internally connected to the VDD1 with a switch to allow disconnect from VDD1 for ultra-low-power consumption mode.
A2 B3 C6 D5 D7	VSS	G	Ground return for internal digital supply *.

(*) Refer to design guide schematics and layout.
Note: GPIO pins are not suitable to drive LEDs directly. See Table 6 for details of the maximum current limit. Any signal with the suffix 'n' indicates an active low signal.

Table 2: Description of Abbreviations

Abbreviation	Description
AI	Analog Input.
AIO	Analog Input / Output.
AO	Analog Output.
DI	Digital Input.
DIO	Digital Input / Output.
DO	Digital Output.
G	Ground.
P	Power Supply.
PD	Power Decoupling.
NC	No Connect.
O-L	Defaults to output, low level after reset.
O-H	Defaults to output, high level after reset.
I	Defaults to input.
RESV	Reserved mode, Defaults to input. Software should switch to preferred mode on start up.

3 Electrical Characteristics

3.1 Absolute Maximum Ratings

Table 3: QM33120W Absolute Maximum Ratings

Parameter	Min.	Max.	Units
Supply voltage	-0.3	4.0	V
Receiver power		14	dBm
Storage temperature	-65	+150	˚C
Operating temperature	-40	+85	˚C

3.2 Nominal Operating Conditions

Table 4: QM33120W Nominal Operating Conditions

Parameter	Min.	Typ.	Max.	Units	Condition / Note
Receiver power			14	dBm	
Supply voltage VDD1	1.62	3.0	3.6	V	
Supply voltage VDD2a and VDD2b	2.4	3.0	3.6	V	
Supply voltage VDD3	1.5	3.0	3.6	V	
Voltage on GPIO0-5, WAKEUP, RSTn, SPICSn, SPICDO, SPICLK			VDD1 + 0.3V	V	Note that 3.6 V is the max voltage that should be applied to these pins.

Note: Unit operation is guaranteed by design when operating within these ranges.
Sufficient headroom for any power supply voltage ripple should be considered in system designs.

3.3 DC Characteristics

Conditions T_{amb} = 25 ˚C, all supplies at 3.0 V unless otherwise stated.

Table 5: QM33120W DC Characteristics

Parameter	Min.	Typ.	Max.	Units	Condition / Note
Supply current DEEP SLEEP mode		210		nA	
Supply current SLEEP mode		810		nA	
Supply current IDLE_PLL mode		16		mA	
Supply current IDLE_RC mode		6		mA	
Supply current INIT mode		4		mA	
Current single frame Tx/Rx with 47uF capacitor					
TX CH5		14		mA	Refer to section 7.4.1 for details of single TX frame configuration.
TX CH9		17		mA	
RX CH5		16		mA	Refer to section 7.4.3 for details of single RX frame configuration.
RX CH9		19		mA	
Peak current continuous Tx/Rx					
TX CH5 (nominal power -41.3 dBm/MHz)	32	40	53	mA	-40°C to 85°C Continuous TX is only used as test mode. In a typical operation, TX is powered up for frame transmission then powered down.
TX CH5 (max power -32.3 dBm/MHz)	40	52	67	mA	
TX CH9 (nominal power -41.3 dBm/MHz)	43	50	62	mA	
TX CH9 (max power -32.3 dBm/MHz)	51	62	76	mA	

Parameter	Min.	Typ.	Max.	Units	Condition / Note
RX CH5	47	68	89	mA	-40°C to 85°C.
RX CH9	61	82	107	mA	-40°C to 85°C.
Digital input voltage high	0.7 * VDD1			V	
Digital input voltage low			0.3 * VDD1	V	
Digital output voltage high	0.7 * VDD1			V	Assumes 500 Ω load.
Digital output voltage low			0.3 * VDD1	V	Assumes 500 Ω load.
Digital output drive current					
GPIOx, IRQ	4	6		mA	
SPICDI	8	10		mA	
EXTON	3	4		mA	

3.4 Receiver AC Characteristics

Conditions T_{amb} = 25 ˚C, all supplies at 3.0 V unless otherwise stated.

Table 6: QM33120W AC Characteristics

Parameter	Min.	Typ.	Max.	Units	Condition / Note
Center Frequency - Channel 5		6489.6		MHz	
Center Frequency - Channel 9		7987.2		MHz	
Channel bandwidth		499.2		MHz	Programmable.
Input P1dB compression point Channel 5		-25.4		dBm	
Input P1dB compression point. Channel 9		-27.1		dBm	
In-band blocking level		-82.3		dBm	Chip-referred (power at the pin) to give 1% PER with 3 dB desense.
Out-of-band blocking level		-22.3		dBm	Chip-referred (power at the pin) to give 1% PER with 3 dB desense (see Receiver Blocking).

3.5 Receiver Sensitivity Characteristics

The receiver sensitivity was measured at the 1% Packet Error Rate (PER).

Table 7: Test conditions of the Rx sensitivity measurements

Parameter	Value
Ambient Temperature	25 ˚C
Supply voltage	3.0V
PHR rate (of data packets)	850Kbps
Payload length (of data packets)	20 bytes
Preamble Code	9
PRF (Pulse repetition frequency)	64 MHz
SFD Type for Preamble for frames length 1024	Decawave-defined 16-symbol SFD
SFD Type for Preamble for frames length 64	IEEE 802.15.4z defined 8-symbol SFD
Carrier frequency offset	±10 ppm

Table 8: Rx Sensitivity Characteristics (Channel 5)

Typical Receiver Sensitivity (dBm/500 MHz)	Data Rate	Preamble length (symbols)	STS length (symbols)	Conditions
-93	6.8 Mbps	64	64	See Table 7
-100	850 Kbps	1024	n/a	See Table 7
-98	-	64	64	No data mode. See Table 7

Table 9: Rx Sensitivity Characteristics (Channel 9)

Typical Receiver Sensitivity (dBm/500 MHz)	Data Rate	Preamble length (symbols)	STS length (symbols)	Conditions
-91	6.8 Mbps	64	64	See Table 7
-98	850 Kbps	1024	n/a	See Table 7
-96	-	64	64	No data mode. See Table 7

3.6 Reference Clock AC Characteristics

T_{amb} = 25 ˚C, all supplies at 3.0 V.

Table 10: QM33120W Reference Clock AC Characteristics

Parameter	Min.	Typ.	Max.	Units	Condition / Note
Crystal oscillator reference frequency		38.4		MHz	A 38.4 MHz signal can be provided from an external reference in place of a crystal if desired.
Crystal specifications					
Load capacitance	10			pF	Depends on the crystal used and PCB parasitics. See section Reference Crystal Oscillator
Shunt capacitance	0		4	pF	
Drive level			200	µW	Depends on the crystal & load capacitance used.
Equivalent Series Resistance (ESR)			60	Ω	
Frequency tolerance			±20	ppm	QM33120W includes circuitry to trim the crystal oscillator to reduce the initial frequency offset.
Crystal trimming range	-20		+20	ppm	Trimming range provided by on-chip circuitry. Depends on the crystal used and PCB design.
External Reference (For example a TCXO)					
Amplitude	0.8		VDD2	Vpp	Must be AC coupled. A coupling capacitor value of 2200 pF is recommended.
SSB phase noise power density			-132	dBc / Hz	@1 kHz offset.
SSB phase noise power density			-145	dBc / Hz	@10 kHz offset.
Duty Cycle	40		60	%	Duty Cycle
Fast and Slow Oscillators					
Slow RC Oscillator	9	23	30	kHz	User programmable*. Minimum at VDD1=1.62 V, Maximum at VDD1=3.6 V
Fast RC Oscillator	105	115	130	MHz	Internally calibrated. Minimum at -40°C, maximum at +85°C

**Note: Chip start-up time depends on this clock. The typical frequency of the Slow RC oscillator is reflected in the chip start-up time of 913 us. With the time, required to download the AON after wake-up, the overall start-up time is ~1000 us. It is possible to trim the oscillator to the higher frequency in software, which would decrease the start-up time to ~770 us.*

3.7 Transmitter AC Characteristics

T_{amb} = 25 ˚C, all supplies at 3.0 V.

Table 11: QM33120W Transmitter AC Characteristics

Parameter	Min.	Typ.	Max.	Units	Condition / Note
Center Frequency - Channel 5		6489.6		MHz	
Center Frequency - Channel 9		7987.2		MHz	
Channel bandwidth		499.2		MHz	Programmable.
Maximum Output power spectral density Channel 5 (programmable)		-32		dBm / MHz	
Maximum Output power spectral density Channel 9 (programmable)		-33.5			
Maximum Output channel power Channel 5		-6		dBm/ 500 MHz	
Maximum Output channel power Channel 9		-7.5			
Load impedance		50		Ω	Single ended
Power level range		30		dB	See Transmit Power Adjustment
Output power variation with temperature		0	0.008	dB / °C	
Output power variation with voltage		0		dB / V	Internally regulated
Transmit bandwidth variation with temperature		0.2		MHz / °C	With internal calibration enabled

3.8 Link Budget

Using the receiver sensitivity above, expected transmission link budgets can be estimated with the following assumptions:

- Receiver sensitivities as per the Table 8 and Table 9. .
- Transmitter and receiver antennas have 0 dBi gain.
- No losses between the antenna and QM33120W RF pins.

The link budget is calculated as follows:
Link Budget (dB) = Maximum Output Channel Power (dBm/500 MHz) – Receiver Sensitivity Level (dBm/500 MHz)

Table 12: Link Budget

Typical Link Budget (dB)		Data Rate	Preamble Length (symbols)	STS length (symbols)	Condition / Note
CH5	CH9				
94	90.5	850 Kbps	1024	n/a	With 12 bytes data → max output power settings are used.
87	83.5	6.8 Mbps	64	64	With 12 bytes data → max output power settings are used.
92	88.5	-	64	64	With 12 bytes data → max output power settings are used.

3.9 Temperature and Voltage Monitor Characteristics

Table 13: Temperature and Voltage Monitor Characteristics

Parameter	Min.	Typ.	Max.	Units	Condition / Note
Voltage Monitor Range	1.62		3.6	V	
Voltage Monitor Accuracy		5		%	
Temperature Monitor Range	-40		85	°C	
Temperature Monitor Accuracy	-3		3	%	

3.10 Location Accuracy Characteristics

Table 14: QM33120W Location Accuracy Characteristics

Parameter	Min.	Typ.	Max.	Units	Condition / Note
Ranging accuracy[1]	-6		6	cm	BPRF3 packet. In line-of-sight conditions.
Ranging standard deviation		3		cm	
PDoA accuracy[3]	-12.5		12.5	deg	Measured over +/- 180 degrees PDoA.
Equivalent AoA accuracy[2]	-6.25		6.25	deg	
Equivalent AoA standard deviation[2]		2.5		deg	

[1] After calibration is applied.
[2] Note: in a typical PDoA based system the computed angle of arrival (AoA) accuracy is better than the PDoA accuracy by a factor of approximately two i.e., if PDoA accuracy is ±12.5° then AoA accuracy is ±6.25°.
[3] For optimal PDoA performance a carrier frequency offset of greater than \|5\| ppm is required between devices..

Table 15: QM33120W AoA standard deviation

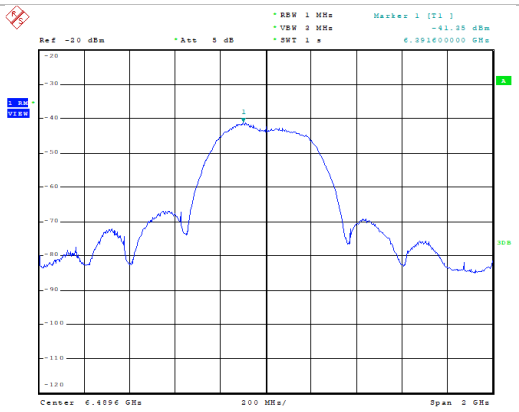
Equivalent AoA standard deviation(deg)		Preamble length (symbols)	STS length (symbols)	Condition / Note
CH5	CH9			
2	2.5	128	256	
3.5	5.5	64	64	

4 Typical Performance

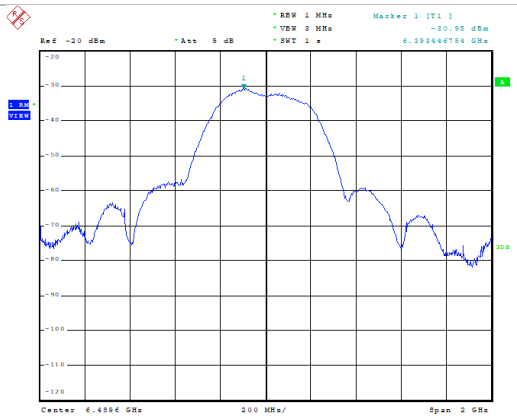
4.1 Transmit Spectrum

The typical transmit spectrums for channel 5 and channel 9 are in the pictures below.

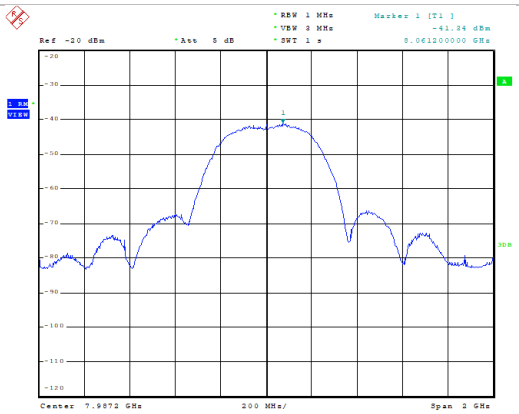
Table 16: QM33120W Transmit Spectrum



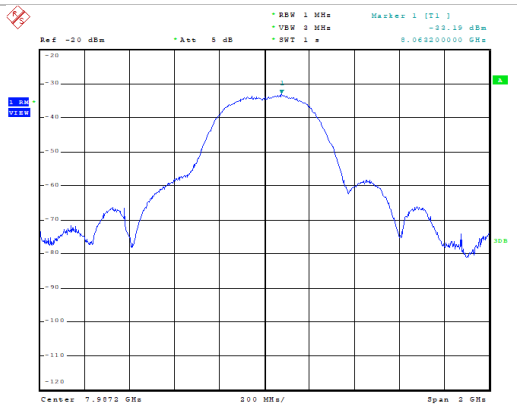
Typical Transmit Spectrum Channel 5



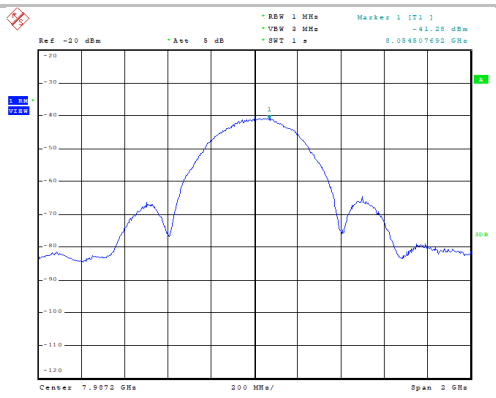
Maximum Transmit Spectrum Channel 5



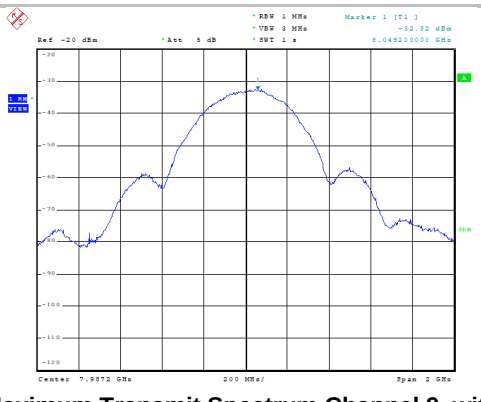
Typical Transmit Spectrum Channel 9



Maximum Transmit Spectrum Channel 9



Nominal Transmit Spectrum Channel 9, with alternative pulse shape

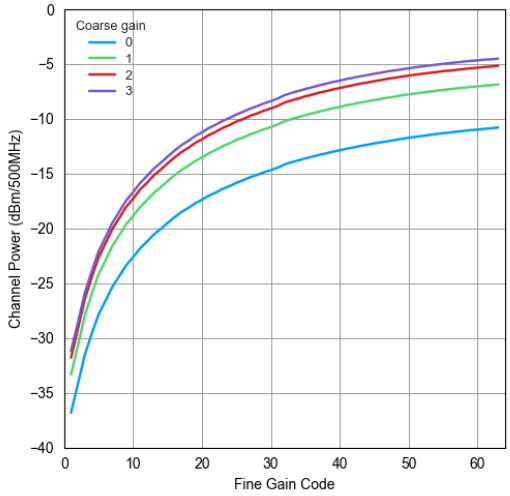


Maximum Transmit Spectrum Channel 9, with alternative pulse shape

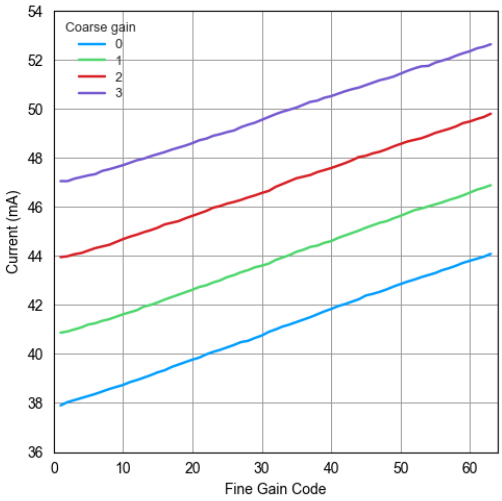
4.2 Transmit Power Adjustment

QM33120W has a coarse TX power adjustment and a fine TX power adjustment. The plots below show the relationship between these adjustments for each channel.

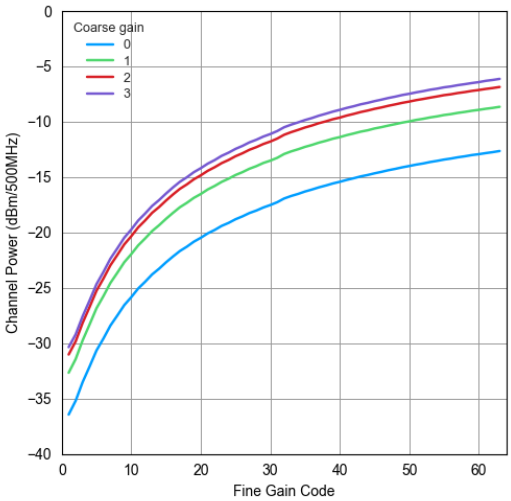
Table 17: QM33120W Transmit Power Adjustment



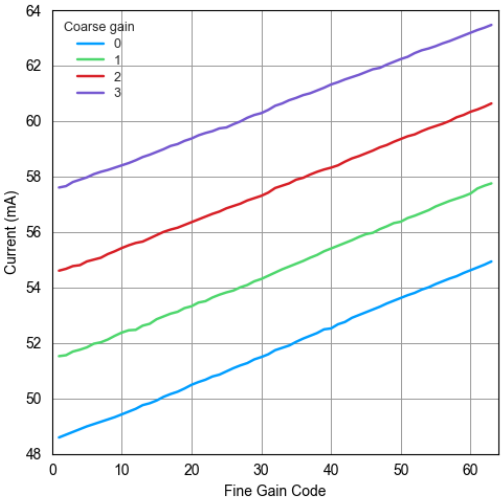
Tx power coarse and fine gain settings Channel 5



Tx current consumption for coarse and fine gain settings Channel 5



Tx power coarse and fine gain settings Channel 9



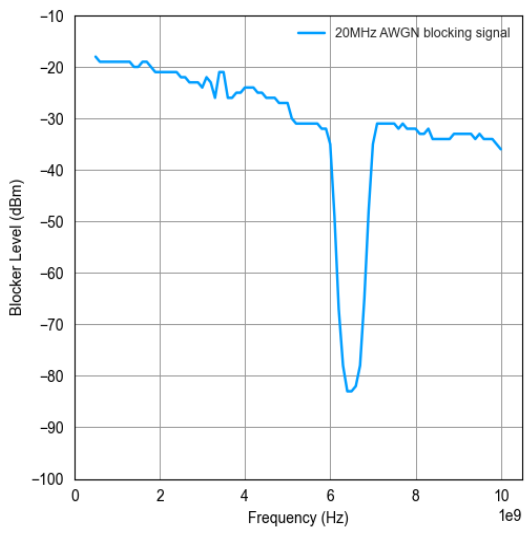
Tx current consumption for coarse and fine gain settings Channel 5

4.3 Receiver Blocking

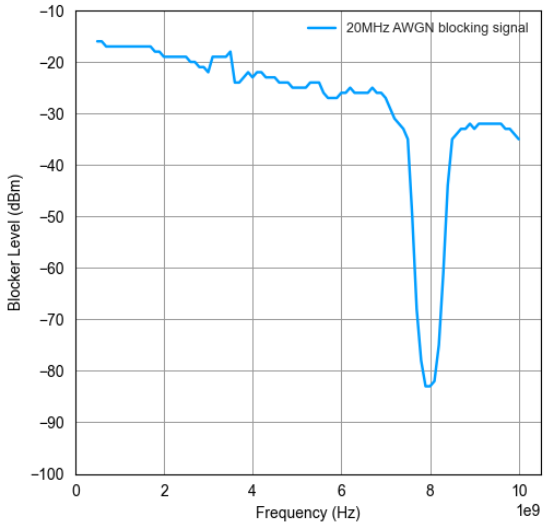
The following plots show typical blocking levels to give 1% UWB PER at 3 dB back off from the sensitivity point. The UWB configuration is:

- PRF = 64 MHz
- Preamble length = 64 symbols
- STS length = 64 symbols

Table 18: QM33120W Receiver Blocking



Blocking Performance Channel 5

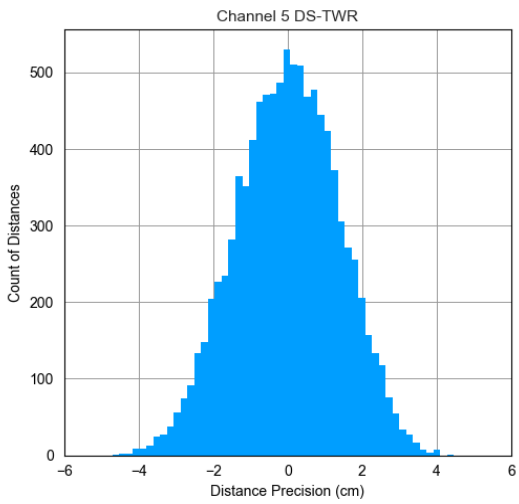


Blocking Performance Channel 9

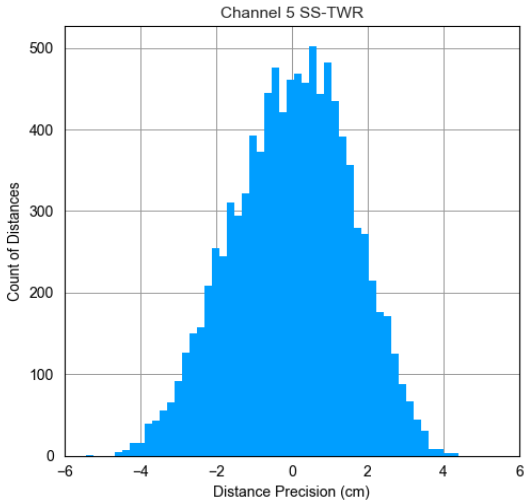
4.4 Ranging

The typically measured distribution of ranging performance (LOS) for 10000 samples.

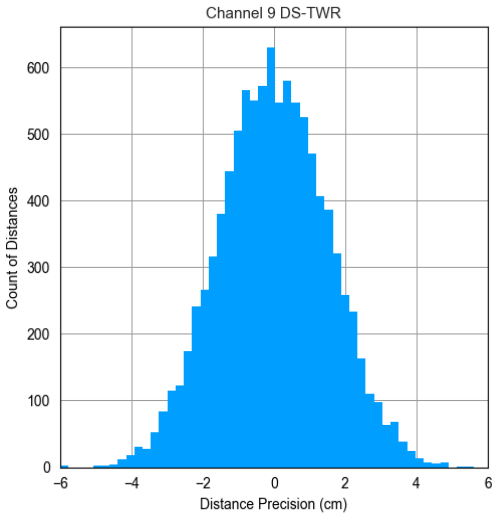
Table 19: QM33120W Ranging



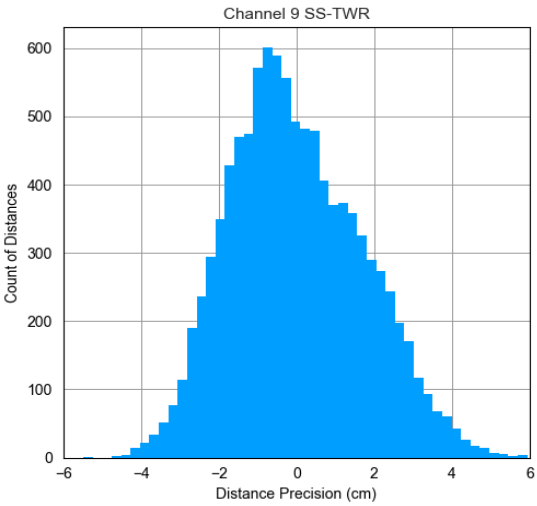
Double-sided Ranging Performance Channel 5



Single-sided Ranging Performance Channel 5



Double-sided Ranging Performance Channel 9



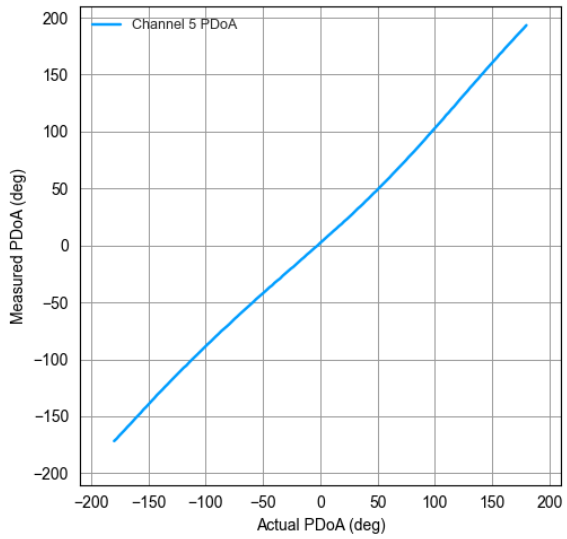
Single-sided Ranging Performance Channel 9

4.5 PDoA

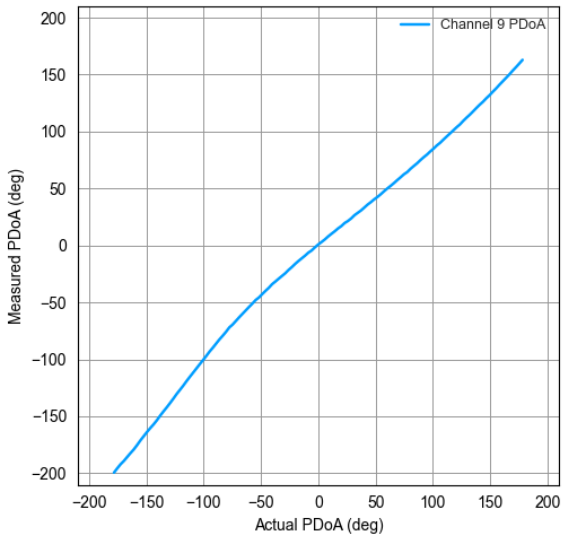
The following plots show typical measured PDoA performance. The UWB configuration is as follows:

- PRF = 64 MHz
- Preamble length = 128
- STS length = 256
- PDoA Mode = 3

Table 20: QM33120W PDoA



PDoA Performance Channel 5



PDoA Performance Channel 9

5 Functional Description

5.1 Physical Layer Modes

Please refer to IEEE Std. 802.15.4™-2020 and IEEE Std. 802.15.4z™-2020 for the PHY specification.

5.2 Supported Channels and Bandwidths

The QM33120W supports the following IEEE Std. 802.15.4™-2020 and IEEE Std. 802.15.4z™-2020 UWB channels:

Table 21: QM33120W Supported Channels and Bandwidth

UWB Channel Number	Center Frequency (MHz)	Bandwidth (MHz)
5	6489.6	499.2
9	7987.2	499.2

5.3 Supported Bit Rates and Pulse Repetition Frequencies (PRF)

The QM33120W supports IEEE Std. 802.15.4-2015, IEEE Std. 802.15.4™-2020 UWB standard bit rates 850 kbps and 6.81 Mbps and nominal PRF values of 16 MHz and 64 MHz, the Base PRF (BPRF) mode of a newly defined draft standard IEEE Std. 802.15.4z™-2020 is also supported.

Table 22: QM33120W Supported Bit Rates and Pulse Repetition Frequencies

PRF (MHz)	Data Rate (Mbps)
16*	0.85
16*	6.81
64**	0.85
64**	6.81

Actual PRF mean values are slightly higher for SHR as opposed to the other portions of a frame. Mean PRF values are 16.1/15.6 MHz and 62.89/62.4 MHz, nominally referred to as 16 MHz and 64 MHz in this document. Refer to [1], [2] (UWB PHY rate-dependent and timing-related parameters) for full details of peak and mean PRFs.
** Backward-compatible for IEEE Std. 802.15.4-2015 UWB devices*
*** Base PRF (BPRF) mode of IEEE Std. 802.15.4z™-2020 and IEEE Std. 802.15.4-2015*

In general, lower data rates give increased receiver sensitivity, increased link margin, and longer range but due to longer frame lengths for a given number of data bytes they result in increased air occupancy per frame and a reduction in the number of individual transmissions that can take place per unit time.

16 MHz PRF gives a marginal reduction in transmitter power consumption over 64 MHz PRF (BPRF).

5.4 Frame Format IEEE Std. 802.15.4-2015, IEEE Std. 802.15.4™-2020

IEEE Std. 802.15.4-2015, IEEE Std. 802.15.4™-2020 frames are structured as shown in Figure 3. Detailed descriptions of the frame format are given in the standard. The frame consists of a synchronization header (SHR) which includes the preamble symbols and start frame delimiter (SFD), followed by the PHY header (PHR) and data. The data frame is usually specified in a number of bytes and the frame format will include 48 Reed-Solomon parity bits following each block of 330 data bits (or less).

While zero length payloads and zero length PHR are supported the maximum frame length is 1023-bytes, including the 2-byte FCS.

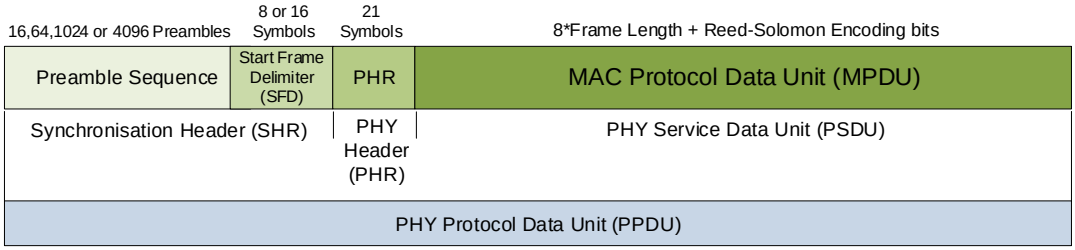


Figure 3: IEEE 802.15.4-2015 PPDU Structure

5.5 Frame Formats of IEEE Std. 802.15.4z™-2020

The 4z amendment added new packet formats to HRP UWB PHY incorporating a Scrambled Timestamp Sequence (STS) into the packet structure, defining four STS Packet Configurations as shown in Figure 4 below.

- Protocol 0 is a standard IEEE 802.15.4-2015 UWB packet structure. This ensures backward compatibility with DW1000, see frame format above.
- Protocol 1 includes Scrambled Timestamp Sequence (STS) between the start of frame delimiter (SFD) and the PHY header (PHR).
- Protocol 2 contains the STS after the payload is complete (there is a short configurable gap between the end of the payload and the start of the STS). The gap can be any integer value from 1 to 127 symbols.
- Protocol 3 is when there is no PHR and no payload.

The STS is a random sequence of positive and negative pulses generated using an AES-128 based deterministic random bit generator (DRBG). Only valid transmitters and receivers have the correct seed (i.e., the key and IV) to generate the sequence for transmission and to validly cross correlate in the receiver to determine the receive timestamp. The STS provides for secure receive timestamping and secure ranging.

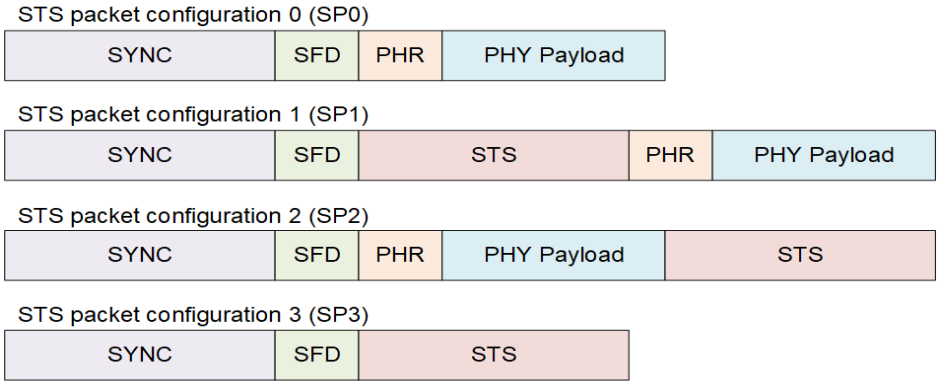


Figure 4: IEEE Std. 802.15.4z™-2020 HRP UWB PHY PPDU Formats

5.6 Proprietary Long Frames

The QM33120W offers a proprietary long frame mode where frames of up to 1023-bytes may be transferred. Refer to the QM33120W user manual for full details.

5.7 No Data Frames

The QM33120W offers zero-length payloads and zero-length PHR. This is for use cases where an alternative method of data communications is available. Refer to the QM33120W user manual for full details.

5.8 Host Controller Interface

The primary interface QM33120W is via a 4-wire SPI interface. QM33120W will act as a SPI peripheral device, in non-daisy-chain mode and operate at SPI clock frequencies up to 32 MHz.

5.9 SPI Functional Description

The host interface to QM33120W is a 4-wire SPI-compatible peripheral. The assertion of SPICSn low by the SPI controller (host) indicates the beginning of a transaction.
The SPI interface is used to read and write registers in the QM33120W device. All data and address transfer on the SPI is most significant bit first. All address bytes are transmitted with MSB first, and all data is transmitted commencing with the lowest addressed byte.

- Assertion low of SPICSn initializes transaction.
- De-assertion high of SPICSn ends the SPI transaction.
- The device supports direct and per-byte sub-addressing access to the full register space.
- Efficient block data reading/writing is allowed. Continuous, long transactions can be carried out while the addressed location is auto incremented on the QM33120W side.

The SPICDI (SPIMISO) I/O is required to go open drain when SPICSn is de-asserted, to allow interoperation with other peripherals on the SPI bus.
SPI daisy-chaining is not supported. This is the mode where the CDO (SPIMOSI), CDI (SPIMISO) lines are passed through a device when it is not chip selected.

5.10 SPI Timing Parameters

The SPI peripheral complies with the Motorola SPI protocol within the constraints of the timing parameters listed in the table below and illustrated in Figure *5* and Figure *6*.

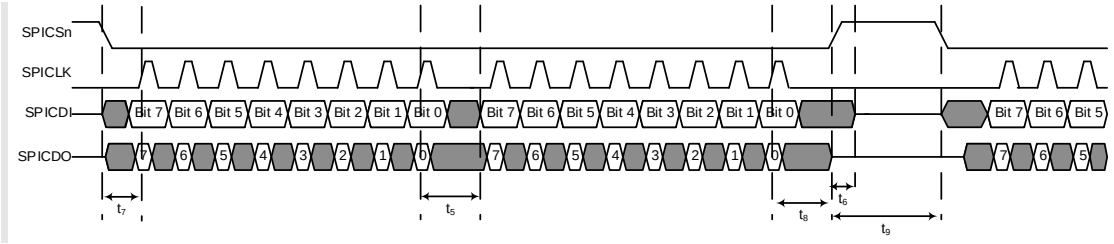


Figure 5: SPI Timing Diagram

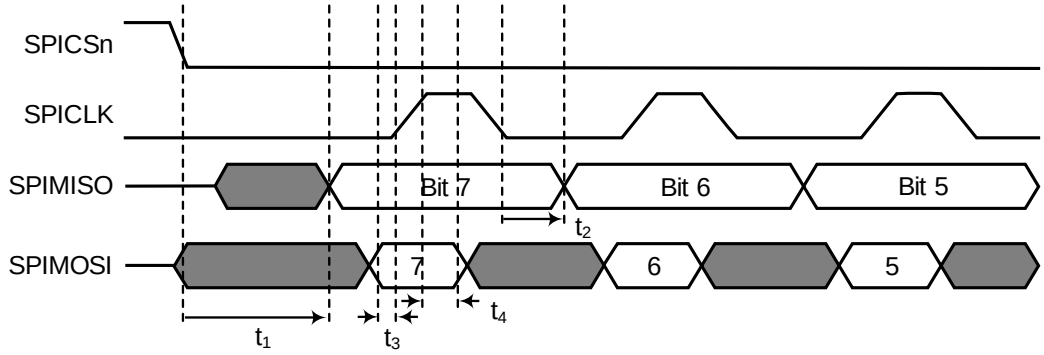


Figure 6: SPI Detailed Timing Diagram

Table 23: SPI Timing Parameters

Parameter	Min.	Max.	Units	Description
t_1		10	ns	SPI select asserted low to valid peripheral output data.
t_2		9.5	ns	SCLK low to valid peripheral output data.
t_3	2.5		ns	Controller data setup time.
t_4	0.7		ns	Controller data hold time.
t_5	31		ns	LSB last byte to MSB next byte. (see maximum SPI frequency).
t_6		10	ns	SPI select deasserted high to CDI tristate.
t_7	10		ns	Start time; time from select asserted to first SCLK.
t_8	42		ns	Idle time between consecutive accesses.
t_9	40		ns	Last SCLK to SEL_n deasserted.
fSPICLK		32	MHz	SPICLK SPI mode 0.

5.11 SPI Operating Modes

Both clock polarities (SPIPOL=0/1) and phases (SPIPHA=0/1) are supported, as defined in the Motorola SPI protocol. The QM33120W transfer protocols for each SPIPOL and SPIPHA setting are given in Figure 7 and Figure 8. Mode 0 is the default mode. The mode can be changed by programming in the OTP memory or writing to the appropriate register, see User Manual.

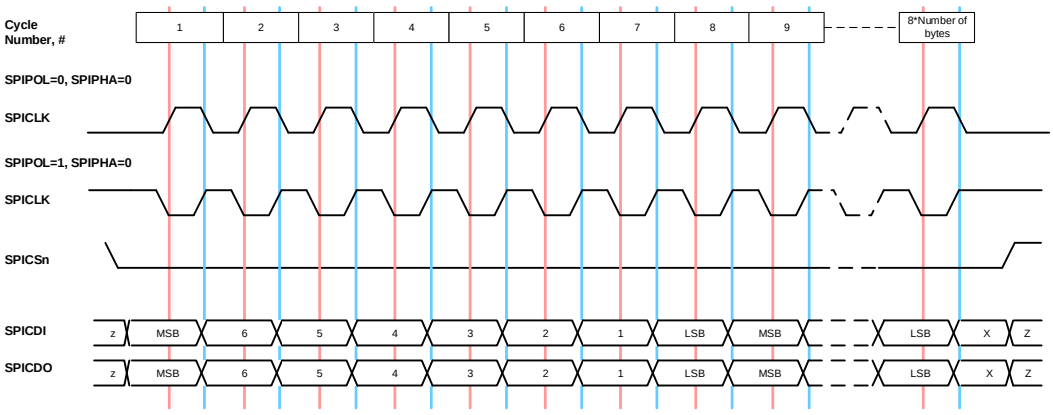


Figure 7: QM33120W SPIPHA=0 Transfer Protocol

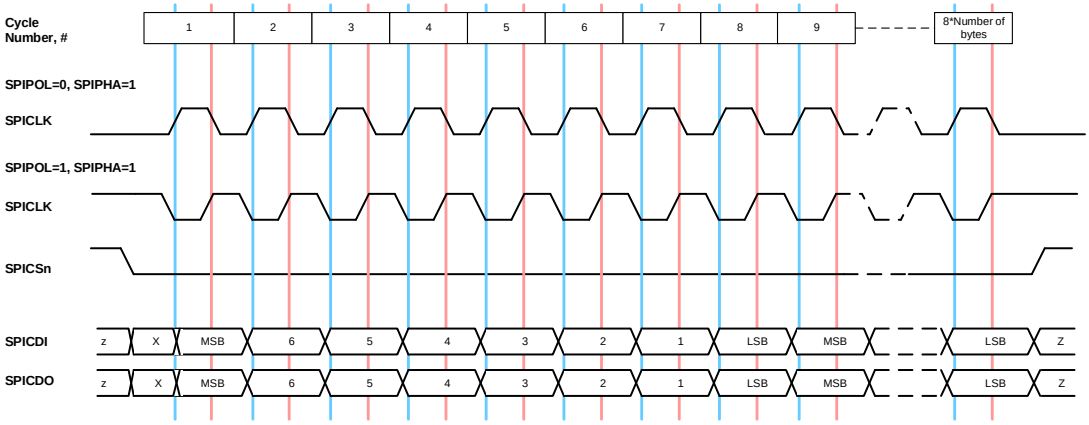


Figure 8: QM33120W SPIPHA=1 Transfer Protocol

5.12 SPI Transaction Formatting

The SPI command structure allows for 4 different types of SPI command:

- Fast, single-byte commands. Up to 32 unique commands such as “TX now”, “TX/RX Off”.
- Fast addressed mode. Allowing for read and write addressing to 32 addresses. This command structure is padded by a trailing bit to allow the SPI address decoder time to fetch any read data. The length of the read is determined by the length of the SPI transaction.
- Full addressed mode. Allowing for read and write addressing to 32 addresses and up to 128-byte offset addressing. This command structure is padded by a trailing bit to allow the SPI address decoder time to fetch any read data. The length of the read or write is determined by the length of the SPI transaction.
- Masked-write transaction. These are intended to simplify read-modify-write operations by allowing the host to write to an address and apply a set, clear, or toggle mask to 1, 2, or 4 bytes. The SPI command decoder then carries out the required read-modify-write instructions internally.

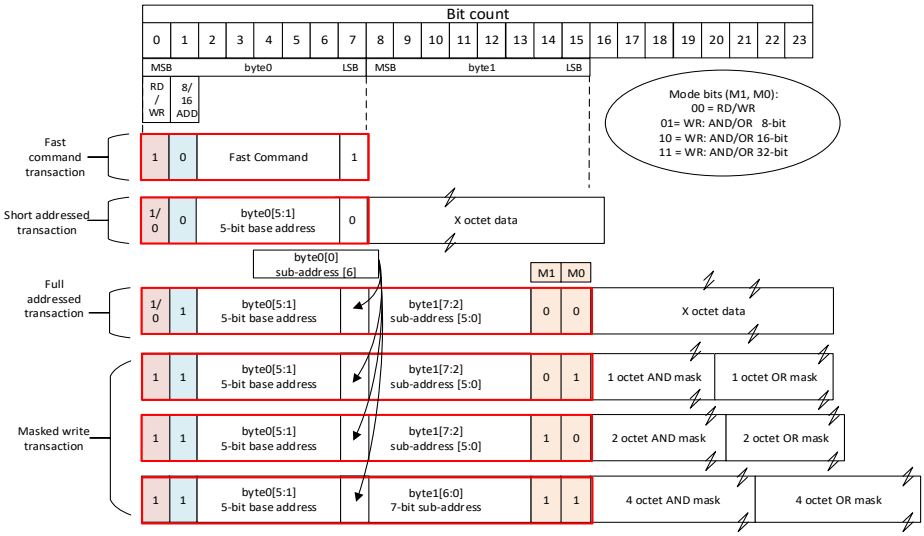


Figure 9: SPI Command Formatting

5.13 GPIO and SPI I/O Internal Pull Up / Down

All the GPIO pins have a software controllable internal pull up/down resistor to ensure safe operation when input pins are not driven. This defaults to enabled and pull-down except for the SPICSn pin which defaults to pull-up. The value of the pull-up/down will vary with the VDD1 supply voltage over a range from 10 kΩ to 30 kΩ.

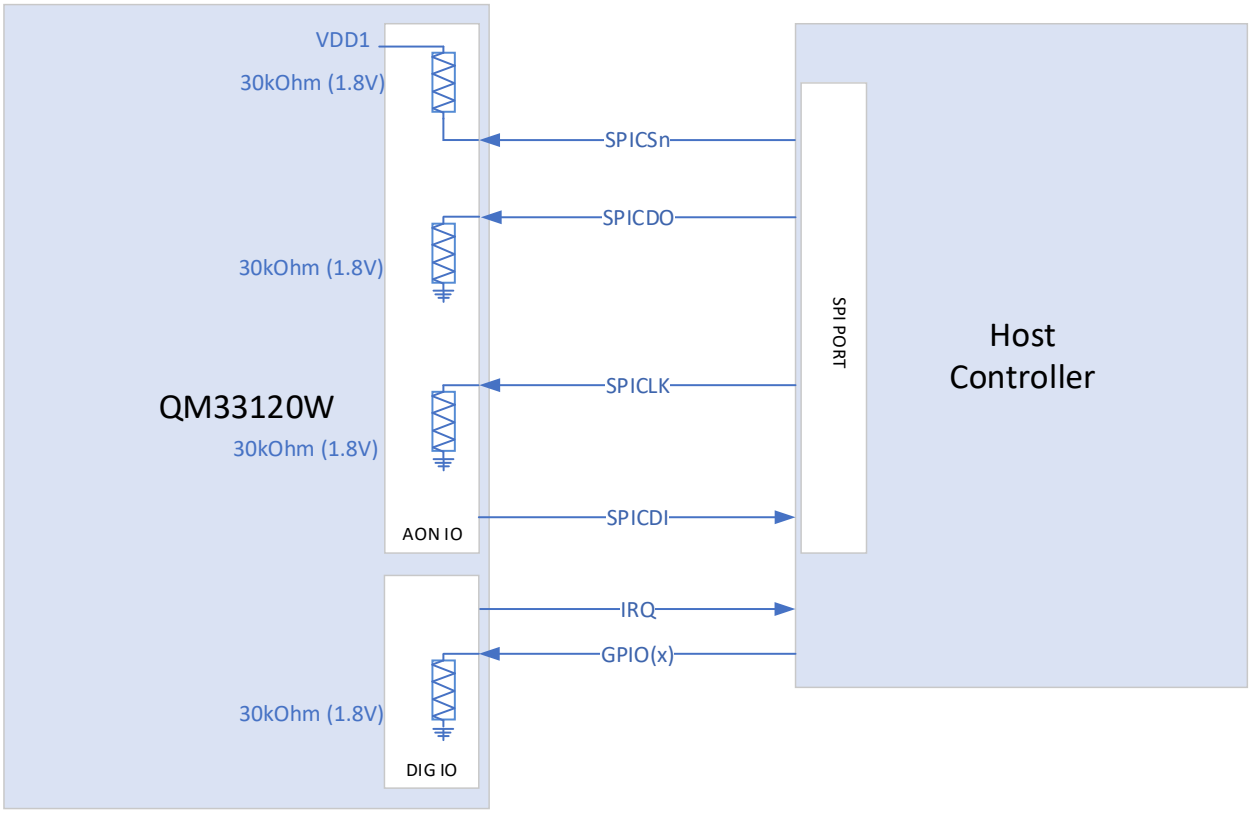


Figure 10: SPI and GPIO Pull Up / Down

5.14 Reference Crystal Oscillator

With the addition of an external 38.4 MHz crystal and appropriate loading capacitors, the on-chip crystal oscillator QM33120W generates the reference frequency for the integrated frequency synthesizer's PLL.
A trim facility is provided which can be used to trim out crystal initial frequency error. Typically, a trimming range of ± 20 ppm is possible using a 6-bit trim value. This trimming in 0.125 pF steps provides for up to 8 pF additional capacitance on the XTI and XTO crystal connections.

5.14.1 Calculation of External Capacitor Values for Frequency Trim

Ideally, the value of external loading capacitors (Cext) should be calculated to give an equal trim range about the center trim value. To do this, one needs to estimate the parasitic capacitance (Cpar) between the crystal pads XTI/XTO and the crystal pads. A good starting estimate for Cext is approximately 3.6 pF. However, some trial and error may be required initially. The values of Cm, Lm, Rm, and Co obtained from the crystal manufacturer are also required.

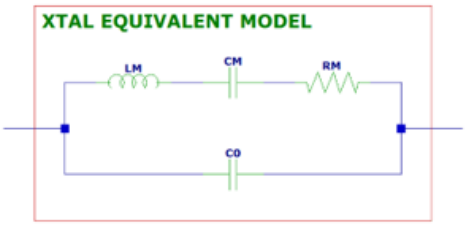


Figure 11: Crystal Model

Using the following formula, the required Cext and trim range can be estimated where:

f_s = series frequency

f_p = parallel frequency

f_L = loaded (desired) frequency

$$f_s = \frac{1}{2\pi\sqrt{C_M L_M}}$$

$$f_p = f_s\left(\sqrt{1+\frac{C_M}{C_0}}\right)$$

$$f_L = f_s\left(\sqrt{1+\frac{C_M}{C_L}}\right)$$

$$C_L = C_0 + \frac{1}{2}(C_{TRIM} + C_{PAR} + C_{EXT})$$

$$\Delta f_{ppm} = 10^6 \times \frac{f_L - f_{L_{nom}}}{f_{L_{nom}}}$$

A typical crystal trimming plot is shown below:

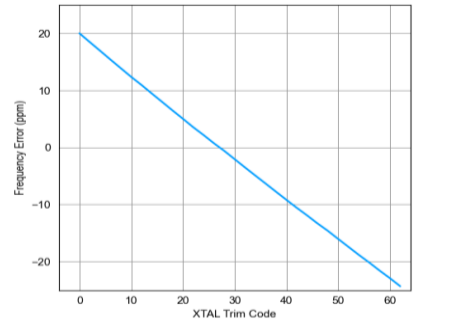


Figure 12: Crystal Trim Plot

6 Operational States

6.1 Overview

The QM33120W has several basic operating states as described in table below.

Table 24: Operating states

State	Description
OFF	The digital core is powered off, digital LDO is disabled. Reset is held low.
INIT_RC	The system is clocked from 30 MHz RC Osc, SPI comms @ 7 MHz. AON download is performed. Automatically goes to IDLE_RC on completion.
IDLE_RC	The system is clocked at ~120 MHz to allow full-speed SPI comms.
IDLE_PLL	The system is clocked from the PLL at 124.8 MHz.
TX_WAIT	TX blocks are sequenced on as required. Includes DELAYED_TX mode.
TX	Active TX state. Automatically reverts to IDLE_PLL after transmission.
RX_WAIT	RX blocks are sequenced on as required. Includes DELAYED RX mode.
RX	Active RX state. Can revert to IDLE_PLL if the packet received or timeout triggers.
SLEEP	Low power state. The sleep counter is clocked from slow RC Osc at ~20 kHz.
DEEPSLEEP	Low power state. All clocks off. Wakeup via IO event on WAKEUP or SPICSn, or by resetting the device (RSTn).

6.2 Operating State Transitions

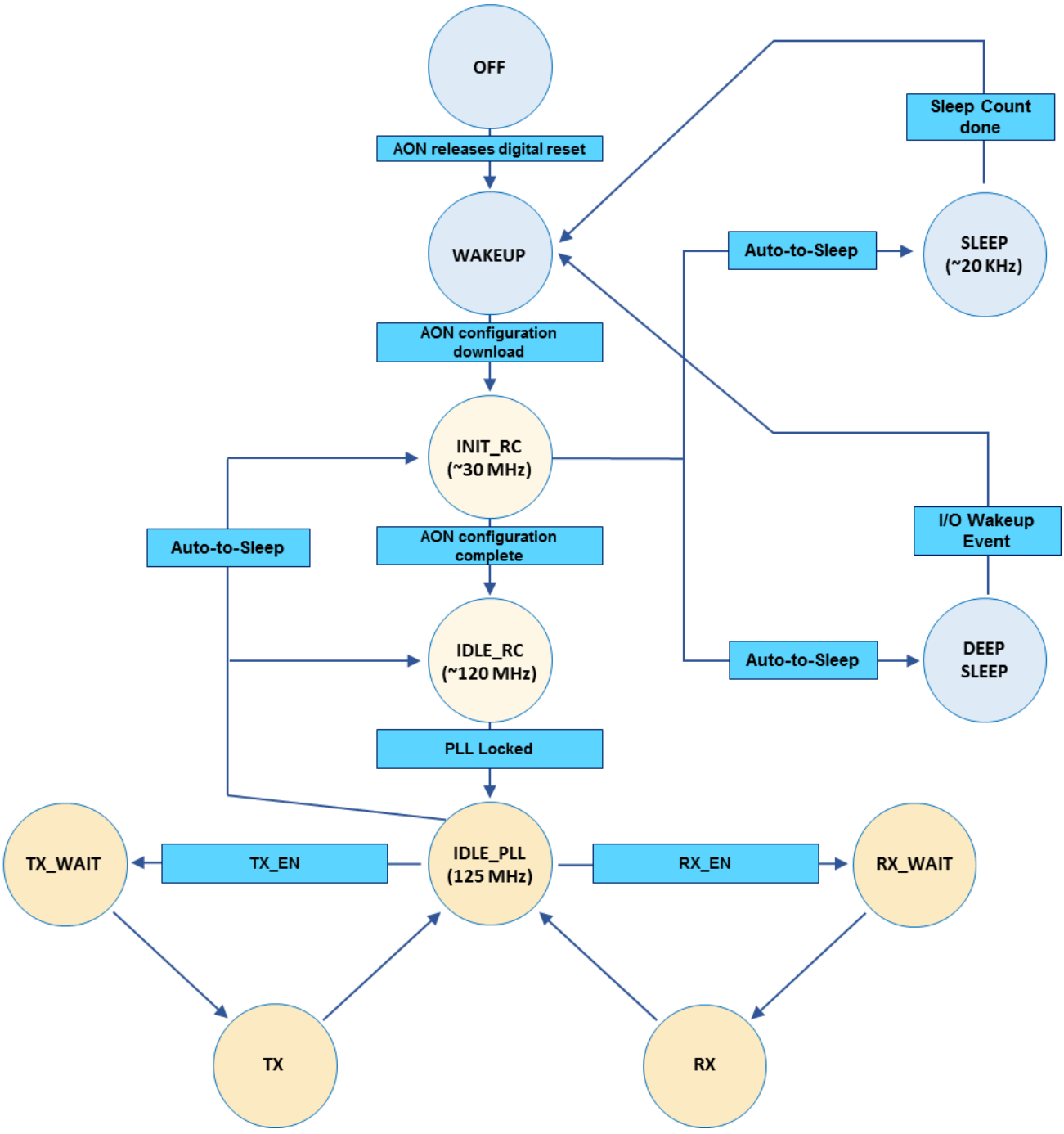


Figure 13: Operating State Transitions

7 Powering QM33120W

QM33120W is designed such that it can be powered in several different configurations depending on the application. These options are described below. Figure 14: Timing Diagram for Cold Start POR shows the power-up sequence when external power sources are applied.

When the external power source is applied to the QM33120W for the first time (cold power-up), the internal Power-On Reset (POR) circuit compares the externally applied supply voltage (VDD1) to an internal power-on threshold (approximately 1.5 V), and once this threshold is passed the AON block is released from reset and the external device enable pin EXTON is asserted.

Then the VDD2a/b and VDD3 supplies are monitored and once they are above the required voltage as specified in the Datasheet (2.2 V and 1.4 V respectively), the fast RC oscillator (FAST_RC) and crystal (XTAL Oscillator) will come on within 500 µs and 1 ms, respectively.

Once the digital reset is de-asserted the digital core wakes up and enters the INIT_RC state, (see **Figure 14** and **Figure 15**). Then, once the configurations stored in AON and OTP have been restored (into the configuration registers), the device will enter IDLE_RC. Then the host can set the AINIT2IDLE configuration bit in SEQ_CTRL and the IC will enable the PLL and wait for it to lock before entering the IDLE_PLL state.

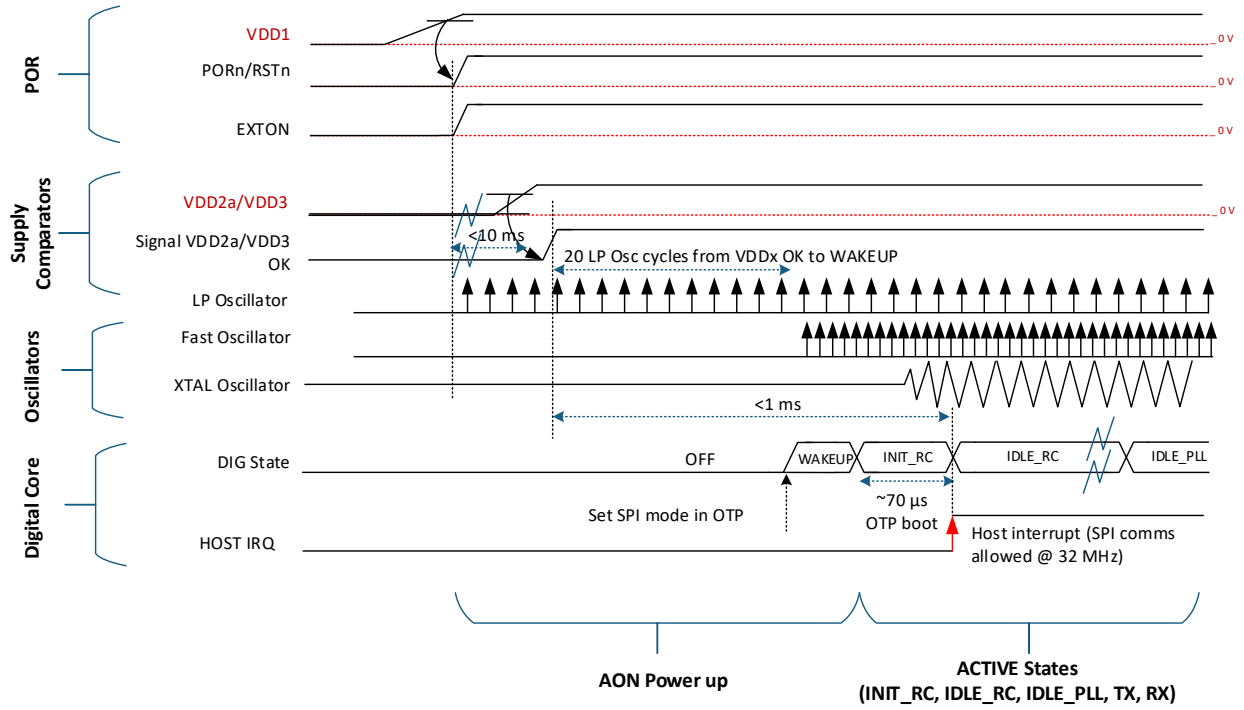


Figure 14: Timing Diagram for Cold Start POR

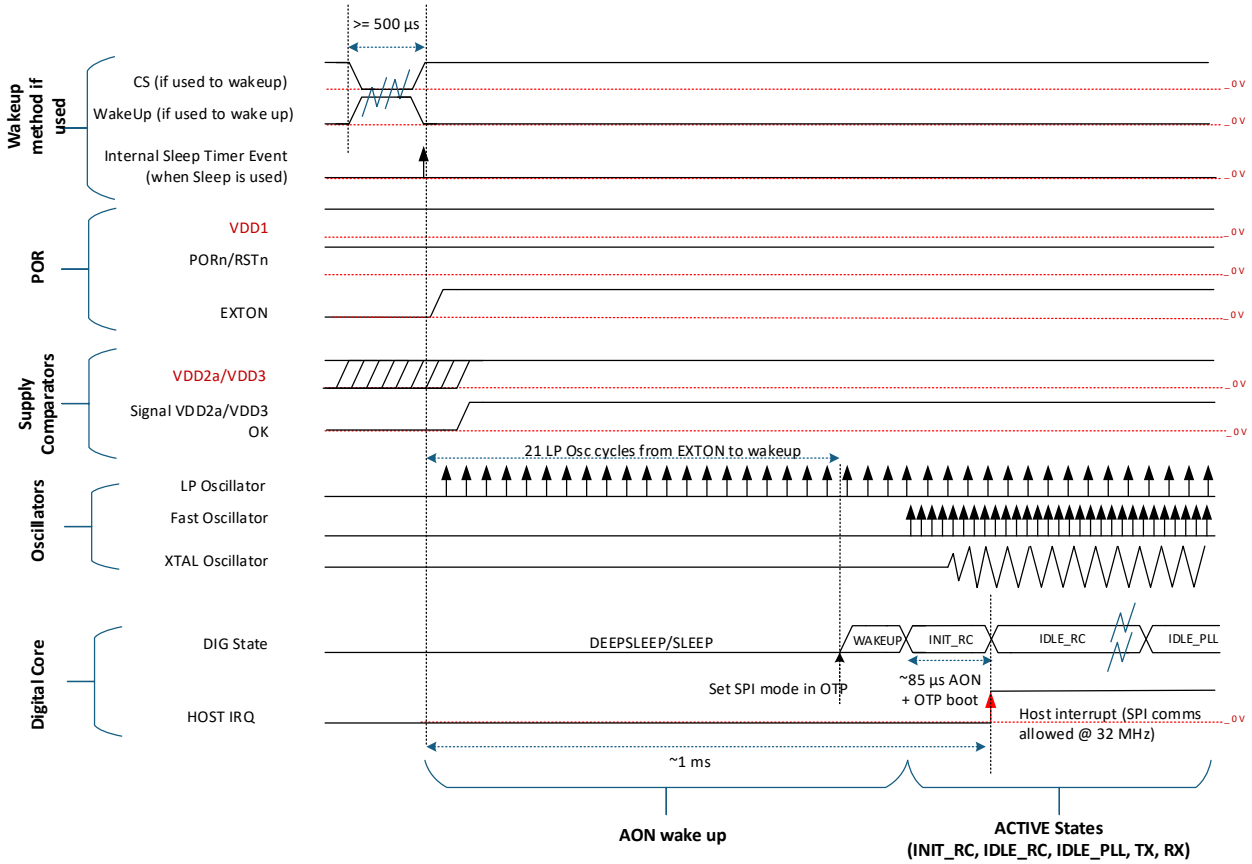


Figure 15: Timing Diagram for Warm Start

7.1 Lowest Bill of Materials (BOM) powering scheme

In the following configuration, the QM33120W is powered directly from a coin-cell battery. This is for applications that require minimal BOM. The bulk capacitor is required to store energy. The value of the capacitor depends on the time the transceiver is in the active Tx/Rx state. Demonstration circuits typically use 47 uF.

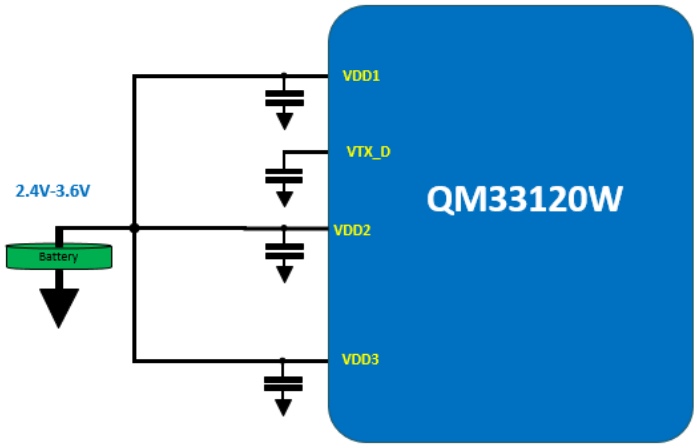


Figure 16: Lowest BOM powering option

7.2 Highest Efficiency powering scheme

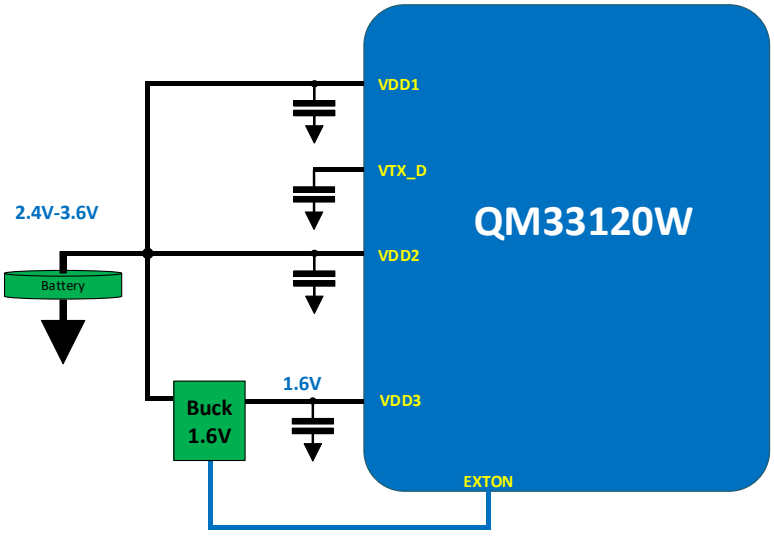


Figure 17: Single O/P Buck SMPS option

7.3 PMIC Powering Scheme

In the following configuration, the external PMIC circuit is used to provide all the power rails to the chip. The VDD1 is used to power Always-On memory and I/O rail only; the current consumption for powering AON is negligible.

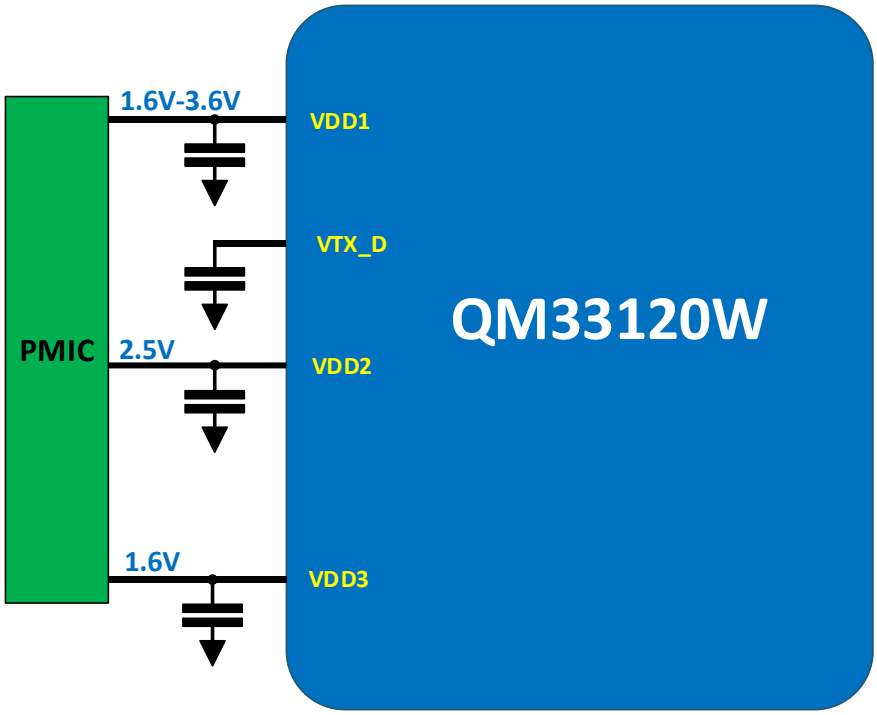


Figure 18: Mobile Option

7.4 Typical Transmit and Receive power profiles

The current drawn during operation with QM33120W will vary depending on supplies used, batteries used, use case, etc. **Figure 19** shows the current drawn from a CR2032 battery with typical TX frames transmitted and the reception of these frames by the receiver.

7.4.1 TX current profile for the minimal BOM

Figure 19 below shows the current profiles during frame transmission without secure preamble and 6.8 Mbps TDoA tag frame. This mode is comparable to a DW1000 TDoA tag blink. All supplies are connected to the battery assumed to be at 3.0 V, i.e., the lowest BOM option, see Lowest Bill of Materials (BOM) Powering Scheme.

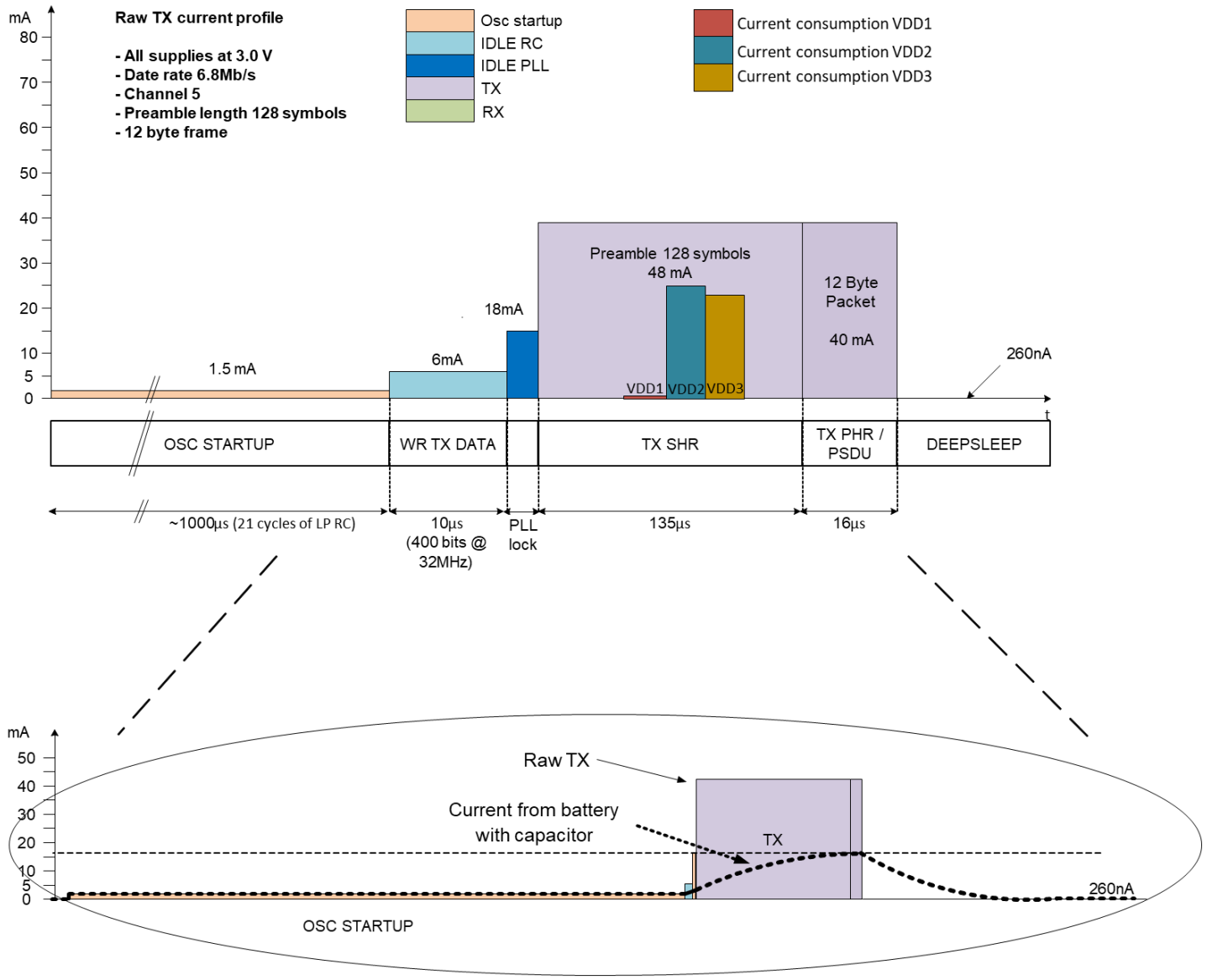


Figure 19: Current Profile when Transmitting a Frame (6.8 Mbps) in Lowest BOM Use Case

7.4.2 TX current profile for high efficiency modes

In the high-efficiency modes, i.e. when an external DC-DC/PMIC is used, the current consumption from VDD3 (1.6V) and VDD2a and VDD2b (2.5V) is different, therefore more efficient current consumption can be achieved using alternative powering schemes, illustrated in section 7.2 and 7.3. The VDD1 is used to power AON memory and I/O rail only; the current consumption for powering AON is negligible.

For high-efficiency schemes, the overall power consumption depends on the efficiency of external DC-DC and/or PMIC. For the QM33120W device, the power consumption during different phases of operation is illustrated in **Figure 20**.

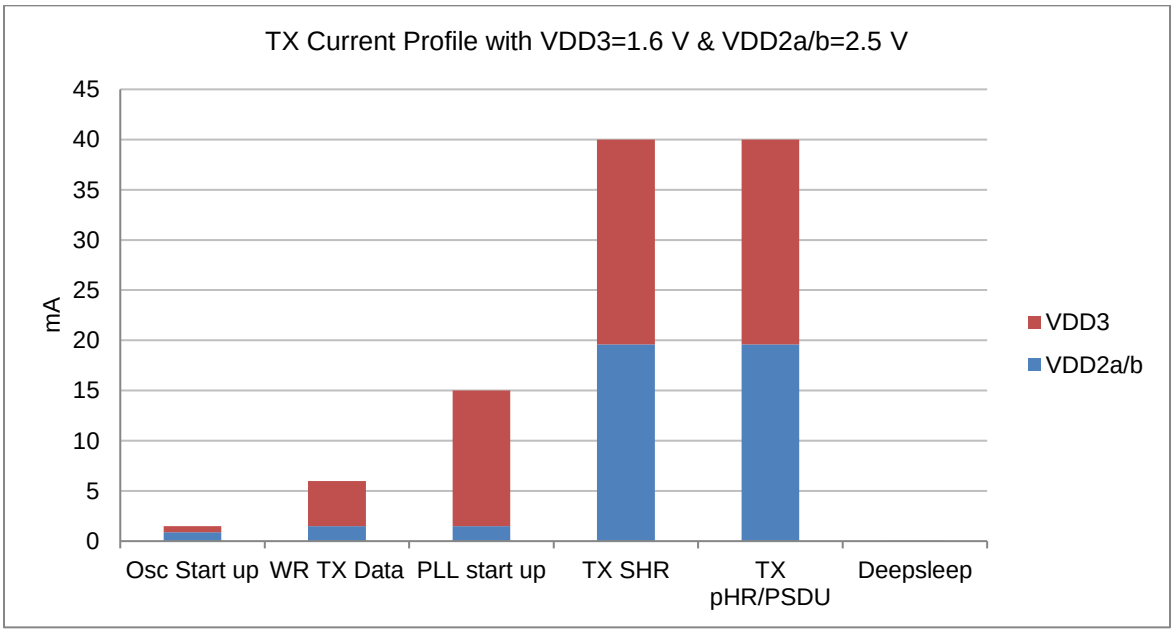


Figure 20: Current Consumption During TX for High Efficiency Powering Modes

7.4.3 RX current profile for minimal BOM

Figure 21 below illustrates the current profiles during the reception of a typical frame. All supplies are connected to the battery assumed to be at 3.0 V, i.e., the lowest BOM option, see Figure 16.

The variable part of Preamble Hunt is 30us for Responder and 0 (zero) when using Delayed RX in Two Way Ranging (TWR) protocol.

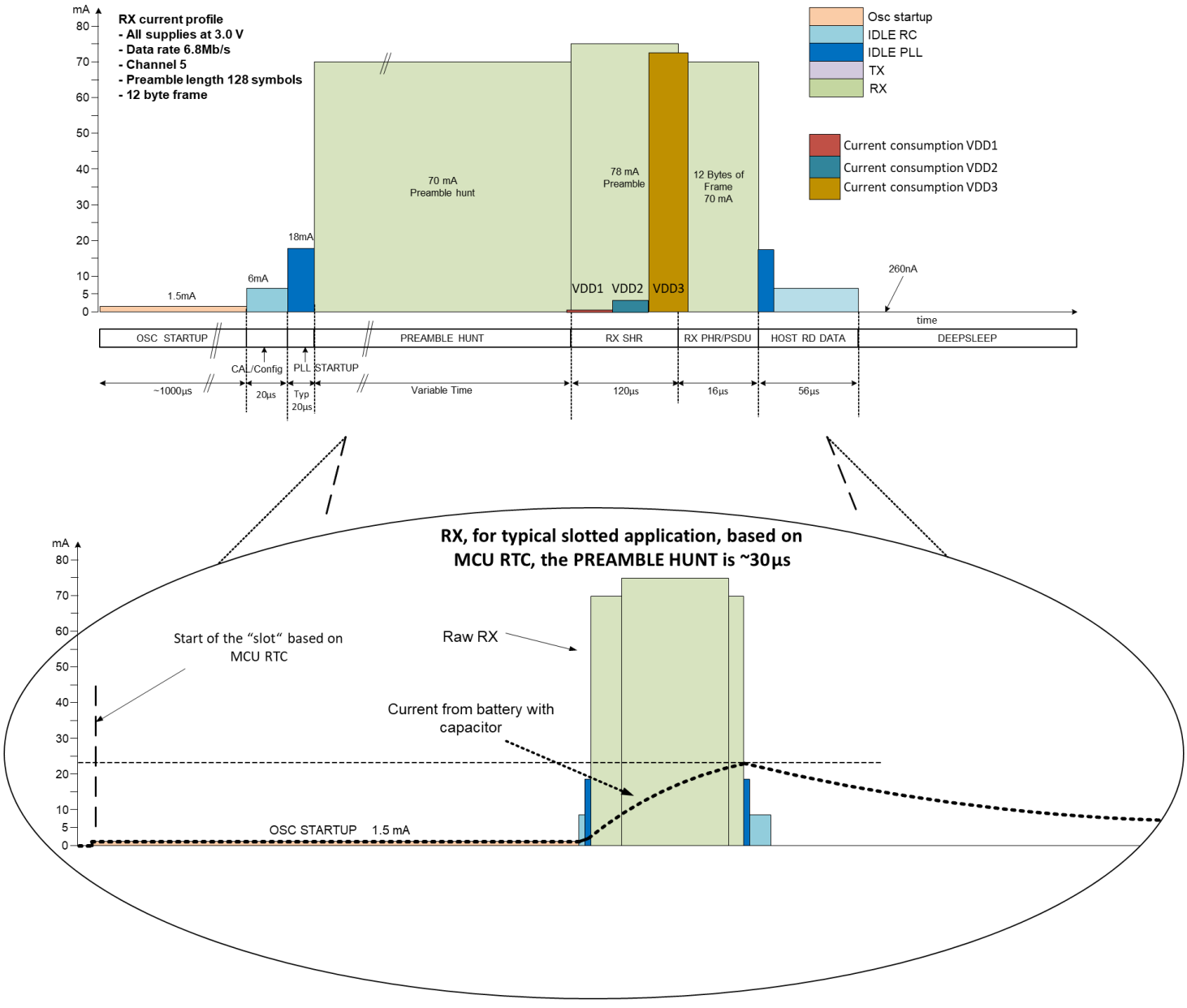


Figure 21: Typical current profiles when receiving a frame for different types of applications

7.4.4 RX Current Profile for High Efficiency BOMs

In the high-efficiency modes, i.e., when an external DC-DC/PMIC is used, the current consumption from VDD2 (2.5V) and VDD3 (1.6V) are different, therefore more efficient current consumption can be achieved using alternative powering schemes, illustrated in section 7.2 and 7.3. The VDD1 is used to power AON memory and IO only, the current consumption for powering AON is negligible.

For high-efficiency schemes, the overall power consumption depends on the efficiency of external the DC-DC and/or PMIC. For the QM33120W device, the power consumption during different phases of operation is illustrated below.

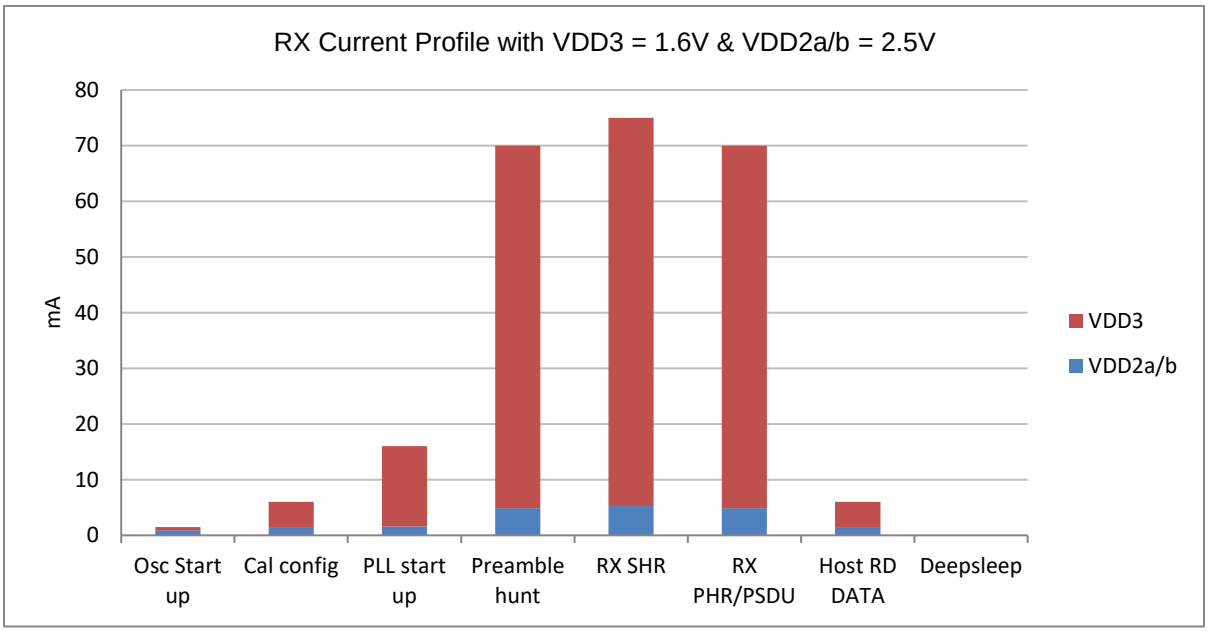


Figure 22: Current Consumption During RX for High Efficiency Powering Modes

7.5 Internal Power Supply Distribution

The block diagram shows the power distribution within the QM33120W device.

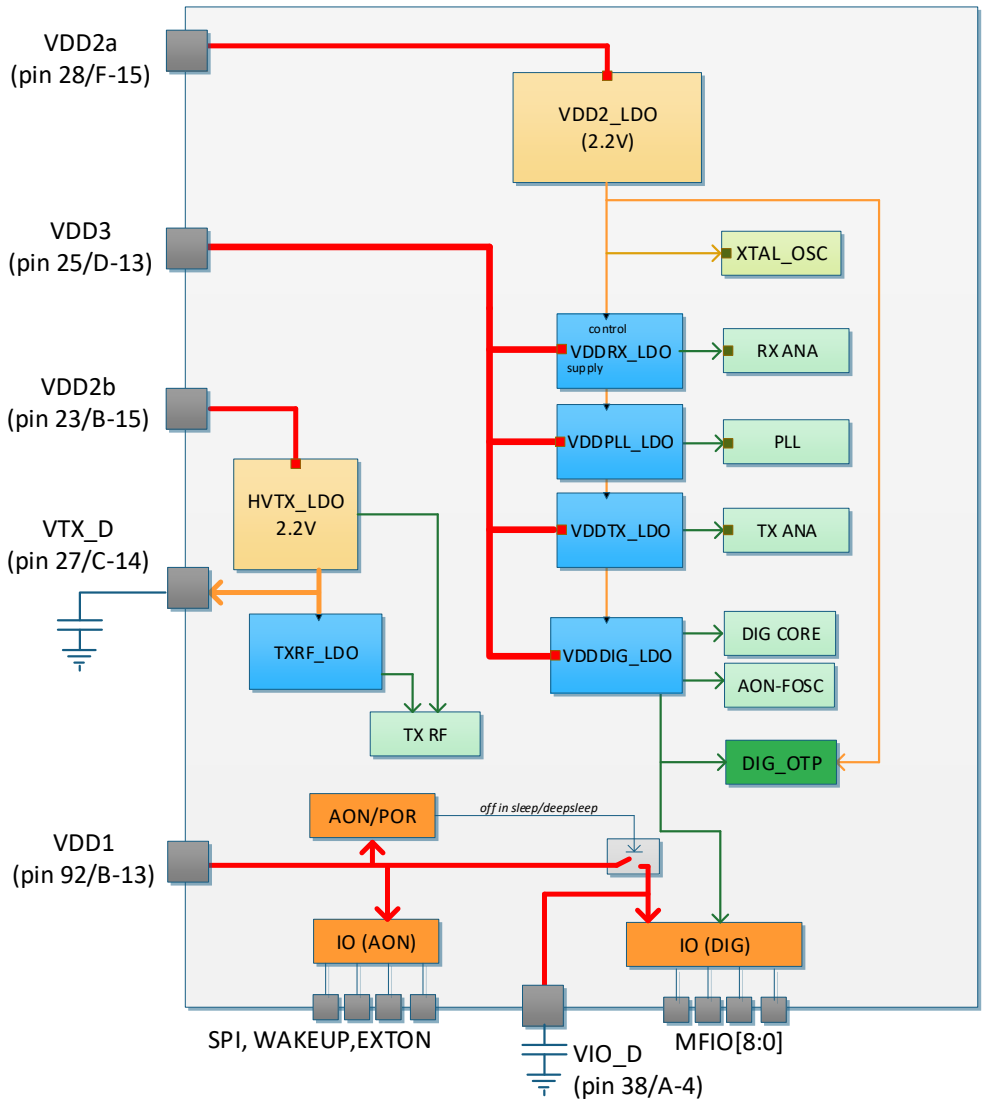


Figure 23: Internal Power Distribution

8 Application Information

8.1 Application Circuit Diagram

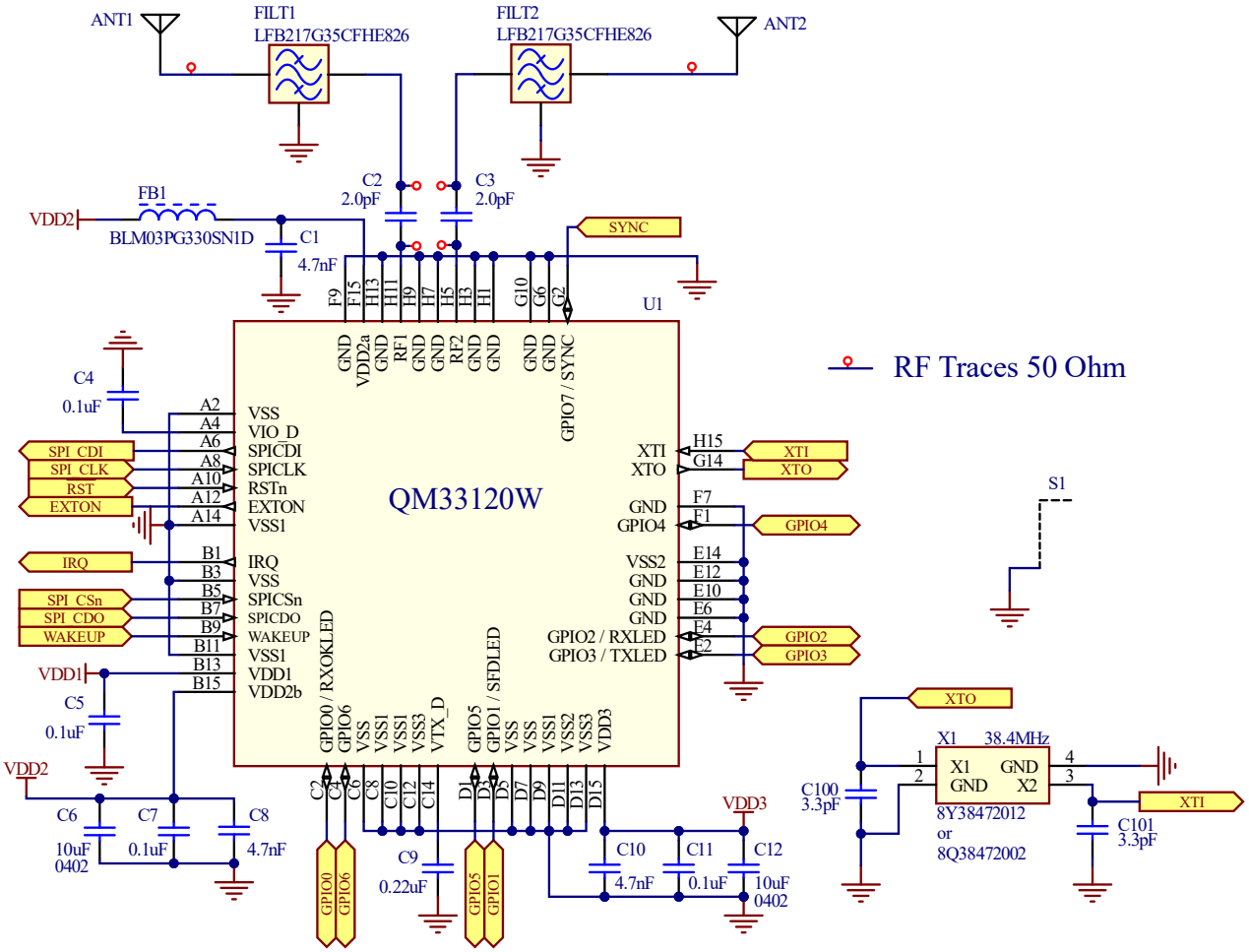


Figure 24: QM33120W Application Circuit

Note: When a PDoA variant (QM33120W) is used as a non-PDoA variant (QM33110W), RF2 should have a 2pF series capacitor and 50 Ohm resistor to ground.

8.2 Recommended Components

The list of components tested and approved by Qorvo is shown in the table below. The use of DC-DC regulators and TCXO's is optional.

Table 25: QM33120W Recommended Components

Function	Manufacturer	Part Number	Web Link
Antenna	Partron	ACS5200HFAUWB	www.partron.co.kr
	Taiyo Yuden	AH086M555003	www.yuden.co.jp
Crystal (38.4 MHz+/-10 ppm)	TXC	8Y38472012	www.txccorp.com
	Rakon	RSX-10	www.rakon.com
DC-DC	TI	TPS62743	www.ti.com
TCXO	TXC	7Z38470005	www.txccorp.com
	Rakon	IT2200K	www.rakon.com

8.3 Recommended PCB Layout and Stackup

Some recommendations for the chip layout are as follows:

- Keep all the traces as short as possible.
- Avoid mixing Analog (RF1, RF2, XIN, XOUT), Power (VDD1, VDD2a/b, VDD3, VDD decoupling), and Digital (SPI, etc) groups together.
- Place all the decoupling capacitors as close to the corresponding chip pads as possible, the smaller capacitor should be closer to the pad. Connect the ground pad of each capacitor to the good ground plane directly to minimize ESR and ESL of the return current path.
- RF1 and RF2 lines should be 50 Ohm impedance-controlled lines. Embed the DC-blocking 2pF capacitor pads into the track or add teardrops to remove any possible discontinuities.
- The ground copper should be removed from under the chip in the areas shown in the picture (Top layer and Inner Layer 1). The first solid ground copper should be on the Inner Layer 2. If a different stack-up will be used – this first solid copper layer should be at least 0.25mm away from the Top Layer, any inner layers close to the Top Layer should have the ground removed in the same manner as in Inner Layer 1 above.

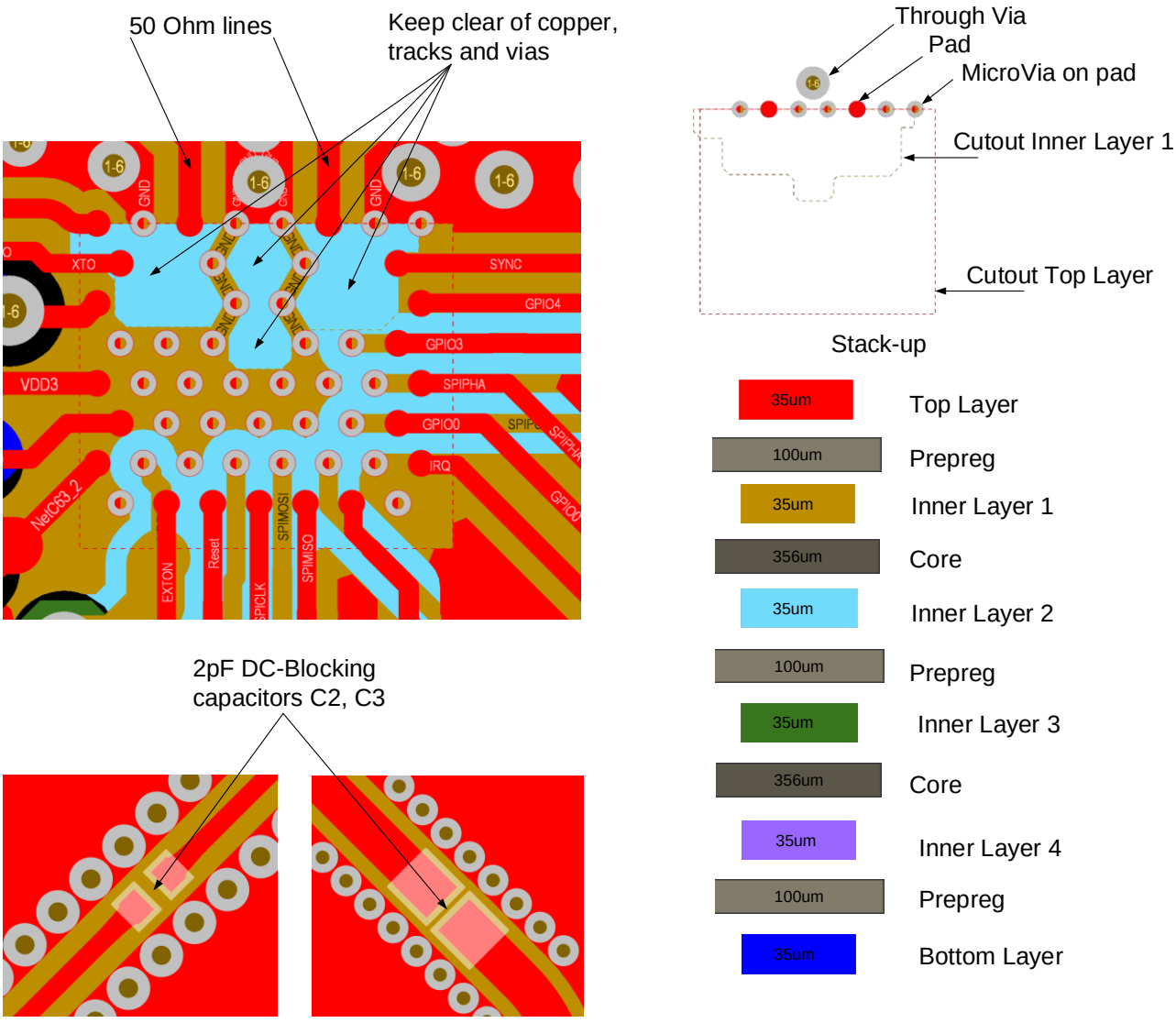
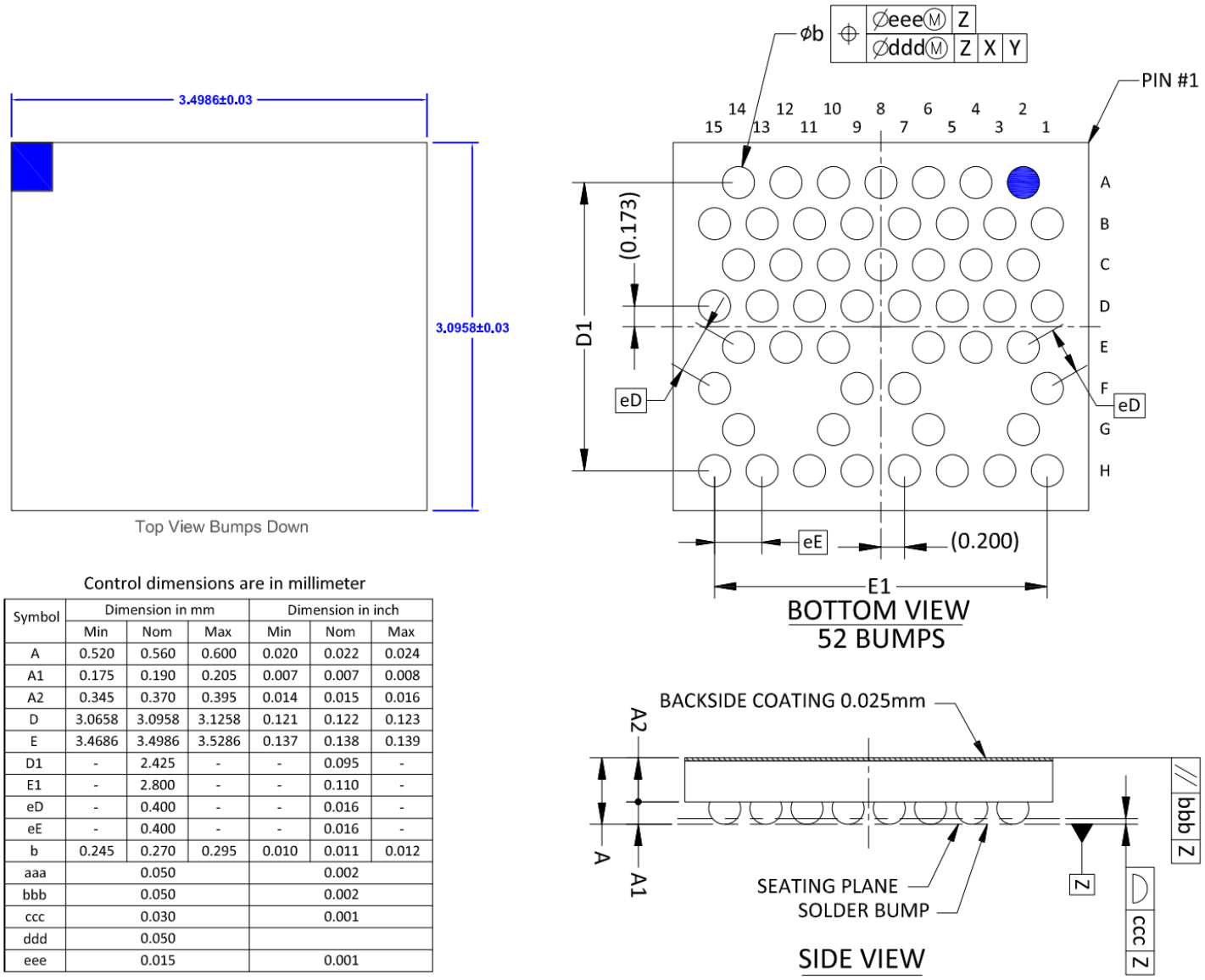


Figure 25: Recommended PCB Layout and Stackup

9 Packaging & Ordering Information

9.1 52-Ball WLCSP

9.1.1 Package Dimensions



Control dimensions are in millimeter

Symbol	Dimension in mm			Dimension in inch		
	Min	Nom	Max	Min	Nom	Max
A	0.520	0.560	0.600	0.020	0.022	0.024
A1	0.175	0.190	0.205	0.007	0.007	0.008
A2	0.345	0.370	0.395	0.014	0.015	0.016
D	3.0658	3.0958	3.1258	0.121	0.122	0.123
E	3.4686	3.4986	3.5286	0.137	0.138	0.139
D1	-	2.425	-	-	0.095	-
E1	-	2.800	-	-	0.110	-
eD	-	0.400	-	-	0.016	-
eE	-	0.400	-	-	0.016	-
b	0.245	0.270	0.295	0.010	0.011	0.012
aaa		0.050			0.002	
bbb		0.050			0.002	
ccc		0.030			0.001	
ddd		0.050				
eee		0.015			0.001	

Figure 26: QM33120W Package Dimensions

9.1.2 Recommended PCB Footprint

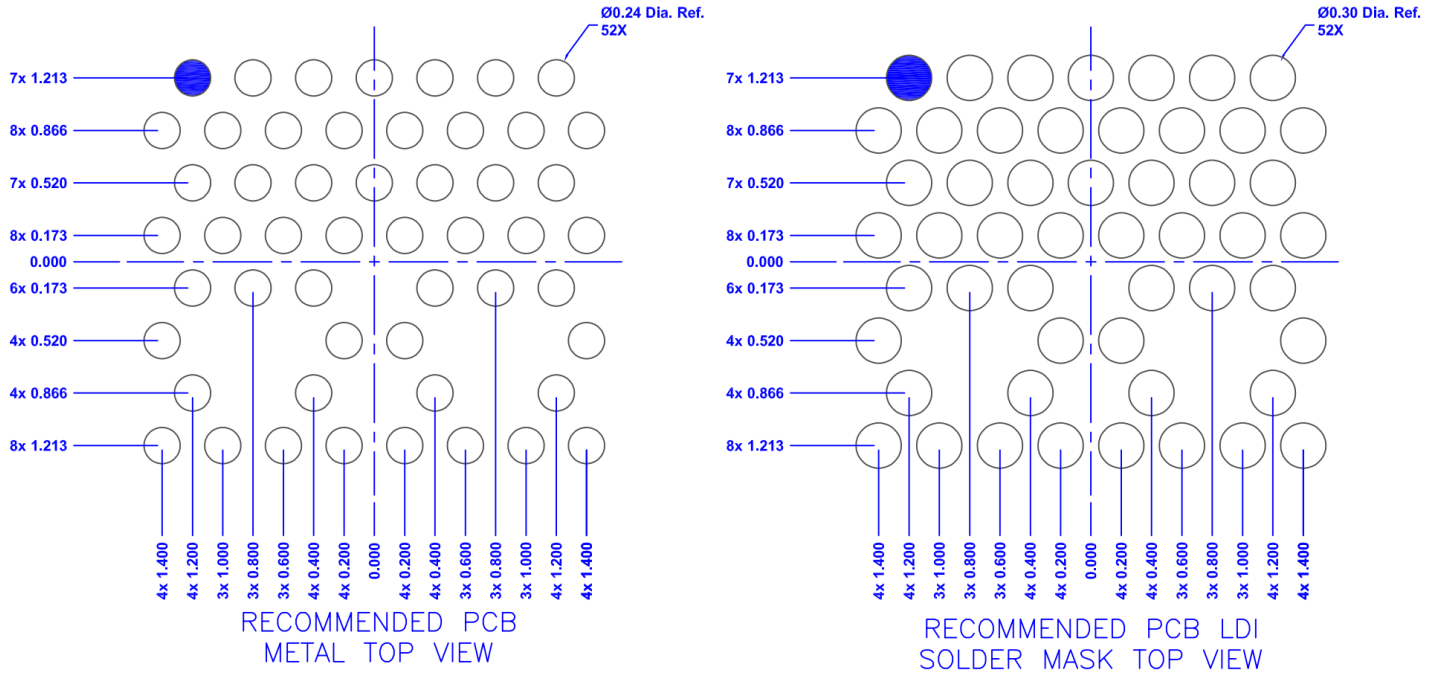


Figure 27: Recommended PCB Footprint

9.1.3 Tape and Reel Packaging Information

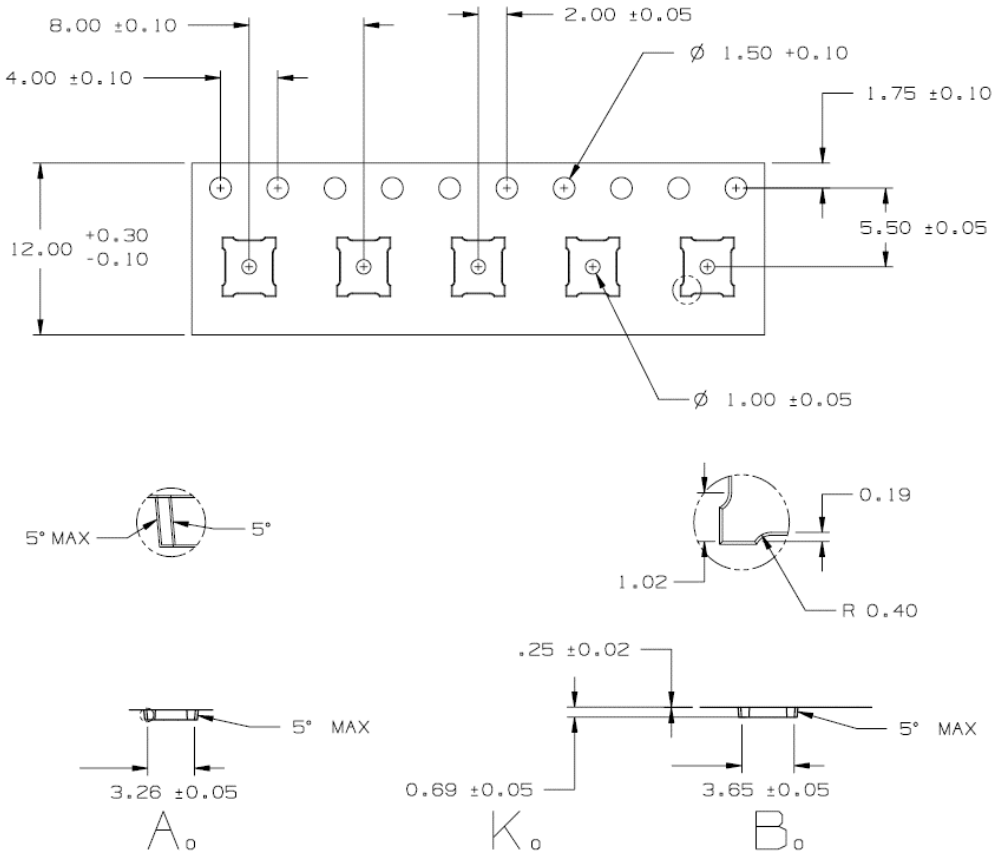
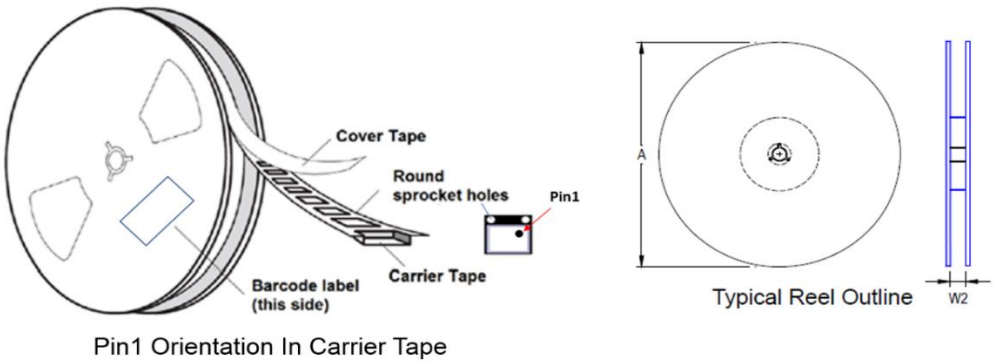


Figure 28: Tape orientation and dimensions



Package Size (mm)	Tape Size (mm)	Pocket Pitch (mm)	Reel Size(A) (mm)	Reel Width(W2) Min. / Max. (mm)	Units per Reel	Pre / Post empty pocket
3.1 x 3.5	12	8	330 (13”)	12.4 / 13.4	3000	200 / 200

Figure 29: Reel Information – 330 mm Reel (13”)

9.1.4 Device Package Marking

The diagram below shows the package markings for QM33120W.

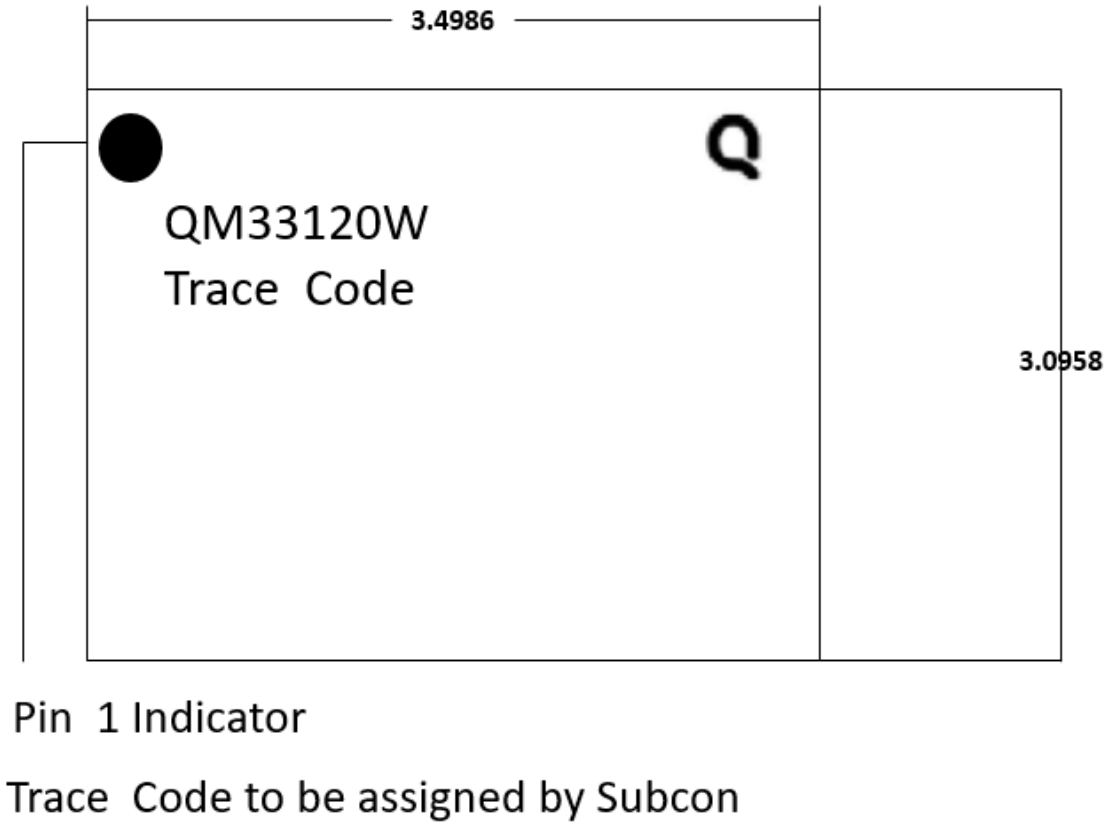


Figure 30: Device Package Marking

10 Glossary

Table 26: Glossary of Terms

Abbreviation	Full Title	Explanation
BPRF	Base PRF mode	64 MHz PRF Mode
CDI	Controller Data input	SPI interface I/O
CDO	Controller Data output	SPI interface I/O
EIRP	Equivalent Isotropically Radiated Power	The amount of power that a theoretical isotropic antenna (which evenly distributes power in all directions) would emit to produce the peak power density observed in the direction of maximum gain of the antenna being used.
GPIO	General Purpose Input / Output	Pin of an IC that can be configured as an input or output under software control and has no specifically identified function.
IEEE	Institute of Electrical and Electronics Engineers	Is the world's largest technical professional society. It is designed to serve professionals involved in all aspects of the electrical, electronic, and computing fields and related areas of science and technology.
LOS	Line of Sight	Physical radio channel configuration in which there is a direct line of sight between the transmitter and the receiver.
NLOS	Non-Line of Sight	Physical radio channel configuration in which there is no direct line of sight between the transmitter and the receiver.
Open Drain	Open Drain	A technique allowing a signal to be driven by more than one device. Generally, each device is permitted to pull the signal to the ground but when not doing so it must allow the signal to float. Devices should not drive the signal high to prevent contention with devices attempting to pull it low.
PDoA	Phase Difference of Arrival	Method of determining the direction of propagation of a radio-frequency wave incident on an antenna array using the phase difference between the signal received on each antenna array element.
PLL	Phase Locked Loop	Circuit designed to generate a signal at a particular frequency whose phase is related to an incoming "reference" signal.
PPM	Parts Per Million	Used to quantify very small relative proportions. Just as 1% is one out of a hundred, 1 ppm is one part in a million.
RF	Radio Frequency	Generally used to refer to signals in the range of 3 kHz to 300 GHz. In the context of a radio receiver, the term is generally used to refer to circuits in a receiver before down-conversion takes place and in a transmitter after up-conversion takes place.
RTLS	Real Time Location System	System intended to provide information on the location of various items in real-time.
SFD	Start of Frame Delimiter	Defined in the context of the IEEE 802.15.4 standard.
SPI	Serial Peripheral Interface	An industry standard method for interfacing between IC's using a synchronous serial scheme first introduced by Motorola.
TDoA	Time Difference of Arrival	Method of deriving information on the location of a transmitter. The time of arrival of a transmission at two physically different locations whose clocks are synchronized is noted and the difference in the arrival times provides information on the location of the transmitter. A number of such TDoA measurements at different locations can be used to uniquely determine the position of the transmitter. Refer to Qorvo's website for further information.
TWR	Two Way Ranging	Method of measuring the physical distance between two radio units by exchanging messages between the units and noting the times of transmission and reception. Refer to Qorvo's website for further information.

11 References

[1] IEEE Std. 802.15.4-2011 or “IEEE Std. 802.15.4™-2011” (Revision of IEEE Std. 802.15.4-2006). IEEE Standard for Local and metropolitan area networks – Part 15.4: Low-Rate Wireless Personal Area Networks (LR-WPANs). IEEE Computer Society Sponsored by the LAN/MAN Standards Committee. Available from http://standards.ieee.org/

[2] IEEE Std. 802.15.4-2015 or “IEEE Std. 802.15.4™-2015” (Revision of IEEE Std. 802.15.4-2011). IEEE Standard for Local and metropolitan area networks – Part 15.4: Low-Rate Wireless Personal Area Networks (LR-WPANs). IEEE Computer Society Sponsored by the LAN/MAN Standards Committee. Available from http://standards.ieee.org/

[3] IEEE Std. 802.15.4™-2020 (Revision of IEEE Std. 802.15.4-2015) “IEEE Standard for Low-Rate Wireless Networks”. IEEE Computer Society Sponsored by the LAN/MAN Standards Committee. Available from http://standards.ieee.org/

[4] IEEE Std. 802.15.4z™-2020 (Amendment to IEEE Std. 802.15.4™-2020) “Amendment 1: Enhanced Ultra-Wideband (UWB) Physical Layers (PHYs) and Associated Ranging Techniques”. IEEE Computer Society Sponsored by the LAN/MAN Standards Committee. Available from http://standards.ieee.org/

12 Revision History

Table 27: Document History

Revision	Date	Description
C	June 2022	- Figure 6, Correction to SPI diagram to illustrate timings more accurately.
B	April 2022	Datasheet updated to reflect latest characterization results and editorial changes. - Receiver sensitivity and Link budget values were added for the data rate 850 Kbps. - Table 10, Crystal Load capacitance value is updated. - PDoA switch losses are updated. - Table 14, suggestions are added to satisfy the best PDoA performance. - Figure 24, update application circuit diagram. - Table 23, update SPI timings t_1 and t_5. - Figure 27, update recommended PCB layout and Stackup.
A	November 2021	Initial release.

13 Handling Precautions

PARAMETER	RATING	STANDARD
ESD – Human Body Model (HBM)	Class 2 (2000 V)	ESDA/JEDEC JS-001
ESD – Charged Device Model (CDM)	Class C2a (500V)	ESDA/JEDEC JS-002
MSL – Moisture Sensitivity Level	MSL 1	IPC/JEDEC J-STD-020

Caution!

ESD sensitive device

14 Solderability

The QM33120W should be soldered using the reflow profile specified below.

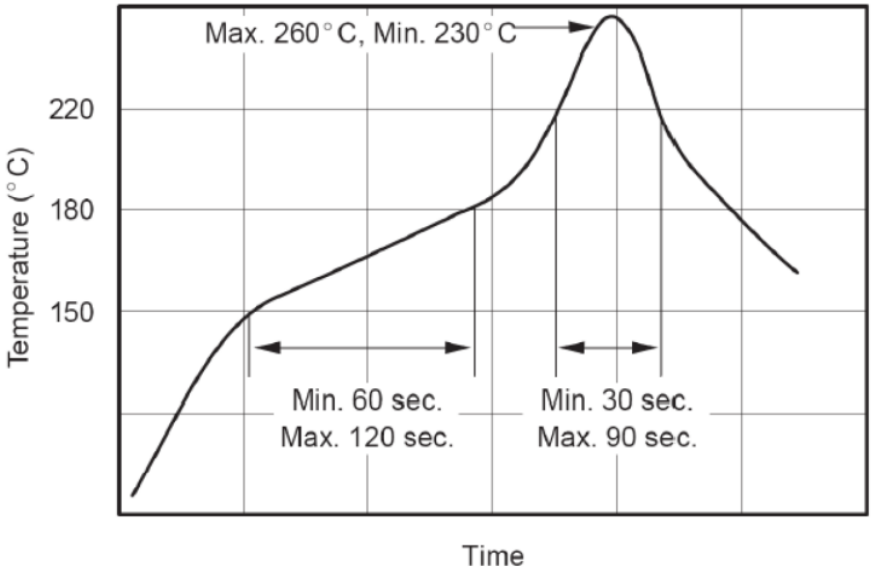


Figure 31: Reflow Profile of the WLCSP package

Table 28: Critical Parameters for Lead Free Solder of the WLCSP package

Process Step	Lead Free Solder
Ramp Rate	3˚C/sec
Pre-Heat	150˚C to 180˚C, 60 to 180 seconds
Time above Liquidius, 220˚C	30 to 90 seconds
Peak Temperature	255˚C +/- 5˚C
Time within 5˚C of Peak Temperature	10 to 20 seconds
Ramp Down Rate	6˚C/sec Max, 0.8˚C/sec to 0.4˚C recommended

15 Further Information

Qorvo develops semiconductors solutions, software, modules, reference designs - that enable real-time, ultra-accurate, ultra-reliable local area micro-location services. Qorvo's technology enables an entirely new class of easy to implement, highly secure, intelligent location functionality and services for IoT and smart consumer products and applications.

For further information on this or any other Qorvo product, please refer to app note on Qorvo website.

RoHS Compliance

This part is compliant with 2011/65/EU RoHS directive (Restrictions on the Use of Certain Hazardous Substances in Electrical and Electronic Equipment) as amended by Directive 2015/863/EU.

This product also has the following attributes:

- Lead Free
- Antimony Free
- TBBP-A ($C_{15}H_{12}Br_40_2$) Free
- SVHC Free

Regulatory Approvals

The QM33120W, as supplied from Qorvo, has not been certified for use in any particular geographic region by the appropriate regulatory body governing radio emissions in that region although it is capable of such certification depending on the region and the manner in which it is used.

All products developed by the user incorporating the QM33120W must be approved by the relevant authority governing radio emissions in any given jurisdiction prior to the marketing or sale of such products in that jurisdiction and user bears all responsibility for obtaining such approval as needed from the appropriate authorities.

Product Status

Marking	Product Status	Definition
ADVANCE INFO	Formative / In Design	Datasheet contains design specifications for product development. Specifications may change in any manner without notice.
PRELIMINARY	First Production	Datasheet contains preliminary data; supplementary data will be published later. Qorvo reserves the right to make changes at any time without notice to improve the design.
(none)	Full Production	Datasheet contains final specifications. Qorvo reserves the right to make changes at any time without notice to improve the design.
OBSOLETE	Not in Production	Datasheet contains specifications on a product that is discontinued. The datasheet is for reference information only.

Contact Information

For the latest specifications, additional product information, worldwide sales and distribution locations:

Web: www.qorvo.com

Tel: 1-844-890-8163

Email: customer.support@qorvo.com

Important Notice

The information contained in this Data Sheet and any associated documents ("Data Sheet Information") is believed to be reliable; however, Qorvo makes no warranties regarding the Data Sheet Information and assumes no responsibility or liability whatsoever for the use of said information. All Data Sheet Information is subject to change without notice. Customers should obtain and verify the latest relevant Data Sheet Information before placing orders for Qorvo® products. Data Sheet Information or the use thereof does not grant, explicitly, implicitly or otherwise any rights or licenses to any third party with respect to patents or any other intellectual property whether with regard to such Data Sheet Information itself or anything described by such information.

DATA SHEET INFORMATION DOES NOT CONSTITUTE A WARRANTY WITH RESPECT TO THE PRODUCTS DESCRIBED HEREIN, AND QORVO HEREBY DISCLAIMS ANY AND ALL WARRANTIES WITH RESPECT TO SUCH PRODUCTS WHETHER EXPRESS OR IMPLIED BY LAW, COURSE OF DEALING, COURSE OF PERFORMANCE, USAGE OF TRADE OR OTHERWISE, INCLUDING THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE. Without limiting the generality of the foregoing, Qorvo® products are not warranted or authorized for use as critical components in medical, life-saving, or life-sustaining applications, or other applications where a failure would reasonably be expected to cause severe personal injury or death. Applications described in the Data Sheet Information are for illustrative purposes only. Customers are responsible for validating that a particular product described in the Data Sheet Information is suitable for use in a particular application.