APPLICATION NOTE AN136

ACT86600 Register Definition

Abstract

This application note identifies the ACT86600 internal registers that help make this IC flexible and configurable for many applications. This is the initial released version therefore some registers might be changed in the future.

Introduction

The ACT86600 PMIC is an integrated ActivePMU™ power management unit. It is highly flexible and can be reconfigured via I2C for multiple applications without the need for PCB changes. The low external component count and high configurability significantly speeds time to market. The core of the device includes 4 high power DC/DC step down converters, a lower power step down converter and a buck-boost converter. Each regulator can be configured for a wide range of output voltages through the I2C interface.

The ACT86600 is a high voltage PMIC that is optimized for single stage voltage conversion from 12V input power sources. It operates with a 2.7V to 14.4V input voltage and can withstand 16V input voltage surges. The four high current regulators can be configured as single-phase outputs or can be paralleled for up to 12A dual phase with outputs.

Register Types

The ACT86600 ICs contain the following register types.

Basic Volatile - Customer R/W (Read and Write) and RO (Read only). The customer can modify these register values to change IC functionality. Any changes to these registers are lost when power is recycled. The default values are fixed and cannot be changed.

Basic Non-Volatile - Customer R/W and RO. The customer can modify these register values to change IC functionality. Any changes to these registers are lost when power is recycled. The default values can be modified at the factory to optimize IC functionality for specific applications. Please consult Sales@Qorvo.com for custom options and minimum order quantities.

The ACT86600 contains eight major register spaces.

MASTER	0x00h to 0x1Ah
BUCK1	0x40h to 0x4Ch
BUCK2	0x60h to 0x6Ch
BUCK3	0x80h to 0x8Ch
BUCK4	0xA0h to 0xACh
BUCK_BOOST	0xC0h to 0xCAh

Register Map Overview

The following table shows an overview of the ACT86600 register map.

ADDR (HEX)	7	6	5	4	3	2	1	0
MASTER								
00	WD TIMER Expired	WD TIMER ALERT	TWARN	AVIN_STAT	WD PC STAT	WD SR STAT	miniBK_OV_FLT	RFU
01	WD TIMER MASK	WD ALERT MASK	TMSK	AVIN_MASK	WD PC STAT MASK	WD SR STAT MASK	miniBK_OV_INT_MASK	RFU
02	DVS_FROM_I2C_DB11	DVS_FROM_I2C_DB10	DVS_FROM_I2C_DB9	RFU	RFU	FACTORY MODE	Over_Temp_Shutdown	AVIN_DAT
03	INTADR							
04	POWER UP FAULT	RFU	POWER OFF	MR	RFU	WD_INT_EN	WD_PC_EN	WD_SR_EN
05	ILED7<3:0>				ILED6<3:0>			
06	RFU	GPIO7 STAT	GPIO6 STAT	GPIO5 STAT	GPIO4 STAT	GPIO3 STAT	GPIO2 STAT	GPIO1 STAT
07	RFU	GPIO7 Toggled	GPIO6 Toggled	GPIO5 Toggled	GPIO4 Toggled	GPIO3 Toggled	GPIO2 Toggled	GPIO1 Toggled
08	RFU	GPIO7 MASK	GPIO6 MASK	GPIO5 MASK	GPIO4 MASK	GPIO3 MASK	GPIO2 MASK	GPIO1 MASK
0A	UNLOCK							
0F	TRST_DLY[1:0]		DPSLP_EN	SLEEP_EN	Dis_GPIO_OP_FallingDly	AVINMON[2:0]		
10	EN_PullUp_GPIO1_Dly	EN_GPIO5_Output Dly	EN_GPIO4_Output Dly	EN_GPIO3_Output Dly	EN_GPIO2_Output Dly	EN_GPIO1_Output Dly	DIS UVOV FAULT	ANALOG MODE Enable
11	I2C Pullup Enable	GPIO7 Pullup Enable	GPIO6 Pullup Enable	GPIO5 Pullup Enable	GPIO4 Pullup Enable	GPIO3 Pullup Enable	GPIO2 Pullup Enable	GPIO1 Pullup Enable
12	MODE1				MUX1			
13	MODE2				MUX2			
14	MODE3				MUX3			
15	MODE4				MUX4			
16	MODE5				MUX5			
17	MODE6				MUX6			
18	MODE7				MUX7			
19	CMI REV ID [3:0]				extpg_blank_time	db_enable_extpg<2:0>		
1A	ENTER_SLEEP	miniBK_OV_STDN_DIS	VINIO1_SEL	VINI2C_SEL	VSET_mBK<1:0>		VSET_LDO<1:0>	

ADDR (HEX)	7	6	5	4	3	2	1	0
BUCK1								
40	POK	VOUT_OV_FLT	RFU	ILIM_SHUT	ILIM_FLT	ILIM_WARN	VIN_OV	VIN_UV
41	UV_INT_MSK	OV_INT_MSK	RFU	ISHUT_INT_MSK	IFLT_INT_MSK	IWARN_INT_MSK	VINOV_INT_MASK	VINUV_INT_MASK
45	VSET0[7:0]							
46	VSET1[7:0]							
47	DBON[3:0]				ON	QLTCH	SLEEP EN	DP SLEEP EN
48	VOOV_MSK	RST	DBQL[2:0]			DBOK[2:0]		

49	ILIM_STDN_DIS	ON_DELAY[2:0]			OFF_DELAY[3:0]			
4A	ILIM[1:0]		VINUVOV_REG_SHUT_MASK	VINUVOV_SYS_SHUT_MASK	UVOV_REG_SHUT_MASK	UVOV_SYS_SHUT_MASK	DB_DVS[1:0]	
4B	SOFT_LSON	DISBBM_L2H	INC_ILIM20PER	POK_OPT	ENHS_Status_HI	HSD_SLEW	LSD_SLEW[1:0]	
4C	DBOK_SEL	EN_LPM	FORCE_PWM	VOUT_OPT	FREQ[3:0]			

ADDR (HEX)	7	6	5	4	3	2	1	0
BUCK2								
60	POK	VOUT_OV_FLT	RFU	ILIM_SHUT	ILIM_FLT	ILIM_WARN	VIN_OV	VIN_UV
61	UV_INT_MSK	OV_INT_MSK	RFU	ISHUT_INT_MSK	IFLT_INT_MSK	IWARN_INT_MSK	VINOV_INT_MASK	VINUV_INT_MASK
65	VSET0[7:0]							
66	VSET1[7:0]							
67	DBON[3:0]				ON	QLTCH	SLEEP EN	DP SLEEP EN
68	VOOV_MSK	RST	DBQL[2:0]			DBOK[2:0]		
69	ILIM_STDN_DIS	ON_DELAY[2:0]			OFF_DELAY[3:0]			
6A	ILIM[1:0]		VINUVOV_REG_SHUT_MASK	VINUVOV_SYS_SHUT_MASK	UVOV_REG_SHUT_MASK	UVOV_SYS_SHUT_MASK	DB_DVS[1:0]	
6B	SOFT_LSON	DISBBM_L2H	INC_ILIM20PER	POK_OPT	ENHS_Status_HI	HSD_SLEW	LSD_SLEW[1:0]	
6C	DBOK_SEL	EN_LPM	FORCE_PWM	VOUT_OPT	FREQ[3:0]			

ADDR (HEX)	7	6	5	4	3	2	1	0
BUCK3								
80	POK	VOUT_OV_FLT	RFU	ILIM_SHUT	ILIM_FLT	ILIM_WARN	VIN_OV	VIN_UV
81	UV_INT_MSK	OV_INT_MSK	RFU	ISHUT_INT_MSK	IFLT_INT_MSK	IWARN_INT_MSK	VINOV_INT_MASK	VINUV_INT_MASK
85	VSET0[7:0]							
86	VSET1[7:0]							
87	DBON[3:0]				ON	QLTCH	SLEEP EN	DP SLEEP EN
88	VOOV_MSK	RST	DBQL[2:0]			DBOK[2:0]		
89	ILIM_STDN_DIS	ON_DELAY[2:0]			OFF_DELAY[3:0]			
8A	ILIM[1:0]		VINUVOV_REG_SHUT_MASK	VINUVOV_SYS_SHUT_MASK	UVOV_REG_SHUT_MASK	UVOV_SYS_SHUT_MASK	DB_DVS[1:0]	
8B	SOFT_LSON	DISBBM_L2H	RFU	POK_OPT	ENHS_Status_HI	HSD_SLEW	LSD_SLEW[1:0]	
8C	DBOK_SEL	EN_LPM	FORCE_PWM	VOUT_OPT	FREQ[3:0]			

ADDR (HEX)	7	6	5	4	3	2	1	0
BUCK4								
A0	POK	VOUT_OV_FLT	RFU	ILIM_SHUT	ILIM_FLT	ILIM_WARN	VIN_OV	VIN_UV
A1	UV_INT_MSK	OV_INT_MSK	RFU	ISHUT_INT_MSK	IFLT_INT_MSK	IWARN_INT_MSK	VINOV_INT_MASK	VINUV_INT_MASK
A5	VSET0[7:0]							

A6	VSET1[7:0]							
A7	DBON[3:0]				ON	QLTCH	SLEEP EN	DP SLEEP EN
A8	VOOV_MSK	RST	DBQL[2:0]			DBOK[2:0]		
A9	ILIM_STDN_DIS	ON_DELAY[2:0]			OFF_DELAY[3:0]			
AA	ILIM[1:0]		VINUVOV_REG_SHUT MASK	VINUVOV_SYS_SHUT _MASK	UVOV_REG_SHUT_M ASK	UVOV_SYS_SHUT_MA SK	DB_DVS[1:0]	
AB	SOFT_LSON	DISBBM_L2H	RFU	POK_OPT	ENHS_Status_HI	HSD_SLEW	LSD_SLEW[1:0]	
AC	DBOK_SEL	EN_LPM	FORCE_PWM	VOUT_OPT	FREQ[3:0]			

ADDR (HEX)	7	6	5	4	3	2	1	0
BUCK_BOOST								
C0	POK	VOUT_OV_FLT	RFU	ILIM_SHUT	RFU	ILIM_WARN	VIN_OV	VIN_UV
C1	UV_INT_MSK	OV_INT_MSK	RFU	ISHUT_INT_MSK	RFU	IWRN_INT_MSK	VINOV_INT_MSK	VINUV_INT_MSK
C5	DBOK_SEL	VSET0[6:0]						
C6	EN_PLDN	VSET1[6:0]						
C7	DBON[3:0]				ON	QLTCH	SLEEP EN	DP SLEEP EN
C8	VOOV_MSK	RST	DBQL[2:0]			DBOK[2:0]		
C9	ILIM_STDN_DIS	ON_DELAY[2:0]			OFF_DLY[3:0]			
CA	OV Pull Down	RFU	VINUVOV_REG_SHUT _MASK	VINUVOV_SYS_SHUT _MASK	UVOV_REG_SHUT_M ASK	UVOV_SYS_SHUT_M ASK	RFU	RFU

MASTER REGISTERS

0x00 - MASTER Configuration Register

Address = 0x00h			Default = 0x00h			Type = Basic Volatile		
BIT	7	6	5	4	3	2	1	0
Name	WD TIMER Expired	WD TIMER ALERT	TWARN	AVIN_STAT	WD PC STAT	WD SR STAT	miniBK_OV_FLT	RFU
Default	0	0	0	0	0	0	0	0
Access	RO	RO	RO	RO	RO	RO	RO	RO

Name	Description	Notes
WD TIMER Expired	0 = Watchdog timer has not expired 1 = Watchdog timer has expired (8.2s)	When this bit = 1, an interrupt is generated on the nIRQ pin if WD_INT_EN = 1 and WD TIMER MSK = 0. This bit is latched and must be read via I2C to clear it back to 0
WD TIMER ALERT	0 = Watchdog timer alert has not expired 1 = Watchdog timer alert has expired (7.4s)	When this bit = 1, an interrupt is generated on the nIRQ pin if WD_INT_EN = 1 and WD ALERT MASK = 0. This bit is latched and must be read via I2C to clear it back to 0
TWARN	0 = Junction temperature < warning threshold TWARN (125deg). 1 = Junction temperature > warning threshold TWARN (125deg).	When this bit = 1, an interrupt is generated on the nIRQ pin if TMSK = 0. This bit is cleared to 0 when die temperature < TWARN falling threshold and this bit is read.
AVIN_STAT	0 = AVIN voltage is above the AVIN_MON threshold 1 = AVIN voltage is below the AVIN_MON threshold	When this bit = 1, an interrupt is generated on the nIRQ pin if AVIN_MASK = 0. When AVIN_STAT = 1, this bit is latched until the register contents are read via I2C. The AVIN_MON warning threshold is programmed with the AVINMON bits in the 0x0F [2:0] register bits. AVINMON monitors voltage at the VBUS pins.
WD PC STAT	0 = Power Cycle status is cleared 1 = Power Cycle has occurred.	Enable Watch Dog Power Cycle by setting register 0x04h bit 1 (WD_PC_EN) to 1. When a Watch Dog Power Cycle occurs, WD PC STAT is set to 1 and an interrupt is generated on the nIRQ pin if the WD PC STAT MASK = 0. Reading this register automatically clears this bit to a 0.
WD SR STAT	0 = Soft reset status is cleared 1 = Soft reset has occurred	Enable Watch Dog Soft Reset by setting register 0x04h bit 0 (WD_SR_EN) to 1. When a Watch Dog Soft Restet occurs, WD SR STAT is set to 1 and an interrupt is generated on the nIRQ pin if the WD SR STAT MASK = 0. Reading this register automatically clears this bit to a 0.
miniBK_OV_FLT	miniBUCK (VCC5) over voltage status: 0: Over voltage does not occur 1: Over voltage has occurred	
RFU	Reserved for future use	

0x01 - MASTER Configuration Register

Address = 0x01h		Default = 0xFEh			Type = Basic Non-Volatile			
BIT	7	6	5	4	3	2	1	0
Name	WD TIMER MASK	WD ALERT MASK	TMSK	AVIN_MASK	WD PC STAT MASK	WD SR STAT MASK	miniBK_OV_INT_MASK	RFU
Default	1	1	1	1	1	1	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	RO

Name	Description	Notes
WD TIMER MASK	0 = unmasks the watch dog timer interrupt 1 = masks the watch dog timer interrupt	When this bit =1, the WD TIMER Expired interrupt is masked but WD TIMER Expired bit still provides the status
WD ALERT MASK	0 = unmasks the watch dog alert interrupt 1 = masks the watch dog alert interrupt	When this bit = 1, the WD TIMER ALERT interrupt is masked but WD TIMER ALERT still provides watchdog status.
TMSK	0 = unmasks the thermal warning interrupt 1 = masks the thermal warning interrupt	When this bit = 1, the TWARN interrupt is masked but TWARN still provides temperature warning status.
AVIN_MASK	0 = unmasks the AVIN_STAT interrupt 1 = masks the AVIN_STAT interrupt	When this bit = 1, the AVIN_STAT interrupt is masked but AVIN_STAT still provides UV warn status.
WD PC STAT MASK	0 = unmasks the WD PC STAT interrupt 1 = masks the WD PC STAT interrupt	When this bit = 1, the WD PC STAT interrupt is masked but WD PC STAT still provides status.
WD SR STAT MASK	0 = unmasks the WD SR STAT interrupt 1 = masks the WD SR STAT interrupt	When this bit = 1, the WD SR STAT interrupt is masked but WD SR STAT still provides status.
miniBK_OV_INT_MASK	0 = unmasks the miniBUCK (VCC5) over voltage interrupt 1 = masks the miniBUCK (VCC5) over voltage interrupt	
RFU	Reserved for future use	

0x02 - MASTER Configuration Register

Address = 0x02h	Default = 0x00h	Type = Basic Volatile/Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	DVS_FROM_I2C_DB11	DVS_FROM_I2C_DB10	DVS_FROM_I2C_DB9	RFU	RFU	FACTORY MODE	Over_Temp_Shutdown	AVIN_DAT
Default	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	RO	RO	RO	RO	RO

Name	Description	Notes
DVS_FROM_I2C_DB11	This bit is used to control regulator DVS by I2C	With EN_DVS_BY_I2C =1, this bit can be used to control regulator DVS by I2C. Contact the factory for the details on each specific CMI.
DVS_FROM_I2C_DB10	This bit is used to control regulator DVS by I2C	With EN_DVS_BY_I2C =1, this bit can be used to control regulator DVS by I2C. Contact the factory for the details on each specific CMI.
DVS_FROM_I2C_DB9	This bit is used to control regulator DVS by I2C	With EN_DVS_BY_I2C =1, this bit can be used to control regulator DVS by I2C. Contact the factory for the details on each specific CMI.
RFU	Reserved for future use	
RFU	Reserved for future use	
FACTORY MODE	0 = chip is not in factory mode. 1 = chip is in factory mode.	
Over_Temp_Shutdown	0 = not in thermal shutdown 1 = in thermal shutdown	Real time status bit for thermal shutdown
AVIN_DAT	0 = AVIN voltage is below AVIN_MON threshold 1 = AVIN voltage is above AVIN_MON threshold	Real time status bit for AVIN_MON threshold set in register 0x0Fh

0x03 - MASTER Configuration Register

Address = 0x03h			Default = 0x00h			Type = Basic Non-Volatile		
BIT	7	6	5	4	3	2	1	0
Name	INTADR[7:0]							
Default	00000000							
Access	RO							

Name	Description	Notes
INTADR[7:0]	Provides the hex address of the function that generated the interrupt on nIRQ	MSTR Interrupt Addr, 0x01 GPIO Interrupt Addr, 0x02 Buck1 Interrupt Addr, 0x41 Buck2 Interrupt Addr, 0x61 Buck3 Interrupt Addr, 0x81 Buck4 Interrupt Addr, 0xA1 BuckBoost Interrupt Addr, 0xC1

0x04 - MASTER Configuration Register

Address = 0x04h			Default = 0x00h			Type = Basic Non-Volatile		
BIT	7	6	5	4	3	2	1	0
Name	POWER UP FAULT	RFU	POWER OFF	MR	RFU	WD_INT_EN	WD_PC_EN	WD_SR_EN
Default	0	0	0	0	0	0	0	0
Access	R/W	RO	R/W	R/W	RO	R/W	R/W	R/W

Name	Description	Notes
POWER UP FAULT	0: Normal, can write to 0 as condition to power start sequence. 1: Fault retry (100ms) occurred 7 times -> assert flag and move to RESET state.	Power up fault status/flag. User can write a 0 to clear the fault bit. It is not possible to write a 1 into this bit.
RFU	Reserved for future use	
POWER OFF	0: Normal 1: Moves the IC into the RESET state and turns off all Regulators. This bit must be changed back to 0 to restart a power on sequence.	
MR	0: Normal. 1: Writing 1 to this bit power cycles all PMU bucks, clears all VM registers, moves IC to RESET state, then restarts the PMU after 0.5s. This is the hard-reset function for PMU bucks and buck-boost.	Hard reset or Manual reset shuts down the buck and buck-boost converters.
RFU	Reserved for future use	
WD_INT_EN	0 = Disables interrupt when the watchdog timer expires 1 = Enables interrupt when the watchdog timer expires	
WD_PC_EN	0 = Disables power cycling when the watchdog timer expires 1 = Enables power cycling when the watchdog timer expires	Power down for 0.5s, then start Power On Sequence
WD_SR_EN	0 = Disables soft reset when the watchdog timer expires 1 = Enables soft reset when the watchdog timer expires	When a watch dog soft reset occurs, WD SR STAT is triggered. nRESET is also triggered then released. nRESET goes low to tell the external MCU to check the fault registers to find the fault.

0x05 - MASTER Configuration Register

Address = 0x05h			Default = 0x00h			Type = Basic Non-Volatile		
BIT	7	6	5	4	3	2	1	0
Name	ILED7[3:0]				ILED6[3:0]			
Default	0000				0000			
Access	R/W				R/W			

Name	Description	Notes
ILED7[3:0]	Config current setting for GPIO D2 in case LED driver	
ILED6[3:0]	Config current setting for GPIO D1 in case LED driver	

0x06 - MASTER Configuration Register

Address = 0x06h			Default = 0x00h			Type = Basic Volatile		
BIT	7	6	5	4	3	2	1	0
Name	RFU	GPIO7 STAT	GPIO6 STAT	GPIO5 STAT	GPIO4 STAT	GPIO3 STAT	GPIO2 STAT	GPIO1 STAT
Default	0	0	0	0	0	0	0	0
Access	RO	RO	RO	RO	RO	RO	RO	RO

Name	Description	Notes
RFU	Reserved for future use	
GPIO7 STAT	GPIO 7 real time status	When a GPIO is configured as input, user can use this bit to monitor status of GPIO. When = ”1” the input voltage is a logic H. When = ”0” the input voltage is logic L.
GPIO6 STAT	GPIO 6 real time status	
GPIO5 STAT	GPIO 5 real time status	
GPIO4 STAT	GPIO 4 real time status	
GPIO3 STAT	GPIO 3 real time status	
GPIO2 STAT	GPIO 2 real time status	
GPIO1 STAT	GPIO 1 real time status	

0x07 - MASTER Configuration Register

Address = 0x07h			Default = 0x00h			Type = Basic Volatile		
BIT	7	6	5	4	3	2	1	0
Name	RFU	GPIO7 Toggled	GPIO6 Toggled	GPIO5 Toggled	GPIO4 Toggled	GPIO3 Toggled	GPIO2 Toggled	GPIO1 Toggled
Default	0	0	0	0	0	0	0	0
Access	RO	RO	RO	RO	RO	RO	RO	RO

Name	Description	Notes
RFU	Reserved for future use	
GPIO7 Toggled	GPIOx toggle detected. Bit set to 1 when GPIOx toggle L to H or H to L. Bit set to 0 means there is no toggle.	When a GPIO is configured as input, user can use this bit to monitor status of GPIO toggle. These bits are latched and must be read via I2C to clear them back to 0.
GPIO6 Toggled		
GPIO5 Toggled		
GPIO4 Toggled		
GPIO3 Toggled		
GPIO2 Toggled		
GPIO1 Toggled		

0x08 - MASTER Configuration Register

Address = 0x08h			Default = 0x7Fh			Type = Basic Non-Volatile		
BIT	7	6	5	4	3	2	1	0
Name	RFU	GPIO7 MASK	GPIO6 MASK	GPIO5 MASK	GPIO4 MASK	GPIO3 MASK	GPIO2 MASK	GPIO1 MASK
Default	0	1	1	1	1	1	1	1
Access	RO	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Name	Description	Notes
RFU	Reserved for future use	
GPIO7 MASK	GPIOx generates the interrupt signal individually when GPIOx config as input. If the MASK bit is asserted, no interrupt is generated when toggle event happens.	
GPIO6 MASK		
GPIO5 MASK		
GPIO4 MASK		
GPIO3 MASK		
GPIO2 MASK		
GPIO1 MASK		

0x0A - MASTER Configuration Register

Address = 0x0Ah			Default = 0x00h			Type = Basic Non-Volatile		
BIT	7	6	5	4	3	2	1	0
Name	UNLOCK[7:0]							
Default	00000000							
Access	R/W							

Name	Description	Notes
UNLOCK[7:0]	The IC implements a special register passcode that enables I2C write transactions. This prevents accidental register changes. Enable I2C write functionality by writing a value of 0xAAh to register 0x0Ah (Unlock Register Key). Change this register to any other value to prevent accidental changes to the I2C register values.	

0x0F - MASTER Configuration Register

Address = 0x0Fh			Default = 0x17h			Type = Basic Non-Volatile		
BIT	7	6	5	4	3	2	1	0
Name	TRST_DLY[1:0]		DPSLP_EN	SLEEP_EN	Dis_GPIO_OP_FallingDly	AVINMON[2:0]		
Default	00		0	1	0	111		
Access	R/W		R/W	R/W	R/W	R/W		

Name	Description	Notes
TRST_DLY[1:0]	Reset Timer Setting: 00=20ms 01=40ms 10=60ms 11=100ms	
DPSLP_EN	DPSLP mode enable 1: Enables DPSLP 0: Disables DPSLP	
SLEEP_EN	SLEEP mode enable 1: Enables SLEEP 0: Disables SLEEP	
Dis_GPIO_OP_FallingDly	1: Disable falling delay of GPIOx when configure as output. 0: Enable falling delay of GPIOx when configure as output.	
AVINMON[2:0]	000 = 3.0V 001 = 3.2V 010 = 3.4V 011 = 3.6V 100 = 3.8V 101 = 4.0V 110 = 8.0V 111 = 9.0V	PMIC AVIN pin voltage monitor setting bits.

0x10 - MASTER Configuration Register

Address = 0x10h			Default = 0x80h			Type = Basic Non-Volatile		
BIT	7	6	5	4	3	2	1	0
Name	EN_PullUp_GPIO1_Dly	EN_GPIO5_Output Dly	EN_GPIO4_Output Dly	EN_GPIO3_Output Dly	EN_GPIO2_Output Dly	EN_GPIO1_Output Dly	DIS UVOV FAULT	ANALOG MODE Enable
Default	1	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Name	Description	Notes
EN_PullUp_GPIO1_Dly	0: no delay (after NVM load done) 1: Delay 2ms.	Enable delay pull up for GPIO1
EN_GPIO5_Output Dly EN_GPIO4_Output Dly EN_GPIO3_Output Dly EN_GPIO2_Output Dly EN_GPIO1_Output Dly	0: disable delay for GPIOx configuration at output mode (both edge, default delay is 1.5ms). 1: enable delay for GPIOx configuration at output mode (both edge, default delay is 1.5ms).	
DIS UVOV FAULT	0: normal 1: Disables OV_UV shutdown for the Bucks and LDOs.	
ANALOG MODE Enable	0: GPIO analog mode is disabled 1: GPIO analog mode is enabled	Analog mode makes GPIO the input to an internal comparator with a 0.8V reference.

0x11 - MASTER Configuration Register

Address = 0x11h			Default = 0x79h			Type = Basic Non-Volatile		
BIT	7	6	5	4	3	2	1	0
Name	I2C Pullup Enable	GPIO7 Pullup Enable	GPIO6 Pullup Enable	GPIO5 Pullup Enable	GPIO4 Pullup Enable	GPIO3 Pullup Enable	GPIO2 Pullup Enable	GPIO1 Pullup Enable
Default	0	1	1	1	1	0	0	1
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Name	Description	Notes
I2C Pullup Enable	0 – disable I2C signals to be pulled up to VIO through a 10k resistor. 1 – enable I2C signals to be pulled up to VIO through a 10k resistor.	To VIO or VCC5
GPIO7 Pullup Enable	0 – disable GPIOx to be pulled up to VIO through a 200k resistor. 1 – enable GPIOx to be pulled up to VIO through a 200k resistor.	
GPIO6 Pullup Enable		
GPIO5 Pullup Enable		
GPIO4 Pullup Enable		
GPIO3 Pullup Enable		
GPIO2 Pullup Enable		
GPIO1 Pullup Enable		To VIO or VCC5

0x12 - MASTER Configuration Register

Address = 0x12h				Default = 0x01h			Type = Basic Non-Volatile	
BIT	7	6	5	4	3	2	1	0
Name	MODE1[3:0]				MUX1[3:0]			
Default	0000				0001			
Access	R/W				R/W			

Name	Description	Notes
MODE1[3:0]	Setting GPIO function	Changing this bit may result in unexpected IC behavior.
MUX1[3:0]		

0x13 - MASTER Configuration Register

Address = 0x13h				Default = 0x42h			Type = Basic Non-Volatile	
BIT	7	6	5	4	3	2	1	0
Name	MODE2[3:0]				MUX2[3:0]			
Default	0100				0010			
Access	R/W				R/W			

Name	Description	Notes
MODE2[3:0]	Setting GPIO function	Changing this bit may result in unexpected IC behavior.
MUX2[3:0]		

0x14 - MASTER Configuration Register

Address = 0x14h			Default = 0x43h		Type = Basic Non-Volatile			
BIT	7	6	5	4	3	2	1	0
Name	MODE3[3:0]				MUX3[3:0]			
Default	0100				0011			
Access	R/W				R/W			

Name	Description	Notes
MODE3[3:0]	Setting GPIO function	Changing this bit may result in unexpected IC behavior.
MUX3[3:0]		

0x15 - MASTER Configuration Register

Address = 0x15h			Default = 0x11h		Type = Basic Non-Volatile			
BIT	7	6	5	4	3	2	1	0
Name	MODE4[3:0]				MUX4[3:0]			
Default	0001				0001			
Access	R/W				R/W			

Name	Description	Notes
MODE4[3:0]	Setting GPIO function	Changing this bit may result in unexpected IC behavior.
MUX4[3:0]		

0x16 - MASTER Configuration Register

Address = 0x16h			Default = 0x13h			Type = Basic Non-Volatile	
BIT	7	6	5	4	3	2	1	0
Name	MODE5[3:0]				MUX5[3:0]			
Default	0001				0011			
Access	R/W				R/W			

Name	Description	Notes
MODE5[3:0]	Setting GPIO function	Changing this bit may result in unexpected IC behavior.
MUX5[3:0]		

0x17 - MASTER Configuration Register

Address = 0x17h				Default = 0x6Fh			Type = Basic Non-Volatile	
BIT	7	6	5	4	3	2	1	0
Name	MODE6[3:0]				MUX6[3:0]			
Default	0110				1111			
Access	R/W				R/W			

Name	Description	Notes
MODE6[3:0]	Setting GPIO function	Changing this bit may result in unexpected IC behavior.
MUX6[3:0]		

0x18 - MASTER Configuration Register

Address = 0x18h			Default = 0x6Eh			Type = Basic Non-Volatile		
BIT	7	6	5	4	3	2	1	0
Name	MODE7[3:0]				MUX7[3:0]			
Default	0110				1111			
Access	R/W				R/W			

Name	Description	Notes
MODE7[3:0]	Setting GPIO function	Changing this bit may result in unexpected IC behavior.
MUX7[3:0]		

0x19 - MASTER Configuration Register

Address = 0x19h	Default = 0x10h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	CMI REV ID [3:0]				extpg_blank_time	db_enable_extpg<2:0>		
Default	0001				0	000		
Access	R/W				R/W	R/W		

Name	Description	Notes
CMI REV ID [3:0]	Setting CMI version	
extpg_blank_time	External PG blank time 0 = 40 ms 1 = 20 ms	
db_enable_extpg<2:0>	choose db line to indicate MSTR the time external regulator is turned on then MSTR start to count blanking time for ext_pg 000 = no ext_reg is on 001 = dB[1] 010 = dB[2] 011 = dB[3] 100 = dB[4] 101 = dB[5] 110 = dB[6] 111 = dB[7]	

0x1A - MASTER Configuration Register

Address = 0x1Ah			Default = 0x04h				Type = Basic Non-Volatile	
BIT	7	6	5	4	3	2	1	0
Name	ENTER_SLEEP	miniBK_OV_STDN_DIS	VINIO1_SEL	VINI2C_SEL	VSET_mBK<1:0>		VSET_LDO<1:0>	
Default	0	0	0	0	01		00	
Access	R/W	R/W	R/W	R/W	R/W		R/W	

Name	Description	Notes
ENTER_SLEEP	0: Normal mode 1: Enable SLEEP mode	
miniBK_OV_STDN_DIS	0: enable to shut down all regulators when miniBK (VCC5) is over voltage. 1: disable to shut down all regulators when miniBK (VCC5) is over voltage.	
VINIO1_SEL	Select Vsupply for GPIO1: 0: VIO 1: VCC5	
VINI2C_SEL	Select Vsupply for SCL/SDA: 0: VIO 1: VCC5	
VSET_mBK<1:0>	Setting VCC5 output voltage when it is in buck mode: 00: 4.9V 01: 5.0V 10: 5.1V 11: 5.3V	
VSET_LDO<1:0>	Setting VCC5 output voltage when it is in LDO mode: 00: 4.75V 01: 5.00V 10: 5.10V 11: 5.25V	

BUCK1 REGISTERS

0x40 – BUCK1 Configuration Register

Address = 0x40h		Default = 0x00h		Type = Basic Volatile			
BIT	7	6	5	4	3	2	1	0
Name	POK	VOUT_OV_FLT	RFU	ILIM_SHUT	ILIM_FLT	ILIM_WARN	VIN_OV	VIN_UV
Default	0	0	0	0	0	0	0	0
Access	RO	RO	RO	RO	RO	RO	RO	RO

Name	Description	Notes
POK	1: VOUT OK 0: VOUT NOT OK	Provides real-time power good status
VOUT_OV_FLT	OV Status. 1: VOUT > VOUT OV (113%/110%) 0: VOUT < VOUT OV	When VOUT > OV, this bit goes high. It stays high until VOUT < OV and it is read.
RFU	Reserved for future use	
ILIM_SHUT	ILIM Shutdown Status. 1: Output Ilim Shutdown is triggered 0: Output Ilim Shutdown is not triggered	If the peak switch current reaches the 125% of ILIMSET threshold, this bit goes high. It stays high until peak switch current < 125% of ILIMSET and it is read.
ILIM_FLT	ILIM Fault Status. 1: Output Ilim Fault is triggered 0: Output Ilim Fault is not triggered	If the peak switch current reaches the ILIMSET threshold, this bit goes high. It stays high until peak switch current < ILIMSET and it is read.
ILIM_WARN	ILIM Warning Status. 1: Output Ilim Warning is triggered 0: Output Ilim Warning is not triggered	If the peak switch current reaches the 80% of ILIMSET threshold, this bit goes high. It stays high until peak switch current < 80% of ILIMSET and it is read.
VIN_OV	PVIN OV Status. 1: PVIN > PVIN OV (5.8V/15V) 0: PVIN is Normal	
VIN_UV	PVIN UV Status. 1: PVIN < PVIN UV (2.9V/2.7V) 0: PVIN is Normal	

0x41 – BUCK1 Configuration Register

Address = 0x41h			Default = 0xDFh		Type = Basic Non-Volatile			
BIT	7	6	5	4	3	2	1	0
Name	UV_INT_MSK	OV_INT_MSK	RFU	ISHUT_INT_MSK	IFLT_INT_MSK	IWARN_INT_MSK	VINOV_INT_MASK	VINUV_INT_MASK
Default	1	1	0	1	1	1	1	1
Access	R/W	R/W	RO	R/W	R/W	R/W	R/W	R/W

Name	Description	Notes
UV_INT_MSK	Mask POK Interrupt 1: Mask POK Interrupt 0: Unmask POK Interrupt	When 1, the Buck1 POK signal does not go to the master controller. This prevents Buck1 from asserting the nIRQ pin when it is disabled or drops out of regulation. BUCK1 POK still provides real-time power good status.
OV_INT_MSK	Mask VOUT_OV Interrupt 1: Mask VOUT_OV Interrupt 0: Unmask VOUT_OV Interrupt	When 1, the Buck1 OV signal does not go to the master controller. This prevents Buck1 from asserting the nIRQ pin when it is above regulation limits. VOUT_OV_FLT still provides OV status.
RFU	Reserved for future use	
ISHUT_INT_MSK	Mask ILIM SHUTDOWN Interrupt 1: Mask ILIM SHUTDOWN Interrupt 0: Unmask ILIM SHUTDOWN Interrupt	When 1, the Buck1 ILIM shutdown signal does not go to the master controller. ILIM_SHUT still provides current limit status.
IFLT_INT_MSK	Mask ILIM FAULT Interrupt 1: Mask ILIM FAULT Interrupt 0: Unmask ILIM FAULT Interrupt	When 1, the Buck1 ILIM fault signal does not go to the master controller. ILIM_FLT still provides current limit status.
IWARN_INT_MSK	Mask ILIM WARM Interrupt 1: Mask ILIM WARM Interrupt 0: Unmask ILIM WARM Interrupt	When 1, the Buck1 ILIM warn signal does not go to the master controller. ILIM_WARN still provides current limit warning status.
VINOV_INT_MASK	Mask PVIN_OV Interrupt 1: Mask PVIN_OV Interrupt 0: Unmask PVIN_OV Interrupt	When 1, the Buck1 VIN_OV signal does not go to the master controller. VIN_OV still provides current limit warning status.
VINUV_INT_MASK	Mask PVIN_UV Interrupt 1: Mask PVIN_UV Interrupt 0: Unmask PVIN_UV Interrupt	When 1, the Buck1 VIN_UV signal does not go to the master controller. VIN_UV still provides current limit warning status.

0x45 – BUCK1 Configuration Register

Address = 0x45h			Default = 0x0Ah			Type = Basic Non-Volatile		
BIT	7	6	5	4	3	2	1	0
Name	VSET0[7:0]							
Default	00001010							
Access	R/W							

Name	Description	Notes
VSET0[7:0]	Buck1 output voltage setting in ACTIVE mode.	VOUT0 = 0.6 +(20 mV or 5mV step)* VSET0[7:0]

0x46 – BUCK1 Configuration Register

Address = 0x46h			Default = 0x05h			Type = Basic Non-Volatile		
BIT	7	6	5	4	3	2	1	0
Name	VSET1[7:0]							
Default	00000101							
Access	R/W							

Name	Description	Notes
VSET1[7:0]	Buck1 output voltage setting for dynamic voltage scaling and SLEEP mode.	VOUT1 = 0.6 +(20 mV or 5mV step)* VSET1[7:0]

0x47 – BUCK1 Configuration Register

Address = 0x47h					Default = 0x0Dh		Type = Basic Non-Volatile	
BIT	7	6	5	4	3	2	1	0
Name	DBON[3:0]				ON	QLTCH	SLEEP EN	DP SLEEP EN
Default	0000				1	1	0	1
Access	R/W				R/W	R/W	R/W	R/W

Name	Description	Notes
DBON[3:0]	Determines startup sequencing from the CMI code	Do not change this
ON	0 – Buck1 is enabled through normal sequencing 1 – Buck1 is enabled via I2C that bypasses normal sequencing	
QLTCH	0 – Buck1 shuts down when its sequenced input shuts down 1 – Buck1 stays on when its sequenced input shuts down	
SLEEP EN	0 – Buck1 stays on when the IC enters Sleep mode 1 – Buck1 turns off when the IC enters Sleep mode	
DP SLEEP EN	0 – Buck1 stays on when the IC enters Deep Sleep mode 1 – Buck1 turns off when the IC enters Deep Sleep mode	

0x48 – BUCK1 Configuration Register

Address = 0x48h		Default = 0xDAh			Type = Basic Non-Volatile			
BIT	7	6	5	4	3	2	1	0
Name	VOOV_MSK	RST	DBQL[2:0]			DBOK[2:0]		
Default	1	1	011			010		
Access	R/W	R/W	R/W			R/W		

Name	Description	Notes
VOOV_MSK	Mask the VOUT_OV_FLT go into DIGNVM 1: Mask 0: Unmask	
RST	0 – Buck1 does not affect nRESET output 1 – Buck1 turning off asserts nRESET output low	
DBQL[2:0]	Determines startup sequencing from the CMI code	Changing this bit may result in unexpected IC behavior.
DBOK[2:0]	Determines startup sequencing from the CMI code	Changing this bit may result in unexpected IC behavior.

0x49 – BUCK1 Configuration Register

Address = 0x49h		Default = 0x32h			Type = Basic Non-Volatile			
BIT	7	6	5	4	3	2	1	0
Name	ILIM_STDN_DIS	ON_DELAY[2:0]			OFF_DELAY[3:0]			
Default	0	011			0010			
Access	R/W	R/W			R/W			

Name	Description	Notes
ILIM_STDN_DIS	Disable ILIM Shutdown 1: Mask ILIM SHUT signal 0: Unmask ILIM_SHUT signal	
ON_DELAY[2:0]	000 = 0ms 001 = 0.25ms 010 = 0.5m 011 = 1ms 100 = 2ms 101 = 4ms 110 = 8m 111 = 16ms	Programs the delay time between the Buck1 input trigger and when it turns on.
OFF_DELAY[3:0]	Sets the delay time between the Buck1 disable input to when it turns off.	Buck1 turnoff delay time is equal to OFF_DELAY * 1ms

0x4A – BUCK1 Configuration Register

Address = 0x4Ah	Default = 0x41h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	ILIM[1:0]		VINUVOV_REG_SHUT_MASK	VINUVOV_SYS_SHUT_MASK	UVOV_REG_SHUT_MASK	UVOV_SYS_SHUT_MASK	DB_DVS[1:0]	
Default	01		0	0	0	0	01	
Access	R/W		R/W	R/W	R/W	R/W	R/W	

Name	Description	Notes
ILIM[1:0]	00: IPEAK=6A, IVALLEY=5A 01: IPEAK=7A, IVALLEY=6A 10: IPEAK=8A, IVALLEY=7A 11: IPEAK=9A, IVALLEY=8A	
VINUVOV_REG_SHUT_MASK	When this bit =0, Buck1 will shutdown if VIN_Buck1 occurs UV/OV.	
VINUVOV_SYS_SHUT_MASK	When this bit =0, system will shutdown if VIN_Buck1 occurs UV/OV.	
UVOV_REG_SHUT_MASK	When this bit =0, Buck1 will shutdown if Buck1_OUT occurs UV/OV.	
UVOV_SYS_SHUT_MASK	When this bit =0, system will shutdown if Buck1_OUT occurs UV/OV.	
DB_DVS[1:0]	Determines DVS setting from the CMI code	Changing this bit may result in unexpected IC behavior.

0x4B – BUCK1 Configuration Register

Address = 0x4Bh		Default = 0xD3h			Type = Basic Non-Volatile			
BIT	7	6	5	4	3	2	1	0
Name	SOFT_LSON	DISBBM_L2H	INC_ILIM20PER	POK_OPT	ENHS_Status_HI	HSD_SLEW	LSD_SLEW[1:0]	
Default	1	1	0	1	0	0	11	
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	

Name	Description	Notes
SOFT_LSON	Enable Weak Turn-on LSON 0: Disable 1: Enable	
DISBBM_L2H	Enable Smooth Gate Driver 0: Simple BBM Gate Driver 1: Enable	
INC_ILIM20PER	0: Do not increase HSILIM/LSILIM 20% for BUCK1 1: Increase HSILIM/LSILIM 20% for BUCK1	
POK_OPT	0: Rising/Falling (87%/84% of VOUT) 1: Rising/Falling (90%/87% of VOUT)	
ENHS_Status_HI	0: HS_Status depend on the circuit working 1: Force the HS_Status signal to high	
HSD_SLEW	Adjust Slew Rate High-Side 0: Slow 1: High	
LSD_SLEW[1:0]	Adjust Slew Rate Low-Side 00: Weak 01: Slow 10: Normal 11: Fast	

0x4C – BUCK1 Configuration Register

Address = 0x4Ch		Default = 0x80h				Type = Basic Non-Volatile		
BIT	7	6	5	4	3	2	1	0
Name	DBOK_SEL	EN_LPM	FORCE_PWM	VOUT_OPT	FREQ[3:0]			
Default	1	0	0	0	0000			
Access	R/W	R/W	R/W	R/W	R/W			

Name	Description	Notes
DBOK_SEL	Determines startup sequencing from the CMI code	Changing this bit may result in unexpected IC behavior
EN_LPM	Enable Low-Power Mode 0: Disable (Works with DCM & CCM) 1: Enable	
FORCE_PWM	0: Not Force PWM Mode 1: Force PWM Mode	
VOUT_OPT	0 = 20mV steps 1 = 5mV steps	Select VOUT Range 0: 0.6V --> 5.25V 1: 0.6V --> - 1.875V
FREQ[3:0]	0000: 400kHz 1111: 1.9MHz Step: 100kHz	Select Frequency Switching

BUCK2 REGISTERS

0x60 – BUCK2 Configuration Register

Address = 0x60h			Default = 0x00h		Type = Basic Volatile			
BIT	7	6	5	4	3	2	1	0
Name	POK	VOUT_OV_FLT	RFU	ILIM_SHUT	ILIM_FLT	ILIM_WARN	VIN_OV	VIN_UV
Default	0	0	0	0	0	0	0	0
Access	RO	RO	RO	RO	RO	RO	RO	RO

Name	Description	Notes
POK	1: VOUT OK 0: VOUT NOT OK	Provides real-time power good status
VOUT_OV_FLT	OV Status. 1: VOUT > VOUT OV (113%/110%) 0: VOUT < VOUT OV	When VOUT > OV, this bit goes high. It stays high until VOUT < OV and it is read.
RFU	Reserved for future use	
ILIM_SHUT	ILIM Shutdown Status. 1: Output Ilim Shutdown is triggered 0: Output Ilim Shutdown is not triggered	If the peak switch current reaches the 125% of ILIMSET threshold, this bit goes high. It stays high until peak switch current < 125% of ILIMSET and it is read.
ILIM_FLT	ILIM Fault Status. 1: Output Ilim Fault is triggered 0: Output Ilim Fault is not triggered	If the peak switch current reaches the ILIMSET threshold, this bit goes high. It stays high until peak switch current < ILIMSET and it is read.
ILIM_WARN	ILIM Warning Status. 1: Output Ilim Warning is triggered 0: Output Ilim Warning is not triggered	If the peak switch current reaches the 80% of ILIMSET threshold, this bit goes high. It stays high until peak switch current < 80% of ILIMSET and it is read.
VIN_OV	PVIN OV Status. 1: PVIN > PVIN OV (5.8V/15V) 0: PVIN is Normal	
VIN_UV	PVIN UV Status. 1: PVIN < PVIN UV (2.9V/2.7V) 0: PVIN is Normal	

0x61 – BUCK2 Configuration Register

Address = 0x61h			Default = 0xDFh		Type = Basic Non-Volatile			
BIT	7	6	5	4	3	2	1	0
Name	UV_INT_MSK	OV_INT_MSK	RFU	ISHUT_INT_MSK	IFLT_INT_MSK	IWARN_INT_MSK	VINOV_INT_MASK	VINUV_INT_MASK
Default	1	1	0	1	1	1	1	1
Access	R/W	R/W	RO	R/W	R/W	R/W	R/W	R/W

Name	Description	Notes
UV_INT_MSK	Mask POK Interrupt 1: Mask POK Interrupt 0: Unmask POK Interrupt	When 1, the Buck2 POK signal does not go to the master controller. This prevents Buck2 from asserting the nIRQ pin when it is disabled or drops out of regulation. BUCK2 POK still provides real-time power good status.
OV_INT_MSK	Mask VOUT_OV Interrupt 1: Mask VOUT_OV Interrupt 0: Unmask VOUT_OV Interrupt	When 1, the Buck2 OV signal does not go to the master controller. This prevents Buck2 from asserting the nIRQ pin when it is above regulation limits. VOUT_OV_FLT still provides OV status.
RFU	Reserved for future use	
ISHUT_INT_MSK	Mask ILIM SHUTDOWN Interrupt 1: Mask ILIM SHUTDOWN Interrupt 0: Unmask ILIM SHUTDOWN Interrupt	When 1, the Buck2 ILIM shutdown signal does not go to the master controller. ILIM_SHUT still provides current limit status.
IFLT_INT_MSK	Mask ILIM FAULT Interrupt 1: Mask ILIM FAULT Interrupt 0: Unmask ILIM FAULT Interrupt	When 1, the Buck2 ILIM fault signal does not go to the master controller. ILIM_FLT still provides current limit status.
IWARN_INT_MSK	Mask ILIM WARM Interrupt 1: Mask ILIM WARM Interrupt 0: Unmask ILIM WARM Interrupt	When 1, the Buck2 ILIM warn signal does not go to the master controller. ILIM_WARN still provides current limit warning status.
VINOV_INT_MASK	Mask PVIN_OV Interrupt 1: Mask PVIN_OV Interrupt 0: Unmask PVIN_OV Interrupt	When 1, the Buck2 VIN_OV signal does not go to the master controller. VIN_OV still provides current limit warning status.
VINUV_INT_MASK	Mask PVIN_UV Interrupt 1: Mask PVIN_UV Interrupt 0: Unmask PVIN_UV Interrupt	When 1, the Buck2 VIN_UV signal does not go to the master controller. VIN_UV still provides current limit warning status.

0x65 – BUCK2 Configuration Register

Address = 0x65h			Default = 0x1Eh			Type = Basic Non-Volatile		
BIT	7	6	5	4	3	2	1	0
Name	VSET0[7:0]							
Default	00011110							
Access	R/W							

Name	Description	Notes
VSET0[7:0]	Buck2 output voltage setting in ACTIVE mode.	VOUT0 = 0.6 +(20 mV or 5mV step)* VSET0[7:0]

0x66 – BUCK2 Configuration Register

Address = 0x66h			Default = 0x14h			Type = Basic Non-Volatile		
BIT	7	6	5	4	3	2	1	0
Name	VSET1[7:0]							
Default	00010100							
Access	R/W							

Name	Description	Notes
VSET1[7:0]	Buck2 output voltage setting for dynamic voltage scaling and SLEEP mode.	VOUT1 = 0.6 +(20 mV or 5mV step)* VSET1[7:0]

0x67 – BUCK2 Configuration Register

Address = 0x67h					Default = 0x09h		Type = Basic Non-Volatile	
BIT	7	6	5	4	3	2	1	0
Name	DBON[3:0]				ON	QLTCH	SLEEP EN	DP SLEEP EN
Default	0000				1	0	0	1
Access	R/W				R/W	R/W	R/W	R/W

Name	Description	Notes
DBON[3:0]	Determines startup sequencing from the CMI code	Do not change this
ON	0 – Buck2 is enabled through normal sequencing 1 – Buck2 is enabled via I2C that bypasses normal sequencing	
QLTCH	0 – Buck2 shuts down when its sequenced input shuts down 1 – Buck2 stays on when its sequenced input shuts down	
SLEEP EN	0 – Buck2 stays on when the IC enters Sleep mode 1 – Buck2 turns off when the IC enters Sleep mode	
DP SLEEP EN	0 – Buck2 stays on when the IC enters Deep Sleep mode 1 – Buck2 turns off when the IC enters Deep Sleep mode	

0x68 – BUCK2 Configuration Register

Address = 0x68h		Default = 0xC3h			Type = Basic Non-Volatile			
BIT	7	6	5	4	3	2	1	0
Name	VOOV_MSK	RST	DBQL[2:0]			DBOK[2:0]		
Default	1	1	000			011		
Access	R/W	R/W	R/W			R/W		

Name	Description	Notes
VOOV_MSK	Mask the VOUT_OV_FLT go into DIGNVM 1: Mask 0: Unmask	
RST	0 – Buck2 does not affect nRESET output 1 – Buck2 turning off asserts nRESET output low	
DBQL[2:0]	Determines startup sequencing from the CMI code	Changing this bit may result in unexpected IC behavior.
DBOK[2:0]	Determines startup sequencing from the CMI code	Changing this bit may result in unexpected IC behavior.

0x69 – BUCK2 Configuration Register

Address = 0x69h		Default = 0x40h			Type = Basic Non-Volatile			
BIT	7	6	5	4	3	2	1	0
Name	ILIM_STDN_DIS	ON_DELAY[2:0]			OFF_DELAY[3:0]			
Default	0	100			0000			
Access	R/W	R/W			R/W			

Name	Description	Notes
ILIM_STDN_DIS	Disable ILIM Shutdown 1: Mask ILIM SHUT signal 0: Unmask ILIM_SHUT signal	
ON_DELAY[2:0]	000 = 0ms 001 = 0.25ms 010 = 0.5m 011 = 1ms 100 = 2ms 101 = 4ms 110 = 8m 111 = 16ms	Programs the delay time between the Buck2 input trigger and when it turns on.
OFF_DELAY[3:0]	Sets the delay time between the Buck2 disable input to when it turns off.	Buck2 turnoff delay time is equal to OFF_DELAY * 1ms

0x6A – BUCK2 Configuration Register

Address = 0x6Ah	Default = 0x41h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	ILIM[1:0]		VINUVOV_REG_SHUT_MASK	VINUVOV_SYS_SHUT_MASK	UVOV_REG_SHUT_MASK	UVOV_SYS_SHUT_MASK	DB_DVS[1:0]	
Default	01		0	0	0	0	01	
Access	R/W		R/W	R/W	R/W	R/W	R/W	

Name	Description	Notes
ILIM[1:0]	00: IPEAK=6A, IVALLEY=5A 01: IPEAK=7A, IVALLEY=6A 10: IPEAK=8A, IVALLEY=7A 11: IPEAK=9A, IVALLEY=8A	
VINUVOV_REG_SHUT_MASK	When this bit =0, Buck2 will shutdown if VIN_Buck2 occurs UV/OV.	
VINUVOV_SYS_SHUT_MASK	When this bit =0, system will shutdown if VIN_Buck2 occurs UV/OV.	
UVOV_REG_SHUT_MASK	When this bit =0, Buck2 will shutdown if Buck2_OUT occurs UV/OV.	
UVOV_SYS_SHUT_MASK	When this bit =0, system will shutdown if Buck2_OUT occurs UV/OV.	
DB_DVS[1:0]	Determines DVS setting from the CMI code	Changing this bit may result in unexpected IC behavior.

0x6B – BUCK2 Configuration Register

Address = 0x6Bh		Default = 0xD3h			Type = Basic Non-Volatile			
BIT	7	6	5	4	3	2	1	0
Name	SOFT_LSON	DISBBM_L2H	INC_ILIM20PER	POK_OPT	ENHS_Status_HI	HSD_SLEW	LSD_SLEW[1:0]	
Default	1	1	0	1	0	0	11	
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	

Name	Description	Notes
SOFT_LSON	Enable Weak Turn-on LSON 0: Disable 1: Enable	
DISBBM_L2H	Enable Smooth Gate Driver 0: Simple BBM Gate Driver 1: Enable	
INC_ILIM20PER	0: Do not increase HSILIM/LSILIM 20% for BUCK2 1: Increase HSILIM/LSILIM 20% for BUCK2	
POK_OPT	0: Rising/Falling (87%/84% of VOUT) 1: Rising/Falling (90%/87% of VOUT)	
ENHS_Status_HI	0: HS_Status depend on the circuit working 1: Force the HS_Status signal to high	
HSD_SLEW	Adjust Slew Rate High-Side 0: Slow 1: High	
LSD_SLEW[1:0]	Adjust Slew Rate Low-Side 00: Weak 01: Slow 10: Normal 11: Fast	

0x6C – BUCK2 Configuration Register

Address = 0x6Ch		Default = 0x00h					Type = Basic Non-Volatile	
BIT	7	6	5	4	3	2	1	0
Name	DBOK_SEL	EN_LPM	FORCE_PWM	VOUT_OPT	FREQ[3:0]			
Default	0	0	0	0	0000			
Access	R/W	R/W	R/W	R/W	R/W			

Name	Description	Notes
DBOK_SEL	Determines startup sequencing from the CMI code	Changing this bit may result in unexpected IC behavior
EN_LPM	Enable Low-Power Mode 0: Disable (Works with DCM & CCM) 1: Enable	
FORCE_PWM	0: Not Force PWM Mode 1: Force PWM Mode	
VOUT_OPT	0 = 20mV steps 1 = 5mV steps	Select VOUT Range 0: 0.6V --> 5.25V 1: 0.6V --> - 1.875V
FREQ[3:0]	0000: 400kHz 1111: 1.9MHz Step: 100kHz	Select Frequency Switching

BUCK3 REGISTERS

0x80 – BUCK3 Configuration Register

Address = 0x80h		Default = 0x00h		Type = Basic Volatile			
BIT	7	6	5	4	3	2	1	0
Name	POK	VOUT_OV_FLT	RFU	ILIM_SHUT	ILIM_FLT	ILIM_WARN	VIN_OV	VIN_UV
Default	0	0	0	0	0	0	0	0
Access	RO	RO	RO	RO	RO	RO	RO	RO

Name	Description	Notes
POK	1: VOUT OK 0: VOUT NOT OK	Provides real-time power good status
VOUT_OV_FLT	OV Status. 1: VOUT > VOUT OV (113%/110%) 0: VOUT < VOUT OV	When VOUT > OV, this bit goes high. It stays high until VOUT < OV and it is read.
RFU	Reserved for future use	
ILIM_SHUT	ILIM Shutdown Status. 1: Output Ilim Shutdown is triggered 0: Output Ilim Shutdown is not triggered	If the peak switch current reaches the 125% of ILIMSET threshold, this bit goes high. It stays high until peak switch current < 125% of ILIMSET and it is read.
ILIM_FLT	ILIM Fault Status. 1: Output Ilim Fault is triggered 0: Output Ilim Fault is not triggered	If the peak switch current reaches the ILIMSET threshold, this bit goes high. It stays high until peak switch current < ILIMSET and it is read.
ILIM_WARN	ILIM Warning Status. 1: Output Ilim Warning is triggered 0: Output Ilim Warning is not triggered	If the peak switch current reaches the 80% of ILIMSET threshold, this bit goes high. It stays high until peak switch current < 80% of ILIMSET and it is read.
VIN_OV	PVIN OV Status. 1: PVIN > PVIN OV (5.8V/15V) 0: PVIN is Normal	
VIN_UV	PVIN UV Status. 1: PVIN < PVIN UV (2.9V/2.7V) 0: PVIN is Normal	

0x81 – BUCK3 Configuration Register

Address = 0x81h			Default = 0xDFh		Type = Basic Non-Volatile			
BIT	7	6	5	4	3	2	1	0
Name	UV_INT_MSK	OV_INT_MSK	RFU	ISHUT_INT_MSK	IFLT_INT_MSK	IWARN_INT_MSK	VINOV_INT_MASK	VINUV_INT_MASK
Default	1	1	0	1	1	1	1	1
Access	R/W	R/W	RO	R/W	R/W	R/W	R/W	R/W

Name	Description	Notes
UV_INT_MSK	Mask POK Interrupt 1: Mask POK Interrupt 0: Unmask POK Interrupt	When 1, the Buck3 POK signal does not go to the master controller. This prevents Buck3 from asserting the nIRQ pin when it is disabled or drops out of regulation. BUCK3 POK still provides real-time power good status.
OV_INT_MSK	Mask VOUT_OV Interrupt 1: Mask VOUT_OV Interrupt 0: Unmask VOUT_OV Interrupt	When 1, the Buck3 OV signal does not go to the master controller. This prevents Buck3 from asserting the nIRQ pin when it is above regulation limits. VOUT_OV_FLT still provides OV status.
RFU	Reserved for future use	
ISHUT_INT_MSK	Mask ILIM SHUTDOWN Interrupt 1: Mask ILIM SHUTDOWN Interrupt 0: Unmask ILIM SHUTDOWN Interrupt	When 1, the Buck3 ILIM shutdown signal does not go to the master controller. ILIM_SHUT still provides current limit status.
IFLT_INT_MSK	Mask ILIM FAULT Interrupt 1: Mask ILIM FAULT Interrupt 0: Unmask ILIM FAULT Interrupt	When 1, the Buck3 ILIM fault signal does not go to the master controller. ILIM_FLT still provides current limit status.
IWARN_INT_MSK	Mask ILIM WARM Interrupt 1: Mask ILIM WARM Interrupt 0: Unmask ILIM WARM Interrupt	When 1, the Buck3 ILIM warn signal does not go to the master controller. ILIM_WARN still provides current limit warning status.
VINOV_INT_MASK	Mask PVIN_OV Interrupt 1: Mask PVIN_OV Interrupt 0: Unmask PVIN_OV Interrupt	When 1, the Buck3 VIN_OV signal does not go to the master controller. VIN_OV still provides current limit warning status.
VINUV_INT_MASK	Mask PVIN_UV Interrupt 1: Mask PVIN_UV Interrupt 0: Unmask PVIN_UV Interrupt	When 1, the Buck3 VIN_UV signal does not go to the master controller. VIN_UV still provides current limit warning status.

0x85 – BUCK3 Configuration Register

Address = 0x85h			Default = 0x3Ch			Type = Basic Non-Volatile		
BIT	7	6	5	4	3	2	1	0
Name	VSET0[7:0]							
Default	00111100							
Access	R/W							

Name	Description	Notes
VSET0[7:0]	Buck3 output voltage setting in ACTIVE mode.	VOUT0 = 0.6 +(20 mV or 5mV step)* VSET0[7:0]

0x86 – BUCK3 Configuration Register

Address = 0x86h			Default = 0x86h			Type = Basic Non-Volatile		
BIT	7	6	5	4	3	2	1	0
Name	VSET1[7:0]							
Default	00111100							
Access	R/W							

Name	Description	Notes
VSET1[7:0]	Buck3 output voltage setting for dynamic voltage scaling and SLEEP mode.	VOUT1 = 0.6 +(20 mV or 5mV step)* VSET1[7:0]

0x87 – BUCK3 Configuration Register

Address = 0x87h					Default = 0x09h		Type = Basic Non-Volatile	
BIT	7	6	5	4	3	2	1	0
Name	DBON[3:0]				ON	QLTCH	SLEEP EN	DP SLEEP EN
Default	0000				1	0	0	1
Access	R/W				R/W	R/W	R/W	R/W

Name	Description	Notes
DBON[3:0]	Determines startup sequencing from the CMI code	Do not change this
ON	0 – Buck3 is enabled through normal sequencing 1 – Buck3 is enabled via I2C that bypasses normal sequencing	
QLTCH	0 – Buck3 shuts down when its sequenced input shuts down 1 – Buck3 stays on when its sequenced input shuts down	
SLEEP EN	0 – Buck3 stays on when the IC enters Sleep mode 1 – Buck3 turns off when the IC enters Sleep mode	
DP SLEEP EN	0 – Buck3 stays on when the IC enters Deep Sleep mode 1 – Buck3 turns off when the IC enters Deep Sleep mode	

0x88 – BUCK3 Configuration Register

Address = 0x88h			Default = 0xC1h			Type = Basic Non-Volatile		
BIT	7	6	5	4	3	2	1	0
Name	VOOV_MSK	RST	DBQL[2:0]			DBOK[2:0]		
Default	1	1	000			001		
Access	R/W	R/W	R/W			R/W		

Name	Description	Notes
VOOV_MSK	Mask the VOUT_OV_FLT go into DIGNVM 1: Mask 0: Unmask	
RST	0 – Buck3 does not affect nRESET output 1 – Buck3 turning off asserts nRESET output low	
DBQL[2:0]	Determines startup sequencing from the CMI code	Changing this bit may result in unexpected IC behavior.
DBOK[2:0]	Determines startup sequencing from the CMI code	Changing this bit may result in unexpected IC behavior.

0x89 – BUCK3 Configuration Register

Address = 0x89h			Default = 0x04h			Type = Basic Non-Volatile		
BIT	7	6	5	4	3	2	1	0
Name	ILIM_STDN_DIS	ON_DELAY[2:0]			OFF_DELAY[3:0]			
Default	0	000			0100			
Access	R/W	R/W			R/W			

Name	Description	Notes
ILIM_STDN_DIS	Disable ILIM Shutdown 1: Mask ILIM SHUT signal 0: Unmask ILIM_SHUT signal	
ON_DELAY[2:0]	000 = 0ms 001 = 0.25ms 010 = 0.5m 011 = 1ms 100 = 2ms 101 = 4ms 110 = 8m 111 = 16ms	Programs the delay time between the Buck3 input trigger and when it turns on.
OFF_DELAY[3:0]	Sets the delay time between the Buck3 disable input to when it turns off.	Buck3 turnoff delay time is equal to OFF_DELAY * 1ms

0x8A – BUCK3 Configuration Register

Address = 0x8Ah	Default = 0x80h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	ILIM[1:0]		VINUVOV_REG_SHUT_MASK	VINUVOV_SYS_SHUT_MASK	UVOV_REG_SHUT_MASK	UVOV_SYS_SHUT_MASK	DB_DVS[1:0]	
Default	10		0	0	0	0	00	
Access	R/W		R/W	R/W	R/W	R/W	R/W	

Name	Description	Notes
ILIM[1:0]	00: IPEAK=4A, IVALLEY=3A 01: IPEAK=5A, IVALLEY=4A 10: IPEAK=6A, IVALLEY=5A 11: IPEAK=7A, IVALLEY=6A	
VINUVOV_REG_SHUT_MASK	When this bit =0, Buck3 will shutdown if VIN_Buck3 occurs UV/OV.	
VINUVOV_SYS_SHUT_MASK	When this bit =0, system will shutdown if VIN_Buck3 occurs UV/OV.	
UVOV_REG_SHUT_MASK	When this bit =0, Buck3 will shutdown if Buck3_OUT occurs UV/OV.	
UVOV_SYS_SHUT_MASK	When this bit =0, system will shutdown if Buck3_OUT occurs UV/OV.	
DB_DVS[1:0]	Determines DVS setting from the CMI code	Changing this bit may result in unexpected IC behavior.

0x8B – BUCK3 Configuration Register

Address = 0x8Bh	Default = 0xD3h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	SOFT_LSON	DISBBM_L2H	RFU	POK_OPT	ENHS_Status_HI	HSD_SLEW	LSD_SLEW[1:0]	
Default	1	1	0	1	0	0	11	
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	

Name	Description	Notes
SOFT_LSON	Enable Weak Turn-on LSON 0: Disable 1: Enable	
DISBBM_L2H	Enable Smooth Gate Driver 0: Simple BBM Gate Driver 1: Enable	
RFU	Reserved for future use	
POK_OPT	0: Rising/Falling (87%/84% of VOUT) 1: Rising/Falling (90%/87% of VOUT)	
ENHS_Status_HI	0: HS_Status depend on the circuit working 1: Force the HS_Status signal to high	
HSD_SLEW	Adjust Slew Rate High-Side 0: Slow 1: High	
LSD_SLEW[1:0]	Adjust Slew Rate Low-Side 00: Weak 01: Slow 10: Normal 11: Fast	

0x8C – BUCK3 Configuration Register

Address = 0x8Ch		Default = 0x81h				Type = Basic Non-Volatile		
BIT	7	6	5	4	3	2	1	0
Name	DBOK_SEL	EN_LPM	FORCE_PWM	VOUT_OPT	FREQ[3:0]			
Default	1	0	0	0	0001			
Access	R/W	R/W	R/W	R/W	R/W			

Name	Description	Notes
DBOK_SEL	Determines startup sequencing from the CMI code	Changing this bit may result in unexpected IC behavior
EN_LPM	Enable Low-Power Mode 0: Disable (Works with DCM & CCM) 1: Enable	
FORCE_PWM	0: Not Force PWM Mode 1: Force PWM Mode	
VOUT_OPT	0 = 20mV steps 1 = 5mV steps	Select VOUT Range 0: 0.6V --> 5.25V 1: 0.6V --> - 1.875V
FREQ[3:0]	0000: 400kHz 1111: 1.9MHz Step: 100kHz	Select Frequency Switching

BUCK4 REGISTERS

0xA0 – BUCK4 Configuration Register

Address = 0xA0h		Default = 0x00h			Type = Basic Volatile			
BIT	7	6	5	4	3	2	1	0
Name	POK	VOUT_OV_FLT	RFU	ILIM_SHUT	ILIM_FLT	ILIM_WARN	VIN_OV	VIN_UV
Default	0	0	0	0	0	0	0	0
Access	RO	RO	RO	RO	RO	RO	RO	RO

Name	Description	Notes
POK	1: VOUT OK 0: VOUT NOT OK	Provides real-time power good status
VOUT_OV_FLT	OV Status. 1: VOUT > VOUT OV (113%/110%) 0: VOUT < VOUT OV	When VOUT > OV, this bit goes high. It stays high until VOUT < OV and it is read.
RFU	Reserved for future use	
ILIM_SHUT	ILIM Shutdown Status. 1: Output Ilim Shutdown is triggered 0: Output Ilim Shutdown is not triggered	If the peak switch current reaches the 125% of ILIMSET threshold, this bit goes high. It stays high until peak switch current < 125% of ILIMSET and it is read.
ILIM_FLT	ILIM Fault Status. 1: Output Ilim Fault is triggered 0: Output Ilim Fault is not triggered	If the peak switch current reaches the ILIMSET threshold, this bit goes high. It stays high until peak switch current < ILIMSET and it is read.
ILIM_WARN	ILIM Warning Status. 1: Output Ilim Warning is triggered 0: Output Ilim Warning is not triggered	If the peak switch current reaches the 80% of ILIMSET threshold, this bit goes high. It stays high until peak switch current < 80% of ILIMSET and it is read.
VIN_OV	PVIN OV Status. 1: PVIN > PVIN OV (5.8V/15V) 0: PVIN is Normal	
VIN_UV	PVIN UV Status. 1: PVIN < PVIN UV (2.9V/2.7V) 0: PVIN is Normal	

0xA1 – BUCK4 Configuration Register

Address = 0xA1h			Default = 0xDFh		Type = Basic Non-Volatile			
BIT	7	6	5	4	3	2	1	0
Name	UV_INT_MSK	OV_INT_MSK	RFU	ISHUT_INT_MSK	IFLT_INT_MSK	IWARN_INT_MSK	VINOV_INT_MASK	VINUV_INT_MASK
Default	1	1	0	1	1	1	1	1
Access	R/W	R/W	RO	R/W	R/W	R/W	R/W	R/W

Name	Description	Notes
UV_INT_MSK	Mask POK Interrupt 1: Mask POK Interrupt 0: Unmask POK Interrupt	When 1, the Buck4 POK signal does not go to the master controller. This prevents Buck4 from asserting the nIRQ pin when it is disabled or drops out of regulation. BUCK4 POK still provides real-time power good status.
OV_INT_MSK	Mask VOUT_OV Interrupt 1: Mask VOUT_OV Interrupt 0: Unmask VOUT_OV Interrupt	When 1, the Buck4 OV signal does not go to the master controller. This prevents Buck4 from asserting the nIRQ pin when it is above regulation limits. VOUT_OV_FLT still provides OV status.
RFU	Reserved for future use	
ISHUT_INT_MSK	Mask ILIM SHUTDOWN Interrupt 1: Mask ILIM SHUTDOWN Interrupt 0: Unmask ILIM SHUTDOWN Interrupt	When 1, the Buck4 ILIM shutdown signal does not go to the master controller. ILIM_SHUT still provides current limit status.
IFLT_INT_MSK	Mask ILIM FAULT Interrupt 1: Mask ILIM FAULT Interrupt 0: Unmask ILIM FAULT Interrupt	When 1, the Buck4 ILIM fault signal does not go to the master controller. ILIM_FLT still provides current limit status.
IWARN_INT_MSK	Mask ILIM WARM Interrupt 1: Mask ILIM WARM Interrupt 0: Unmask ILIM WARM Interrupt	When 1, the Buck4 ILIM warn signal does not go to the master controller. ILIM_WARN still provides current limit warning status.
VINOV_INT_MASK	Mask PVIN_OV Interrupt 1: Mask PVIN_OV Interrupt 0: Unmask PVIN_OV Interrupt	When 1, the Buck4 VIN_OV signal does not go to the master controller. VIN_OV still provides current limit warning status.
VINUV_INT_MASK	Mask PVIN_UV Interrupt 1: Mask PVIN_UV Interrupt 0: Unmask PVIN_UV Interrupt	When 1, the Buck4 VIN_UV signal does not go to the master controller. VIN_UV still provides current limit warning status.

0xA5 – BUCK4 Configuration Register

Address = 0xA5h			Default = 0x87h			Type = Basic Non-Volatile		
BIT	7	6	5	4	3	2	1	0
Name	VSET0[7:0]							
Default	10000111							
Access	R/W							

Name	Description	Notes
VSET0[7:0]	Buck4 output voltage setting in ACTIVE mode.	VOUT0 = 0.6 +(20 mV or 5mV step)* VSET0[7:0]

0xA6 – BUCK4 Configuration Register

Address = 0xA6h			Default = 0x00h			Type = Basic Non-Volatile		
BIT	7	6	5	4	3	2	1	0
Name	VSET1[7:0]							
Default	00000000							
Access	R/W							

Name	Description	Notes
VSET1[7:0]	Buck4 output voltage setting for dynamic voltage scaling and SLEEP mode.	VOUT1 = 0.6 +(20 mV or 5mV step)* VSET1[7:0]

0xA7 – BUCK4 Configuration Register

Address = 0xA7h					Default = 0x0Fh		Type = Basic Non-Volatile	
BIT	7	6	5	4	3	2	1	0
Name	DBON[3:0]				ON	QLTCH	SLEEP EN	DP SLEEP EN
Default	0000				1	1	1	1
Access	R/W				R/W	R/W	R/W	R/W

Name	Description	Notes
DBON[3:0]	Determines startup sequencing from the CMI code	Do not change this
ON	0 – Buck4 is enabled through normal sequencing 1 – Buck4 is enabled via I2C that bypasses normal sequencing	
QLTCH	0 – Buck4 shuts down when its sequenced input shuts down 1 – Buck4 stays on when its sequenced input shuts down	
SLEEP EN	0 – Buck4 stays on when the IC enters Sleep mode 1 – Buck4 turns off when the IC enters Sleep mode	
DP SLEEP EN	0 – Buck4 stays on when the IC enters Deep Sleep mode 1 – Buck4 turns off when the IC enters Deep Sleep mode	

0xA8 – BUCK4 Configuration Register

Address = 0xA8h		Default = 0x80h			Type = Basic Non-Volatile			
BIT	7	6	5	4	3	2	1	0
Name	VOOV_MSK	RST	DBQL[2:0]			DBOK[2:0]		
Default	1	0	000			000		
Access	R/W	R/W	R/W			R/W		

Name	Description	Notes
VOOV_MSK	Mask the VOUT_OV_FLT go into DIGNVM 1: Mask 0: Unmask	
RST	0 – Buck4 does not affect nRESET output 1 – Buck4 turning off asserts nRESET output low	
DBQL[2:0]	Determines startup sequencing from the CMI code	Changing this bit may result in unexpected IC behavior.
DBOK[2:0]	Determines startup sequencing from the CMI code	Changing this bit may result in unexpected IC behavior.

0xA9 – BUCK4 Configuration Register

Address = 0xA9h		Default = 0x53h			Type = Basic Non-Volatile			
BIT	7	6	5	4	3	2	1	0
Name	ILIM_STDN_DIS	ON_DELAY[2:0]			OFF_DELAY[3:0]			
Default	0	101			0011			
Access	R/W	R/W			R/W			

Name	Description	Notes
ILIM_STDN_DIS	Disable ILIM Shutdown 1: Mask ILIM SHUT signal 0: Unmask ILIM_SHUT signal	
ON_DELAY[2:0]	000 = 0ms 001 = 0.25ms 010 = 0.5m 011 = 1ms 100 = 2ms 101 = 4ms 110 = 8m 111 = 16ms	Programs the delay time between the Buck4 input trigger and when it turns on.
OFF_DELAY[3:0]	Sets the delay time between the Buck4 disable input to when it turns off.	Buck4 turnoff delay time is equal to OFF_DELAY * 1ms

0xAA – BUCK4 Configuration Register

Address = 0xAAh	Default = 0x80h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	ILIM[1:0]		VINUVOV_REG_SHUT_MASK	VINUVOV_SYS_SHUT_MASK	UVOV_REG_SHUT_MASK	UVOV_SYS_SHUT_MASK	DB_DVS[1:0]	
Default	10		0	0	0	0	00	
Access	R/W		R/W	R/W	R/W	R/W	R/W	

Name	Description	Notes
ILIM[1:0]	00: IPEAK=4A, IVALLEY=3A 01: IPEAK=5A, IVALLEY=4A 10: IPEAK=6A, IVALLEY=5A 11: IPEAK=7A, IVALLEY=6A	
VINUVOV_REG_SHUT_MASK	When this bit =0, Buck4 will shutdown if VIN_Buck4 occurs UV/OV.	
VINUVOV_SYS_SHUT_MASK	When this bit =0, system will shutdown if VIN_Buck4 occurs UV/OV.	
UVOV_REG_SHUT_MASK	When this bit =0, Buck4 will shutdown if Buck4_OUT occurs UV/OV.	
UVOV_SYS_SHUT_MASK	When this bit =0, system will shutdown if Buck4_OUT occurs UV/OV.	
DB_DVS[1:0]	Determines DVS setting from the CMI code	Changing this bit may result in unexpected IC behavior.

0xAB – BUCK4 Configuration Register

Address = 0xABh			Default = 0xD3h			Type = Basic Non-Volatile		
BIT	7	6	5	4	3	2	1	0
Name	SOFT_LSON	DISBBM_L2H	RFU	POK_OPT	ENHS_Status_HI	HSD_SLEW	LSD_SLEW[1:0]	
Default	1	1	0	1	0	0	11	
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	

Name	Description	Notes
SOFT_LSON	Enable Weak Turn-on LSON 0: Disable 1: Enable	
DISBBM_L2H	Enable Smooth Gate Driver 0: Simple BBM Gate Driver 1: Enable	
RFU	Reserved for future use	
POK_OPT	0: Rising/Falling (87%/84% of VOUT) 1: Rising/Falling (90%/87% of VOUT)	
ENHS_Status_HI	0: HS_Status depend on the circuit working 1: Force the HS_Status signal to high	
HSD_SLEW	Adjust Slew Rate High-Side 0: Slow 1: High	
LSD_SLEW[1:0]	Adjust Slew Rate Low-Side 00: Weak 01: Slow 10: Normal 11: Fast	

0xAC – BUCK4 Configuration Register

Address = 0xACh		Default = 0x02h			Type = Basic Non-Volatile			
BIT	7	6	5	4	3	2	1	0
Name	DBOK_SEL	EN_LPM	FORCE_PWM	VOUT_OPT	FREQ[3:0]			
Default	0	0	0	0	0010			
Access	R/W	R/W	R/W	R/W	R/W			

Name	Description	Notes
DBOK_SEL	Determines startup sequencing from the CMI code	Changing this bit may result in unexpected IC behavior
EN_LPM	Enable Low-Power Mode 0: Disable (Works with DCM & CCM) 1: Enable	
FORCE_PWM	0: Not Force PWM Mode 1: Force PWM Mode	
VOUT_OPT	0 = 20mV steps 1 = 5mV steps	Select VOUT Range 0: 0.6V --> 5.25V 1: 0.6V --> - 1.875V
FREQ[3:0]	0000: 400kHz 1111: 1.9MHz Step: 100kHz	Select Frequency Switching

BUCK_BOOST REGISTERS

0xC0 – BUCK_BOOST Configuration Register

Address = 0xC0h		Default = 0x00h		Type = Basic Volatile			
BIT	7	6	5	4	3	2	1	0
Name	POK	VOUT_OV_FLT	RFU	ILIM_SHUT	RFU	ILIM_WARN	VIN_OV	VIN_UV
Default	0	0	0	0	0	0	0	0
Access	RO	RO	RO	RO	RO	RO	RO	RO

Name	Description	Notes
POK	1: VOUT OK 0: VOUT NOT OK	Provides real-time power good status
VOUT_OV_FLT	OV Status. 1: VOUT > VOUT OV (112%/109%) 0: VOUT < VOUT OV	When VOUT > OV, this bit goes high. It stays high until VOUT < OV and it is read.
RFU	Reserved for future use	
ILIM_SHUT	ILIM Shutdown Status. 1: Output Ilim Shutdown is triggered 0: Output Ilim Shutdown is not triggered	If the peak switch current reaches the 122.5% of ILIMSET threshold, this bit goes high. It stays high until peak switch current < 122.5% of ILIMSET and it is read.
RFU	Reserved for future use	
ILIM_WARN	ILIM Warning Status. 1: Output Ilim Warning is triggered 0: Output Ilim Warning is not triggered	If the peak switch current reaches the 80% of ILIMSET threshold, this bit goes high. It stays high until peak switch current < 80% of ILIMSET and it is read.
VIN_OV	PVIN OV Status. 1: PVIN > PVIN OV (5.8V or 15V) 0: PVIN is Normal	
VIN_UV	PVIN UV Status. 1: PVIN < PVIN UV (2.9V/2.7V) 0: PVIN is Normal	

0xC1 – BUCK_BOOST Configuration Register

Address = 0xC1h	Default = 0xD7h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	UV_INT_MSK	OV_INT_MSK	RFU	ISHUT_INT_MSK	RFU	IWRN_INT_MSK	VINOV_INT_MSK	VINUV_INT_MSK
Default	1	1	0	1	0	1	1	1
Access	R/W	R/W	RO	R/W	RO	R/W	R/W	R/W

Name	Description	Notes
UV_INT_MSK	Mask POK Interrupt 1: Mask POK Interrupt 0: Unmask POK Interrupt	When 1, the Buck-boost POK signal does not go to the master controller. This prevents Buck-boost from asserting the nIRQ pin when it is disabled or drops out of regulation. Buck-boost POK still provides real-time power good status.
OV_INT_MSK	Mask VOUT_OV Interrupt 1: Mask VOUT_OV Interrupt 0: Unmask VOUT_OV Interrupt	When 1, the Buck-boost OV signal does not go to the master controller. This prevents Buck-boost from asserting the nIRQ pin when it is above regulation limits. VOUT_OV_FLT still provides OV status.
RFU	Reserved for future use	
ISHUT_INT_MSK	Mask ILIM SHUTDOWN Interrupt 1: Mask ILIM SHUTDOWN Interrupt 0: Unmask ILIM SHUTDOWN Interrupt	When 1, the Buck-boost ILIM shutdown signal does not go to the master controller. ILIM_SHUT still provides current limit status.
RFU	Reserved for future use	
IWRN_INT_MSK	Mask ILIM WARM Interrupt 1: Mask ILIM WARM Interrupt 0: Unmask ILIM WARM Interrupt	When 1, the Buck-boost ILIM warn signal does not go to the master controller. ILIM_WARN still provides current limit warning status.
VINOV_INT_MSK	Mask PVIN_OV Interrupt 0: Unmask PVIN_OV Interrupt 1: Mask PVIN_OV Interrupt	
VINUV_INT_MSK	Mask PVIN_UV Interrupt 0: Unmask PVIN_UV Interrupt 1: Mask PVIN_UV Interrupt	

0xC5 – BUCK_BOOST Configuration Register

Address = 0xC5h		Default = 0x30h				Type = Basic Non-Volatile		
BIT	7	6	5	4	3	2	1	0
Name	DBOK_SEL	VSET0[6:0]						
Default	0	0110000						
Access	R/W	R/W						

Name	Description	Notes
DBOK_SEL	DBOK are selected from POK or TILE ON 0: Selected from POK 1: Selected from TILE ON	
VSET0[6:0]	Buck-boost output voltage setting in ACTIVE mode.	Buck-boost mode: VOUT = 9.6V + VSET0[6:0] * 0.05V. Only buck mode: VOUT = 1V + VSET0[6:0] * 0.025V.

0xC6 – BUCK_BOOST Configuration Register

Address = 0xC6h		Default = 0x30h			Type = Basic Non-Volatile			
BIT	7	6	5	4	3	2	1	0
Name	EN_PLDN	VSET1[6:0]						
Default	0	0110000						
Access	R/W	R/W						

Name	Description	Notes
EN_PLDN	Enable resistor pulldown function when buck-boost is off 0: Disable 1: Enable	
VSET1[6:0]	Buck-boost output voltage setting in ACTIVE mode.	Buck-boost mode: VOUT = 9.6V + VSET1[6:0] * 0.05V. Only buck mode: VOUT = 1V + VSET1[6:0] * 0.025V.

0xC7 – BUCK_BOOST Configuration Register

Address = 0xC7h			Default = 0x0Bh		Type = Basic Non-Volatile			
BIT	7	6	5	4	3	2	1	0
Name	DBON[3:0]				ON	QLTCH	SLEEP EN	DP SLEEP EN
Default	0000				1	0	1	1
Access	R/W				R/W	R/W	R/W	R/W

Name	Description	Notes
DBON[3:0]	Determines startup sequencing from the CMI code	Do not change this
ON	0 – Buck-boost is enabled through normal sequencing 1 – Buck-boost is enabled via I2C that bypasses normal sequencing	
QLTCH	0 – Buck-boost shuts down when its sequenced input shuts down 1 – Buck-boost stays on when its sequenced input shuts down	
SLEEP EN	0 – Buck-boost stays on when the IC enters Sleep mode 1 – Buck-boost turns off when the IC enters Sleep mode	
DP SLEEP EN	0 – Buck-boost stays on when the IC enters Deep Sleep mode 1 – Buck-boost turns off when the IC enters Deep Sleep mode	

0xC8 – BUCK_BOOST Configuration Register

Address = 0xC8h			Default = 0x10h			Type = Basic Non-Volatile		
BIT	7	6	5	4	3	2	1	0
Name	VOOV_MSK	RST	DBQL[2:0]			DBOK[2:0]		
Default	0	0	010			000		
Access	R/W	R/W	R/W			R/W		

Name	Description	Notes
VOOV_MSK	0: Mask output OV fault 1: UnMask output OV fault	
RST	0 – Buck-boost does not affect nRESET output 1 – Buck-boost turning off asserts nRESET output low	
DBQL[2:0]	Determines startup sequencing from the CMI code	Changing this bit may result in unexpected IC behavior.
DBOK[2:0]	Determines startup sequencing from the CMI code	Changing this bit may result in unexpected IC behavior.

0xC9 – BUCK_BOOST Configuration Register

Address = 0xC9h		Default = 0x60h			Type = Basic Non-Volatile			
BIT	7	6	5	4	3	2	1	0
Name	ILIM_STDN_DIS	ON_DELAY[2:0]			OFF_DLY[3:0]			
Default	0	110			0000			
Access	R/W	R/W			R/W			

Name	Description	Notes
ILIM_STDN_DIS	Disable ILIM Shutdown 0: Unmask ILIM_SHUT signal 1: Mask ILIM SHUT signal	
ON_DELAY[2:0]	000 = 0ms 001 = 0.25ms 010 = 0.5m 011 = 1ms 100 = 2ms 101 = 4ms 110 = 8m 111 = 16ms	Programs the delay time between the Buck-boost input trigger and when it turns on.
OFF_DLY[3:0]	Sets the delay time between the Buck-boost disable input to when it turns off.	Buck-boost turnoff delay time is equal to OFF_DLY * 1ms

0xCA – BUCK_BOOST Configuration Register

Address = 0xCAh			Default = 0xC0h			Type = Basic Non-Volatile		
BIT	7	6	5	4	3	2	1	0
Name	OV Pull Down	RFU	VINUVOV_REG_SHUT_MASK	VINUVOV_SYS_SHUT_MASK	UVOV_REG_SHUT_MASK	UVOV_SYS_SHUT_MASK	RFU	RFU
Default	1	1	0	0	0	0	0	0
Access	R/W	RO	R/W	R/W	R/W	R/W	RO	RO

Name	Description	Notes
OV Pull Down	Enable 50mA pull down at VOUT when VOU_OV happen.	
RFU	Reserved for future use	Changing this bit may result in unexpected IC behavior.
VINUVOV_REG_SHUT_MASK	Buck-boost PVIN Monitor and Response.	
VINUVOV_SYS_SHUT_MASK		
UVOV_REG_SHUT_MASK	Buck-boost VOUT Monitor and Response.	
UVOV_SYS_SHUT_MASK		
RFU	Reserved for future use	Changing this bit may result in unexpected IC behavior.
RFU	Reserved for future use	Changing this bit may result in unexpected IC behavior.

Referenced Documents

The reference documents below take precedence over the contents of this application note and should always be consulted for the latest information.

ACT86600 Preliminary Data Sheet

Contact Information

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