PAC25140 EVK User Manual

***Power Application Controller*® Battery Management**

Introduction

Qorvo's PAC25140EVK development platform is a complete hardware solution enabling users not only to evaluate the PAC25140 device, but also develop battery management solution revolving around this powerful and versatile ARM® Cortex®-M4 based microcontroller. The module contains a PAC25140 Power Application Controller® (MCU) and all the necessary circuitry to properly energize the MCU and its internal peripherals once power is applied.

To aid in the application development the PAC25140EVK offers access to every one of the PAC25140 device's signals by means of a series of male header connectors.

The PAC25140EVK also contains access to an external USB to UART module enabling users to connect the evaluation module to a PC computer through a conventional Virtual Comm Port which can then be used in the communication efforts by taking advantage of the PAC25140's UART interface. Graphical User Interface (GUI) software suites can be employed to externally control application's features.

Finally, the PAC25140EVK module gives access to the PAC25140's SWD port allowing users to both program the application into the device's FLASH memory, as well as debugging the application in real time. The provided 4 pin connector is compatible with a decent variety of SWD based debugger/programmer modules, widely available. See PAC25140 BMS Getting Started Guide for additional information.

Qorvo's PAC25140EVK evaluation kit consists of the following:

- PAC25140EVK hardware module
- PAC25140EVK User's Manual
- Schematics, BOM and Layout Drawings

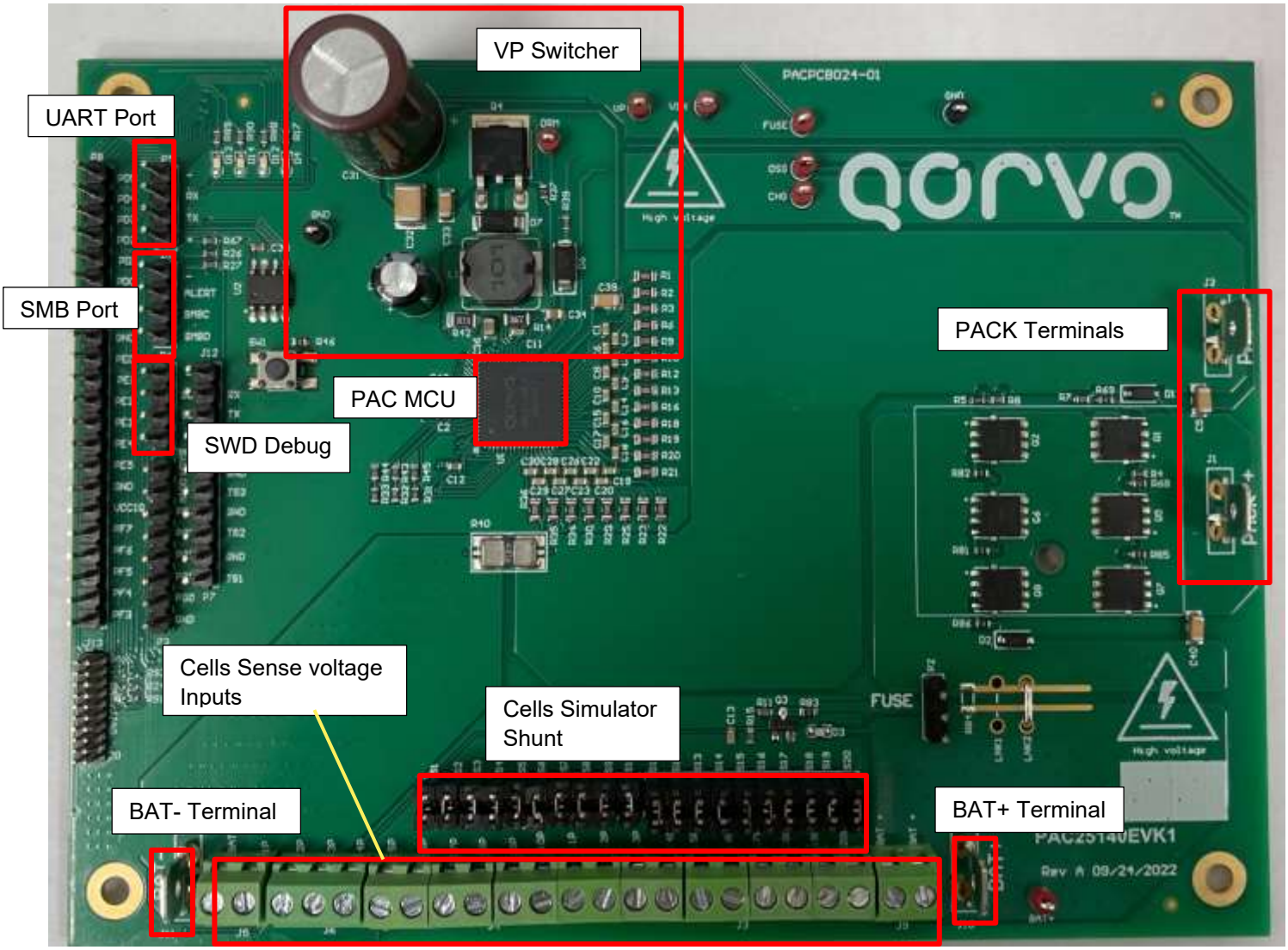

Figure 1: PAC25140EVK Block Diagram

Solution Benefits:

- The Qorvo® PAC25140 is a Smart Battery Monitoring System (BMS) that can monitor 10-series to 20-series Li-Ion, Li-Polymer and LiFePO4 battery packs.
- There is a single supply 145V input Buck DC/DC controller, used to generate gate drive voltages for external charge and discharge FETs and external FUSE FET, as well as all the sub-regulators required for the MCU and other sub-systems. There are high-side gate drivers for a charge and discharge FET, as well as a low-side driver to blow a battery pack fuse.
- Single-IC PAC25140 with configurable PWM outputs, ADC inputs, SMB/I2C, UART, SPI communication ports and GPIO.
- Resistor cell simulator for quick setup with only a power supply.
- Schematics, BOM, Layout drawings available

The following sections provide information about the hardware features of Qorvo's PAC25140EVK turnkey solution.

PAC25140AEVK Resources

Pinout and Signal Connectivity

The following diagram shows the male header pinout for the PAC25140EVK evaluation module, as seen from above:

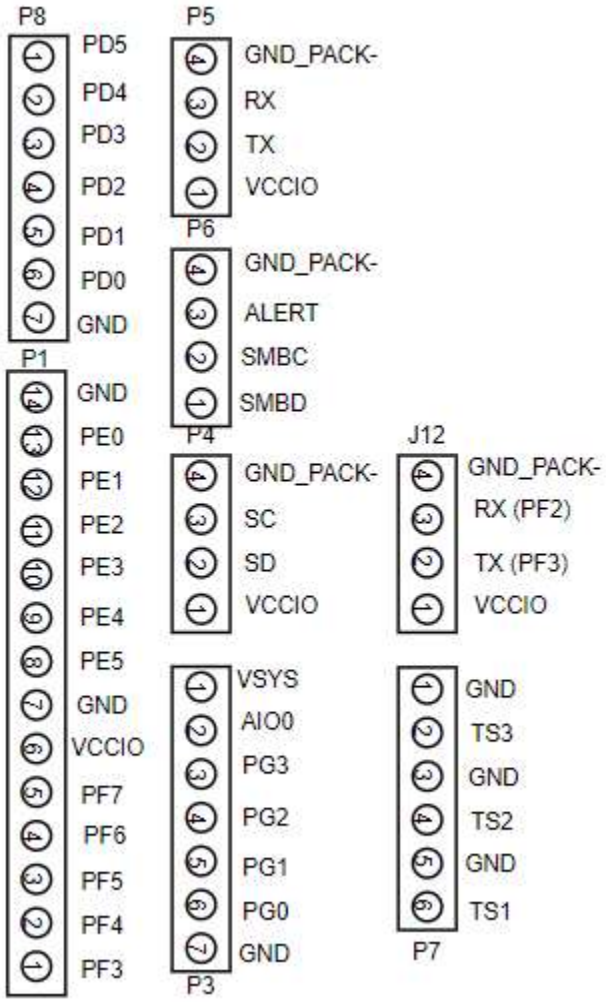

Figure 2: PAC25140AEVK Headers and Test Stakes Pinout

Power Input

Power to the PAC25140EVK evaluation module can be applied to the BAT+ and BAT- spade connectors. Power to the PAC25140EVK evaluation module should not exceed 145V (Abs Max).

The PAC25140EVK is optimized to operate with voltages ranging from 19V to 90V Nominal (100V Abs Max FETs). When the VIN input voltage goes above 19V, the system exits UVLO protection and all subsystems, including voltage regulators, analog front end and microcontroller, are enabled.

LED's

When an operational voltage is applied, LED D4 will light up. This is the LED which notifies VSYS (5V) rail is up and running. VP (12V gate drive), 3.3V (for analog circuitry) and 1.8V (for CPU core) regulators will also be operating at this point in time. Module is ready for use.

The following table shows the available LEDs and their associated diagnostic function.

LED	Description
D4	VSYS (5V). Light up when the PAC25140 device is successfully powered up by VIN.
D12, D13, D14	They are used for spare indicator in particular application or debugging.

SWD Debugging

Connector P4 offers access to the PAC25140 SWD port lines.

P4 Pin	Terminal	Description
1	+	VCCIO (3.3V)
2	SD	SWD Serial Data
3	CL	SWD Serial Clock
4	-	GND of PACK side (PACK-)

Serial Communications

Connector P5 offers access to the PAC25140 UART port lines.

P5 Pin	Terminal	Description
1	+	VCCIO (3.3V)
2	TX	MCU Transmit Line (PE3)
3	RX	MCU Receive Line (PE2)

4	-	GND of PACK side (PACK-)

Spare Serial Communications

Connector J12 offers access to the PAC25140 spare UART port lines.

P5 Pin	Terminal	Description
1	+	VCCIO (3.3V)
2	TX	MCU Transmit Line (PF3)
3	RX	MCU Receive Line (PF2)
4	-	GND of PACK side (PACK-)

SMB/I2C Communications

When enabled, connector P6 provides access to SMBUS port lines.

P6 Pin	Terminal	Description
1	SMBD	SMBDAT Line (PE5)
2	SMBC	SMBCLK Line (PE4)
3	ALERT	Optional interrupt signal (PE0)
4	-	GND of PACK side (PACK-)

NTC Thermistor Option

Connector P7 offers access to the PAC25140 resources on PORTF utilized for temperature sensor using MCU's ADC inputs. Each temperature sensor input includes TS and GND (System ground). However, the PAC25140EVK uses three 10k resistor instead of NTC resistors as default. In order to use NTC for temperature sensor, remove R43, R44, R45 resistors and connect NTC resistors at P7 port.

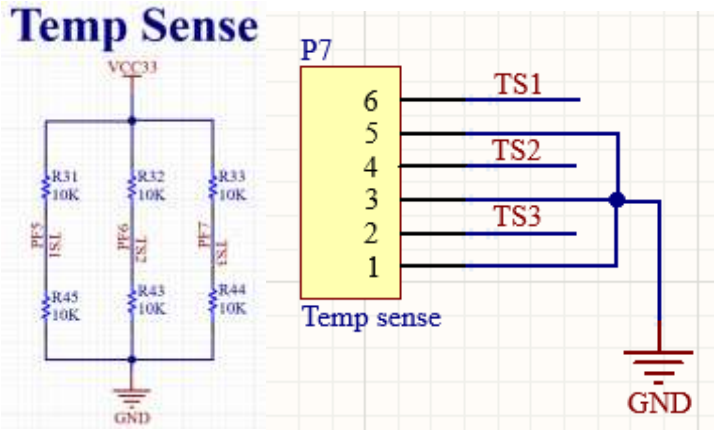

Figure 3: ADC Inputs for Temperature sensor

P7 Pin	Terminal	Description
1, 3, 5	GND	System Ground
2	TS3	Thermistor terminal TS3 (PF7)
4	TS2	Thermistor terminal TS2 (PF6)
6	TS1	Thermistor terminal TS1 (PF5)

PAC25140EVK SETUP

The PAC25140EVK contains the PAC25140 device and related circuitry to demonstrate IC features. The high current path is provided by three surface mount FETs and other components for IC support, connections to the board and cell simulator.

Cell Simulator

The PAC25140EVK is designed as a simple way to evaluate the PAC25140 IC features with minimized power equipment. Cell simulation can be achieved through the provided resistive load, resembling a battery pack with all equilibrium cells, when voltage is applied by an external power supply source at the BAT+ and BAT- terminals. The Cell Simulator is formed by a series resistor bank of 200R-1% resistors. The resistor network's tabs are connected to each respective cell input, VBx, through cell balancing resistor using shunts on the J7 and J8 headers. The shunts are labeled from S1 to S20 corresponding to VB1 to VB20. BAT- spade tab is always connected to the resistor divider network. Installing a shunt on the top cell location connects the top cell input to the resistor divider to provide simulated voltages for the other cell inputs. If the shunt is not installed on the top cell position of the header, all lower inputs are pulled to system Ground or VSS of IC.

Cell Count Selection

The Qorvo PAC25140 is a Smart Battery Monitoring System that can monitor a 10-series to 20 series battery pack. In the actual application, the number of used cells may be less than 20 cells. PAC25140EVK cell count can be configured by using the selection resistor which connects the corresponding top cell to the BAT+ connector. The bottom resistors from R70 to R80 are used to connect VB20 to VB10 respectively or may be shorted directly by wire and screw connectors J3, J4, J9. When using less than 20 cells, the unused cells corresponding VBx pins should be shorted together. An example of a 16 cells battery pack is shown below.

BAT+ Connector

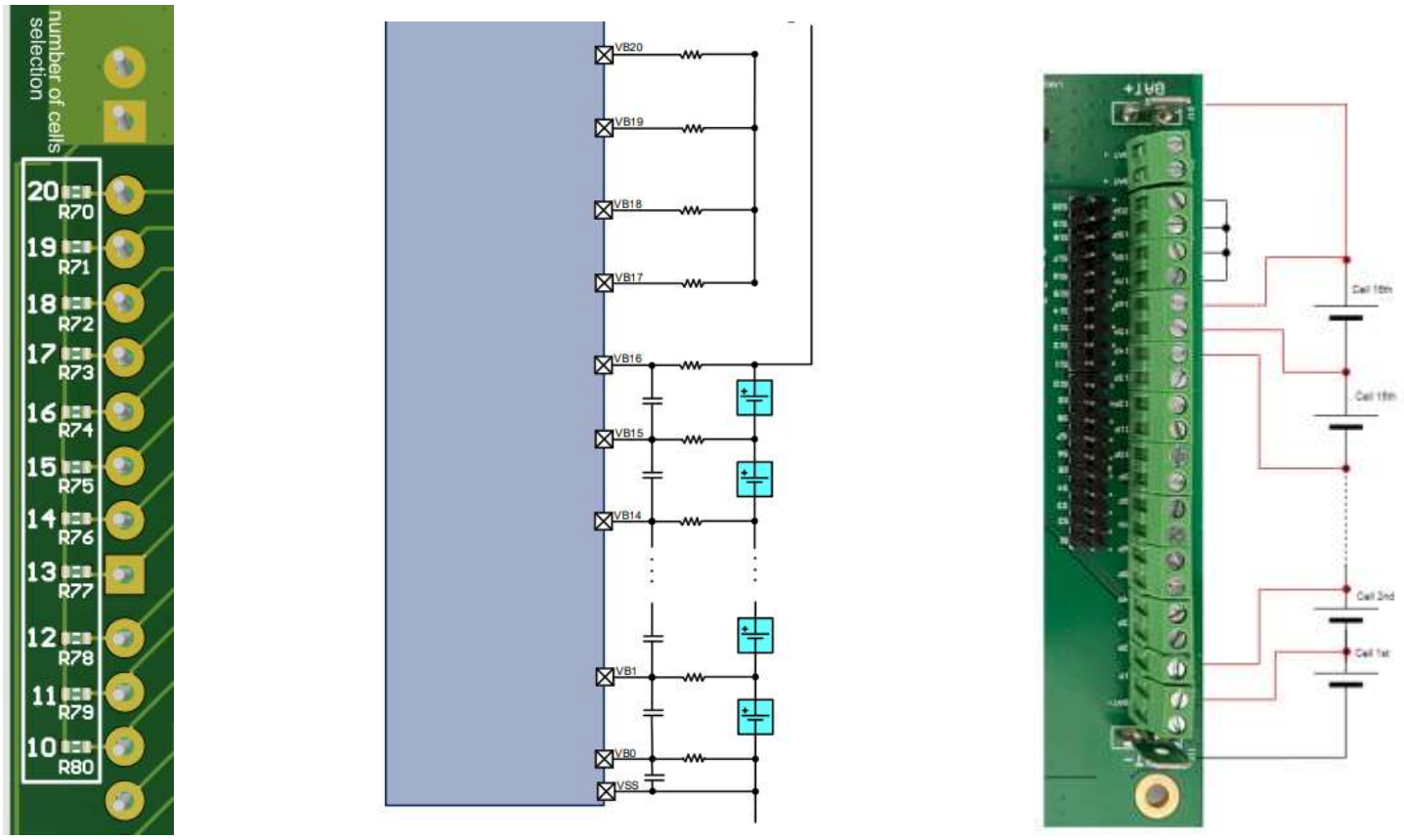

Figure 4: Cell Count Connection guide

PAC25140EVK Setup for Evaluating with Load current

The setup for the PAC25140EVK evaluation module with load current requires the following connections:

1. Install cell simulator shunts on J7, J8 headers. Please follow the *Cell Count Selection* section to configure battery pack accordingly.
2. Connect the VBAT power source via spade tab connectors BAT+ and BAT-. As VBAT power is applied, the LED D4 will light up. Once VBAT voltage goes above 19V, the PAC25140's Power Manager will be engaged and the VSYS (5V) regulator will be enabled. This event will result in LED D4 lighting up.
3. If Serial Communications are desired, connect the USB to UART module's 4 pin connection to P5.
4. For debugging/programming, connect a suitable USB SWD module to P4 by using a standard 4 wire cable.
5. With the configured PAC25140 and the FETs enabled, discharge current can be demonstrated by adding suitable resistor, or DC load, at PACK terminals as shown in Figure 5

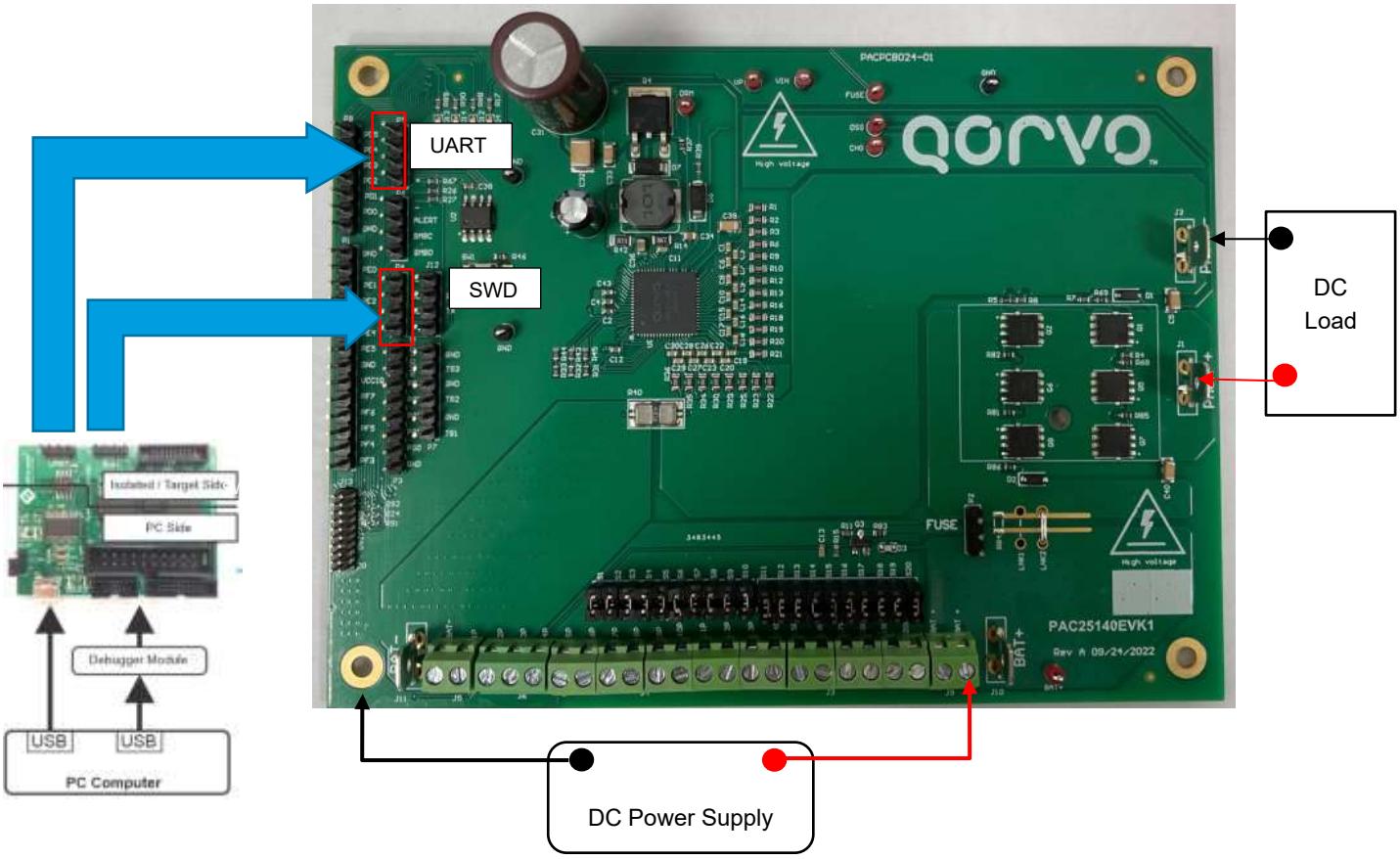

Figure 5: Evaluate PAC25140EVK with Load Current

PAC25140EVK Setup for Evaluating Charge and Discharge Currents

To evaluate the Charge and Discharge, PAC25140EVK can be setup by using bipolar power supplies which feature current sink and source capabilities. If the bipolar supplies are available, they can be used for both BAT and PACK side without re-connecting the equipment.

1. Install cell simulator shunts on J7, J8 headers and configure bipolar supplies appropriately to prevent exceeding the rate of EVK. Please follow the *Cell Count Selection* section to configure battery pack accordingly.
2. Connect the VBAT bipolar power supply via spade tab connectors BAT+ and BAT-. As VBAT power is applied, once VBAT voltage goes above 19V, the PAC25140's Power Manager will be engaged and the VSYS (5V) regulator will be enabled. This event will result in LED D4 lighting up.
3. If Serial Communications are desired, connect the USB to UART module's 4 pin connections to P5.
4. For debugging/programming, connect a suitable USB SWD module to P4 by using a standard 4 wire cable.
5. Connect PACK side with bipolar supply via PACK+ and PACK- spade connectors.
6. With the configured PAC25140EVK and the FETs enabled, discharge and charge current can be demonstrated by adjusting the bipolar power supplies.

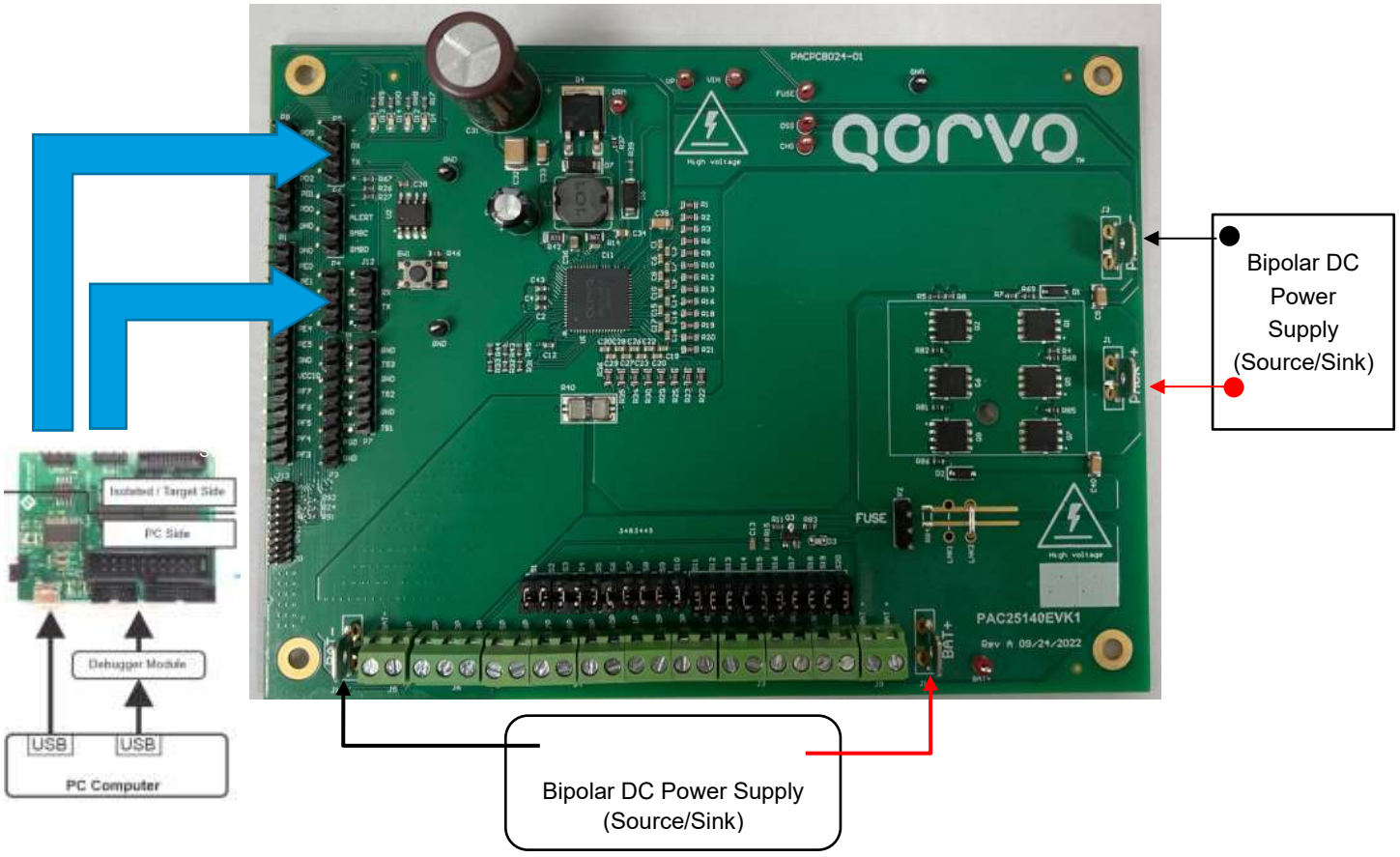

Figure 6: PAC25140EVK with Dual Sink Source Supply Evaluation

PAC25140EVK Setup for Connecting Cells

To evaluate the PAC25140 with real battery cells stack, please follow the *Cell Count Selection* section to connect wires accordingly. The top and bottom of the cell stack are connected to BAT+ and BAT- spade tab connector, cells voltage are connected by corresponding screw terminal connectors. Although the PAC25140EVK has designed with low side drive protection fuse, the short link components are installed to allow easy evaluation without the concern of activating the Fuse Blow. In quick evaluation, use a fuse in the current path of cell stack as an option.

1. Remove cell simulator shunts to avoid draining cells. Connect unused cells VBx together as detailed within the *Cell Count Selection* section.
2. Connect BAT- to bottom cell stack. BAT- is the VSS of PAC25140 IC.
3. Connect cells from bottom up: Cell#1, Cell#2, Cell#3…to Cell# top.
4. As VBAT power is applied, once VBAT voltage goes above 19V, the PAC25140's Power Manager will be engaged and the VSYS (5V) regulator will be enabled. This event will result in LED D4 lighting up.
5. If Serial Communications are desired, connect the USB to UART module's 4 pin connections to P5.
6. For debugging/programming, connect a suitable USB SWD module to P4 by using a standard 4 wire cable.
7. Connect PACK side with bipolar supply via PACK+ and PACK- spade connectors and turn it on as appropriately setting.

Figure 7: Evaluate PAC25140EVK with Cells Stack

Contact Information

For the latest specifications, additional product information, worldwide sales and distribution locations:

Web: www.qorvo.com

Tel: 1-844-890-8163

Email: customer.support@qorvo.com

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