United Silicon Carbide, Inc.

AEC-Q101 Product Qualification Report

Discrete TO Packaged SiC Cascodes

Included Products:

TO-247-3L	TO-220-3L	TO-247-4L
UJ3C120150K3S	UJ3C065080T3S	UF3C120150K4S
UJ3C120080K3S	UF3C065040T3S	UF3C120080K4S
UJ3C120070K3S	UJ3C065030T3S	UJ3C120070K4S
UJ3C120040K3S	UF3C065080T3S	UF3C120040K4S
UJ3C065080K3S	UF3C065030T3S	UF3C065080K4S
UF3C065040K3S		UF3C065040K4S
UJ3C065030K3S		UF3C065030K4S
UF3C065080K3S		
UF3C065030K3S		
UF3C120080K3S		
UF3C120040K4S		
UF3C170400K3S		
UF3C120400K3S		

Scope

This report summarizes the AEC-Q101 qualification results for the UJ3C and UF3C family of discrete SiC Cascodes in TO-220-3L, TO-247-3L and TO-247-4L plastic packages.

The environmental stress tests listed below are performed with pre-stress and post-stress electrical tests. Reviewing the electrical results for new failures and any significant shift performance satisfies the AEC-Q101 qualification standards, as well as UnitedSiC Quality requirements.

Reliability Stress Test Summary

Test Name	Test Standard	# Samples x # Lots	Failures
High Temperature Reverse Bias (HTRB)	MIL-STD-750-1 M1038 Method A (**1000 Hours**) T_J=175°C, V=80% V_{max}	77x10 lots	0/770
High Temperature Reverse Bias (HTRB)	MIL-STD-750-1 M1038 Method A (**500 Hours**) T_J=175°C, V=100% V_{max}	77x3 lots	0/231
High Temperature Reverse Bias (HTRB)	MIL-STD-750-1 M1038 Method A (**168Hours**) T_J=175°C, V=80% V_{max}	77x4 lots	0/308
High Temperature Gate Bias (HTGB)	JESD22 A-108 (1000 Hours) T_J=175°C, V=100% V_{max} (+25V), bias in on direction	77x10 lots	0/770
Highly Accelerated Stress Test (HAST)	JESD22 A-110 (96 Hours) T_A=130°C/85%RH	77x8 lots	0/616
High Humidity, High Temperature, Reverse Bias	JESD22 A-110 (1000 Hours) T= 85°C, 85% RH, V_{GS}=0V, V_{DS}=100V	77x3 lots	0/231
Intermittent Operating Life	MIL-STD-750 Method 1037	77x10 lots	0/770

(IOL)	DT$_J$ ≥125°C, 3000 cycles (5 minutes on/ 5 minutes off)		
Temperature Cycle (TC)	JESD22 A-104 (1000 Cycles)	77x10 lots	0/770
Autoclave (PCT)	JESD22 A-102 121°C/ RH = 100%, 96 hours, 15psig	77x10 lots	0/770
Parametric Verification	Per Datasheet	100% FT x 9 lots	
Physical Dimensions	Per AEC-Q101 Rev D	30x3 packages	0/90
ESD – Charged Device Model	AEC-Q101-005 Field Induced Charged-Device Model, 3 positive and 3 negative pulses applied to All Pins	10x2 lots	0/20
ESD – Human Body Model	AEC-Q101-001 Human Body Model: R=1500 ohm, C=100 pf, 3 positive and 3 negative pulses applied to All Pins	10x2 lots	0/20
Bondline Thickness	Per Assembly Spec	10x6 lots	0/60
Die Shear	Per Assembly Spec	10x6 lots	0/60
Die Attach Voids	Per Assembly Spec	10x6 lots	0/60
Wire Pull	Per Assembly Spec	10x6 lots	0/60
Wedge Shear	Per Assembly Spec	10x6 lots	0/60
CSAM	Per Assembly Spec	60x6 lots	0/360
Lead Integrity Test	Per AEC-Q101 Rev D	30x2 lots	0/60
Solderability Test	Per AEC-Q101 Rev D	10x2 lots	0/20

ESD Testing:

UnitedSiC FETs have integrated ESD protection. The ESD protection will vary with the chip size. All products will meet a minimum rating of C3 (>1000V) for the Charged Device Model, and H2 (>2000V and <4000V) for the Human Body Model.

Reliability Evaluation:

The FIT rate data presented below is determined according to JEDEC Standard JESD 85 and is determined from the HTRB and HTGB Burn-In sample size.

FIT = 0.75697 failures per billion device hours

MTTF = 150,805.79 years

From the equations:

$$\lambda_{hours} = \frac{X^2(\alpha, \nu)}{2 \times D \times H \times A_f}$$

$$FIT = \lambda_{hours} \times 10^9$$

$$MTTF_{hours} = 1/\lambda_{hours}$$

And

$$A_f = e^{\frac{E_a}{k}\left(\frac{1}{T_{use}} - \frac{1}{T_{test}}\right)}$$

Where:

X^2 = Chi-Squared probability function for a given Confidence Level (α) and Degree of Freedom ($\nu = 2r+2$, where r = the number of failures in the Test Population),

D = Number of Devices in the Test Population,

H = Test Hours per Device,

A_f = Acceleration Factor from the Arrhenius equation,

E_a = Activation Energy (eV),

T_{use} = standardized Use Temperature,

T_{test} = Temperature of Stress Test, and

k = Boltzmann's Constant.

In our calculations, we used our HTRB and HTGB Burn-In data:

D = 770 devices for HTRB (1000H), 308 devices for HTRB (168H), and 770 for HTGB,

H = 1000 hours or 168 hours for HTRB and 1000 hours for HTGB,

$1 - \alpha$ = 0.6 (60% Confidence Level)

r = 0 Failures

E_a = 0.7 eV

T_{use} = 55 °C or 328 K

T_{test} = 175 °C or 448 K