



United Silicon Carbide, Inc.

Product Qualification Report

Discrete D2PAK-7L SiC JFETs

Products:

UF3N170400B7S



This report summarizes the AEC-Q101 qualification results for United Silicon Carbide, Inc.'s UF3N170400B7S SiC JFET in D2PAK-7L plastic package.

The environmental stress tests listed below are performed with pre-stress and post-stress electrical tests. Reviewing the electrical results for new failures and any significant shift performance satisfies the AEC-Q101 qualification requirements, as well as UnitedSiC's Quality requirements. This device was tested to MSL1 standards.

Reliability Stress Test Summary

| Test Name | MSL 1 PreCon | Test Standard | # Samples x # Lots | Failures |
|-----------------------------------------------------|--------------|--------------------------------------------------------------------------------------------------------------------|------------------------------|----------|
| MSL1 Preconditioning | | JESD22-A113D J-STD-020E | 77 pcs x 3 lots x 4 tests | 0/924 |
| High Temperature Reverse Bias (HTRB) | | JESD22 A108 (1000 Hours) $T_J=175^{\circ}\text{C}$, $V_{GD}=1360\text{V}$, Floating Source | 77pcs x 3 lots | 0/231 |
| High Temperature Gate Bias (HTGB) | | JESD22 A108 (1000 Hours) $T_J=175^{\circ}\text{C}$, $V_{GS}= -20\text{V}$, $V_{DS}= 0\text{V}$ | 77pcs x 3 lots | 0/231 |
| High Humidity High Temperature Reverse Bias (H3TRB) | Y | JESD22 A-101D (500 Hours) $T_A=85^{\circ}\text{C}/85\%\text{RH}$, $V_{GD}=100\text{V}$, Floating source | 77x3 lots | 0/231 |
| Intermittent Operating Life (IOL) | Y | MIL-STD-750 Method 1037 $DT_J \geq 125^{\circ}\text{C}$, 3000 cycles (5 minutes on/ 5 minutes off) | 77x3 lots | 0/231 |
| Temperature Cycle (TC) | Y | JESD22 A-104 (1000 Cycles) -55°C to $+150^{\circ}\text{C}$ | 77x3 lots | 0/231 |
| Autoclave (PCT) | Y | JESD22 A-102 $121^{\circ}\text{C}/\text{RH} = 100\%$, 96 hours, 15psig | 77x3 lots | 0/231 |
| Parametric Verification | | Per Datasheet | 100% FT x 3 lots | |

| | | | | |
|---------------------|--|----------------------------|---------------|-------|
| Physical Dimensions | | Per AEC-Q101 Rev D | 30x1 packages | 0/30 |
| Bondline Thickness | | Per Assembly Spec | 10x3 lots | 0/30 |
| Die Shear | | Per Assembly Spec | 10x3 lots | 0/30 |
| Die Attach Voids | | Per Assembly Spec | 10x3 lots | 0/30 |
| Wire Pull | | Per Assembly Spec | 10x3 lots | 0/30 |
| Wedge Shear | | Per Assembly Spec | 10x3 lots | 0/30 |
| CSAM | | Per Assembly Spec | 60x3lots | 0/180 |
| Lead Integrity Test | | Tested in the Cascode Qual | -- | -- |
| Solderability Test | | Tested in the Cascode Qual | -- | -- |

Reliability Evaluation:

The FIT rate data presented below is determined according to JEDEC Standard JESD 85 and is determined from the HTRB and HTGB Burn-In sample size.

FIT = 2.608 failures per billion device hours

MTTF = 43771 years

From the equations:

$$\lambda_{hours} = \frac{X^2(\alpha, \nu)}{2 \times D \times H \times A_f}$$

$$FIT = \lambda_{hours} \times 10^9$$

$$MTTF_{hours} = 1/\lambda_{hours}$$

And

$$A_f = e^{\frac{E_a}{k} \left(\frac{1}{T_{use}} - \frac{1}{T_{test}} \right)}$$

Where:



χ^2 = Chi-Squared probability function for a given Confidence Level (α) and Degree of Freedom ($\nu = 2r+2$, where r = the number of failures in the Test Population),

D = Number of Devices in the Test Population,

H = Test Hours per Device,

A_f = Acceleration Factor from the Arrhenius equation,

E_a = Activation Energy (eV),

T_{use} = standardized Use Temperature,

T_{test} = Temperature of Stress Test,

and

k = Boltzmann's Constant.

In our calculations, we used our HTGRB Burn-In data:

D = 231 devices for HTRB, and 231 devices for HTGB

H = 1000 hours for HTRB, and HTGB

$1 - \alpha = 0.6$ (60% Confidence Level)

$r = 0$ Failures

$E_a = 0.7$ eV

$T_{use} = 55$ °C or 328 K

$T_{test} = 175$ °C or 448 K