APPLICATION NOTE

PAC2x140 BMS VADC and IADC Calibration

Introduction

The Qorvo PAC2x140 is an Intelligent Battery Monitoring System (BMS) that can monitor 10-series to 20-series Lion, Li-Polymer and LiFePO4 battery packs. The device integrates for current sense a programmable-gain differential amplifier along with a 16-bit Sigma-Delta ADC for current sense additionally the device has a 16-bit Sigma-Delta ADC for voltage sense. The PAC2x140 BMS devices require calibration to achieve the best performance.

This application note goes through in detail the calibration methods used for the PAC22140 and PAC25140.

Reference

- PAC22140, 10s-20s Intelligent BMS with Integrated ARM Cortex M0 MCU and Cell Balancing, Product Documents.
- PAC25140, 10s-20s Intelligent BMS with Integrated ARM Cortex M4F MCU and Cell Balancing, Product Documents.

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1. Offset Error and Gain Error

The ADCs discussed in this application note are the current ADC, IADC and voltage sensing, VADC for voltage sensing of the individual cells via MUX. These ADCs has the offset error and gain error as internal error. In order to correct these errors, the PAC2x140 device includes the calibration performed during factory testing and the calibration factors are stored in the INFO FLASH memory, please refer to PAC2x140 datasheet and user guide for more detail about the INFO FLASH memory description.

ADC Offset error is defined as the deviation between the first ideal code transition and the first actual code transition. The first ideal code transition takes place at 0.5 LSB. Both positive and negative offset errors limit the available range of the ADC. A large positive offset error causes the ADC to saturate before the input voltage reaches maximum. A large negative offset error results in zero ADC output code for small input voltages.

Gain error is defined as the deviation of the midpoint of the last step of the ideal ADC transfer from the midpoint of the last step of the actual ADC, after the offset error is compensated. If the transfer function of the actual ADC results in ADC saturation before the input voltage reaches maximum, a positive gain error is produced. If the transfer function of the actual ADC is such that the ADC does not reach full-scale value when the input voltage is at maximum, a negative gain error is produced.

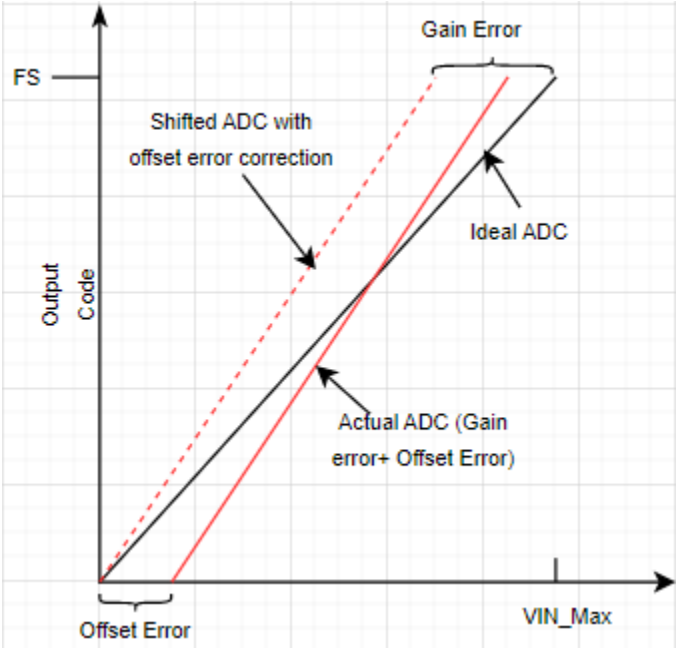

Figure 1 Gain Error, Offset Error in ADC

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2. Calibration the Offset and Errors using Two-Point Method

The two-point calibration method is used to calculate the gain and offset. Using this method is a simple method and uses the equation of a straight-line

$$y = ma * x - b \quad (1)$$

where **ma** is the actual gain of the line and **b** is the actual offset.

The calibration is performed by feeding two known reference values into ADC channel and calculating a calibration gain and offset. The two calibration points should be chosen such that one calibration point is slightly below 10% and the second calibration point is slightly above 90% of full-scale range.

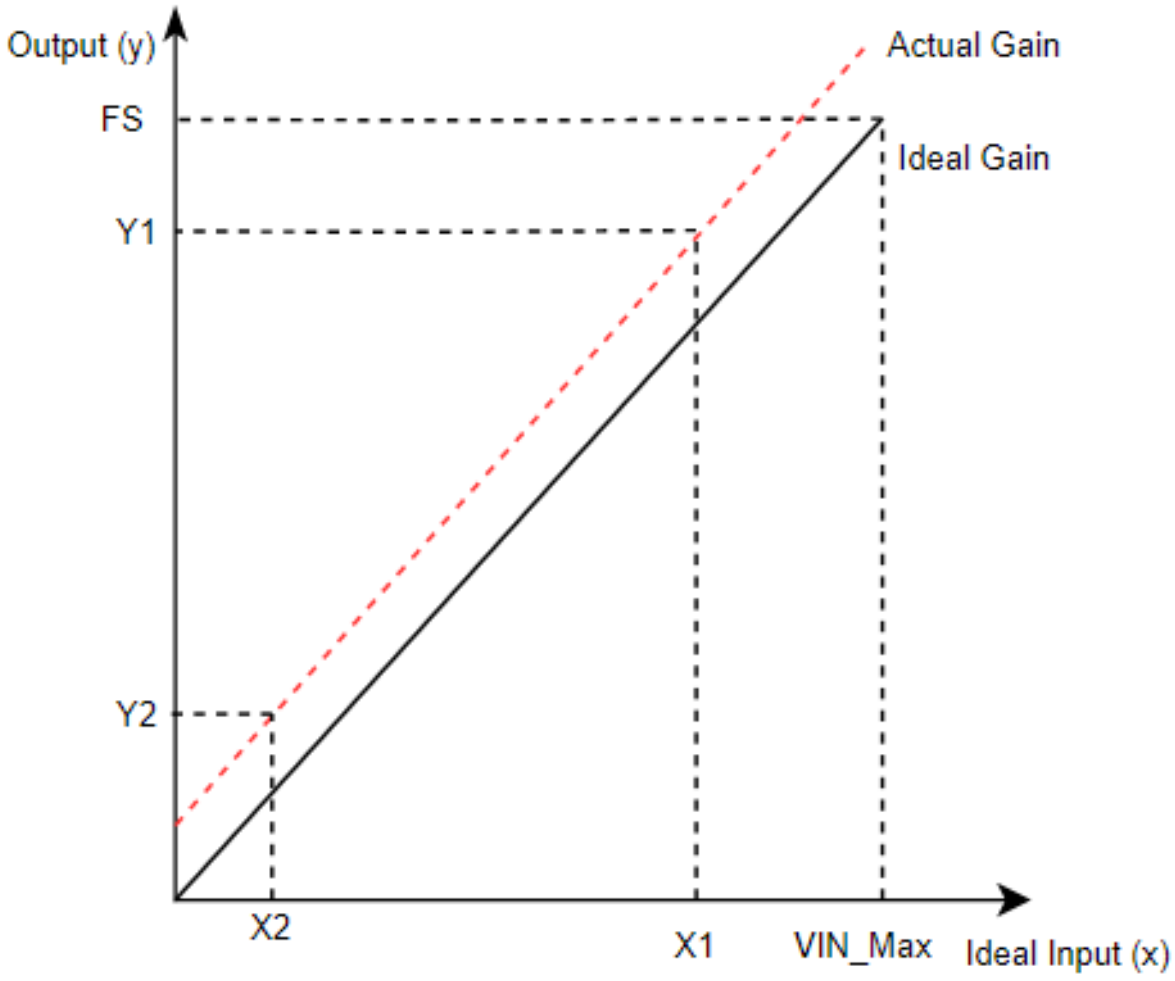

Figure 2 Actual Gain and Ideal Gain

As the Figure 2, the X_1 and X_2 are the known reference input voltages. Using an accurate voltage source apply X_1 and save actual ADC output value as Y_1 value. Similarly, apply X_2 voltage and get Y_2 ADC output value. The ADC conversation Y_1 and Y_2 should be averaged of sum conversations to archive best value.

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The actual gain **ma** is calculated by:

$$\mathrm{ma} = \frac{(Y_2 - Y1)}{(X_2 - X_1)} \quad (2)$$

Then the offset **b** is calculated by:

$$\mathrm{b} = \mathrm{ma} * \mathrm{X}_2 - \mathrm{Y}_2 \quad (3)$$

The calibration equation is derived by inverting the input and output of equation (1) describing the ADC actual gain and offset:

$$\mathrm{x} = \frac{(y+b)}{\mathrm{ma}} \quad (4)$$

$$\mathrm{x} = \frac{y}{ma} + \frac{b}{ma} \quad (5)$$

Then we get,

$$x = y * CALGAIN + CALOFFSET, \text{ where} \quad (6)$$

$$\mathrm{CALGAIN} = \frac{1}{ma} = \frac{(X_2 - X_1)}{(Y_2 - Y_1)} \quad (7)$$

$$CALOFFSET = \frac{b}{ma} = X_2 - Y_2 * CALGAIN \quad (8)$$

PAC2x140 BMS VADC and IADC Calibration

3. Error Calibration Storing on PAC2x140 BMS devices

Cell Sensing ADC Calibration Storing Format

The PAC2x140 BMS device includes the internal Gain and Offset calibration after factory testing.
The data of Gain and Offset Calibration factor of VADC are stored in the INFO-2 memory as follow table

Address	Byte Offset															
	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0x0010 0460	VB01ADCAL				VB02ADCAL				VB03ADCAL				VB04ADCAL			
0x0010 0470	VB05ADCAL				VB06ADCAL				VB07ADCAL				VB08ADCAL			
0x0010 0480	VB09ADCAL				VB10ADCAL				VB11ADCAL				VB12ADCAL			
0x0010 0490	VB13ADCAL				VB14ADCAL				VB15ADCAL				VB16ADCAL			
0x0010 04A0	VB17ADCAL				VB18ADCAL				VB19ADCAL				VB20ADCAL			
0x0010 04B0	IADCAL1X_Gain				IADCAL1X_Offset				IADCAL2X_Gain				IADCAL2X_Offset			
0x0010 04C0	IADCAL4X_Gain				IADCAL4X_Offset				IADCAL8X_Gain				IADCAL8X_Offset			
0x0010 04D0	IADCAL16X_Gain				IADCAL16X_Offset				IADCAL32X_Gain				IADCAL32X_Offset			
0x0010 04E0	IADCAL64X_Gain				IADCAL64X_Offset				IADCAL128X_Gain				IADCAL128X_Offset			

Figure 3 VADC and IADC Calibration Storing Address

The PAC2x140BMS features to measure up to 20 individual cells, each channel cell input has its Gain and Offset calibration separately. Refer to ideal VADC equation in PAC2x140 Datasheet, the ideal Offset factor in straight line function is -6.25V, the CALOFFSET of a cell channel VADC is formatted as the delta of actual CALOFFSET and ideal OFFSET equation. This delta value is scaled up by 2^{15} to improve the accuracy with a signed bit, named SCALED_DELTA.
In summary,

$$\text{OFFSET\_DELTA} = -6.25 - \text{CALOFFSET} \quad (9)$$

$$\text{SCALED\_DELTA} = \text{OFFSET\_DELTA} * 2^{15} \quad (10)$$

The CALGAIN is also scaled up and rounded to improve the accuracy.

$$SCALED\_GAIN = CALGAIN * 2^{28} \quad (11)$$

The formatted Gain and Offset Calibration are stored in a DWORD format number.

INFO-ROM Format		
INFO-ROM [31:14]	INFO-ROM [13]	INFO-ROM [12:0]
SCALED_GAIN	sign of SCALED_DELTA	SCALED_DELTA

Figure 4 VADC Calibration Store Format

PAC2x140 BMS VADC and IADC Calibration

Current Sensing IADC Calibration Storing Format

The PAC22140 contains circuitry for battery pack current sensing. The positive terminal (ISNSP) and negative terminal (ISNSN) are connected to each side of an external sense resistor. The ISNSP pin is connected to the positive terminal of a differential amplifier and the ISNSN pin is connected to the negative terminal of the amplifier. The differential amplifier has a programmable gain up to x128 with an input range of -0.3V to 0.5V.
The IADC is tested during factory testing to get the Gain and Offset Calibration respective to each DPGA gain setting. Otherwise, each a DPGA gain setting has it is a set of CALGAIN and CALOFFSET. These CALGAIN and CALOFFSET are calculated following the two-point method.
The CALGAIN is scaled up following:

$$\text{SCALED\_GAIN} = \text{CALGAIN} * 2^{(31+n)} \quad (12)$$

$$SCALED\_OFFSET = CALOFFSET * 2^{(15+n)} \quad (13)$$

$Where,$ n is corresponding to gain setting as 2^n, n is from 0 to 7 as x1 Gain to x128 Gain setting.

The SCALED_GAIN and SCALED_OFFSET are stored in two DWORD numbers separately.

PAC2x140 BMS VADC and IADC Calibration

4. How to do the System Level Gain and Offset Calibration

In a running system application, there is always external gain and offset of external circuitry and the accuracy of ADCs can be improved by repeating calibration on system level. This section describes more detail of calibration to remove error at system application level.

Cell Voltage Sensing ADC Calibration

After the PAC2x140 BMS device powers up, all need AFE registers is set as expectation and the CAFE is enabled.

- Step1: Enable VADC and select desired cell channel by AFE register
- Step2: Apply precision voltage 4.2V between VBn and VB(n-1) for X1 voltage. VBn is the positive of cell in calibration
- Step3: Run VADC conversation twice and average then store ADC reading to Y1 code.
- Step4: Apply precision voltage 3.2V between VBn and VB(n-1) for X2 voltage.
- Step5: Run VADC conversation twice and average then store ADC reading to Y2 code.
- Step6: Calculate CALGAIN= (X2-X1)/(Y2-Y1) as equation (7). It is actual CALGAIN and able to use directly if need.
- Step7: Calculate SCALED_GAIN= CALGAIN*2^{28}
- Step8: Round and put it to a dump variable.
- Step9: Calculate CALOFFSET as equation (8).
- Step10: Calculate OFFSET_DELTA= -6.25-CALOFFSET as equation (9).
- Step11: Calculate SCALED_DELTA= OFFSETDELTA*2^{15} as equation (10).
- Step12: Round the SCALED_DELTA and merge with SCALED_GAIN and save to a defined Flash memory.
- Step13: Select next Channel and repeat step1 to Step13

Hardware Connectivity

For system level calibration, the reference voltage can be created using the resistor divider as battery cell simulator. To change the reference voltages, the BATTOP-BAT is adjusted and a DMM measures the actual voltage at VBx for each calibrating step. See setup in Figure 5.

PAC2x140 BMS VADC and IADC Calibration

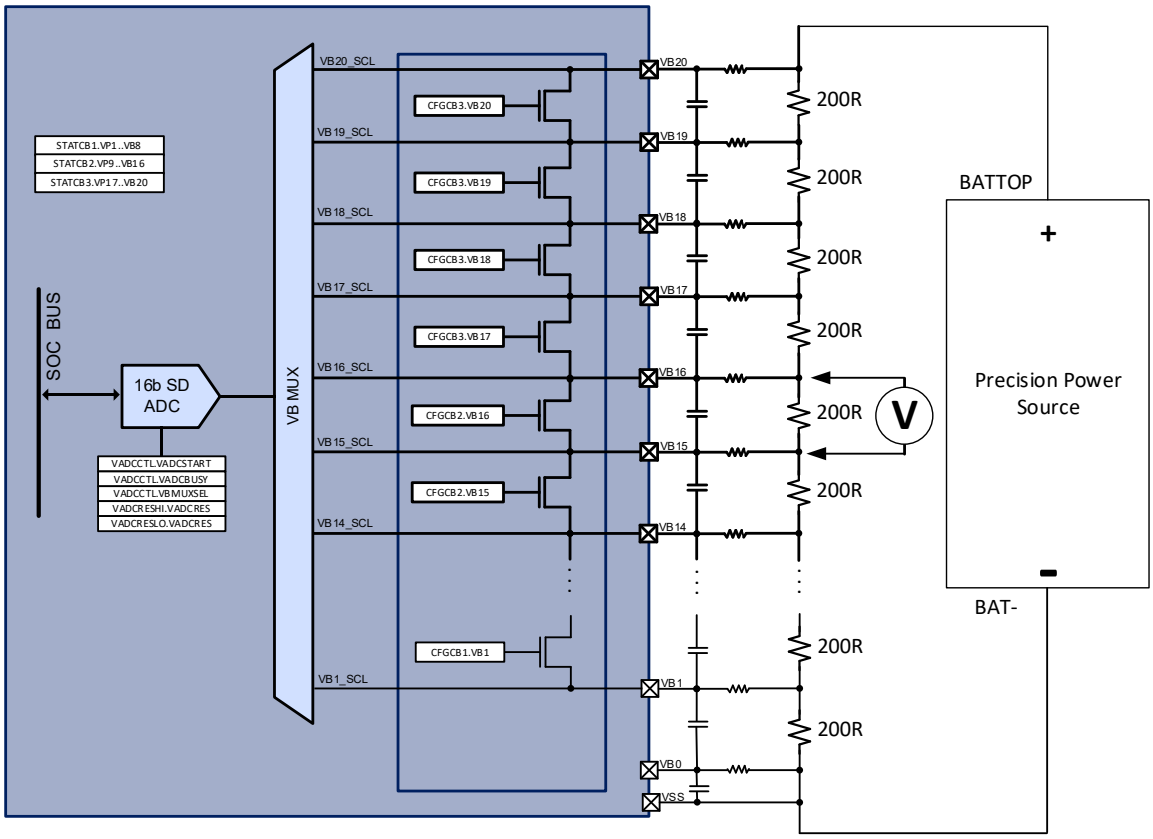

Figure 5 VBx Calibration Connectivity

Current Sensing ADC Calibration

The system error of current sensing is come from external circuitry at each Gain Setting, and it requires the calibration for each Gain setting. To ensure accurate ADC conversation of differential amplifier's out signal V_{ISEN}*DA_{Gain} must remain within a voltage range of -0.3V/+0.5V. The Offset error can be removed by short the inputs at current sense resistor.

Follow the two-point method, the IADC may be use known reference voltage points, -0.2V as short input and 0.2V after the DPGA so the input signal voltage is -0.2V/DA_{GAIN} and 0.2V/DA_{GAIN}. This input signal is the drop voltage on current shunt resistor so a current should be pulled though the resistor during the calibration processing. The shunt resistance should be selected such that it sufficient to required maximum current at a Gain setting. Select the gain that best covers the operational conditions of the system application. If two conditions exists, then two calibration steps may be necessary.

For an example, we assume a 0.5mR precision shunt resistor, the calibration process for Gain x128 setting follows steps below:

After the PAC2x140 BMS device powers up, all need AFE registers is set as expectation and the CAFE is enabled.

- Step1: Enable ISENSE and select DPGA gain of 2^n by configure the AFE registers, with n is 0 to 7. Here, n=7 as DPGA Gain is 128.
- Step2: Use an external source to pull a current through the shunt resistor, I= -0.2V/128/Rshunt, as -3A. X_1 voltage is the drop voltage, the precision DMM is used to measure this current then X1= I_{DMM}*Rshunt*128
- Step3: Run IADC conversation 8 times and average to get IADC reading code, save it as Y_1 code.
- Step4: Push a current though the resistor from ISNSP sensing to ISNSN sensing as a charging current direction, I= 0.2V/128/Rshunt, as 3A. Use a DMM to measure actual current following then save $X_2 = \mathrm{IPull\_Actual} * \mathrm{R} * \mathrm{DA_{GAIN}}$

PAC2x140 BMS VADC and IADC Calibration

- Step5: Run IADC conversation 8 times and average to get IADC reading code, save it as Y_2 code.
- Step6: Calculate CALGAIN, CALGAIN= (X2-X1)/(Y2-Y1) as equation (7). It is actual CALGAIN and able to use directly if need.
- Step7: Calculate SCALED_GAIN=CALGAIN* $2^{(31+n)}$ as equation (12), n=7 for Gain 128 setting.
- Step8: Round the SCALED_GAIN and save to a defined flash memory as 32bit value.
- Step9: Calculate CALOFFSET as equation (8).
- Step10: Calculate $SCALED\_OFFSET = CALOFFSET * 2^{(15+n)}$ as equation (13), n=7 for Gain 128 setting.
- Step11: Round the SCALED_OFFSET and save to a defined flash memory as 32bit value.

Hardware Connectivity

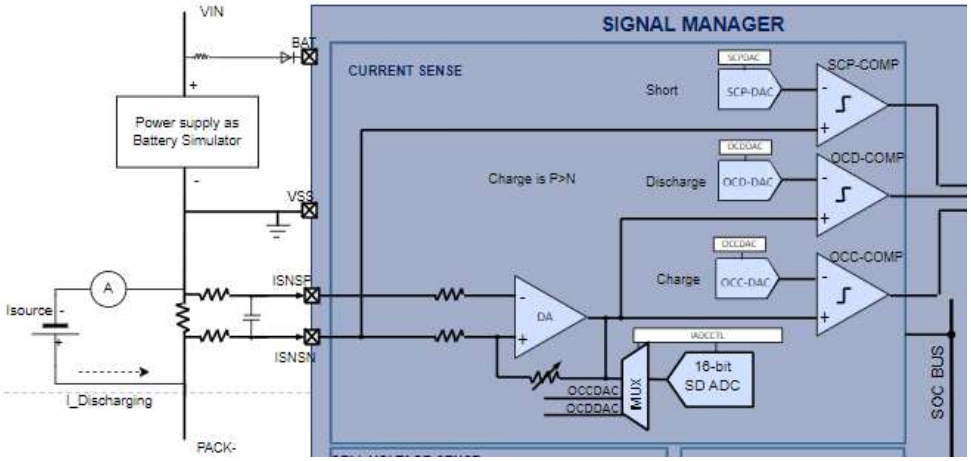

Figure 6 Current sense Discharging ADC force reference Input Connectivity

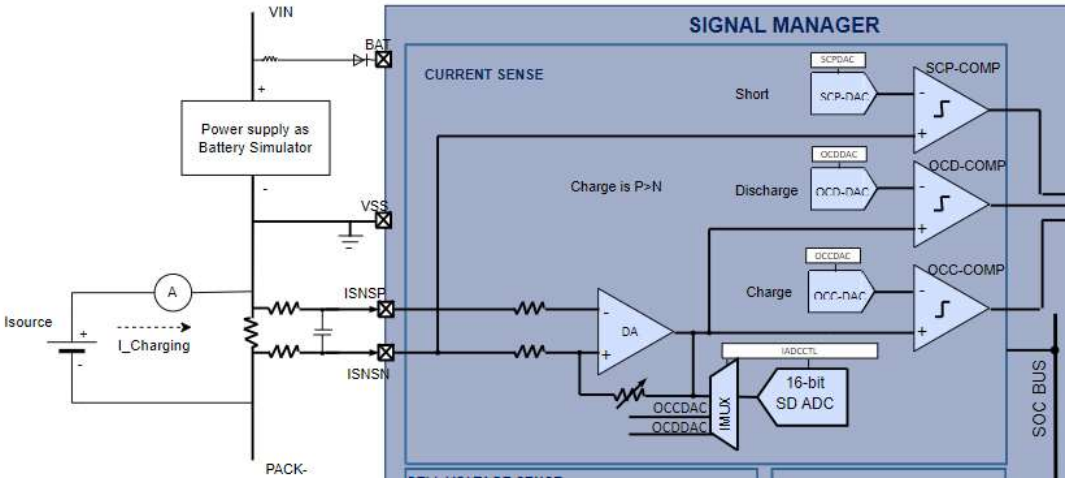

Figure 7 Current sense Chargin ADC force reference Input Connectivity

Other way in application, user can calculate the Gain and Offset Calibration via Amp meter vs ADC code directly. However, calibration in this application note keeps the Gain Calibration and Offset Calibration in a consistent format the same as factory Calibration Format.

PAC2x140 BMS VADC and IADC Calibration

5. Performance Calibration of PAC2x140 BMS ADCs

In application, an ADC conversation returns a result code value. The calibrated output voltage is simply applied via Equation (6) instead of using the ideal function of ADCs.

The Figure 9 shows the error voltage at cell#6 in case no calibration, factory calibration and system calibration.

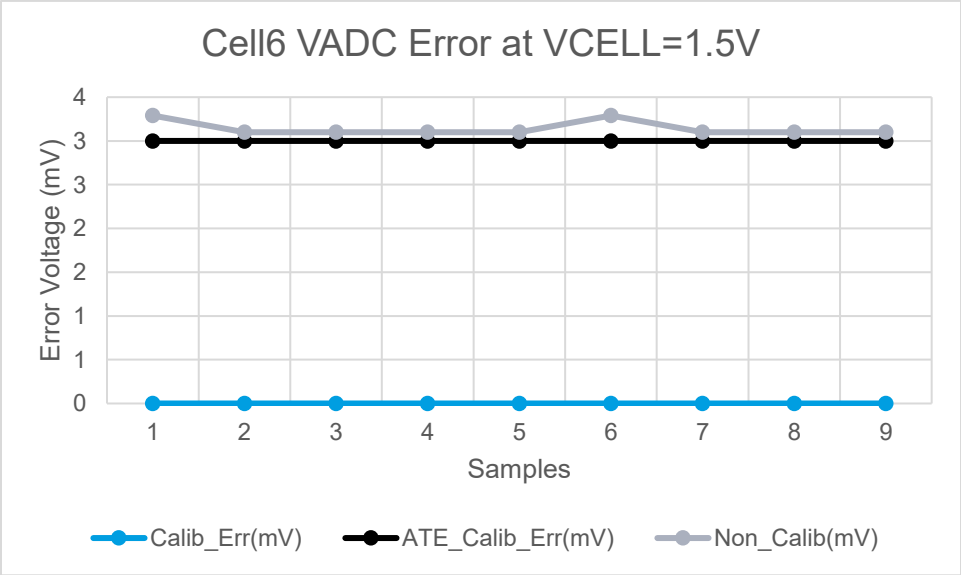

Figure 8 Cell6 Voltage Calibration at 1.5V

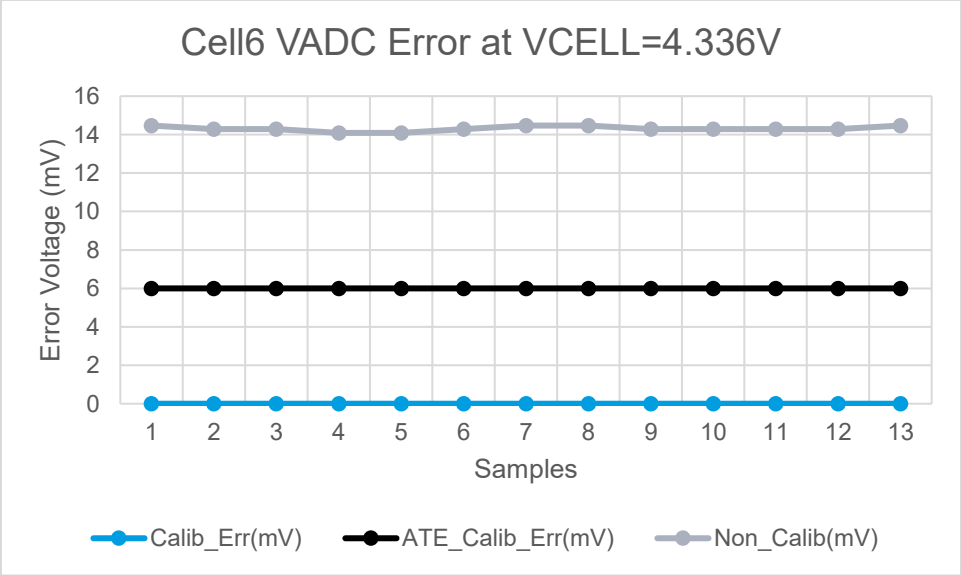

Figure 9 Cell6 Voltage Calibration at 4.3V

and Figure10 shows the performance of the PAC25140 system Gain and Offset calibration routine

PAC2x140 BMS VADC and IADC Calibration

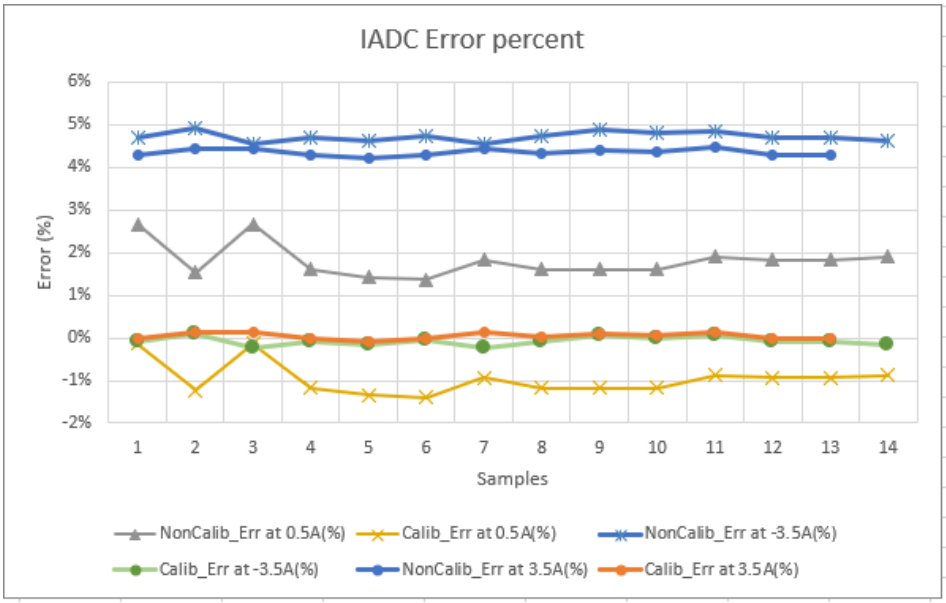

Figure 10 PAC25140 Gain128 IADC error comparision

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Contact Information

For the latest specifications, additional product information, worldwide sales and distribution locations:

Web: www.qorvo.com

Tel: 1-844-890-8163

Email: customer.support@qorvo.com

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