APPLICATION NOTE

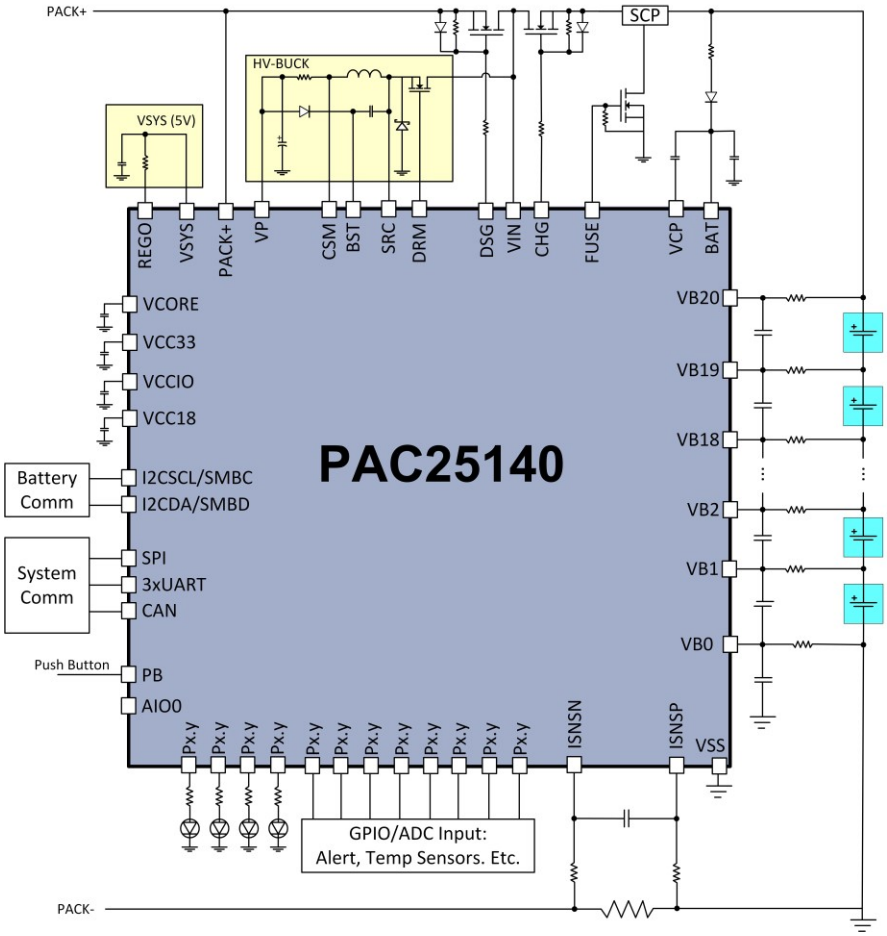
PAC2x140 BMS PCB Layout Guidelines

1. Introduction

Today's electronic devices have higher mobility and are greener than ever before. These applications often require high-performance control with high-power at high frequencies in a compact size. The energy source is supplied by a battery pack and Battery advancements are fueling in a wide range of products from portable power tools, backup Power Supplies to electric Bike or vehicles. The Qorvo® PAC2x140 is an Intelligent Battery Monitoring System (BMS) that can monitor 10-series to 20-series Li-Ion, Li-Polymer and LiFePO4 battery packs.

Systems like this with a small form factor, but with high-power and high-frequency components, require special attention to the system design and layout. A poorly designed PCB can lead to bad application performance as well as other issues such as difficulty passing Electromagnetic Interference (EMI) testing. This document provides an overview of the design and layout guidelines, as well as strategies ensure a stable and well-performing application.

This application note covers details for the PCB layout for the PAC22140 and PAC25140.



2. Contents

3. Reference

- PAC22140, Intelligent Battery Management SOC with integrated Arm Cortex M0 MCU & Cell Balancing Product Documents.
- PAC25140, Intelligent Battery Management SOC with integrated Arm Cortex M4F MCU & Cell Balancing Product Documents.
- Qorvo products with QFN package layout guidelines, see the following application note PCB Layout Guidelines for QFN Package, AN-104 Application Note Link.

4. Grounding

Typical BMS systems implemented with the PAC2x14x devices can have two ground groups. The first is a low-current ground net for reference in the system and the second is a high-current path supporting a LOAD or CHARGER current from the PACK- connection. The low-current ground net can be further separated to two different types of ground nets for the PCB:

1) IC GND – The ground connection to the IC.
2) DC/DC GND – The ground connection to the DC/DC.

In the design, each of these grounds should be isolated from each other by using a star configuration connected at the main power supply bus capacitor. Then it is important that this low-current ground systems only connect to the PACK- at the negative of lowest battery cell in battery pack as shown in Figure 1.

Using an optional inner layer ground plane is recommended for the low-current ground nets.

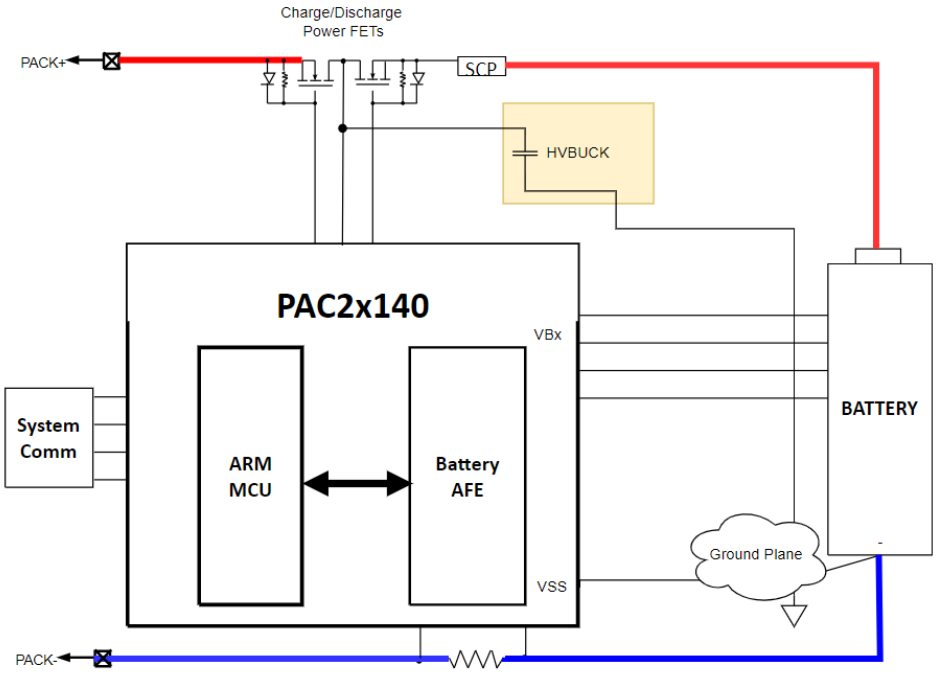


Figure 1 Low-current Ground Nets

In application design, the wire and PCB trace connections between negative of bottom individual cell to the sense resistor must be short and low resistance as much as possible.

5. Power Pad Consideration

The PAC family of controllers all have power pads on the bottom of the packaged products to help with thermal resistance and provide improved ground resistance.

It is highly recommended using multiple vias inside the thermal pad area to conduct heat from the top layer to the inner or bottom layers. Correct layout of these vias greatly improves the thermal characteristics of the IC as well as electrical performance.

The recommended via pitch and diameter for thermal pad area vias are:

- Pitch: Minimum of 1mm
- Hole diameter: 0.3mm to 0.33mm

The design should include as many vias to ground as can fit, based on the pitch and diameter requirements above.

When designing the footprint for the PAC, the copper area for the pad should match the size of the power pad on the IC to maximize grounding between the IC and PCB. This will also provide the maximum mechanical adherence.

The diagram below shows an example of the power pad thermal vias

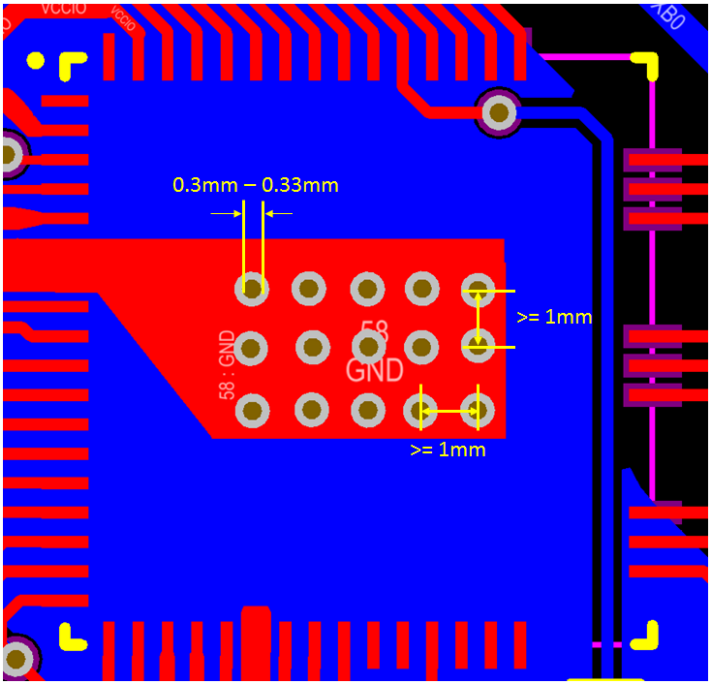


Figure 2 Example of Power Pad thermal vias

For guidelines on design and layout using Active-Semi products with QFN packages, see the following application note available on Qorvo website, *PCB Layout Guidelines for QFN Package (AN-104)*

6. Power Decoupling Capacitors

The PAC2X140 family of BMS, Intelligent Battery Monitoring System generates several power supplies internally to supply the IC and system.

The PAC2X140 contains the following power supplies that are internally generated[1]:

- **VSYS** – 5V system supply
- **VCC18** – 1.8V Flash supply (PAC25140)
- **VCCIO** – 3.3V/5V IO supply
- **VCC33** – 3.3V ADC supply
- **VCORE** – 1.2V/1.8V Core supply (PAC25140/PAC22140)

Each of these power supplies should be bypassed to ground via decoupling capacitors.

Each decoupling capacitors should be placed as close as possible to the IC and routed with the shortest trace possible. There should also be generous copper for these connections. This will help reduce any parasitic components that could cause ringing and other emissions such as electromagnetic interference (EMI).

In the diagram below the decoupling capacitors are shown as components C2, C4, C11, C12, C43. Note the traces and copper from the IC pins and power pad to these decoupling capacitors in this example.

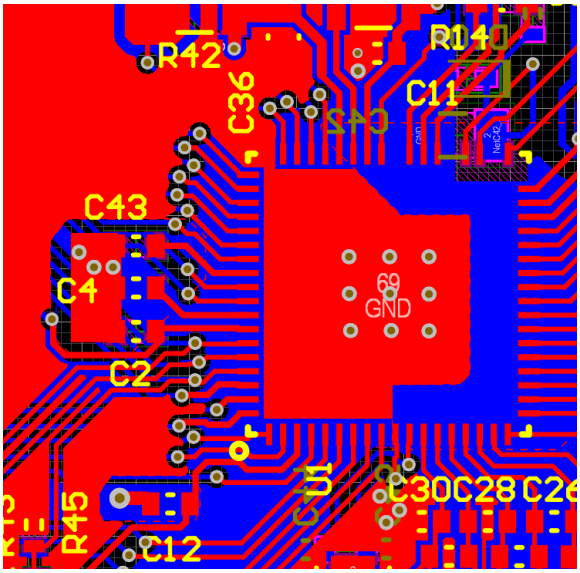


Figure 3 LDOs Decopuling Capacitors

In the example above, the IC has a ground pin that is used for the copper polygon connecting the bypass capacitors to the power pad. The power pad has several vias to the ground plane to decrease impedance to the ground plane.

The ground plane for LDOs should be separated from any switching power source as DC/DC power ground.

In addition to **VSYS**, **VCC18**, **VCCIO, VCORE** and **VCC33** supplies, the PAC2X140 also contains a DC/DC controller to convert the bus voltage to a system voltage 12V to power the IC as well as supply the high side gate driver charge pump and low side driver high voltage output.

The DC/DC has the following power supply signals that also need to be bypassed:

- **VHM** – DC/DC Input (C39)

[1] Note that other PAC® family members may have different LDOs, but the guidelines for bypass layout are the same.

- **VP** – DC/DC Output (C36, C37)

Like with the LDO decouple capacitors above, these also need to be placed as close as possible to the IC, with as much copper as possible connecting to the IC and to ground to reduce any parasitic components.

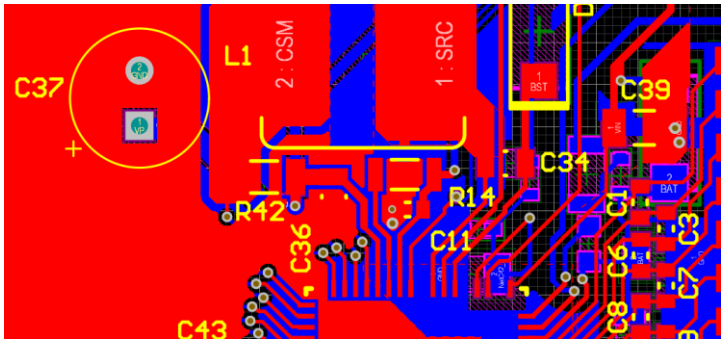


Figure 4 DC/DC Decoupling Capacitors

7. Communication Line Protection

To protect the communication pins of the PAC2x140 from ESD, the TVS devices must be located as close as possible to the pack connector, UART, SPI, I2C, etc. The grounded end of these TVS diodes must be returned to the PACK– node, rather than to the low-current digital ground system, VSS. Implemented this way, the ESD event is diverted away from the sensitive electronics as much as possible.

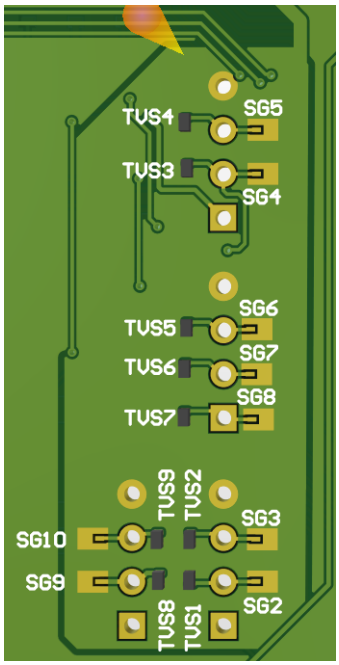


Figure 5 TVS Protection for the Communication Line s

8. FETs Bypass and Pack Terminal Bypass Capacitors

The Figure 6 shows the copper trace of capacitors bypass to protect FETs and PACK+/- terminal, the trace should be wide to lower the inductance of the bypass capacitor circuit.

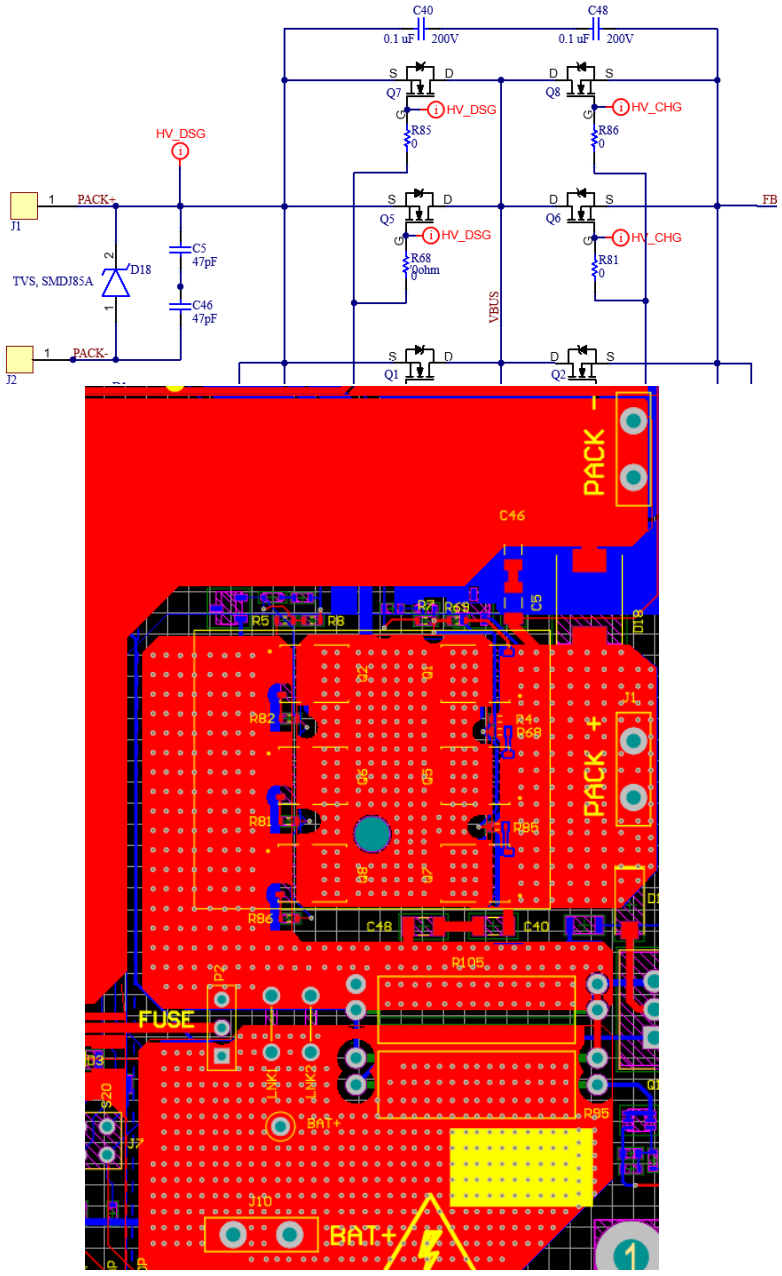


Figure 6 Copper trace of Bypass Capacitors C5, C46, C40, C48.

9. Cell Voltage and Current Sense Kelvin Connections

In the BMS system, the cells voltage sensing is extremely important to guarantee the accuracy measurement result. This high accuracy requires Kelvin voltage sensing. The VBx sensing signals must be connected as close as possible to battery terminals, it should not include any high current passing through the connection.

The current sensing is implemented by measuring the voltage on a high precision, low resistance sense resistor via input pins, ISNSP and ISNSN. These input signals must be Kelvin connected to sense resistor and not include any high current passing through the connection.

Figure 7 demonstrates a poor Kelvin connection where high current path is included.

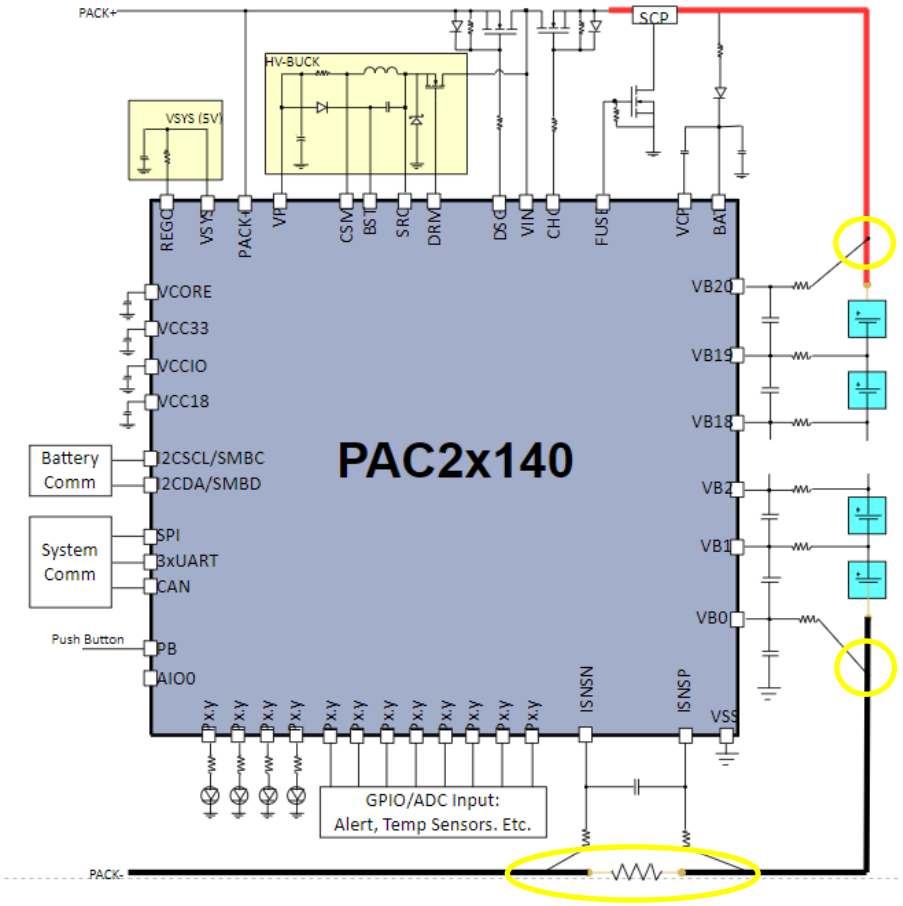


Figure 7 Incorrect Kelvin, the sensing includes High-Current Path

Figure 8 shows the correct technique, the Kelvin signals are close to the sensing point and minimize any high current path trace. The high-current path between the negative of the bottom individual cell battery to the current sense resistor, the dash bold black line, must be short and very low resistance.

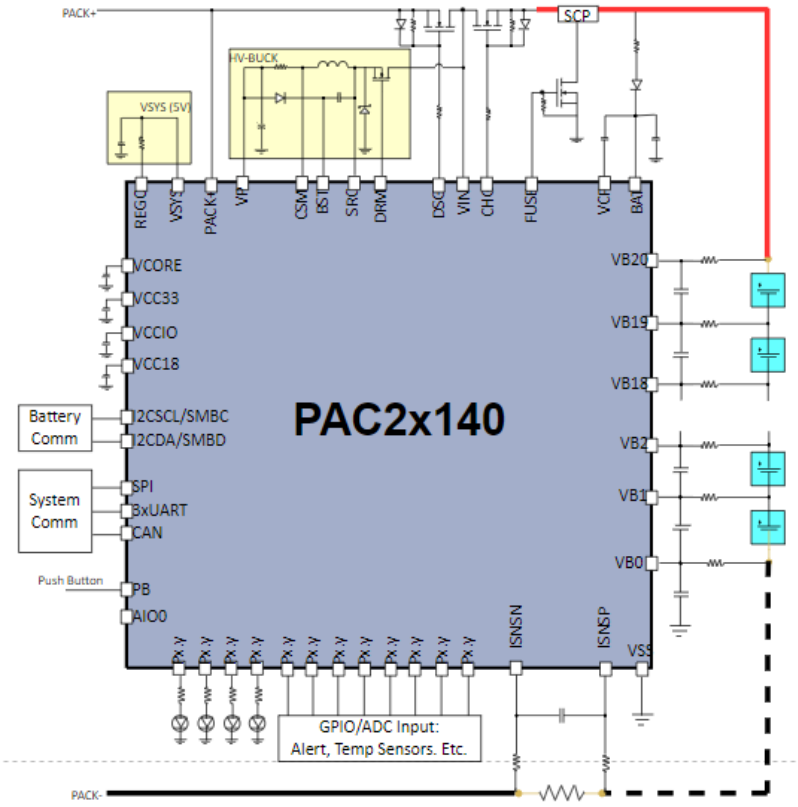


Figure 8 Correct Kelvin Signal Connection

10. Coulomb Counter Differential Network

The PAC2X140 contains integrated signal conditioning, such as programmable gain Differential Amplifiers. These Differential Amplifiers are often used for measuring pack current for both current measurement and protection of the BMS system, OCC, OCD.

The value of the current sense resistor (RSENSE) is selected based on the current range requirements of the application. The low-pass filter for the current sense circuit should be placed close to the IC for best performance. If the low-pass filter for the current sense circuit cannot be placed close to the IC, then at least the capacitor portion of this filter should be close to the IC. The differential signals for the current sense circuit should be routed as symmetrically as possible from the current sense circuit's low-pass filter to the analog input channels on the IC. The trace widths should also be the same for each of these differential signals. Maintaining the symmetrical placement shown for optimum current offset performance. The filter network symmetrical traces should be shielded if it is possible, from the sense resistor to the filter network resistors.

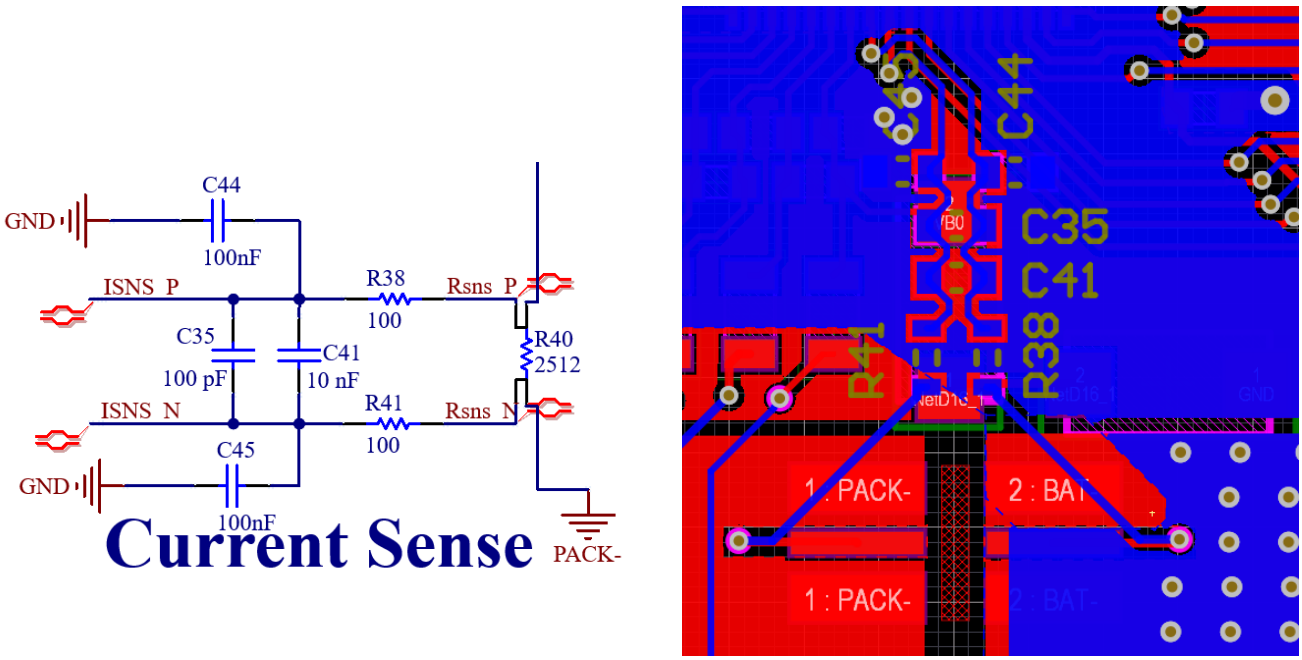


Figure 9 Current Filter Routing

11. ESD Spark Gap Protection

Beside the protection of communication lines, I2C, UART, SPI from ESD by using TVS devices, a spark gap close to connector should be recommended, 0.2mm spacing between points is typical. The SG devices on the board are these spark gaps layout pattern.

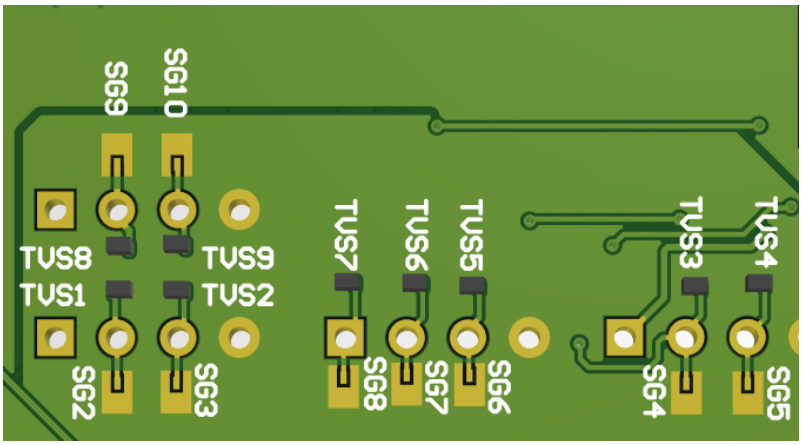


Figure 11 Recommended Spark-Gap Pattern to protect Communication Lines from ESD

12. Routing Signals and Unwanted Magnetic Coupling

When routing both analog and digital signals, it may be beneficial to use 45^{O} angles when routing traces rather than 90^{O} angles. Using sharp corners to traces may increase emissions at the corners, so it is recommended to use 45^{O} angles whenever possible.

A BMS fuel gauge circuit board needs critical attention to layout of grounds and other traces due to the fundamental incompatibility of high-current path and low-current path of signals critical to the performance of the BMS devices. In PCB layout, the trace to trace coupling between the high-current path and low-current path should be considered and traces should be places away from each other. In other words, ensure the high-current traces from BAT and PACK+ are routed away from the signal traces, and ground is star connected separately from the high current ground path typically PACK- .

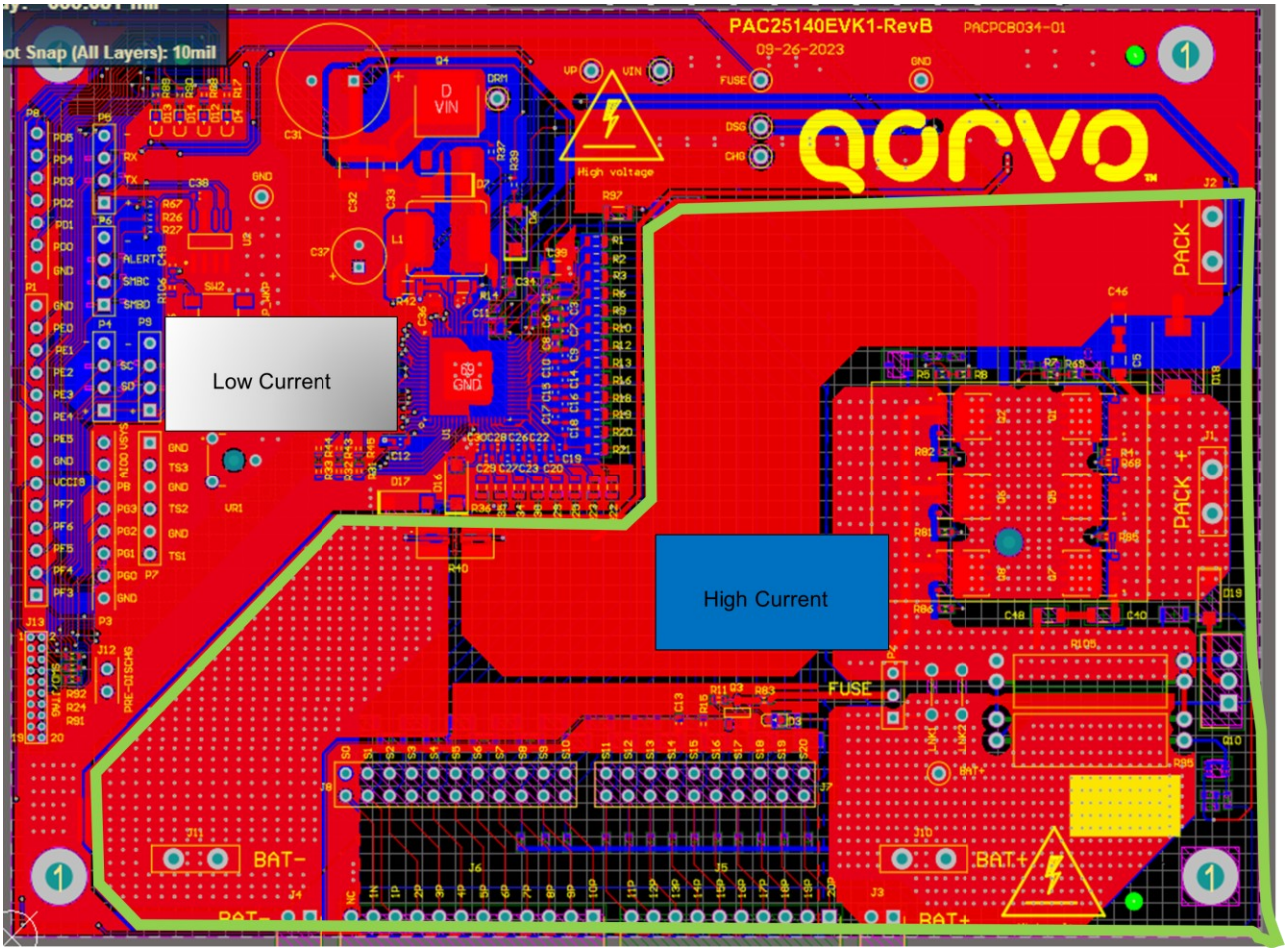


Figure 12 Seprating High and Low Current Paths

13. LEGAL INFORMATION

For the latest specifications, additional product information, worldwide sales and distribution locations:

Web: www.qorvo.com
Tel: 1-844-890-8163
Email: customer.support@qorvo.com

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