QPB9351

1.7 – 2.7 GHz Dual Channel Rx VGA

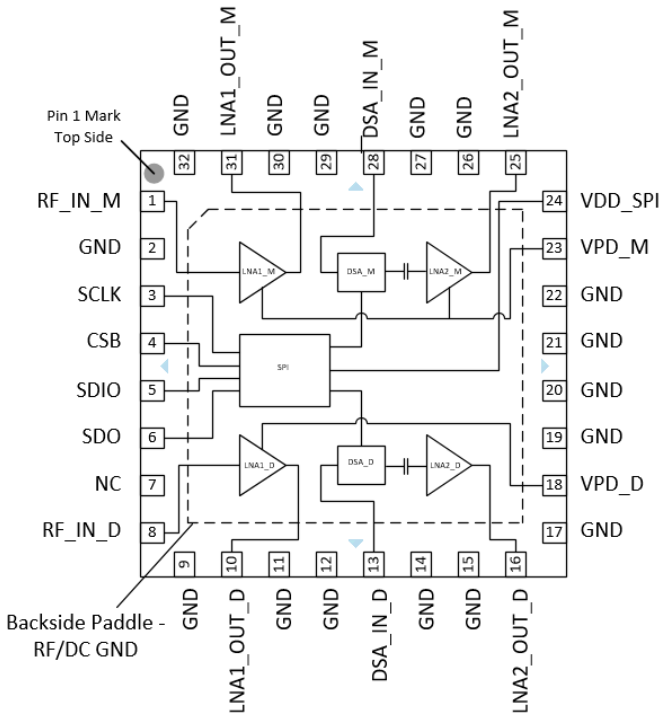
Product Description

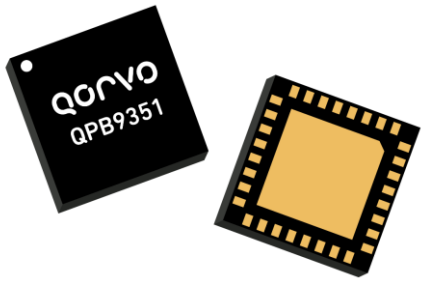
The QPB9351 is a highly integrated Rx front-end module targeted for high performance macro base station receivers. The RX VGA SiP (receive variable gain amplifier system in package) integrates high performance first stage low noise amplifiers (LNA), digital step attenuators (DSA), second stage LNA in a dual channel configuration. Power down capability for the amplifiers can be controlled through dedicated shutdown pins for each channel.

The LNAs utilize Qorvo's high performance E-pHEMT process to provide 0.4 dB noise figure for the first stage LNA. Gain control is implemented through a 31 dB range DSA in 1 dB steps.

The QPB9351 is packaged in a RoHS-compliant, compact 5 x 5 mm 32 pin surface-mount leadless package.

Functional Block Diagram





32 Pin 5 X 5 mm Leadless SMT Package

Product Features

- 1.7 – 2.7 GHz Frequency Range
- Integrates LNAs, DSA
- Dual Channel Configuration
- Integrated Shutdown Capability
- LNA1: 0.4 dB NF, 16.5 dB Gain, 38 dBm OIP3
- 31 dB Gain Control Range, 1 dB Step Size
- +5 V Supply Voltage
- SPI Control Interface
- +1.8 V Logic

Applications

- Wireless Infrastructure
- Diversity Receivers
- TDD or FDD systems

Ordering Information

Part No.	Description
QPB9351TR13	2500 pieces on a 13" reel
QPB9351EVB	1.7-2.7 GHz Evaluation Board

Absolute Maximum Ratings

Parameter	Range / Value	Units
Storage Temperature	-55 to 150	°C
RF Input Power, CW, 50Ω, T=25°C	+20	dBm
Supply Voltage (V_{DD}) Pins 10, 16, 24, 25, 31	6.0	V
Reverse Supply Voltage	-0.3	V

Exceeding any one or a combination of the Absolute Maximum Rating conditions may cause permanent damage to the device.

Recommended Operating Conditions

Parameter	Min	Typ	Max	Units
Supply Voltage (V_{DD})	+3.3	+5.0	+5.25	V
T_{CASE}	-40		+105	°C
T_j for > 10^6 hours MTTF			+190	°C

Electrical specifications are measured at specified test conditions. Specifications are not guaranteed over all recommended operating conditions. Application of conditions to the device outside the Recommended Operating Conditions may reduce device reliability and performance.

Electrical Specifications: Overall Module

Test conditions unless otherwise noted: V_{DD}=+5 V, Temp.=+25 °C, 50 Ω system

Parameter	Conditions	Min	Typ	Max	Units
Operational Frequency Range		1700		2700	MHz
Channel Isolation			40		dB
Current	All 4 LNAs (On state)		270		mA
	LNA in Off state (per LNA)		3		mA
	SPI+DSA (pin 24)		3		mA
Control Voltage (pins 18 & 23)	V_{high}	1.17		3.0	V
	V_{low}	0		0.63	V
Switching Speed (2)	LNAs OFF to ON		45		ns
	LNAs ON to OFF		65		ns
Thermal Resistance, θ_{jc}	Junction to backside paddle		15		°C/W

Notes:
1. Control voltage at pins 18 & 23 under TDD mode.

Electrical Specifications: LNA1

Test conditions unless otherwise noted: V_{DD}=+5 V, Temp.=+25 °C, 50 Ω system

Parameter	Conditions	Min	Typ	Max	Units
Test Frequency			2600		MHz
Gain			16.5		dB
Input Return Loss	With external matching		13.0		dB
Output Return Loss			16.0		dB
Output P1dB			+22.5		dBm
Output IP3	P_{out} = +5 dBm/tone, Δf = 1MHz		+38.0		dBm
Noise Figure (1)			0.4		dB
LNA2 Current	On state		65		mA
	Off state		3		mA

Notes:
1. Trace loss de-embedded from NF data.

Electrical Specifications: DSA + LNA2

Test conditions unless otherwise noted: V_{DD}=+5 V, Temp.=+25 °C, 50 Ω system

Parameter	Conditions	Min	Typ	Max	Units
Test Frequency			2600		MHz
Gain	Max gain setting		20.0		dB
Gain Control Range			31		dB
Gain Control Step Size			1		dB
Attenuation Accuracy	Major states	+/- (0.5 + 5% of attenuation level)			dB
Input Return Loss	With external matching		12.0		dB
Output Return Loss			14.0		dB
Output P1dB			+19.0		dBm
Output IP3	P_{out} = +5 dBm/tone, Δf = 1MHz		+39.0		dBm
Noise Figure (1)	Max gain setting		2.4		dB
LNA1 Current	On state		70		mA
	Off state		3		mA
Attenuation Settling Time	To 10% of target attenuation level		145		ns

Notes:
1. Trace loss de-embedded from NF data.

Serial Control Interface Register Definitions

Register Address	Bit	Description	Notes
0x00	All	Not cleared by soft reset.	Mirror register [7:4] = [0:3] to accommodate MSB or LSB first designs
0x00	7	Soft Reset	Register 0x00 not cleared by soft reset. 1'b1 Reset active. Registers 0x02 through 0x12 will be set to Defaults values. 1'b0 (Default)
	6	LSB/MSB First	Ignored since the design is MSB first only
	5	Address Ascend/Descend	Ignored since design is Address Ascend only
	4	SDO Active	Used to configure the optional SDO port. 1'b1 SDO Port active (4-wire mode) 1'b0 SDO inactive (3-wire mode). (Default)
	[3:0]	Mirror of [7:4] – (Not Used)	Ignored since the design is MSB first only
0x01	All	Not cleared by soft reset (0x00)	
	7	Single Instruction Enable	1'b1 -> Single byte mode 1'b0 -> Streaming mode (Default). Data wrapping supported in streaming mode (address to 0x12 to 0x00).
	6	Unused	
	5	Read back active/buffered registers	A mux is used to select which of the two data registers is used for read back. 1'b1-> read back from buffer. 1'b0 -> read back from active register (Default)
	[4:0]	Unused	
0x02	All	Cleared by soft reset (0x00). Double-buffered.	Output updated only on assertion of the transfer bit.
	[7:2]	User defined	Default = 0.
	[1:0]	Power Mode	2'b00 – Normal operation mode, (Default) 2'b01 – not supported. 2'b10 –not supported. 2'b11– Sleep mode with lowest power dissipation, which is characterized by chip inactivity except for the SPI port. DSAs=min attenuation. Equivalent of setting registers 0x10 = 1, 0x11 = 1.
0x03	[7:0]	Chip Type [7:0]	Read-only. Qorvo-defined chip types. Value = 0x03 8'b 00000011
0x04	[7:0]	Chip ID [7:0]	Read-only. Qorvo-defined chip ID. Value = 0x01=QPB9351 8'b 00000001
0x05	[7:0]	Chip ID [15:8]	Read-only. Qorvo-defined chip ID. Default=0x00.
0x06	[7:0]	Chip Version	Read-only. Qorvo-defined chip version.
0x07 to 0x0B	[7:0]	Unconnected	Read back will be 0x00.
0x0C	[7:0]	Vendor ID [7:0]	Read-only. 0x9A (Qorvo USB ID = 0x259A)
0x0D	[7:0]	Vendor ID [15:8]	Read-only. 0x25 (Qorvo USB ID = 0x259A)
0x0E	[7:0]	Unconnected	Read back will be 0x00.

Serial Control Interface Register Definitions (contd.)

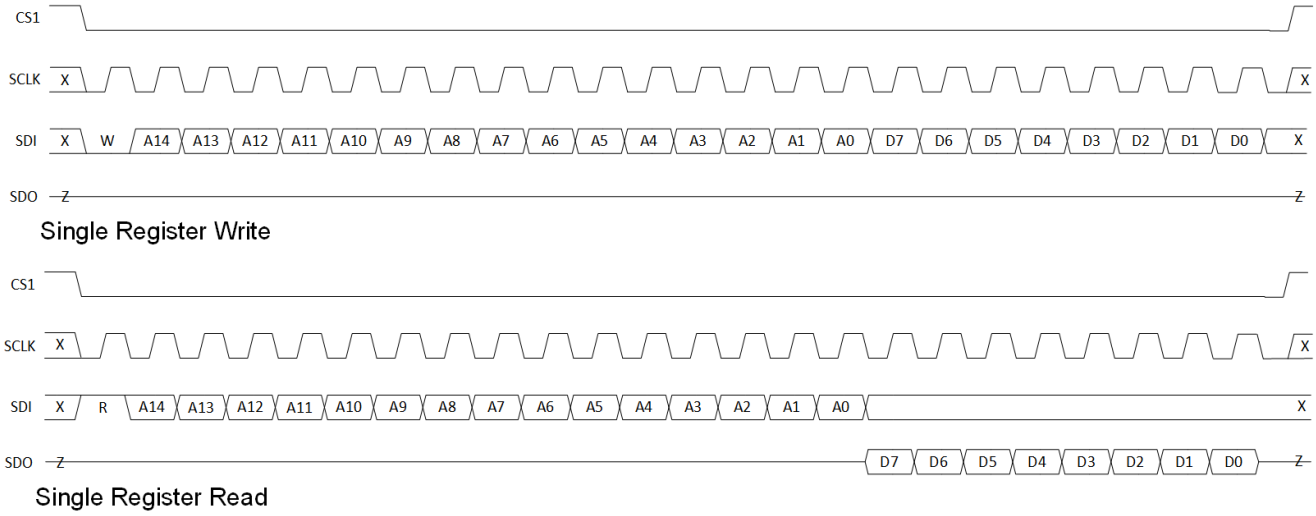
Register Address	Bit	Description	Notes
0x0F	[7:1]	Unused	Can be written and read back but has no functionality. Default = 0.
	[0]	Transfer Bit	1'b1 -> Transfer buffer to active registers 1'b0 -> (Default) This bit is self-clearing once the transfer has taken place.
0x10	[7:5]	Unused	Can be written and read back but has no functionality. Default = 0.
	[4:0]	DSA_M Control	5-bit DSA control, main channel. MSB=bit [4], LSB = bit [0]. LSB Step Size =1dB 5'b 00000 = 31 dB 5'b 11111 = 0 dB (Default)
0x11	[7]	General Purpose Output – Ext. Component Control	Output for controlling component external to the QPB9351.Output high voltage is VDD_SPI. Default = 0.
	[6:5]	Unused	Can be written and read back but has no functionality. Default = 0.
	[4:0]	DSA_D Control	5-bit DSA control, diversity channel. MSB=bit [4], LSB = bit [0]. LSB Step Size =1dB 5'b 00000 = 31 dB 5'b 11111 = 0 dB (Default)
0x12	[7:0]	Unused	Can be written and read back, but it has no functionality. Default = 0

Electrical Specifications – Serial Control Interface

Parameter	Conditions (1)	Min	Typ	Max	Units
V_{IL}	Input Voltage for Low State	-0.2		0.5	V
V_{IH}	Input Voltage for High State	1.2		V_{DD_SPI}	V
V_{OL}	Output Voltage for Low State			0.3	V
V_{OH}	Output Voltage for High State			V_{DD_SPI}	V
I_{IN}	Digital Input Current (V_{IH} = V_{DD_SPI} for High State and 0 V for Low State)		+/- 0.95		µA
T_{rs}	Power up reset time		< 500		µS
T_r	V_{DD_SPI} Supply ramp time (2)		> 10		µS
I_{DD_SPI}	Input Current		< 8		mA

Notes:
1. Test conditions unless otherwise noted: $V_{DD\text{-}SPI}$=+5 V, Temp.=+25 °C
2. It is recommended that V_{DD_SPI} be turned on first before the serial lines signals.

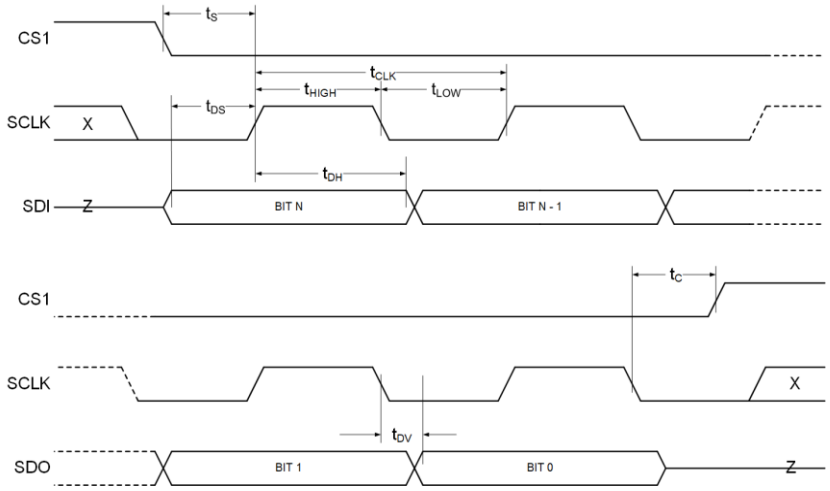
Timing Diagrams



Single Register Write

Single Register Read

4-Wire SPI Write and Read Instructions – MSB First, 24-bit

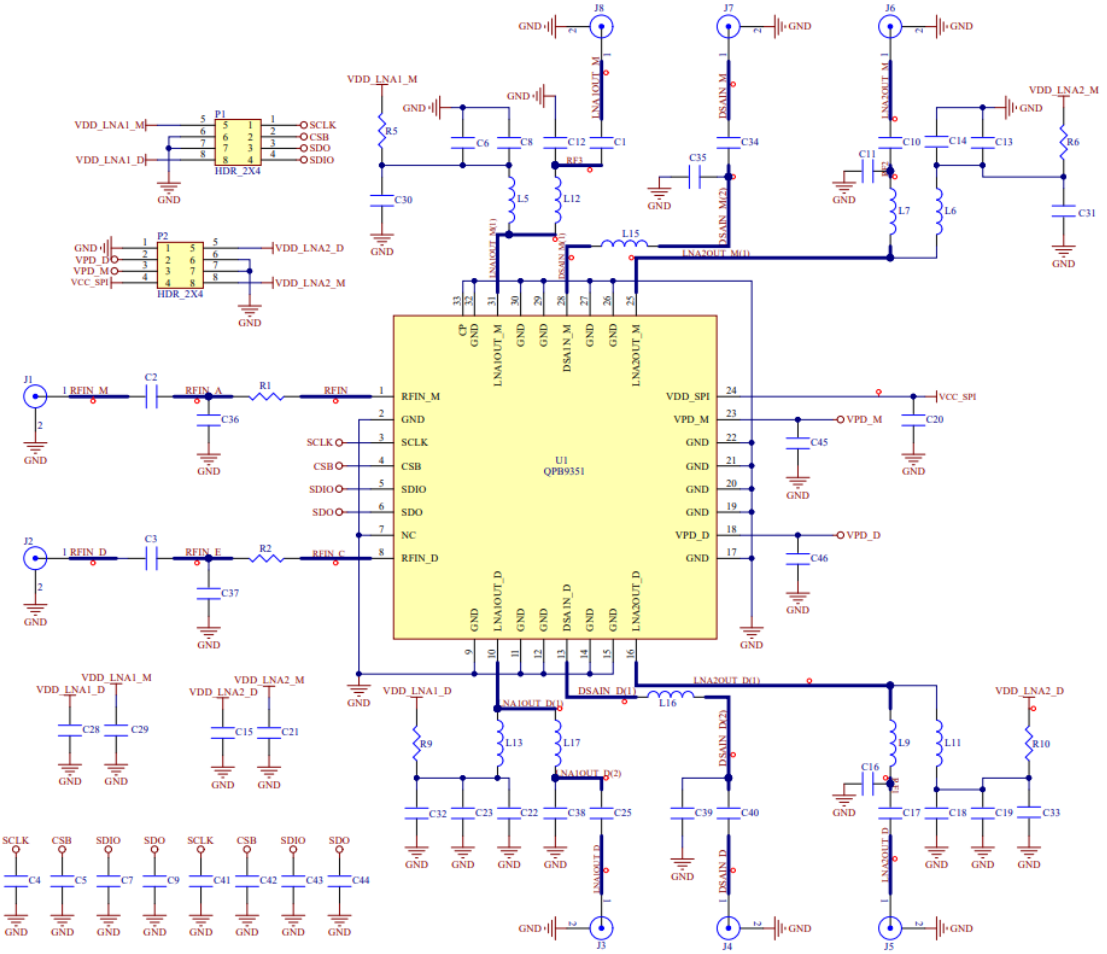


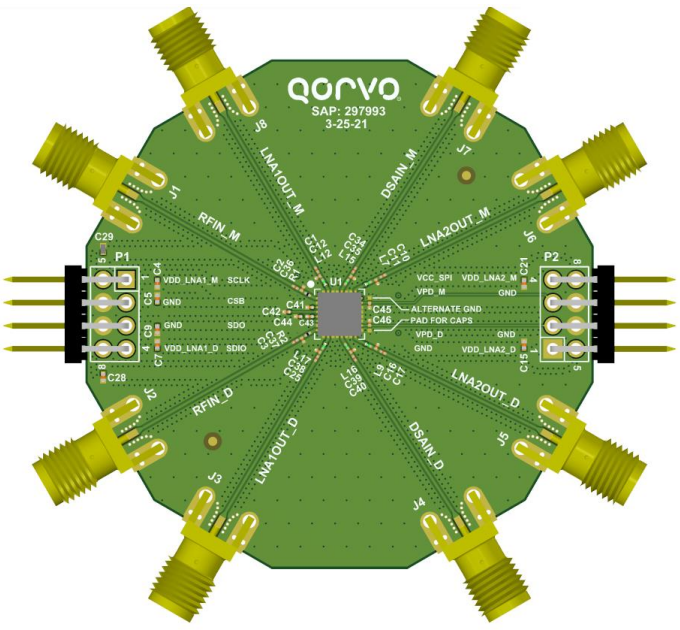
Serial Control Interface

Parameter	Description	Min	Max
t_{ds}	SDI to SCLK rising edge setup	10ns	
t_{dh}	SCLK rising edge to SDI hold	10ns	
t_{clk}	Period of SCLK	50ns	
t_{high}	High width of SPI CLK	25ns	
t_{low}	Low width of SPI CLK	25ns	
t_s	CS falling edge to SCLK rising edge, setup time	10ns	
t_c	SCLK falling edge to CS rising edge, hold time	20ns	
t_{dv}	SCLK falling edge to valid readback data, SDIO/SDO, t_{dv}	20ns	

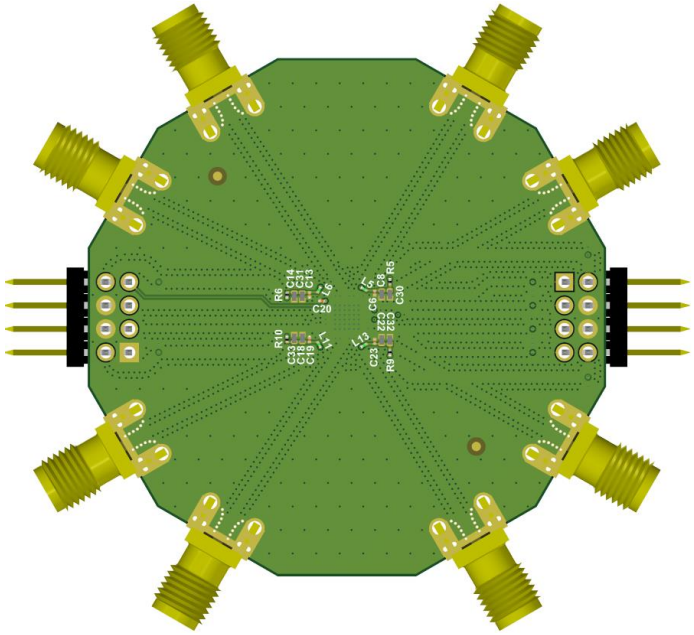
Note: All rates less than 20MHz are usable, including 20MHz. The rising edge of the SCLK is used to latch data.

QPB9351 Evaluation Board Schematic and Layout





TOP VIEW



BOTTOM VIEW

Bill of Material – QPB9351EVB

Reference Des.	Value	Description	Manuf.	Part Number
U1	NA	1.7-2.7 Dual channel DVGA	Qorvo	QPB9351
C1, C2, C3, C6, C10, C13, C17, C19, C23, C25, C34, C40	100 pF	CAP, 5%, 25V, C0G, 0201	Murata	GRM0335C1E101JA01D
C11	0.5 pF	CAP, +/-0.05pF, 25V, Hi-Q, 0201	Murata	GJM0335C1ER50WB01D
C39	0.8 pF	CAP, +/-0.05pF,25V,Hi-Q,0201	Murata	GJM0335C1ER80WB01D
C12, C36, C37, C38	0.7 pF	CAP, +/-0.05pF, 25V, Hi-Q, 0201	Murata	GJM0335C1ER70WB01D
C35	1 pF	CAP, +/-0.05pF, 25V, HI-Q, 0201	Murata	GJM0335C1E1R0WB01D
C41, C42, C43, C44, C45, C46	18 pF	CAP, 2%, 25V, C0G, 0201	Murata	GRM0335C1E180GA01D
C15, C21	0.01 uF	CAP, 10%, 50V, X7R, 0402	Murata	GCM155R71H103KA55D
C14, C30, C32, C33	0.1 uF	CAP, 10%, 50V, X5R, 0402	AVX	04025D104KAT2A
C8, C31, C18, C22	1 uF	CAP, 10%, 25V, X6S, 0402	Murata	GRM155C81E105KE11D
C29	4.7 uF	CAP, 20%, 10V, X5R, 0.65mm, 0402	Murata	GRM155R61A475MEAAD
C20	0.01 uF	CAP, 10%, 16V, X7R, 0201	Murata	GRM033R71C103KE14D
C28	100 pF	CAP, 5%, 50V, C0G, 0402	Murata	GRM1555C1H101JA01D
R5, R6, R9, R10	0 Ω	RES, 5%, 1/20W, 0201	Kamaya	RMC1/20JPPA15
L9	1.5 nH	IND, +/-0.1nH, T/F, HI-Q, 0201	Murata	LQP03TN1N5B02D
L7	2.2 nH	IND, +/-0.1nH, T/F, HI-Q, 0201	Murata	LQP03TN2N2B02D
L15, L16	2.5 nH	IND, +/-0.1nH, T/F, HI-Q, 0201	Murata	LQP03TN2N5B02D
L12, L17	3 nH	IND, +/-0.1nH, T/F, ULTRA-Q, 0201	Murata	LQP03HQ3N0B02D
R1, R2	2.6 nH	IND, +/-0.1nH, T/F, ULTRA-Q, 0201	Murata	LQP03HQ2N6B02D
L5, L6, L11, L13	18 nH	IND, 3%, T/F, ULTRA-Q, 0201	Murata	LQP03HQ18NH02D
C4, C5, C7, C9, C16	NA	Not Populated	NA	NA

Typical Performance – QB9351EVB

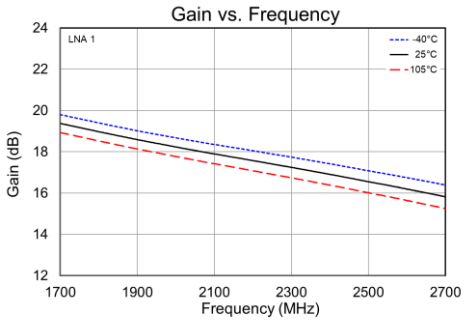
Test conditions unless otherwise noted: V_{DD} = +5 V, Temp = +25°C

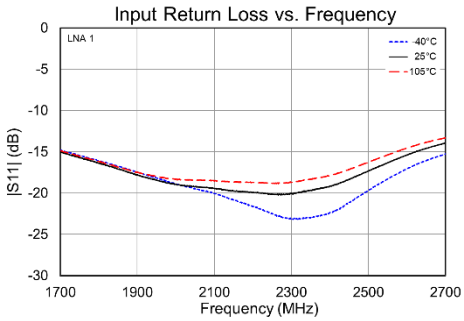
Parameter	Conditions	Typical Values					Units
Frequency		1700	1900	2300	2600	2700	MHz
Gain	LNA1	19.4	18.5	17.2	16.1	15.8	dB
Input Return Loss		15.1	17.7	20.0	15.3	13.9	dB
Output Return Loss		12.2	12.7	17.6	19.6	17.9	dB
Noise figure (1)		0.34	0.35	0.42	0.49	0.52	dB
OIP3 (2)		37.2	37.2	37.6	38.0	37.4	dBm
Input P1dB		22.5	22.4	22.5	22.5	22.2	dBm
Gain	DSA + LNA2	19.0	19.2	19.8	20.2	20.2	dB
Input Return Loss		8.4	9.1	11.8	13.1	13.3	dB
Output Return Loss		14.2	15.3	17.1	13.5	12.6	dB
Noise figure (1)		2.07	2.16	2.28	2.40	2.46	dB
OIP3 (2)		35.5	36.1	37.0	37.8	37.9	dBm
Input P1dB		20.6	20.4	19.7	19.5	19.3	dBm
Cross Isolation		42.6	41.5	50.9	41.3	40.3	dB

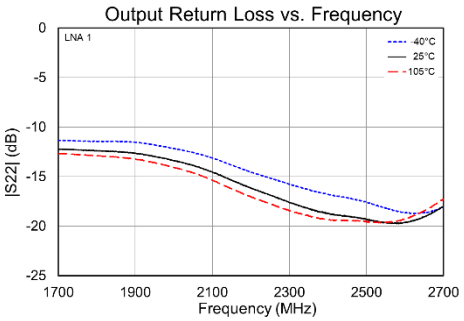
Notes:
1. Input trace loss de-embedded from NF data.
2. Pout/tone = +5 dBm, Δf = 1MHz

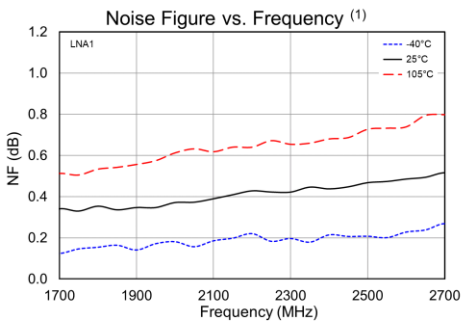
Performance Plots – QPB9351EVB

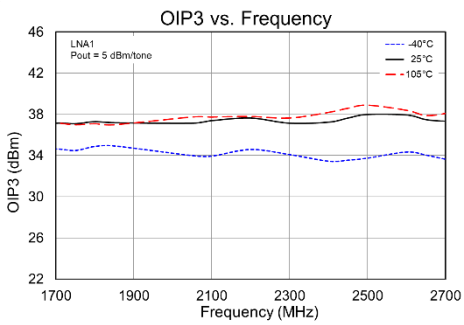
Test conditions unless otherwise noted: V_{DD} = +5 V.

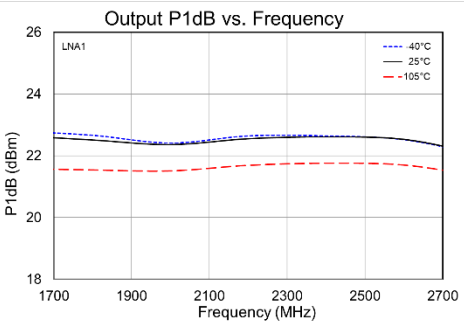










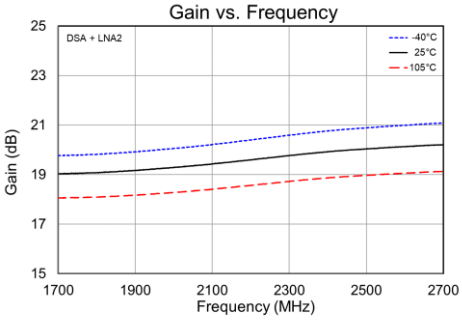


Notes:
1. Trace loss de-embedded from Noise Figure data. NF data at -40°C may have +/-0.1dB measurement uncertainty.

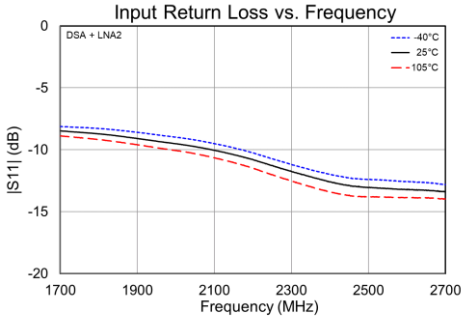
Performance Plots – QPB9351EVB (Continued)

Test conditions unless otherwise noted: V_{DD} = +5 V.

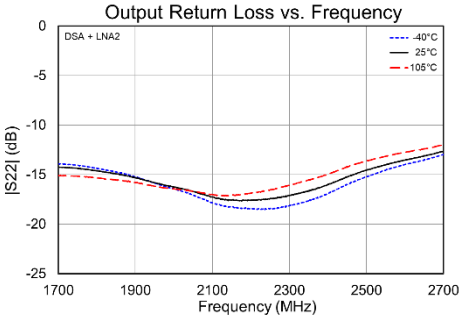
Gain vs. Frequency



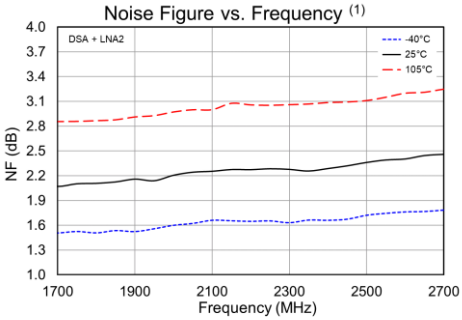
Input Return Loss vs. Frequency



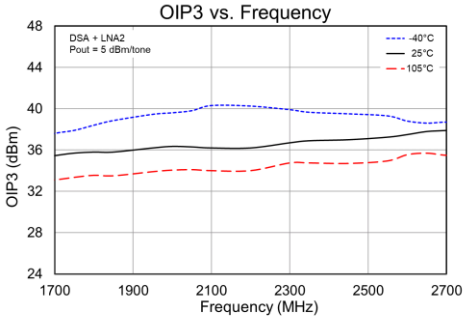
Output Return Loss vs. Frequency



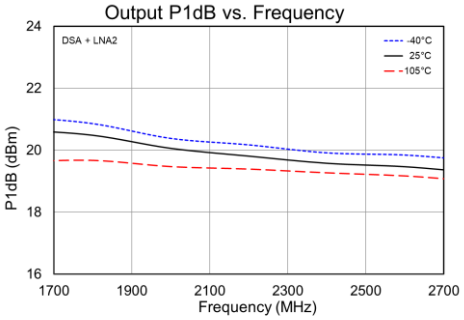
Noise Figure vs. Frequency (1)



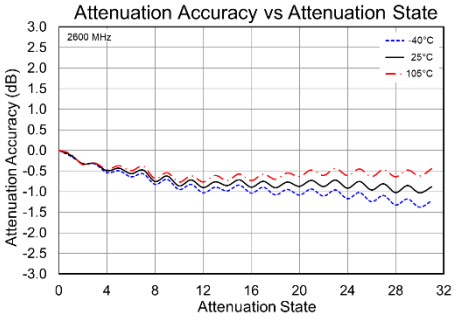
OIP3 vs. Frequency



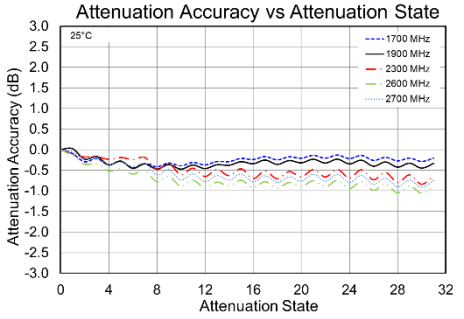
Output P1dB vs. Frequency



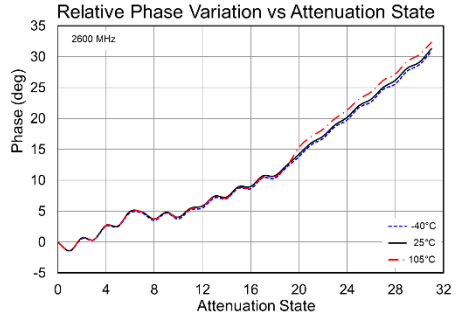
Attenuation Accuracy vs Attenuation State



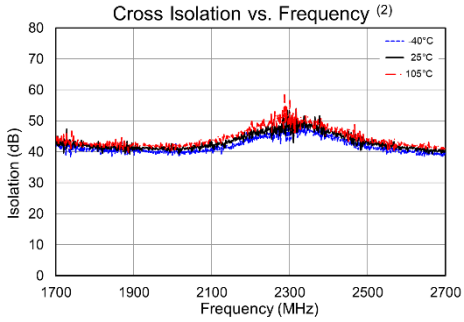
Attenuation Accuracy vs Attenuation State



Relative Phase Variation vs Attenuation State

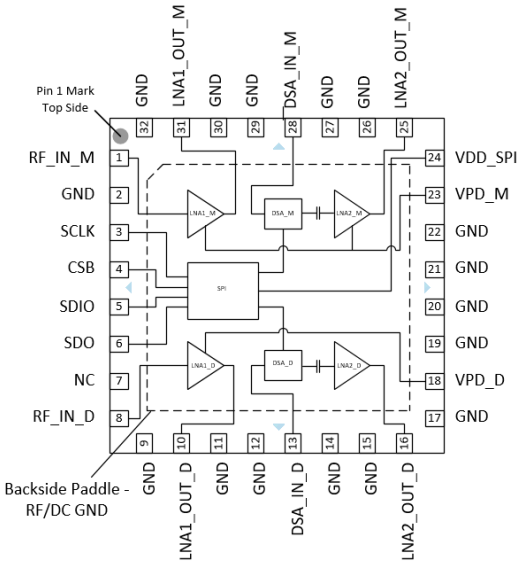


Cross Isolation vs. Frequency (2)



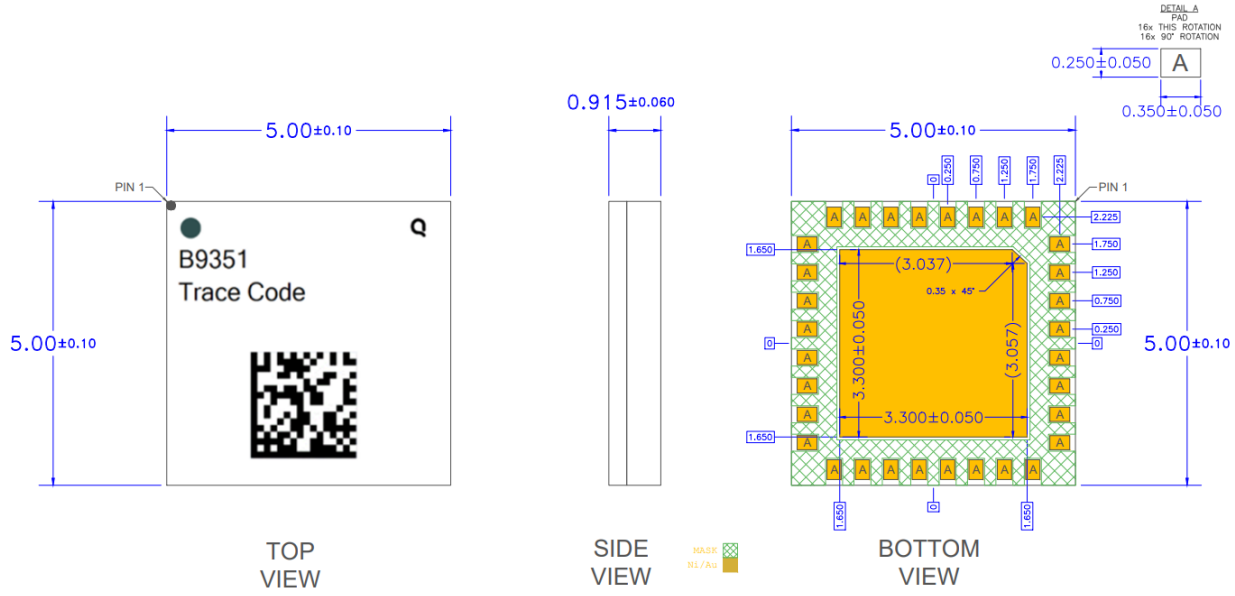
Notes:
1. Trace loss de-embedded from Noise Figure data.
2. Cross Isolation is defined as S21-S41 or S43-S23, where Port 1 is RF_IN_M Port 2 is LNA2_OUT_M, Port3 is RF_IN_D & Port4 is LNA2_OUT_D.

Pin Configuration and Description



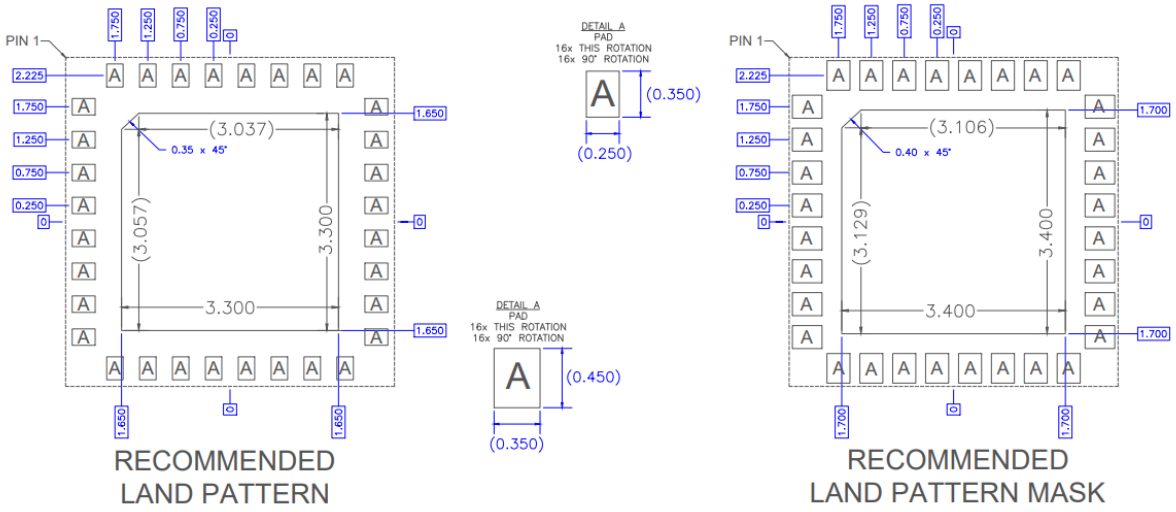
Pin No.	Label	Description
1	RFIN_M	LNA1 input for main channel. Band-specific matching circuit can be employed to optimize performance. External DC block required.
3	SCLK	Serial Clock
4	CSB	Chip select bit
5	SDIO	Serial input data
7	NC	No Internal connection. Can be grounded for mounting integrity.
6	SDO	Serial Output Data
8	RFIN_D	LNA1 input for diversity channel. Band-specific matching circuit can be employed to optimize performance. External DC block required.
10	LNA1_OUT_D	LNA1 output and DC bias on diversity channel. Band-specific matching circuit can be employed to optimize performance. External choke and DC block required.
13	DSA_IN_D	RF input to DSA on main channel. Band-specific matching circuit can be employed to optimize performance. External DC block required.
16	LNA2_OUT_D	LNA2 output and DC bias on diversity channel. Band-specific matching circuit can be employed to optimize performance. External choke and DC block required.
18	VPD_D	Power down control pin for LNAs on diversity channel for TDD operation.
23	VPD_M	Power down control pin for LNAs on main channel for TDD operation.
24	VDD_SPI	DC supply pin to SPI chip. Also, the supply to the DSA dies. Recommend turning this ON before the serial lines come ON.
25	LNA2_OUT_M	LNA2 output and DC bias on main channel. Band-specific matching circuit can be employed to optimize performance. External choke and DC block required.
28	DSA_IN_M	RF input to DSA on diversity channel. Band-specific matching circuit can be employed to optimize performance. External DC block required.
31	LNA1_OUT_M	LNA1 output and DC bias on main channel. Band-specific matching circuit can be employed to optimize performance. External choke and DC block required.
2, 9, 11, 12, 14, 15, 17, 19, 20, 21, 22, 26, 27, 29, 30, 32, Backside Paddle	GND	Internally grounded pins. Use recommended via pattern to minimize inductance and thermal resistance. See PCB Mounting Pattern for suggested footprint.

Package Marking and Dimensions



Notes:
1. All dimensions are in millimeters. Angles are in degrees.
2. Dimension and tolerance formats conform to ASME Y14.4M-1994.
3. The terminal #1 identifier and terminal numbering conform to JESD 95-1 SPP-012.

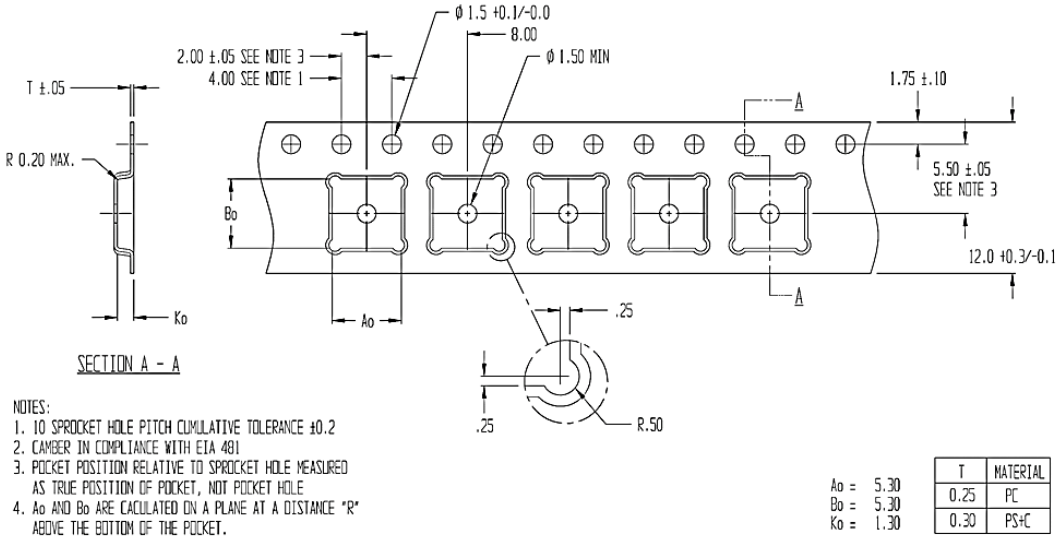
Recommended PCB Layout Pattern



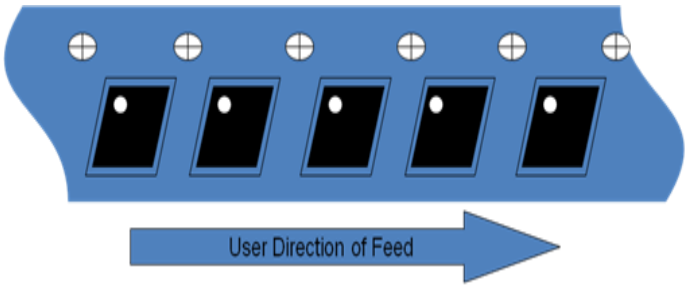
Notes:
1. All dimensions are in millimeters. Angles are in degrees.
2. Use 1 oz. copper minimum for top and bottom layer metal.
3. Via holes are required under the backside paddle of this device for proper RF/DC grounding and thermal dissipation. We recommend a 0.35mm (#80/.0135") diameter bit for drilling via holes and a final plated thru diameter of 0.25 mm (0.01").
4. Ensure good package backside paddle solder attach for reliable operation and best electrical performance.

Tape and Reel Information – Carrier and Cover Tape Dimensions

Tape and reel specifications for this part are also available on the Qorvo website.
Standard T/R size = 2500 pieces on a 13” reel.

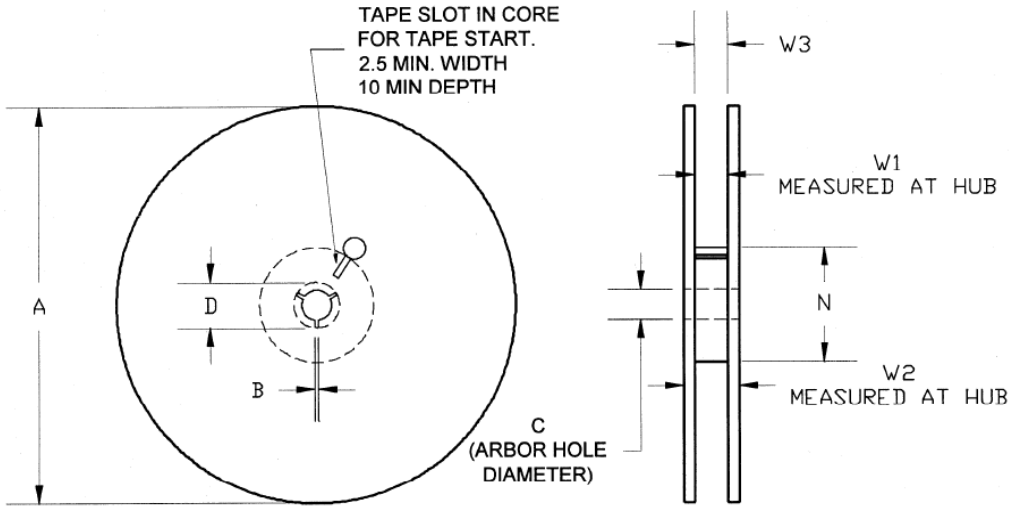


Feature	Measure	Symbol	Size (in)	Size (mm)
Cavity	Length	A0	0.209	5.30
	Width	B0	0.209	5.30
	Depth	K0	0.051	1.30
	Pitch	(P1)	0.315	8.00
Centerline Distance	Cavity to Perforation - Length Direction	(P2)	0.079	2.00
	Cavity to Perforation - Width Direction	(F)	0.217	5.50
Carrier Tape	Width	(W)	0.472	12.0
Cover Tape	Width	(C)	0.362	9.20



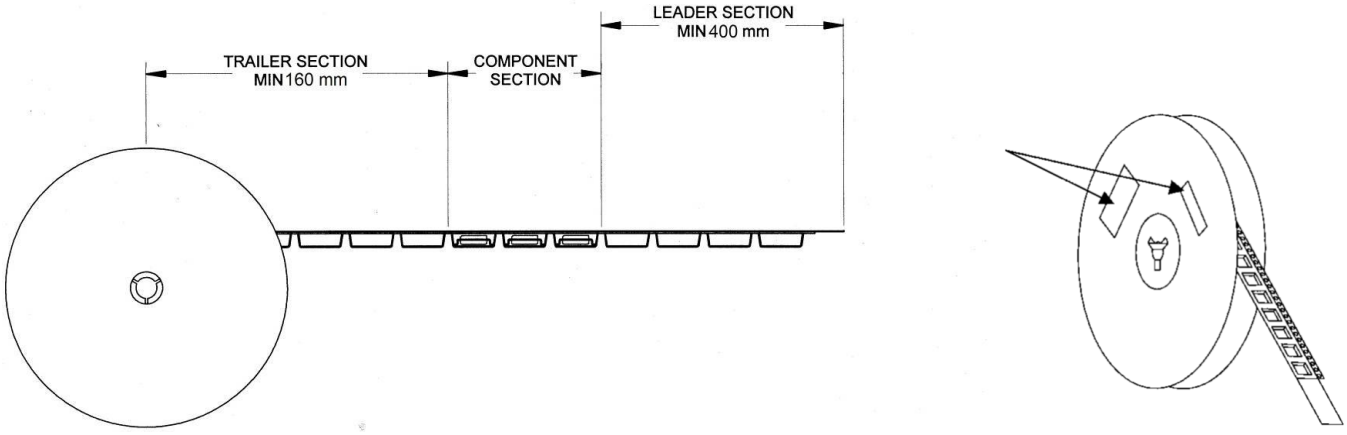
Tape and Reel Information – Reel Dimensions

Tape and reel specifications for this part are also available on the Qorvo website.
Standard T/R size = 2500 pieces on a 13” reel.



Feature	Measure	Symbol	Size (in)	Size (mm)
Flange	Diameter	A	12.992	330
	Thickness	W2	0.717	18.2
	Space Between Flange	W1	0.504	12.8
Hub	Outer Diameter	N	4.016	102.0
	Arbor Hole Diameter	C	0.512	13.0
	Key Slit Width	B	0.079	2.0
	Key Slit Diameter	D	0.787	20.0

Tape and Reel Information – Tape Length and Label Placement



Notes:
1. Empty part cavities at the trailing and leading ends are sealed with cover tape. See EIA 481-1-A.
2. Labels are placed on the flange opposite the sprockets in the carrier tape.

Handling Precautions

Parameter	Rating	Standard
ESD – Human Body Model (HBM)	1B	ESDA / JEDEC JS-001-2012
ESD – Charged Device Model (CDM)	C3	JEDEC JESD22-C101F
MSL – Moisture Sensitivity Level	3	IPC/JEDEC J-STD-020

Caution!
ESD-Sensitive Device

Solderability

Compatible with both lead-free (260°C max. reflow temp.) and tin/lead (245°C max. reflow temp.) soldering processes.
Solder profiles available upon request.

Contact plating: Electroless NiPdAu *(Thickness: Ni(0.40 ± 0.10 µm), Pd(0.145 ± 0.035 µm), Au(0.095 ± 0.025 µm))*

RoHS Compliance

This part is compliant with the 2011/65/EU RoHS directive (Restrictions on the Use of Certain Hazardous Substances in Electrical and Electronic Equipment) as amended by Directive 2015/863/EU. This product also has the following attributes:

- Product uses RoHS Exemption 7c-I to meet RoHS Compliance requirements.
- Halogen Free (Chlorine, Bromine)
- Antimony Free
- PFOS Free
- TBBP-A ($C_{15}H_{12}Br_4O_2$) Free
- SVHC Free

Contact Information

For the latest specifications, additional product information, worldwide sales and distribution locations:

Web: www.qorvo.com
Tel: 1-844-890-8163
Email: customer.support@qorvo.com

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