# Increasing Range Using an External LNA

DW3000/QM33100

Application Note

## 1 Introduction

This application note provides an overview of an Ultra-Wideband (UWB) wireless transceiver communication system and link budget. The document reviews UWB transceiver performance, focusing on the receiver cascaded system noise figure and overall system sensitivity improvements, both with and without an external discrete Low Noise Amplifier (LNA) and Band-Pass Filter (BPF).

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## 1.1 Overview

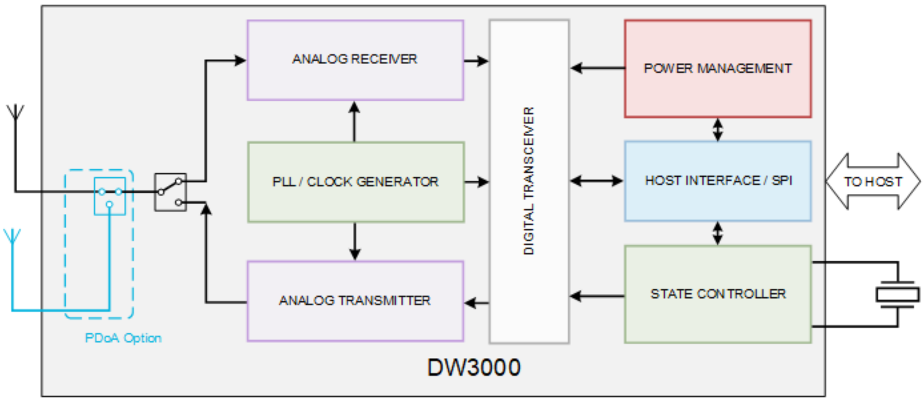


**Figure 1: DW3000 high level function diagram**

In any wireless communications system, the link budget is determined by several factors. These include:

- Transmitted power level
- Transmitter antenna gain
- Losses in the propagation channel (e.g. over the air)
- Receiver antenna gain
- Receiver sensitivity

QM33100 [1] and DW3000 [2] have a receiver sensitivity of between -92.6 dBm and -102.6 dBm depending on the chosen configuration parameters (data rate), hardware setup (carrier frequency offset between TX and RX nodes) and the acceptable system performance limits for particular applications (acceptable packet error rate, for example).

The transmit output power of the QM33100 and DW3000 are limited by design to a maximum value of -31 dBm/MHz. This is more than adequate to meet the regulatory maximum limit of -41.3 dBm/MHz. That limit applies in most countries where UWB is permitted and provides some margin to allow for PCB, temperature, antenna and enclosure losses.

Although the QM33100 and DW3000 have an internal LNA, it is possible to improve the noise figure and consequently the sensitivity of the receiver by adding an external LNA to the front end. Choosing an LNA with a low noise figure and high gain is important.

The insertion of an LNA amplifier into the receiver path, between the antenna and the RF pins on the QM33100 and DW3000, can typically result in a 4 to 6 dB improvement in receiver sensitivity.

## 1.2 Hardware and Software Modifications

The QM33100/DW3000 has been designed to provide the necessary signals to control an external LNA. These signals can control LNA power supply switching and RF switches to select between transmit and receive paths.

The hardware required is discussed in section 2 while the software modifications to enable the operation of the external circuitry are discussed in section 3.

# 2 Hardware Description

## 2.1 Overview

The basic scheme for incorporating an LNA into the QM33100/DW3000 receive/transmit path is illustrated in Figure 2, below:

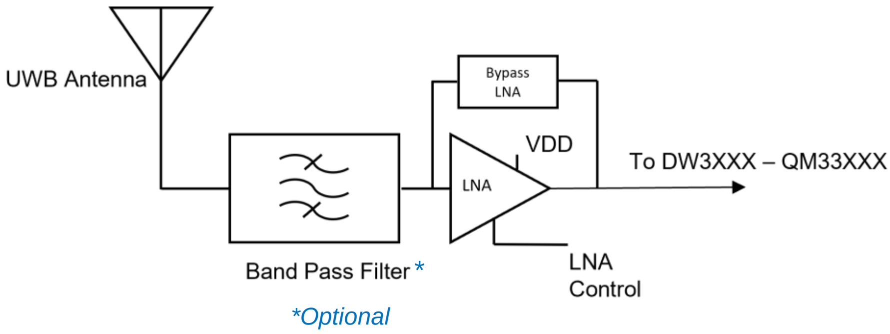


**Figure 2: Basic scheme for incorporating an LNA**

The noise figure of the LNA must be lower than the noise figure of the DW3000/QM33100. The LNA can provide 10 to 30 dB of gain depending on the channel frequency and the amplifier used.

Adding a BPF between the antenna and the LNA is important to support Japan regulatory tests, where spurious emissions from the transmitter are measured in conducted mode. The BPF also improves resilience to desensitization of the receiver due to out-of-band blockers, such as Wi-Fi signals. On the other hand, the BPF's additional insertion loss has an obvious downside in terms of reduced Tx power headroom and receiver sensitivity (see section 4.2). The inclusion of the BPF is therefore considered optional.

SPDT switches are used to bypass the LNA when transmitting UWB frames. Qorvo offers the QM14068 LNA [3] with a bypass function designed and optimized for UWB channels 5 and 9. The basic scheme for incorporating a QM14068 LNA with DW3000/QM33100 transceivers is given in Figure 3, below.

Recommended BPF components are referenced in section 2.7 of this document.

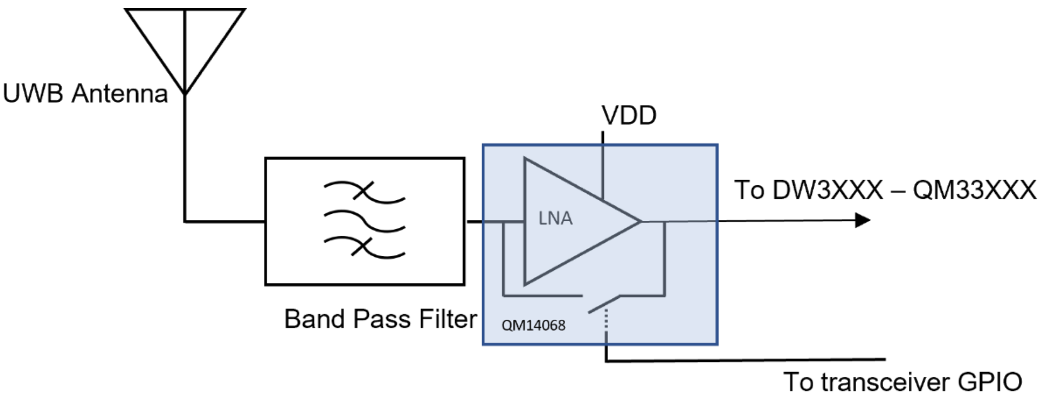


**Figure 3: Basic scheme for using QM14068 LNA with DW3000/QM33100**

## 2.2 Designing an LNA Scheme

The sensitivity of a receiver (S) is a function of its noise figure (NF), the minimum required signal-to-noise ratio for detection of the modulation and the thermal noise of the system. S can be written as:

$$S = NF + n_0 + \frac{S}{N}$$

**Equation 1: Receiver Sensitivity**

where $n_0$ is the thermal noise power of the receiver in dBm.

At room temperature (T = 290°K), in a 1 Hz bandwidth, $n_0 = -174\ dBm$. For a 500 MHz channel bandwidth, $n_0 = -119\ dBm$. $\frac{S}{N}$ is the required output signal-to-noise ratio for detection of the modulation.

The QM33100 and DW3000 have a noise figure of 7 to 8 dB depending on the channel and the frame parameters. The sensitivity of the DW3000 receiver is between -93.2 dBm and -100 dBm and for the QM33100, between -92.8 dBm and -102.6 dBm.

Let us consider adding an LNA to the input of our transceiver. The overall sensitivity of the system can be written as:

$$S_{WithLNA} = NF_{WithLNA} + n_0 + \frac{S}{N}$$

**Equation 2: Overall system sensitivity**

$NF_{WithLNA}$ corresponds to the cascade of the LNA and transceiver. Referring to Equation 1 and Equation 2:

$$\Delta_S = NF_{QM33} - NF_{WithLNA}$$

**Equation 3: Change in system sensitivity**

Thus, the overall increase in the sensitivity of the transceiver depends on the noise figure of the amplifying stage. The lower the noise figure of the stages between the antenna and the transceiver, the greater the increase in receiver sensitivity.

The LNA circuitry should be designed to give the lowest noise figure while not compressing the receiver's internal LNA. The strongest receiver signal presented to the QM33100 should not exceed -25.4 dBm for channel 5 and -27.1 dBm for channel 9. For the DW3000 this signal should not exceed -25 dBm for channel 5 and -32 dBm for channel 9.

### 2.2.1 Calculating the Noise Figure

The QM33100 and DW3000 receivers have a typical antenna referenced noise figure between 7 and 8 dB. The design of the external LNA scheme should aim to reduce this noise figure to 4 to 6 dB, giving a corresponding 4 to 6 dB improvement in sensitivity.

To calculate the improvement (reduction) in noise figure we need to use the cascade formula for noise factor.

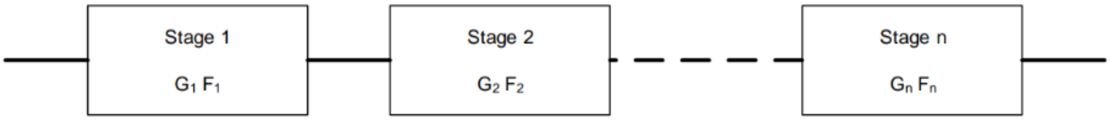


**Figure 4: Cascaded gain stages**

In the general case of a cascade of n devices, as depicted in Figure 4, the total noise factor is given by:

$$F_{total} = F_1 + \frac{F_2 - 1}{G_1} + \frac{F_3 - 1}{G_1 G_2} + \cdots + \frac{F_n - 1}{G_1 G_2 \ldots\ G_n}$$

**Equation 4: Total noise factor**

where:

- $F_{total}$ is the total noise factor (to be converted to a noise figure)
- $F_n$ is the noise factor of stage $n$
- $G_n$ is the linear gain of stage $n$

Noise factor $(F)$ is converted to a noise figure $(NF)$ using the formula below:

$$NF = 10 \log_{10} F$$

### 2.2.2 Example of Noise Figure Calculation

Taking the scheme shown in Figure 3, above, we have a BPF and an LNA followed by the DW3000/QM33100 transceiver. The table below gives some typical gain and NF values for these stages and converts them into linear gain and noise factor. In this example we will consider trace losses in the connection between stages to be 0 dB. Short trace length between LNA and antenna will minimize the trace losses and provide a lower total noise figure.

**Table 1: Example RX stage specifications**

| | Stage | | |
|---|---|---|---|
| **Parameter** | **BPF** | **LNA (QM14068)** | **Receiver IC (DW3000/QM33100)** |
| Gain (linear) | 0.83 | 31.62 | - |
| Gain (dB) | -0.8 | 15 | - |
| Noise Factor | 1.2 | 1.51 | 5.01 |
| Noise Figure (dB) | 0.8 | 1.8 | 8 |

Inserting the linear gain and noise factor values, shown in Table 1, into Equation 4, we can calculate the overall receiver noise figure:

$$F_{total} = 2.02$$

$$NF_{total} = 3.06\,dB$$

This is a 5 dB reduction in overall noise figure compared to the case with no LNA since the QM33100 and DW3000 have a noise figure of 8 dB. Referring to Equation 3, the 5 dB $NF$ reduction will result in 5 dB improvement in the receiver sensitivity.

### 2.2.3 Dynamic Range Calculation

The NF is a key parameter when designing a front end with an LNA. Nevertheless, we must also ensure that the amplifying stage gain is not compressing the DW3000/QM33100 receiver. The strongest receiver signal presented to the QM33100 should not exceed -25.4 dBm for channel 5 and -27.1 dBm for channel 9.

The following formula can be used to check that this condition is met.

$$RSL_{max} = Tx_{pwr} + Tx_{antgain} - Prop_{Loss} + Rx_{antgain} + LNA_{gain} - BPF_{loss}$$

where:

$RSL_{max}$ is the maximum signal at the QM33100 input,

$Tx_{pwr}$ is the EIRP at the output of the transmitter antenna,

$LNA_{gain}$ is the gain of the external LNA,

$Prop_{Loss}$ is the propagation loss in free space,

$BPF_{loss}$ is the insertion loss of the BPF,

$Tx_{antgain}$ and $Rx_{antgain}$ are the gain of the transmitter and the receiver antenna, respectively.

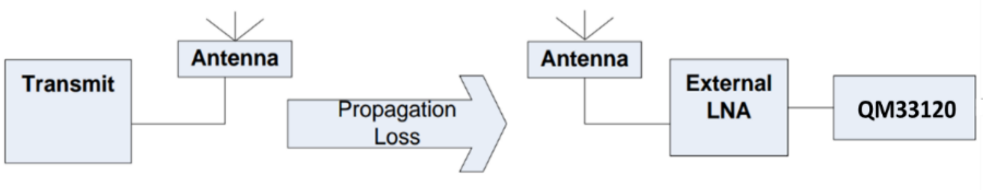


**Figure 5: Link budget calculation**

### 2.2.4 Example Calculation of Highest Supportable Signal Power

Taking the line-up shown in Figure 2, we have a BPF and an LNA followed by the QM33100. If we use the LNA gain value from the previous example (15 dB) and assume channel 9 operation at 1 m separation between receiver and transmitter, a transmitter $Tx_{pwr} = -14.3\, dBm/500Mhz$ and $0\, dBi$ antenna gain for both transmitter and receiver, then we have:

$$RSL_{max} = -14.3 + 0 - 50.5 + 0 + 15$$

$$RSL_{max} = -49.8\, dBm$$

This gives us a margin of:

$$P1dB_{QM33120} - RSL_{max} = 23\, dB$$

For very short distances between the receiver and the transmitter, the LNA may saturate. For example, with 7 cm separation the propagation loss for UWB channel 9 is 27.5 dB. The receiver will be operating very close to its compression point.

Note that the maximum transmitted power used for this calculation is -14.3 dBm/500MHz. This value is extrapolated from the FCC specification for max-mean power limit per 1 MHz (-41.3 dBm/MHz). In practice, the maximum output power will be around -16 dBm/500MHz, due to the natural sloping of the transmit spectrum at the sides.

## 2.3 Control Signals

The DW3000/QM33100 transceiver provides GPIO signals to control switching of the path between the transceiver RF pins and the antenna, to include or exclude the LNA, depending on whether the transceiver is in RX or TX mode.

**Table 2: Control signals**

| Chip | Signal Name | I/O | Description |
|---|---|---|---|
| DW3000 | GPIO6 / EXTRXE / SPIPOL | DIO | General Purpose I/O pin.<br>On power-up it acts as the SPIPHA (SPI phase selection) pin for configuring the SPI mode of operation.<br>It may be configured for use as EXTRXE (External Receiver Enable).<br><br>This pin goes high when the DW3000 is in receive mode.<br>After power-up, the pin will default to a General Purpose I/O pin |
| QM33100 | GPIO5 / COEXOUT / EXTRXE | DIO | General Purpose I/O pin.<br>After power-up this pin will default to a General Purpose I/O pin.<br><br>Can be configured for use either as:<br>COEX_OUT<br>an output that can be configured via software to indicate an RX, TX, or both.<br>or<br>PDoA_SW1<br>An output that goes high 100ns before the start of RX |

## 2.4 Power Supplies

If an LNA is added to the UWB RF front-end, it is important that adequate decoupling is provided to keep the supply "quiet" and avoid injecting noise into the receiver. The LNA manufacturer's recommendations should be followed in this regard.

## 2.5 Detailed Schematic

The schematic using a QM14068 is shown in Figure 6. The QM14068 requires a control signal to select between high gain mode or bypass mode. AC coupling is used throughout to remove DC components in the signal.

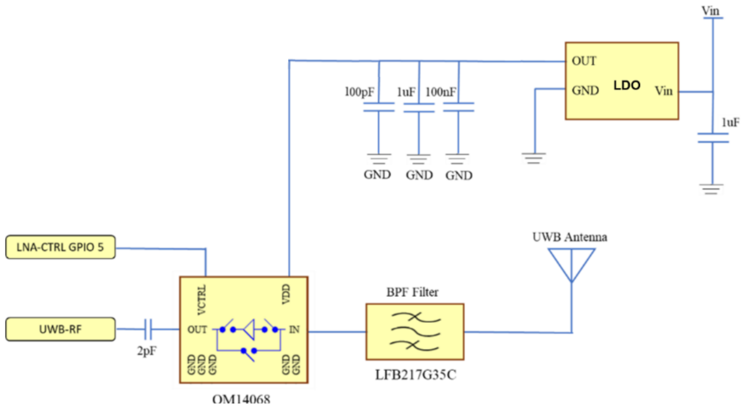


**Figure 6: Hardware schematic using QM14068 and DW3000/QM33100**

## 2.6 RF Paths and PCB Layout

The frequency of the RF signals (6.25 – 8.25 GHz) and the bandwidths (500 MHz) are high, so attention must be paid to the RF signal trace layout.

Switching RF signals at these frequencies is challenging. To prevent a significant reduction in performance, great care must be paid to following RF PCB layout guidelines and the avoidance of discontinuities in RF traces. Refer to application note APH301 [4] for hardware design guidelines. The use of an LNA with an internal switch avoids routing more RF lines.

Generally, the front-end circuit is printed on classic FR4 substrate. Losses can be high for long lines and the insertional loss will directly add to the overall NF of the receiver.

## 2.7 List of Suitable Components

The BPFs listed below can be used.

**Table 3: Recommended band-pass filters**

| Vendor | Part No. |
|---|---|
| Murata | LFB217G35CFHE826 |
| TDK | DEA167240BT |
| Johanson Technology | 7240BP15B2000E-AEC |
| Mini Circuits | LFCN-9170+ (LPF)* |

**A low-pass filter, included if only harmonics suppression is needed.*

# 3 Software Implementation

## 3.1 Introduction

There is little software interaction required to control an external LNA. Because the DW3000/QM33100 hardware supports this mode of operation, the software simply needs to enable the relevant portions of the hardware.

Enabling the hardware consists of correctly configuring the relevant GPIO pin to act as the control for the external RF switches. GPIO pins are configured via the GPIO mode control register.

## 3.2 Register Programming

The GPIO mode control register is a 32-bit register:

| REG:05:00 – GPIO_MODE – GPIO mode control register | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| - | - | - | - | - | MSGP8 | | | MSGP7 | | | MSGP6 | | | MSGP5 | | | MSGP4 | | | MSGP3 | | | MSGP2 | | | MSGP1 | | | MSGP0 | | |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

When using the QM33100 family, we need to set field MSGP5 to 010:

| Field | Description of fields within REG:05:00 GPIO_MODE |
|---|---|
| MSGP5<br><br>reg: 05:00<br>bits: 17-15 | Mode Selection for GPIO5/COEXOUT. Allowed values are:<br>000: The pin operates as GPIO5 – This is the default (reset) state.<br>001 : The pin is configured for use as COEX_OUT.<br>010 : The pin is configured for use as AOA_SW_1.<br>011 : The pin is configured for use as dbg_mux_5.<br>100 – 111: Reserved. Do not select this value |

**Table 4: QM33100 Register**

When using the DW3000 family, set MSGP6 to 001:

| Field | Description of fields within REG:05:00 GPIO_MODE |
|---|---|
| MSGP6<br><br>reg: 05:00<br>bits: 20-18 | Mode Selection forGPIO6/EXTRXE. Allowed values of MSGP6 are:<br>000: The pin operates as GPIO6– This is the default (reset) state.<br>001: The pin is configured for use as EXTRXE (External Receiver Enable). This pin goes high when the DW3000 is in receive mode.<br>010 – 111: Reserved. Do not select this value. |

**Table 5: DW3000 Register**

### 3.3 Source Code Changes

To enable the GPIO for external LNA functionality, we need to call the function:

```
void dwt_setlnapamode (int lna_pa)
```

**Parameters:**

| Type | Name | Description |
|---|---|---|
| int | lna_pa | This parameter is treated as a bit field.<br>If bit 0 is set (DWT_LNA_ENABLE), it will enable LNA functionality.<br>If bit 1 is set (DWT_PA_ENABLE), it will enable PA functionality.<br>If bit 2 is set (DWT_TXRX_EN), it will enable RX/TX sampling on GPIOs 0 & 1.<br>To disable LNA/PA functionality, set bits 0 and 1 to 0. |

**Return Parameters:**

none

Please also refer to the QM33100 Software API Guide for details on the *setlnapamode()* function.

# 4 Other Considerations

## 4.1 Effect on Antenna Delay and Antenna Calibration

Adding an LNA and its associated internal or external RF switches in the RF path, between the antenna and the DW3000/QM33100, introduces additional delay and affects the timestamps of the exchanged frames. This additional delay needs to be calibrated-out during the antenna delay calibration process, as discussed in [5]. It is important when choosing an LNA that this additional delay remains constant over the expected operating parameter range (voltage, temperature) for a given channel.

## 4.2 Effect on Transmitter Maximum Power

The insertion loss of QM14068 in bypass mode followed by a BPF could be around 2.5 dB. This will reduce the maximum output power in TX mode and increase the total noise figure of the receiver.

## 4.3 Potential Receiver Saturation

When a transmitter is near a receiver with an LNA, the incident signal power at the RF pins can be so strong as to saturate the DW3000/QM33100 receiver and drive it into compression. This can result in incorrect operation and an increase in packet error rate. Special care should be taken to ensure that such a situation does not arise if an LNA is being used.

Systems in which transmitting nodes come very close to receiving nodes should either not use LNAs or else dynamically alter LNA gain to avoid receiver saturation.

## 4.4 RF Blocking Performance

The RF blocking performance of the receiver will be degraded at least by the amount of the gain of the LNA. At certain frequencies, such as half of the carrier frequency, this degradation can be even worse. Degradation occurs mainly because the LNA produces harmonics at the output and the second and third harmonics of the incoming signal can fall at in-band frequencies. To avoid this, the band-pass filter can be used to attenuate potential blockers.

## References


[1] Qorvo, "QM33100 Datasheet".
[2] Qorvo, "DW3000 Datasheet".
[3] Qorvo, "QM14068 Datasheet".
[4] Qorvo, "APH301 Hardware Design Guide".
[5] Qorvo, "APS014 Antenna Delay Calibration of DW1000 Systems".


## Abbreviations

| | |
|---|---|
| AC | Alternating Current |
| BPF | Band-Pass Filter |
| DC | Direct Current |
| DIO | Digital Input Output |
| EIRP | Equivalent Isotropic Radiated Power |
| GPIO | General Purpose Input Output |
| LNA | Low-Noise Amplifier |
| LPF | Low-Pass Filter |
| PCB | Printed Circuit Board |
| RF | Radio Frequency |
| RX | Receive |
| SPDT | Single-Pole Double-Throw |
| TX | Transmit |
| UWB | Ultrawide Band |

## Important Notices



## Document History

| Rev | Date | Section | Changes |
|---|---|---|---|
| 1.0 | 13 Feb 2024 | | Initial release. |