APPLICATION NOTE

APH301

Hardware Design Guide for DW3000 and QM33100 Series ICs

Referenced Documents

The reference documents below take precedence over the contents of this application note and should always be consulted for the latest information.

DW3000 Data Sheet

DW3000 User Manual

QM33100 Data Sheet

QM33100 User Manual

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1 Overview

1.1 Introduction

Guidelines for successful hardware design of systems using the DW3000 and QM33100 UWB transceiver ICs are presented in this application note. The DW3000 series has two package options; WLCSP and QFN. The QM33100 is available in the WLCSP package, which is identical to the DW3000 WLCSP package option. Hardware design guidelines for both package types are included in this document.

The ICs are categorised by the number of RF ports (i.e. with or without AoA), IC package type and ability to support an additional alternative UWB pulse shape.

IC Variant	Type of Package	Number of Pins	AoA support (Single or Double RF Ports)	UWB Pulse Shape
DW3110	WLCSP	52	No	Default
DW3120	WLCSP	52	Yes	Default
DW3210	QFN	40	No	Default
DW3220	QFN	40	Yes	Default
QM33110W	WLCSP	52	No	Default, Alternative
QM33120	WLCSP	52	Yes	Default, Alternative

Table 1. List of part numbers

Included in this document are typical application circuits, a recommended PCB specification, power supply routing advice and PCB layout guidelines. Layout graphics for the QM33120WEVB evaluation board are also provided.

Application note APH001, for the Qorvo DW1000 UWB transceiver IC provides general recommendations about power management, capacitive decoupling, RF connectors, RF layout, antenna design and electromagnetic interference [1]. This is also a useful document to consult before starting a design.

2 Hardware System Overview

2.1 System Block Diagram

A simplified system block diagram of an example system for DW3000/QM33100 is given in Figure 1. An antenna connects to the IC's RF port to provide the radio air interface for both receive and transmit operations, while a host microcontroller (MCU) processes data and controls the DW3000 via the serial peripheral interface (SPI) and GPIO interfaces. Optional front-end components are also shown, which can enhance the RF performance of the IC in terms of increasing communication range.

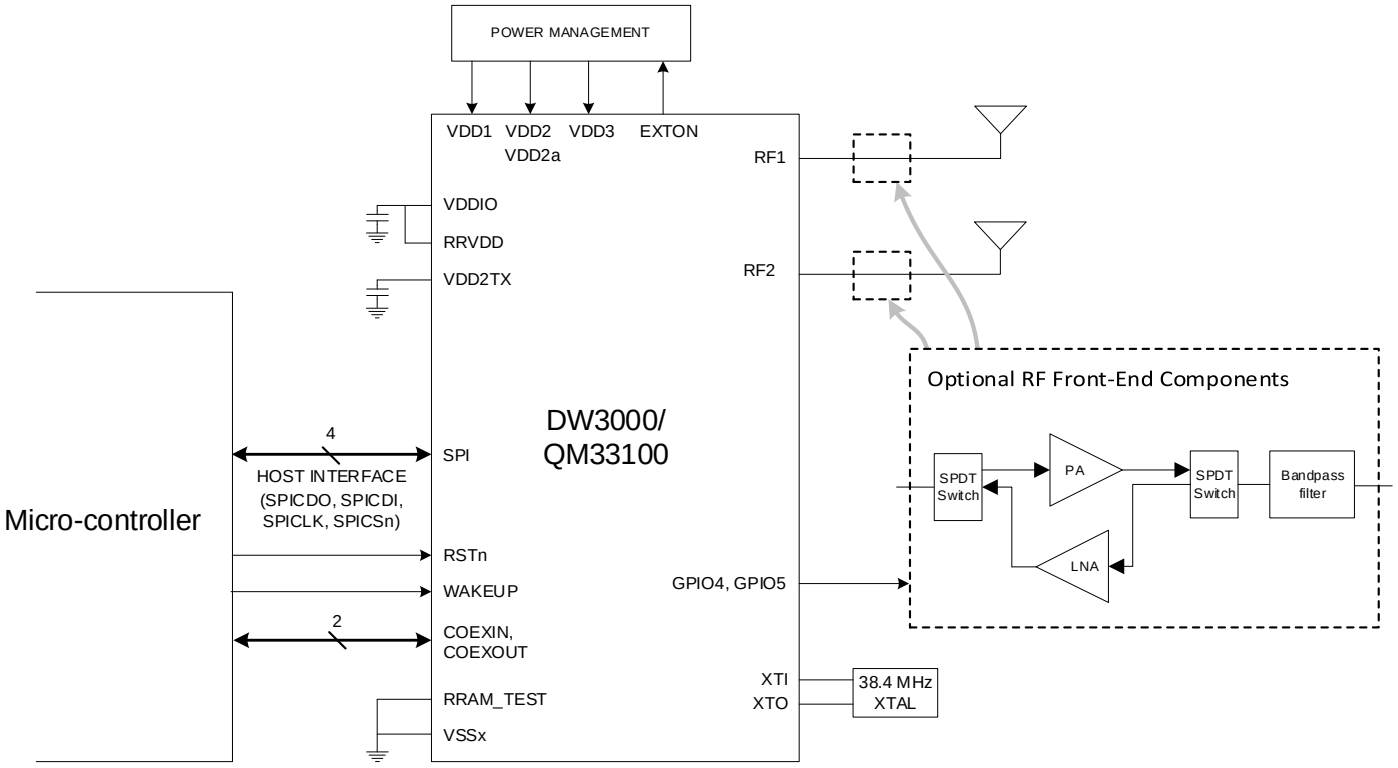


Figure 1. System block diagram

2.2 Application Circuits

Application circuits for both QFN and WLCSP versions of the DW3000 and QM33100 ICs are shown in Figure 2 and Figure 3. A general description of the external components used is as follows.

- ***Power Supplies and Decoupling:***
  The ICs have four power supply pins, with nominal voltage ranges and required decoupling components as indicated in Table 2.

Power Supply Pin	Voltage (V)			Decoupling
	Min	Typ	Max	
VDD1	1.62	3.0	3.6	100 nF
VDD2a	2.4	3.0	3.6	4.7 nF, Ferrite Bead
VDD2b				4.7 nF, 100 nF, 10 uF
VDD3	1.5	3.0	3.6	4.7 nF, 100 nF, 10 uF

Table 2. Power supply voltage ranges

  External capacitors are required to be connected at pins VIO_D and VTX_D, for decoupling of internal regulators.

- ***Voltage Regulators:***
  Since the VDD3 power rail can be supplied with a lower voltage than the VDD2 rail, it's common to use a voltage regulator, such as a DCDC converter, to supply the VDD3 pin at a lower voltage, such as 1.8 V. This is a way to reduce the power consumption of the overall system.

- ***RF Front-End:***
  Series capacitors are placed in the RF paths next to pins RF1 and RF2, for DC blocking purposes. Two RF ports are generally used for angle-of-arrival systems, for which DW3120, DW3220 and QM33120 are suitable. For applications such as two-way ranging (TWR), only one antenna is needed and the DW3110, DW3210 and QM33110 are recommended. For these parts, the RF2 port is unused and should be terminated using a 50 Ω resistor.

  Other RF front-end components, such as low-noise amplifiers (LNA), power amplifiers (PA) or band-pass filters can also be used in UWB systems, in-between the transceiver and the antenna, depending on the application.

- ***Frequency Reference:***
  A commonly-used frequency reference for the internal oscillator circuit is a 38.4 MHz crystal. It's also possible to use a temperature-compensated crystal oscillator (TCXO) or a digital clock signal from another source within the system, such as from a PMIC.

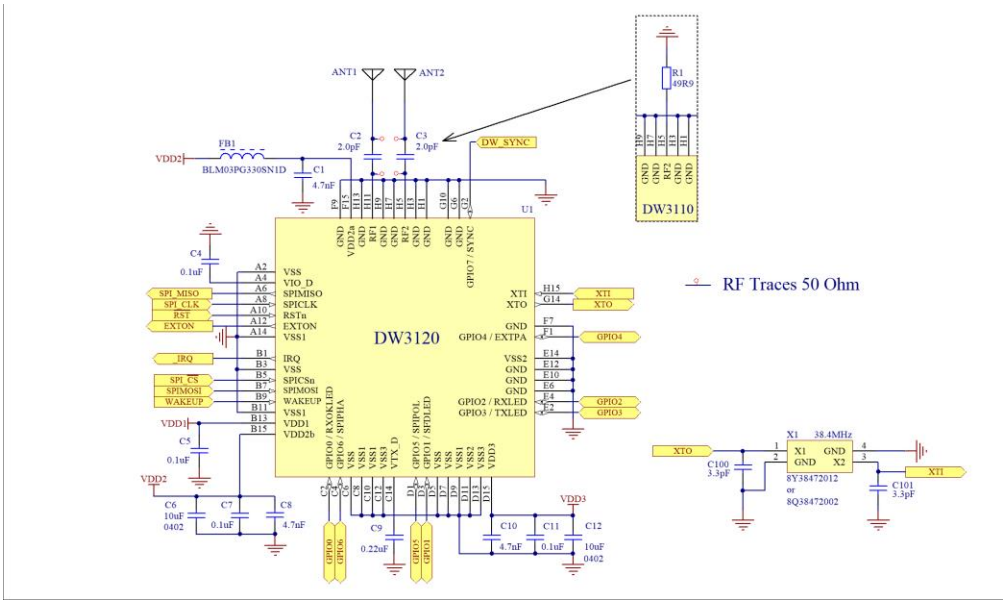


Figure 2. DW3000/QM33100 application circuit for WLCSP package

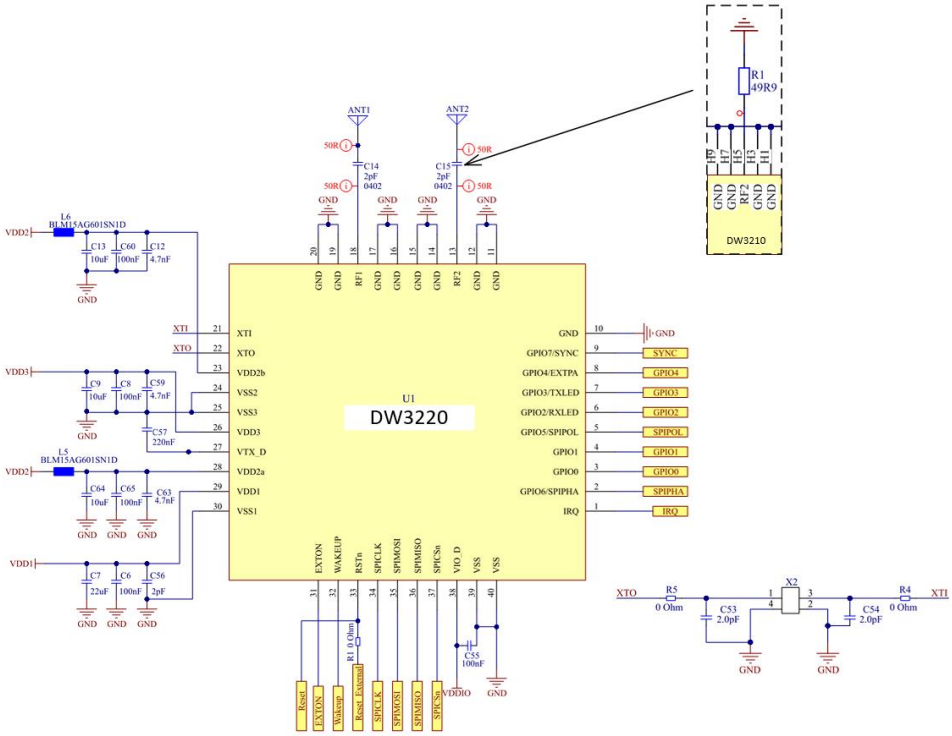


Figure 3. DW3000 application circuit for QFN package

3 PCB Specification

Before starting the design of the PCB, specifications such as the number of layers and area dedicated to the IC and its peripheral components should be determined according to the application type and design requirements. Many applications use a 6-layer PCB stack-up but it is also possible to design a 4-layer PCB. It's not feasible to use fewer than 4 layers, mainly because the width of the 50 Ω RF traces becomes unacceptably wide.

Considering the IC and peripherals are placed on the top layer, the thickness and electrical specifications of the substrate between the top layer and reference layer determine the width of the 50 Ω controlled RF traces. The trace width should also match the width of the IC pads, in order to minimise impedance discontinuity. The RF line width can be determined through consultation with the PCB manufacturer and coplanar or microstrip impedance calculators can be used to ensure the trace impedances are accurate. It is recommended to use an impedance control option with the PCB manufacturer.

3.1 Example PCB Stack-ups

Examples of 4 and 6-layer PCB stack-ups are shown in Figure 4. These are the PCB stack-ups used in Qorvo's QM33120WEVB (6 layer) and DWM3000 (4 layer) board designs.

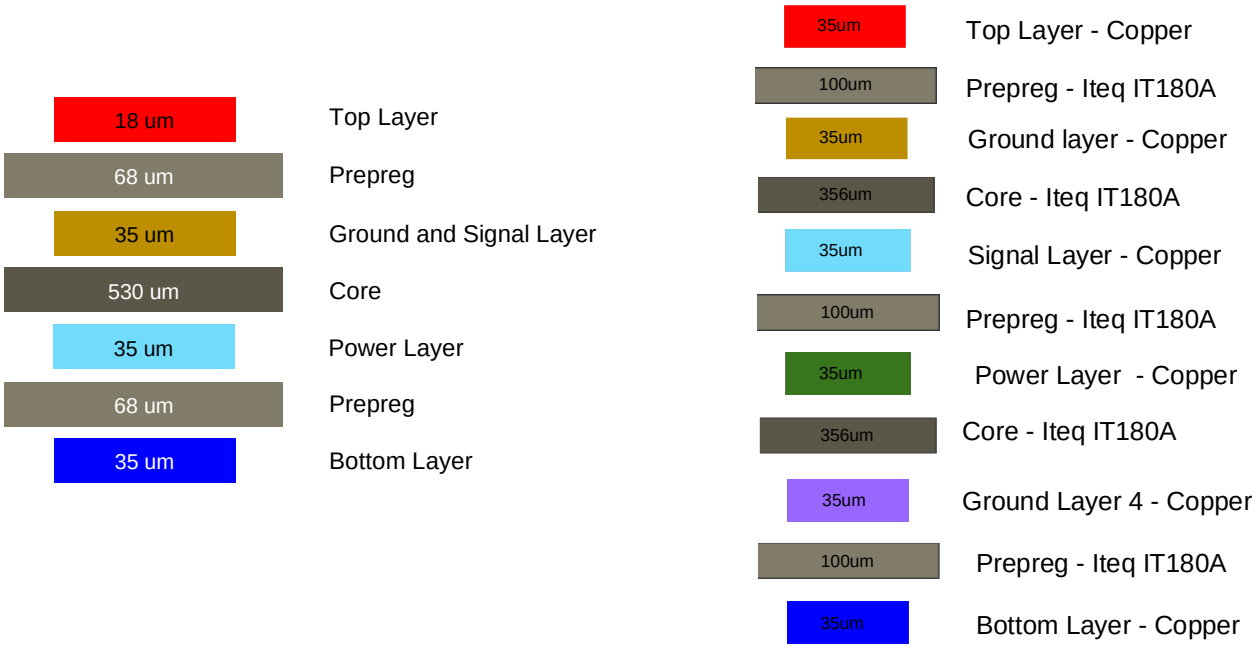


Figure 4. Example 4 and 6-layer PCB stack-ups

In the 4-layer stack-up, due to the decreased number of layers, the second layer serves as both a ground and signal layer. Therefore, special care should be taken when routing signals on this layer such that signal traces should not pass beneath any other trace on the top layer to avoid crosstalk and provide a continuous ground layer for signals on the top layer.

4 Component Placement and Routing

4.1 Power Supply Distribution

The distribution of power supply rails and decoupling component placement is illustrated graphically in Figure 5. To maximise isolation between pins, the power trace leading to each voltage pin is routed in a star topology. For effective decoupling of any high-frequency noise generated within the IC, the decoupling capacitors should be placed in the order of lowest value closest to the pin and higher values further away.

A ferrite bead is required between pins VDD2a and VDD2b, with a suggested impedance of around 33 Ω at 100 MHz.

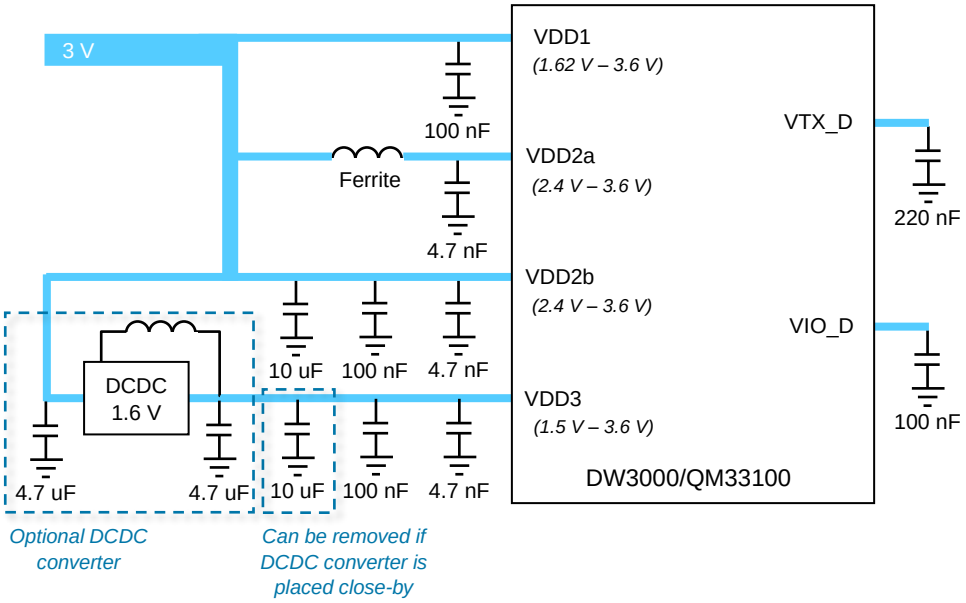


Figure 5. Local power supply distribution

4.1.1 MLCC Capacitance Derating

Multi-layer ceramic capacitors (MLCC) are a popular choice due to their low cost but it's important to consider how their effective capacitance can differ from their nominal value, especially as case sizes reduce. Figure 6 and Table 3 illustrate the extent to which the effective capacitance reduces as the applied DC voltage is increased for 0603, 0402 and 0201 component case sizes.

The data is from a comparison of options from a manufacturer with 1 µF nominal capacitance and 6.3 V and X5R voltage and temperature ratings.

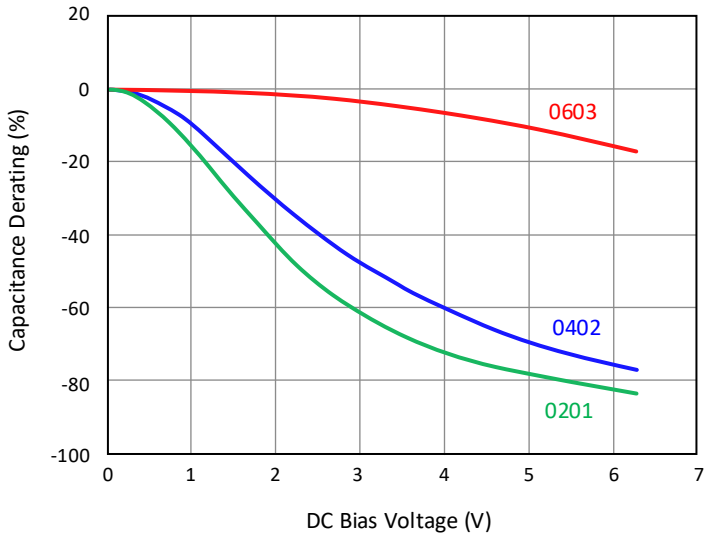


Figure 6. Example capacitance derating with DC voltage

Capacitor Case Size	Dimensions (Typical)		Capacitance Reduction with DC Bias
	Imperial (inches)	Metric (mm)	
0603/1608M	L: 0.06, W: 0.03, T: 0.3	L: 1.6, W: 0.8, T: 0.8	3.3 V: 4.2% (1.0 µF → 0.96 µF) 1.8 V: 0.9% (1.0 µF → 0.99 µF)
0402/1005M	L: 0.04, W: 0.02, T: 0.2	L: 1.0, W: 0.5, T: 0.5	3.3 V: 52% (1.0 µF → 0.48 µF) 1.8 V: 27% (1.0 µF → 0.73 µF)
0201/0603M	L: 0.02, W: 0.01, T: 0.1	L: 0.6, W: 0.3, T: 0.3	3.3 V: 66% (1.0 µF → 0.34 µF) 1.8 V: 37% (1.0 µF → 0.63 µF)

Table 3. Capacitor case sizes and derating

4.2 Component Placement

This section illustrates the arrangement of components in a typical PCB layout using DW3000 or QM33100 in the WLCSP package. The pin configuration is such that the required external components are generally placed to the left-hand side of the IC, as shown in Figure 7. The decoupling components for each power supply pin are colour-coded. The layout shown is from the DWM3000 module design.

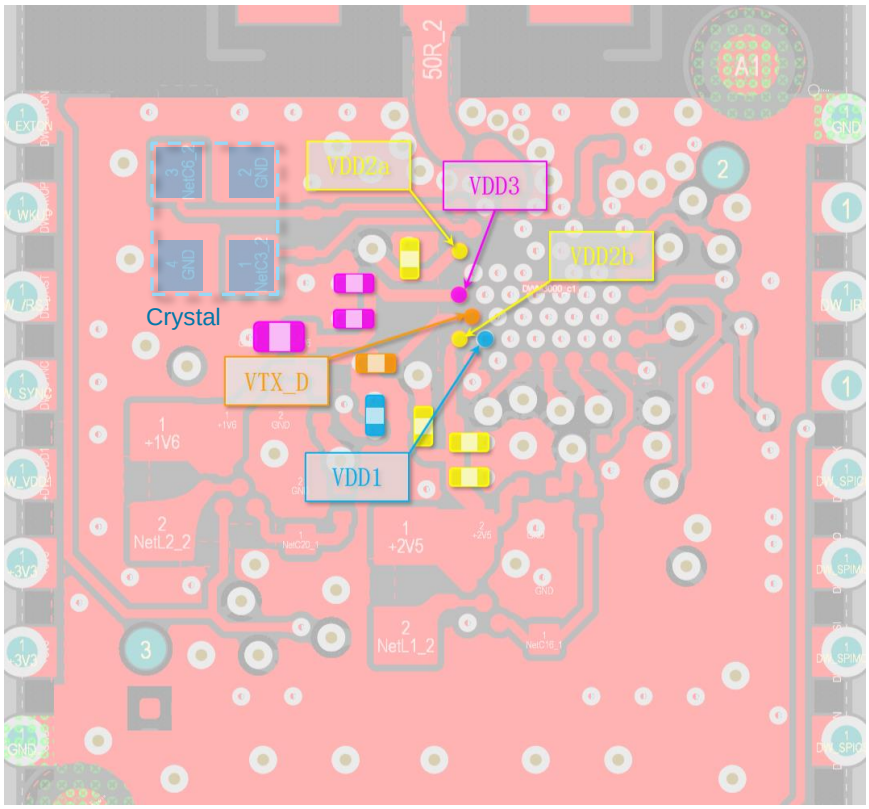


Figure 7. Placement of peripheral components

4.3 Land Patterns and Escape Routing

Examples of PCB land patterns of the ICs and escape routing for WLCSP and QFN package types are shown in Figure 8. In the context of the 6-layer stack-up from Figure 4, certain regions of copper beneath the ICs need to be cut out in order to maintain the 0.25 mm copper-free clearance requirement beneath the ICs. Since the separation of the first prepreg (100 um) is not enough to satisfy this requirement, the ground layer and top layer are removed from the area beneath the IC indicated as 'Cutout Inner Layer 1'. Therefore a 456 um separation is obtained in total.

The pads of the IC have a 10 mil diameter for the WLCSP package and 8 mil width for the QFN package. Therefore, the width of the RF trace is optimised to 8 mil to minimise impedance discontinuities at the RF pin of the IC.

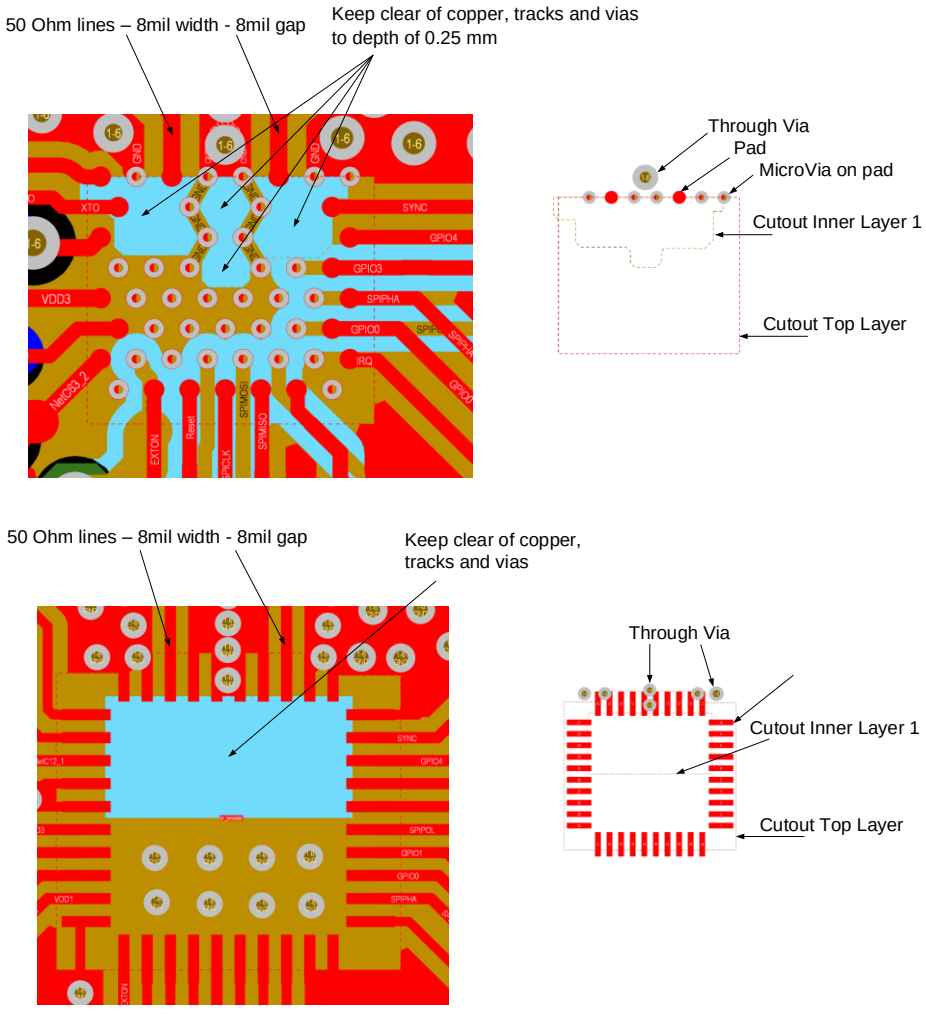


Figure 8. WLCSP and QFN package land patterns and routing

5 Power Management

VDD1, VDD2 and VDD3 are the main supply voltages of the IC. Among these supplies, VDD2 and VDD3 are the most power-hungry voltage rails. All the voltage signals can be supplied with 3.3 V to minimise the BOM (Bill of Materials) or more power-efficient solutions can be used, such as using DC-DC voltage regulators for VDD3 or using a dedicated PMIC (Power Management Integrated Circuit).

5.1 Voltage Regulators

Linear (LDO) or switched-mode (DCDC) regulators are used to provide the voltage rails for the DW3000 and QM33100 ICs. DCDC converters have greater efficiency than linear regulators but are known to generate switching noise, the harmonics from which can corrupt the operation of sensitive RF circuits. As long as the correct layout guidelines are followed, however, DCDC converters are a perfectly acceptable choice for use in designs with DW3000 and QM33100. Many of the circuit blocks within the IC are also powered by on-chip LDOs, which offer noise rejection aswell.

Please note that when using regulators, always follow supplier design guidelines in order to minimise any switching noise or ripple that might degrade the RF performance. Checking the voltage and current ratings of the preferred regulator and using the recommended land pattern and components are suggested.

5.1.1 DCDC Converters

A step-down, or buck DCDC converter IC requires bulk capacitors at the input and output aswell as an output inductor. Current loops are formed at the input and output stages and the area of these loops must be minimised in order to limit parasitic inductance. Excessive inductance can compromise the stability of the regulator and generate electromagnetic interference (EMI) due to the regulator's switching process, which can then propagate to other sensitive circuits on the PCB.

An example DCDC circuit diagram with Torex XC9282 is shown in Figure 9 below. The current loops highlighted can be minimised by placing components as close as possible to the regulator IC, with short, wide tracks connecting component terminals to the IC pins.

Always follow the specific layout guidelines in the regulator vendor's datasheet.

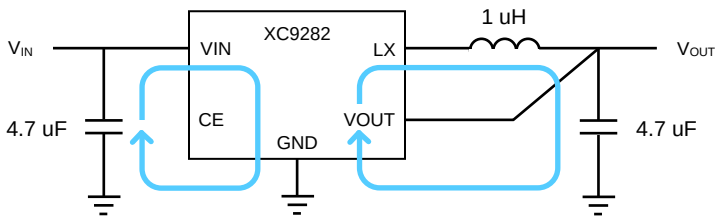


Figure 9. Current loops in a DCDC converter circuit

5.2 Power Trace Layout

In order to isolate the power traces from the RF and digital signals, using a dedicated power signal layer is suggested. It is also possible to use the same plane of the IC as a power plane. An example of power signal routing and decoupling capacitor placement is given in Figure 10 below.

Lower value capacitors should be placed closer to the supply pin of the IC because the higher frequency noise return path should be minimised. Moreover, all the capacitors should be as close as possible to the IC for the same reason. Adding ground vias at the ground legs of the decoupling capacitor would also help to minimise the noise return path.

The width of the power signals should be as wide as possible to decrease the series resistance of the power signal and voltage drop. It is inevitable to narrow the power signal when it gets closer to the IC. In these cases, it is recommended to keep the narrow part as short as possible.

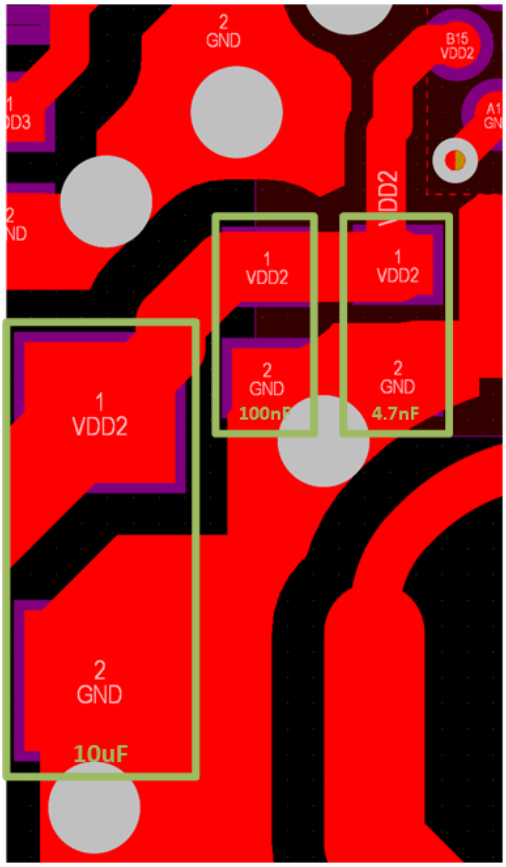


Figure 10. Decoupling capacitor placement on power trace

6 RF Signals and Components

An important and vulnerable part of the hardware design is the RF front-end. Excessive losses, mismatch and crosstalk may cause serious degradation to the performance of the IC. It is therefore recommended to keep this part as simple as possible to avoid any issues.

To improve the overall performance, decreasing the number of passive components on RF traces is recommended. When choosing the front-end components, parameters like insertion loss or gain, return loss, and group delay response should be considered. The general rules of thumb are listed below for passive components.

- Minimise the insertion loss at Channel 5 and Channel 9.
- Minimise the group delay variation over the 500 MHz bandwidth at respective channel frequencies. Group delay variation should be within ±100 ps.
- Choose components with a minimum -10 dB return loss in both directions (equivalent to VSWR = 2).
- Use reciprocal components (i.e. S21 = S12).
- Recommended land patterns of the front-end components in vendor's datasheet should be used.

6.1 DC Block Capacitor

A DC blocking capacitor is required at the RF ports of DW3000 and QM33100. A value of 2 pF is recommended so that the self-resonant frequency falls roughly between channel 5 and 9 center frequencies and the insertion loss of the capacitor is minimised.

It is also important to choose the package and type of the DC coupling capacitor. The package should be chosen to minimise the RF trace width discontinuity. For example, for 10 mil trace width, an 0201 package DC block capacitor is suitable and for a 20 mil trace width, an 0402 package would be a good choice. An ideal example of using an embedded RF signal to the capacitor pad is shown in Figure 11 below.

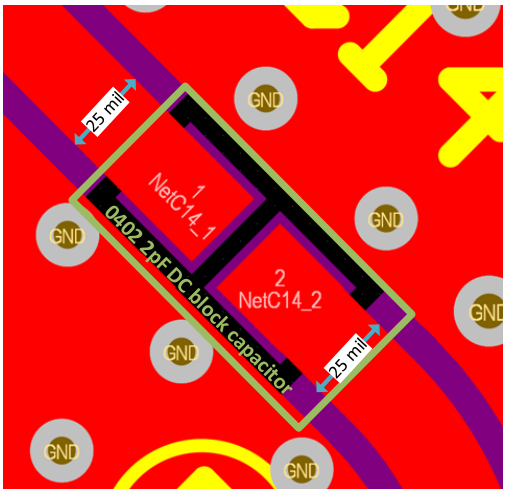


Figure 11. DC block capacitor matching to RF Trace

For the non-AoA (single port) part numbers, the unused port RF2 should be connected to ground via 50 Ω resistor (i.e. terminated). For the AoA part (double port), if the second port (RF2) is not used, it should be terminated after adding a DC block capacitor.

6.2 Frequency References

The transceiver requires a reference clock signal to derive internal clock signals such as PLL and digital clocks. Therefore, the quality of the clock signal has significant importance for both RF and digital performance.

38.4 MHz is used which is an industry standard to provide the two main channel frequencies Channel 5 (6.4896 GHz) and Channel 9 (7.9872 GHz) which are an integer multiple 38.4 MHz. There are two main options to provide a 38.4 MHz reference clock signal to the IC which are using a crystal oscillator and temperature compensated crystal oscillator (TCXO).

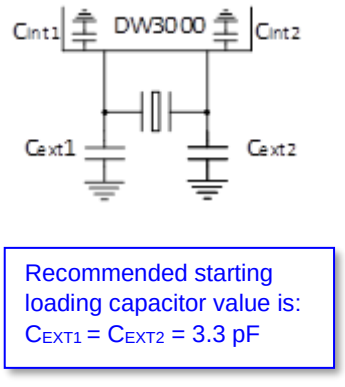
6.2.1 Crystal Oscillator

As a component crystal does not have the ability to produce a reference clock signal but it is an L-C resonator with a 38.4 MHz resonant frequency. Therefore, it is a frequency-selective component. Internal reference clock circuits which are connected to XTI and XTO pins of the IC, excite the crystal and consequently produce 38.4 MHz.

The main advantage of using crystal oscillators over the TCXO is that it is possible to trim the center frequency of the resonator by using the internal variable loading capacitors. Therefore, any frequency drift due to temperature, ageing and vibration can be eliminated by using these variable loading capacitors. DW3000 and QM33100 have the capability of changing the internal loading capacitors up to 8 pF with 0.125 pF steps.

Moreover, choosing the value of fixed external capacitors has a key role to center the trimming range of ±20 ppm. Since the real value of the loading capacitor is also dependent on the PCB parasitic, choosing the right value may require a couple of iterations. A good starting point for recommended crystal component is 3.3 pF. If another crystal is chosen for this purpose, choosing a crystal with similar specifications denoted in the DW3000 and QM33100 datasheets is strongly recommended.

In the PCB layout, since the clock frequency of 38.4 MHz falls in the VHF region (30 MHz - 300 MHz), it can be considered an RF signal. Therefore, particular care should be taken to route the clock signal. Keeping the crystal as close as possible to the IC provides better signal integrity.



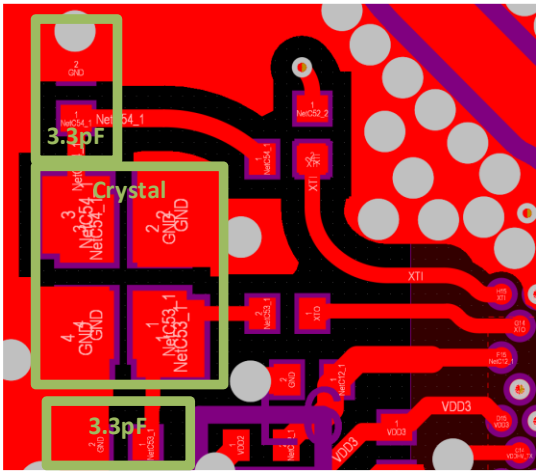


Figure 12. Crystal generic schematic and layout

6.2.2 Temperature-Compensated Crystal Oscillator (TCXO)

Another option to produce the reference frequency is using an external oscillator such as a TCXO. In this case, there are no loading capacitors available and therefore it is not possible to trim the reference frequency. For this reason, the frequency stability of the TCXO has a critical role. There are VCTCXOs (Voltage-Controlled TCXO) on the market which have the capability to trim the frequency over a certain range with an external variable control voltage (typically between 0 to 3.3 V). Such an application would increase the complexity of the clock circuitry and DW3000 and QM33100 do not have an output DAC to drive this signal.

TXC 7Z38470005 and Rakon IT2200K are examples of suitable external reference clock sources. An example schematic and layout for a TCXO is given below. The clock signal is required to be AC-coupled to the XTI pin via a DC blocking capacitor. A separate LDO to supply the TCXO and isolate noise may be needed, though some TCXOs have internal regulators which may offer enough noise rejection.

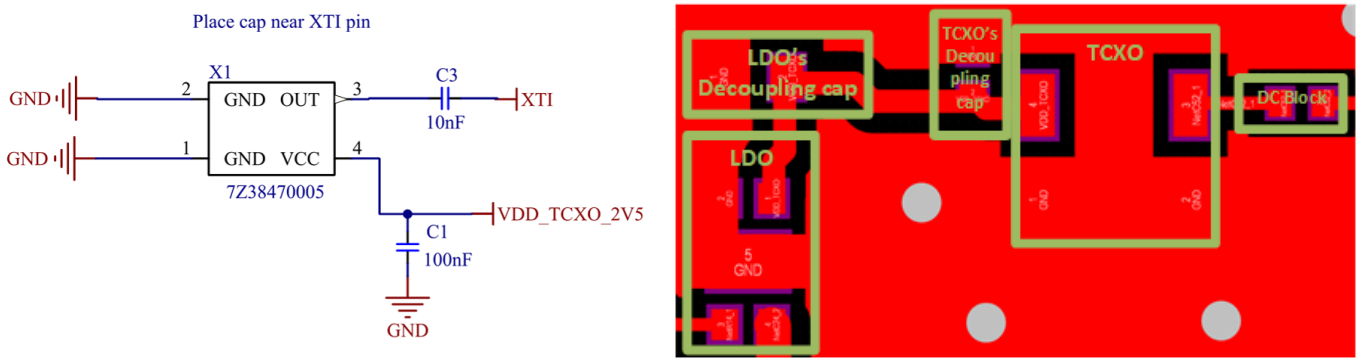


Figure 13. TCXO circuit and layout

A TCXO has the capability to produce the clock signal by itself. Therefore there is greater freedom for placement anywhere on the PCB. Ideally, the TCXO could be placed on the opposite side of the layer to the IC. This would provide sufficient isolation between the RF signals and the clock signal. Similarly to the crystal case, using a 50 Ω impedance-controlled clock trace and minimizing the impedance discontinuities are suggested.

6.3 Band Pass Filters

A band-pass filter (BPF) can be used as a front-end component, which allows passing Channel 5 and Channel 9 frequencies with minimum insertion loss and suppressing the other frequency components as much as possible. It is strongly recommended to use BPF in regions where spectrum emission mask requirements exist such as Japan ARIB T91.

There are two main reasons to use a band pass filter (BPF), which are improving the selectivity of the receiver and suppressing any out-of-band emissions. The main drawbacks of adding a BPF are the sensitivity of the receiver and the maximum power of the transmitter will be degraded by the amount of insertion loss of the BPF.

Murata LFB217G35CFHE826 and TDK DEA167240BT-2380B1 are suggested band-pass filter parts. An example of the layout floorplan for Murata BPF and 2 pF DC block capacitor is given below.

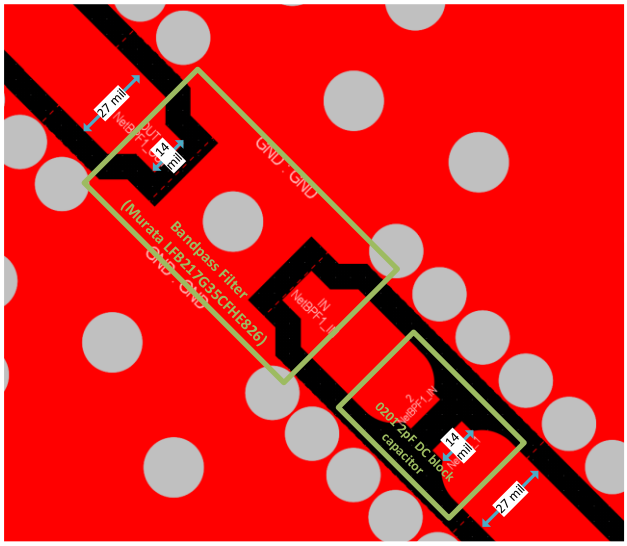


Figure 14. DC block capacitor and bandpass filter layout floorplan

In Figure 14, the 50 Ω controlled transmission line has a width of 27 mils and the BPF and DC block land patterns have 14 mils width. The transition between 27 mil and 14 mil is obtained by using the tapered transmission line to minimise the discontinuity in 50 Ω impedance.

6.4 Antennas and Matching Elements

Antennas are the interface between air and conducted metal. Therefore, antenna specifications such as antenna gain, return loss, antenna bandwidth and group delay are important parameters whether a commercially available antenna or a newly designed antenna is used. A comprehensive guide is available in the APH007 application note regarding antenna selection and design.

Similar to the DC block capacitor and BPF, the recommended land pattern of the antenna should be used. Generally, the pad of antennas is bigger than the RF trace. In these cases, a tapered RF trace can be used. On top of that, clearing the reference ground plane beneath the wider pad improves the pad's matching. If any matching elements are recommended in the vendor's datasheet, they should be embedded into the RF trace to avoid any impedance discontinuity. Otherwise, using extra matching elements may cause additional insertion loss and group delay variation.

As a general rule of thumb, at least -10 dB return loss or 2 VSWR matching is required for typical performance.

Qorvo has planar antenna designs for two-way ranging (TWR) and angle of arrival (AoA) applications such as CP-Wings, Mona Lisa and Jolie antennas. There are different versions of these antennas depending on the channel frequency and chip variation. Specifications regarding these antennas can be found in antenna report documents such as ARJL159, ARJL359, ARML005, ARML009, ARWB005 and ARWB09.

If a custom AoA antenna will be used, the antenna separation is critical and should be adjusted to λ/0.45 to cover ±90 degree angles of operation. Further UWB AoA antenna guidelines can be found in application note APH511.

6.5 RF Connectors and Cables

For testing the RF performance of the design, using coaxial switch connectors and for external antenna applications using edge-mount SMA connectors are the two suggested methods of using RF connectors.

6.5.1 SMA Connectors

Though they can be costly and bulky for many applications, SMA connectors can be used to provide a connection to an antenna in a product. They can also provide a very solid and reliable connection for RF validation of prototypes in the development stage, allowing you to independently verify the integrity of your board design in isolation of the antenna. End-launch SMA connectors should be used and not through-hole ones, so as to avoid a sharp right-angle bend and stubs that could cause reflections in the RF signal path.

A recommended high-performance end-launch SMA connector, as used in Qorvo UWB evaluation boards, is shown in Table 4.

Manufacturer	Part Number	Rated Frequency Range
Gigalane	PSF-S01-008	DC to 26.5 GHz

Table 4. Recommended SMA connector information

An example layout to an SMA connector is illustrated in Figure 15. It is recommended to clear solder mask on RF traces because usually the thickness of the solder mask can't be well controlled and may cause a change in the characteristic impedance of the traces. Clearing the solder mask all the way along the RF trace may cause an overflow of solder at the central pin of the connector which is not desired. For this reason, a small area of solder mask remains as a barrier to solder flow. Moreover, this method can be applied to all front-end components.

6.5.1.1 Correct SMA Connector Soldering

At high radio frequencies, such as those used for UWB, it's important to use a large enough quantity of solder between the SMA connector and PCB. In particular, the soldered connection must not just be around the legs of the connector but it must also extend as close as possible to the central signal pin on the top layer of the PCB. On the bottom of the PCB, the soldering should spread continuously between the legs of the connector. This ensures the current return path isn't excessively lengthened and the impedance matching is optimal.

Figure 15 illustrates how the SMA connector should be soldered.

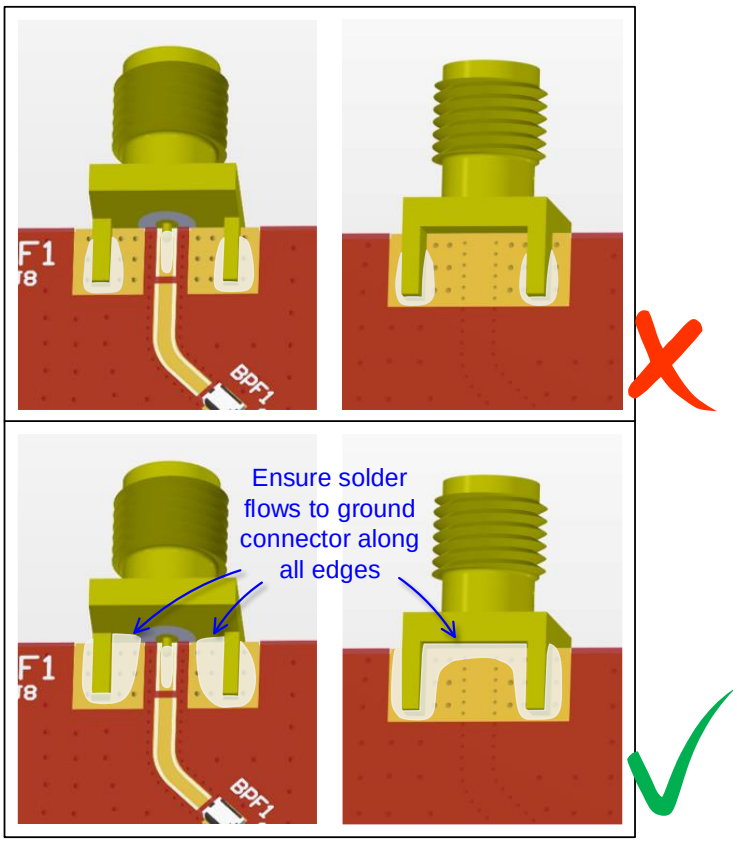


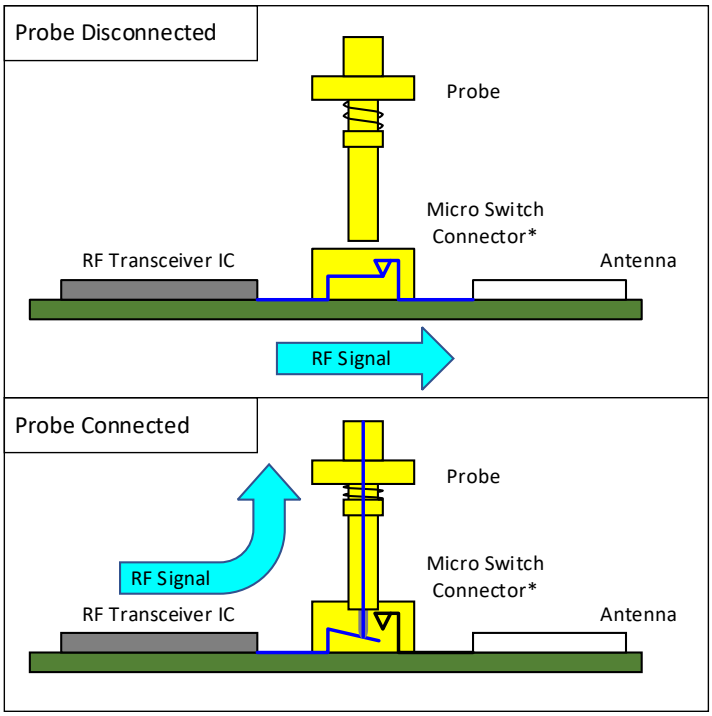
Figure 15. Edge-mount SMA connector and layout

6.5.2 Micro-Coax Connectors

Micro coaxial connectors offer a way to make a connection to an RF signal in a miniature connector form factor. Some connectors have a mechanical switch within the connector, which allows a conducted measurement to be made within a continuous RF signal path.

6.5.2.1 Connectors with Mechanical Switch Functionality

Coaxial switch connectors provide a switching ability to the connected port and when they remain unconnected provide a minimal insertion loss. Therefore, they can be useful to test any part of the RF signal. The most common way of using this type of connector is by adding in between the antenna (and matching elements, if they exist) and other front-end components. An illustration of how a switch connector is used with a matching probe in shown in Figure 16. Depending on the orientation, either the transmitted power before the antenna can be measured or the matching of the antenna can be measured and tuned. Table 5 shows a couple of suitable parts.



*Switch connector size exaggerated

Figure 16. Micro-switch connector functionality

Manufacturer	Part Number	Rated Frequency Range
Hirose	MS-156C	DC to 11 GHz
Murata	MM8030-2610	DC to 11 GHz

Table 5. RF connector parts

6.5.2.2 Connectors without Switch Function

Another connector option is U.FL, which provides a transition from PCB to coaxial cable. This kind of connector is commonly used for connecting antennas implemented in flexible printed circuits (FPC), as illustrated in Figure 17.

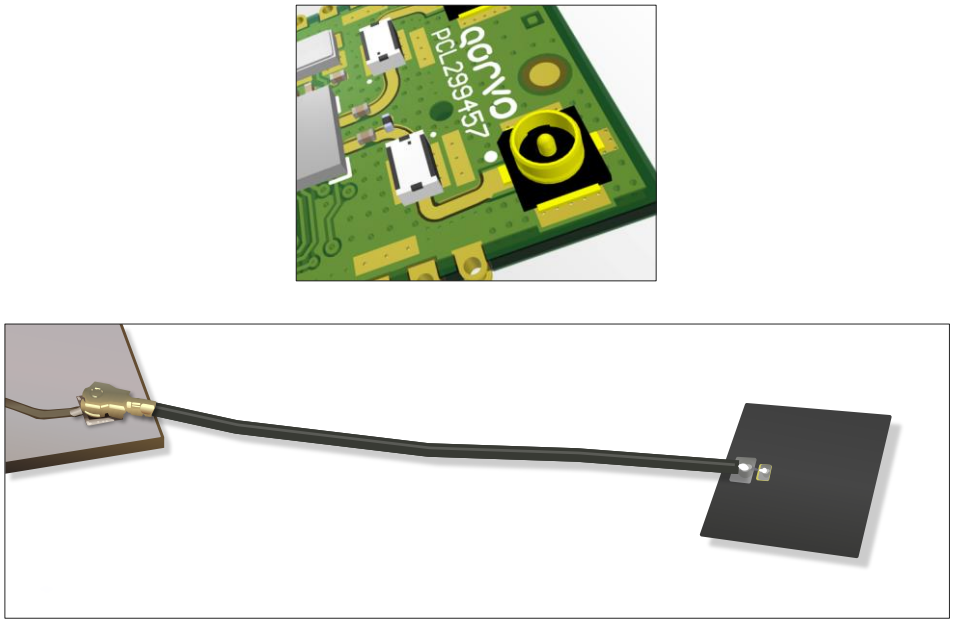


Figure 17. U.FL recepticle and connection to FPC antenna

6.5.3 Micro-Coax Cables

As depicted in Figure 17, the RF signal can often transition from a PCB to antenna via a micro-coaxial cable. A precaution to highlight when using these cables is that changes in position and small variations in length from cable to cable can result in phase variation leading to significant angle offset errors in AoA systems.

As a rough indication, a differential length variation of 1 mm between AoA paths can lead to a phase error of 10°.

6.5.4 Semi-Rigid Adapters

Semi-rigid adapters (sometimes called probes or ‘pig-tails’) are thin, copper-clad coaxial cables, with the inner conductor exposed at one end and an SMA connector attached at the other end. These adapters typically have 50 Ω characteristic impedance are useful during product development for making conducted RF measurements such as observing the transmit signal spectrum and receiver sensitivity.

The RF track may need to be cut in order to attach the inner conductor of the adapter. The length of exposed inner conductor should be minimised. Soldermask on the top layer of the PCB should be removed so that the outer shield of the adapter can be soldered to the board. The shield of the adapter should be soldered to the board as close as possible to the point where the inner conductor of the adapter is soldered to the RF track. Connections should be made to ground on either side of the RF track. By following these guidelines, the transmission line impedance from PCB to adapter can be kept as consistent as possible.

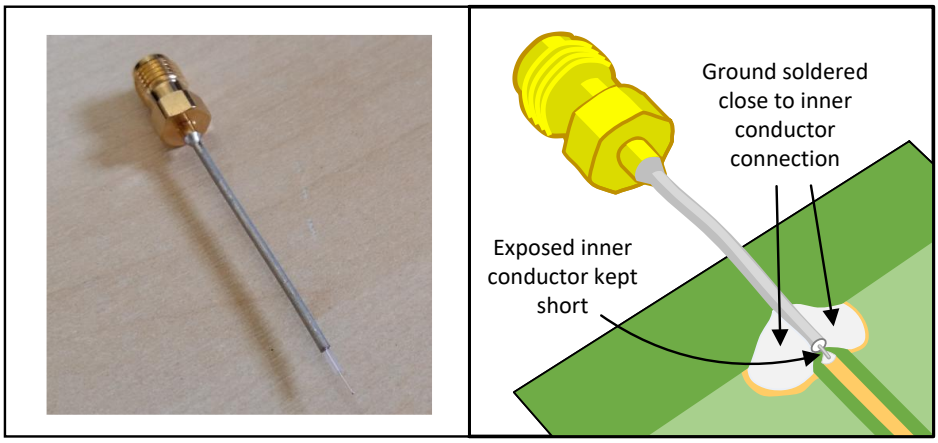


Figure 18. Semi-rigid adapter and connection to PCB

6.6 General RF Layout Guidelines

Follow these guidelines for the layout of RF transmission lines.

- If possible, route RF transmission lines on the same layer as the DW3000 or QM33100 IC. Vias in the RF signal path should ideally be avoided as they create impedance discontinuity and reduce isolation.
- Ensure transmission line impedances are controlled accurately from source to load. The PCB manufacturer can advise how to implement transmission lines for the PCB specification used.
- Ensure there is an unbroken ground path beneath transmission lines so that current paths in the RF track and ground plane beneath it are of matching lengths. Figure 19 shows an example of how the return current path could be lengthened by the presence of another track in the ground layer beneath the RF track.
- Use more vias at source and load ends of the transmission line to minimise impedance in the return current path.
- Place vias joining ground planes on adjacent layers around the border of transmission lines to shield the RF signal. This technique is sometimes called ‘stitching’ or ‘picket fencing’. The distance between adjacent vias should be small relative to the wavelength (λ) of the highest frequency signal on the RF trace. The recommended distance is λ/20.
- Remove soldermask above transmission lines. It is difficult to control the uniformity of the soldermask thickness which can result in impedance variation. Use thin strips of soldermask at the ends of the transmission line where they connect to component pads to prevent solder from the pads from spreading over the tracks.
- Keep tracks short to minimise insertion loss, which is significant at UWB frequencies.
- Keep the RF track as straight as possible as bends can introduce impedance discontinuities. If a bend must be used, make the bend radius as large as possible, as shown in Figure 20.

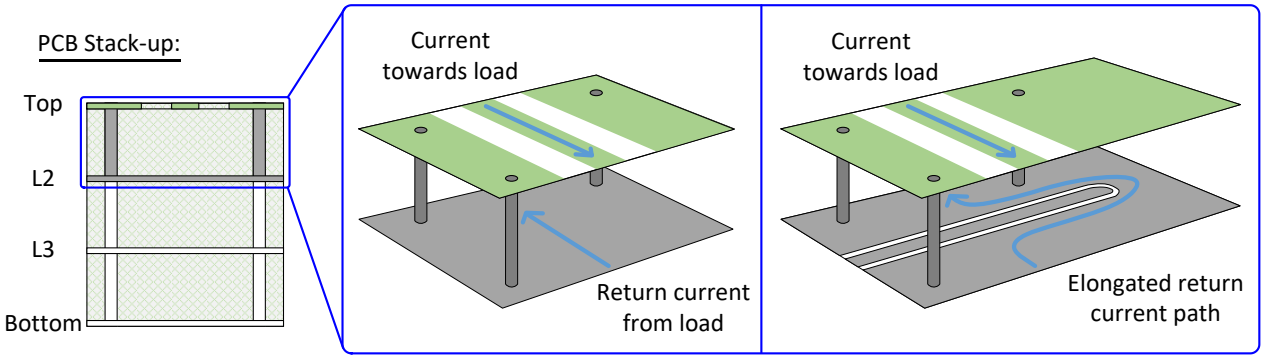


Figure 19. RF transmission line return current paths

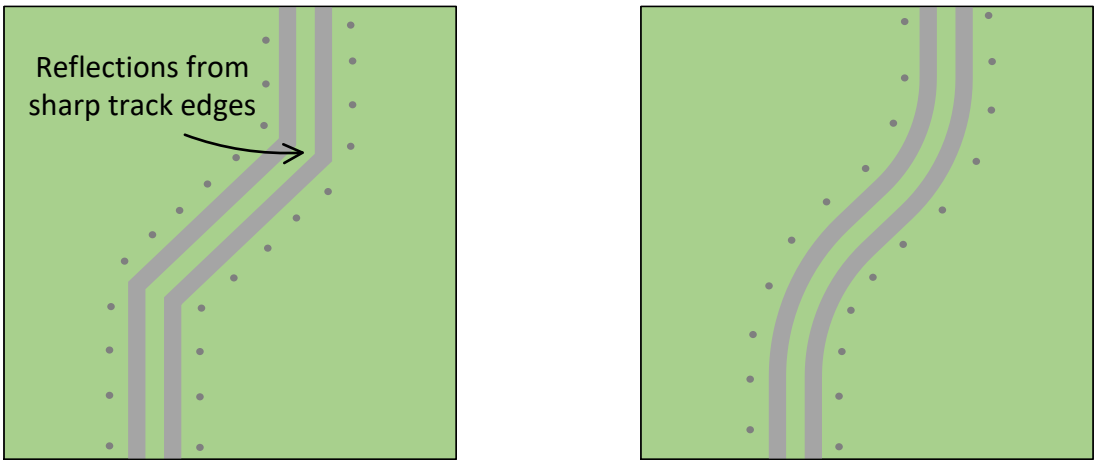


Figure 20. Smooth bends in RF track

- For AoA designs, try to keep trace lengths leading to each antenna element of equal length, if possible [2].

6.7 External Low Noise Amplifier (LNA)

Although the DW3000/QM33100 has an internal LNA, it is possible to improve the noise figure and consequently the sensitivity of the design by adding an external LNA to the front end. For this reason, choosing an LNA with a lower noise figure and high gain is important.

Another important point is that the reverse direction of the LNA which is also the transmitter direction should be suitable for the UWB signal. Therefore, a bypass path should be implemented for the transmission. This can be achieved either by adding single pole double throw (SPDT) switches or using an LNA which has a bypass function. This requirement also brings a need for a control signal to control the SPDT switches or bypass function. This can be achieved by configuring the GPIO6 pin as the EXTRXE function which goes high when DW3000 is in receive mode. In the QM33100 case, GPIO5 can be assigned as EXTRXE.

A generic LNA block diagram is given below.

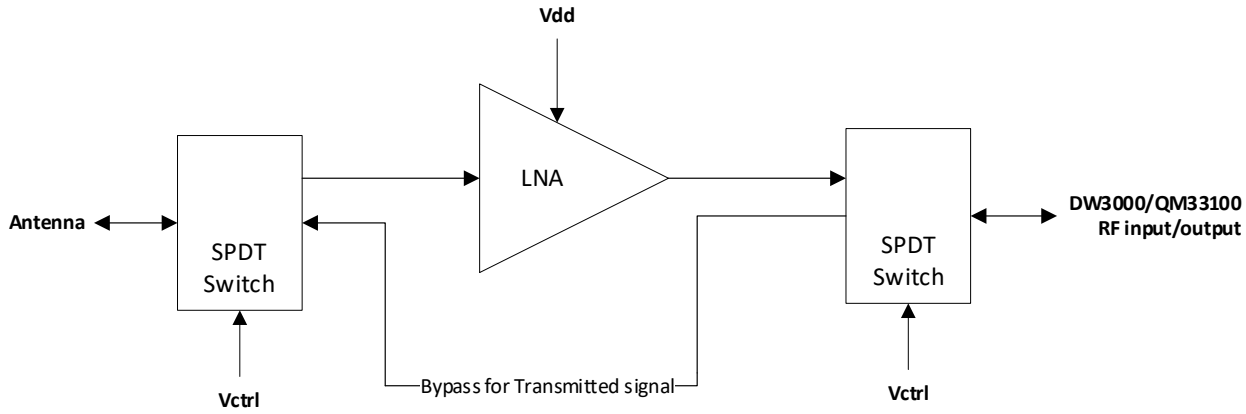
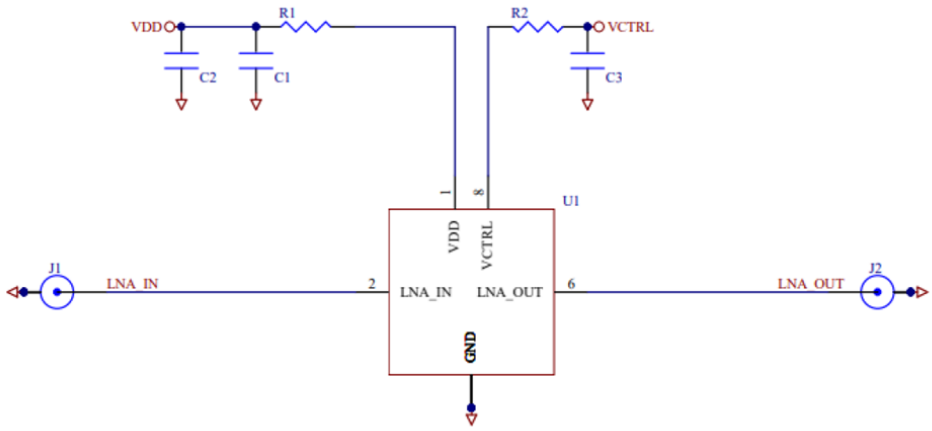


Figure 21. Generic external LNA block diagram

To minimise the complexity of the front end, it is suggested to use an LNA with a bypass function. Qorvo offers the QM14068 LNA with a bypass function designed and optimised for UWB [3]. The application circuit diagram of this LNA is given below.



DESCRIPTION	DESIGNATOR	FOOTPRINT
CAP, 250pF, +/-0.25pF, 25V, C0G, 0201	C1	0201_C
CAP,1µF 5%, 25V, C0G, 0201	C2	0201_C
RES, 0 OHM 1%, 1/20W, 0201	R1,R2	0201_R

Figure 22. QM14068 application circuit diagram

QM14068 does not need any DC-block capacitor on input and output ports and the bypass functionality is controlled by the VCTRL signal. Moreover, it requires a 1.8 V typical voltage supply source. Therefore, the level of control voltage cannot exceed 1.8 V and the direct connection of EXTRXE to the VCTRL signal may harm the LNA if the VDD1 supply level is above 1.8 V.

QM14068 requires a 1.8 V supply voltage. This can be supplied either with a separate LDO or DC-DC converter or combined with VDD1 or VDD3 (if they are 1.8 V). Decoupling capacitor values should be as indicated in Figure 22 to obtain the performance indicated in the QM14068 datasheet. If the combined version of the power supply scheme is chosen, adding a ferrite bead between the supply voltages to improve the isolation between them is preferred.

The timing performance of the LNA also plays an important role in optimal reception. Therefore, if another part number is chosen, then the turn-on and turn-off time of the LNA should not exceed 300 ns. The turn-on and off time will be directly affected by the values of the decoupling capacitors on the power signal and control signal. Increasing the value of these capacitors increases the time constant rise and fall time of control and supply signal and consequently increases the turn on and off time. Therefore, the capacitor values should be optimised during the design process by measuring the timings.

Application note APS304 gives further detail on the hardware, software and system considerations involved in using DW3000 and QM33100 with an external LNA [4].

6.8 External Power Amplifier (PA)

There can be large PCB trace losses between the IC and antenna and limited antenna efficiency. In such cases, the maximum transmit power level of the IC may not be sufficient to reach the maximum allowable transmit power level (-41.3 dBm/MHz). A power amplifier may be required to reach these levels to maintain the link budget performance of the overall system.

There are also certain circumstances in which transmitting above the regulatory limit is allowed, such as in LAES applications (Location tracking Applications for Emergency Services). In these cases, an external PA is also required.

Similarly to the external LNA case, a dedicated GPIO signal (EXTPA) can be used to control SPDT switches or the enable signal of the PA IC. A generic block diagram of the external PA is given in Figure 23 below. For even greater range, the link budget could be further increased by adding an external LNA in the bypass path.

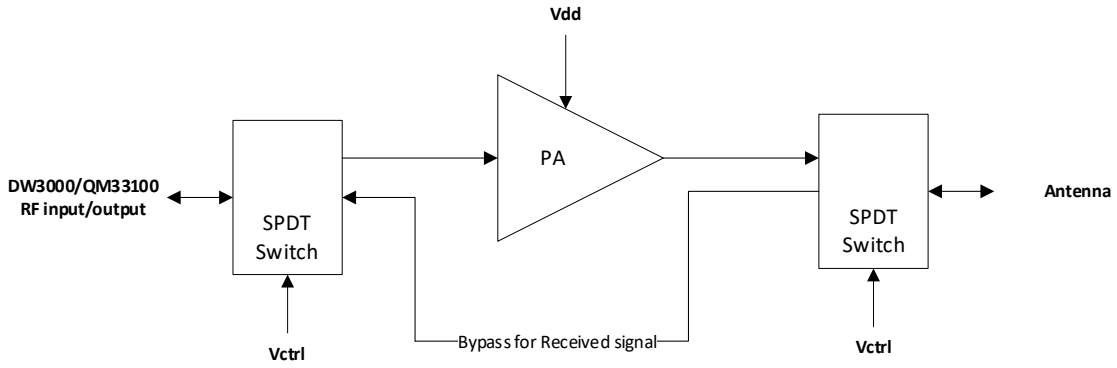
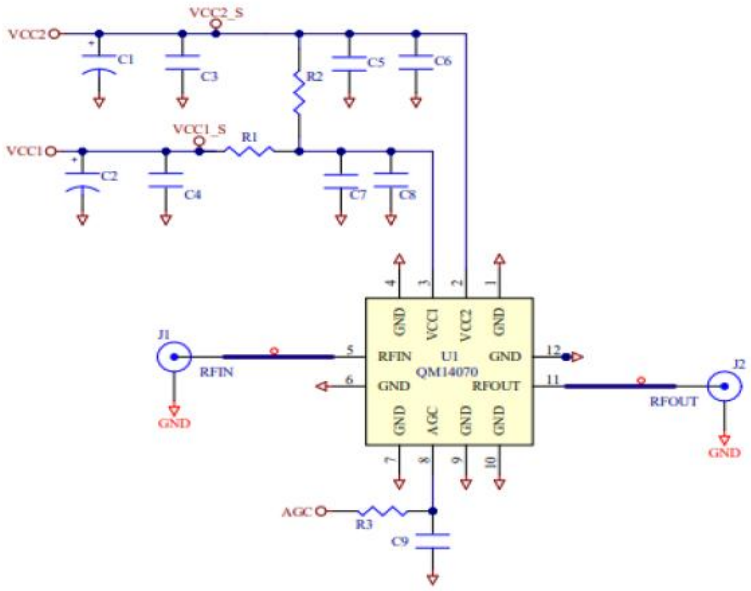


Figure 23. Generic external PA block diagram

Qorvo offers a UWB power amplifier IC, QM14070, with high gain and bypass modes for use in Channel 5 and Channel 9 frequencies [5]. It can be used to provide enhanced transmit power level performance in UWB applications to minimise the complexity of the front-end circuitry. The application circuit diagram is shown below. Further details are provided in the QM14070 datasheet.



REF. DES.	VALUE	DESCRIPTION	MANUF.	PART NUMBER
C3, C4	4.7uF	Capacitor, Chip, 0603	Murata Electronics	GRM188R60J475KE19D
C6, C8	1000pF	Capacitor, Chip, 0201	TDK	C0603X5R1E102K030BA
R1, R2, R3	0 Ω	Resistor, Chip, 0402, 5%	Kamaya, Inc.	RMC1/16SJPTH
P1	N/A	CONN, HDR, RT ANG, 2x14, 0.100"	Molex	90122-0774
J1, J2	N/A	CONN, SMA, End Launch	Gigalane Co.	PSF-S01-003
C1, C2, C5, C7, C9*	N/A	Capacitor, Chip, 0402		
Note: (*) indicates "Do Not Populate" and are not included on a standard EVB.				

Figure 24. QM14070 application circuit diagram

6.9 Digital Signals

Digital signals consist of four-wire Serial Peripheral Interface (SPI) interface (SPICSn, SPICLK, SPIMISO, SPIMOSI), General Purpose Input/Output (GPIO) signals, and EXTON, WAKEUP, RSTn signals. Among these signals, SPI signals can go up to 36 MHz in frequency. Therefore, digital signals can be divided into two sections which are High-Speed Digital signals (SPI) and GPIOs.

As illustrated in the system block diagram in Figure 1, the DW3000 and QM33100 ICs have a SPI digital interface, GPIOs and EXTON, WAKEUP and RSTn pins. This section outlines guidelines for these.

6.9.1 High-Speed Digital Signals (SPI)

High-speed digital signals can behave like RF signals and any noise coupled from these signals may cause performance degradation of the IC. Therefore, a list of suggestions for the layout floorplan of SPI signals is given below.

- Keep all SPI layout traces as short as possible.
- Run the trace as straight as possible and avoid using serpentine routing.
- Select materials to aid signal integrity. For high-speed design, your material selection is important as the dielectric constant will impact impedances and signal propagation.
- Run the clock signal at least 3x of the trace width away from all other signal traces. This helps to keep the clock signal clean from noise. An example of this is given in Figure 25 below.
- Keep a continuous ground in the next layer as the reference plane.
- It should be avoided to route the traces with 90 angle corner. The recommendation is to cut the corner and smooth the trace when the trace route needs to change direction. An example of this is given in Figure 25 below.
- To improve isolation between RF, power and clock signals, a dedicated layer can be used for digital signals. Moreover, avoid routing these signals over RF signals and clock signals to minimise crosstalk.

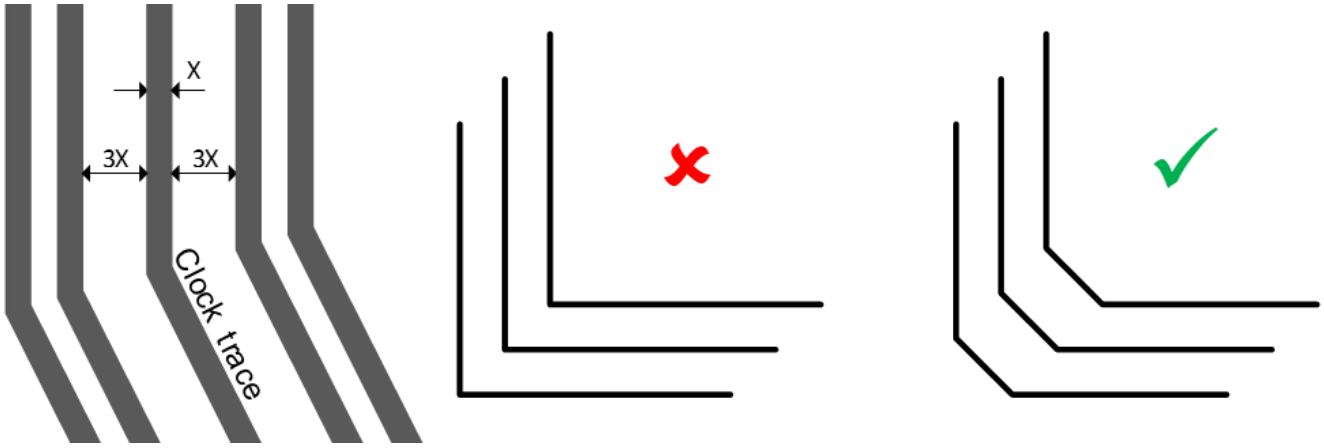


Figure 25. SPI clock trace routing and 90 degree trace routing

6.9.2 GPIO Signals

There are nine GPIO signals available on the chip. The level of the GPIO signal is dependent on the VDD1 supply voltage level. Therefore, if these signals are going to be used as output states, the level of the VDD1 signal should be chosen accordingly. They are straightforward to use and for the correct method of operation, check the DW3000/QM33100 datasheet. To improve the robustness of the application, the following list of suggestions should be applied.

- Driving LEDs directly with GPIO pins should be avoided because the current rating of these signals is not enough to drive LEDs.
- Applying an input voltage level higher than VDD1 may cause damage to the IC. IRQ/GPIO8 pin can be pulled low with a 10 kΩ resistor to avoid any spurious interruptions.
- WAKEUP should be connected to ground if not used.
- RSTn is active-low and must not be pulled high by an external resistor.

6.9.3 Coexistence Signaling

It is recommended to connect COEX_IN and COEX_OUT signals to GPIO4 and GPIO5 when management of coexistence between UWB and, say, WiFi is required. As illustrated in the simple diagram in Figure 26, the WiFi radio alerts it is in receive mode to the UWB transceiver on the COEX_IN GPIO, so that it can abort UWB Tx and Rx operations. The UWB transceiver alerts it is in receive mode to the WiFi radio on the COEX_OUT GPIO, so that the WiFi radio can abort Tx and Rx operations.

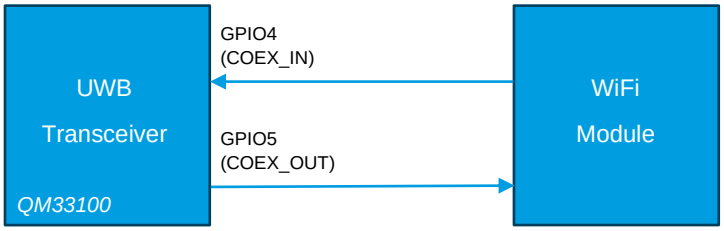


Figure 26. Coexistence signaling

7 References

Reference is made to the following documents in the course of this application note: -

Ref	Author	Version	Title
[1]	Qorvo	Current	APH001 DW1000 Hardware Design Guide
[2]	Qorvo	Current	APH511 UWB AoA Antenna Fundamentals
[3]	Qorvo	Current	QM14068 Data Sheet
[4]	Qorvo	Current	APS304 Maximising Range using an External LNA
[5]	Qorvo	Current	QM14070 Data Sheet

Table 6: Table of references

8 Document History

Revision	Date	Description
A	January 2024	First release

Table 7: Document history

9 Contact Information

For the latest specifications, additional product information, worldwide sales and distribution locations:

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Email: customer.support@qorvo.com

10 FURTHER INFORMATION

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