APPLICATION NOTE AN152

Powering the QM35825 Using the ACT88329 PMIC

Abstract

This application note shows Qorvo's ACT88329 integrated PMIC power solution for Qorvo's QM35825. It also shows how the PMIC performs in the QM35825's system against a power solution using discrete power converters.

Introduction

The ACT88329 PMIC is an integrated ActiveCiPS™ power management integrated circuit. It powers a wide range of processors, including solidstate disk drives, video processors, FPGA's, wearables, peripherals, and microcontrollers. It is highly flexible and can be reconfigured via I^2C for multiple applications without the need for PCB changes. The low external component count and high configurability significantly speeds time to market. The core of the device includes three DC/DC step down converters using integrated power FETs and two low-dropout regulators (LDOs). Buck1 and LDO1 can be configured as a load switch. Table 1 shows some of the key specifications of the ACT88329.

The QM35825 is a fully integrated Ultra Wideband (UWB) solution. It integrates 4 flexible RF ports, LNAs, PA and RF switches.

Qorvo has optimized the ACT88329VU110 to meet the QM35825's bias voltage requirements and support its system level performance such as sensitivity and power consumption. The ACT88329 solution provides a smaller, more optimized solution than a power solution using discrete power converters. It also offers configurability and the proprietary ACOT (asynchronous constant on-time) control architecture to achieve robust load transient response, which is beneficial for key system metrics such as packet error rate (PER) in transient situations.

Table 1. ACT88329 Key Specifications

Input voltage range	Vin = 2.7V to 5.5V
Number of Power rails	5 (3 Bucks + 2LDOs)
Buck1 Max Current	4A
Buck2 Max Current	4A
Buck3 Max Current	2A
LDO1 Max Current	390mA
LDO2 Max Current	390mA
Number of GPIOs	7
Operating Temperature	-40 to 150°C
Package	2.2×2.6mm WLCSP-30

Block Diagram of the ACT88329 Power Solution for QM35825

The QM35825 requires 5 bias voltages with low bias currents, which can be easily met by the ACT88329. The block diagram in Figure 1 shows the power connections from the ACT88329 to the QM35925 in a reference design for the UWB application.

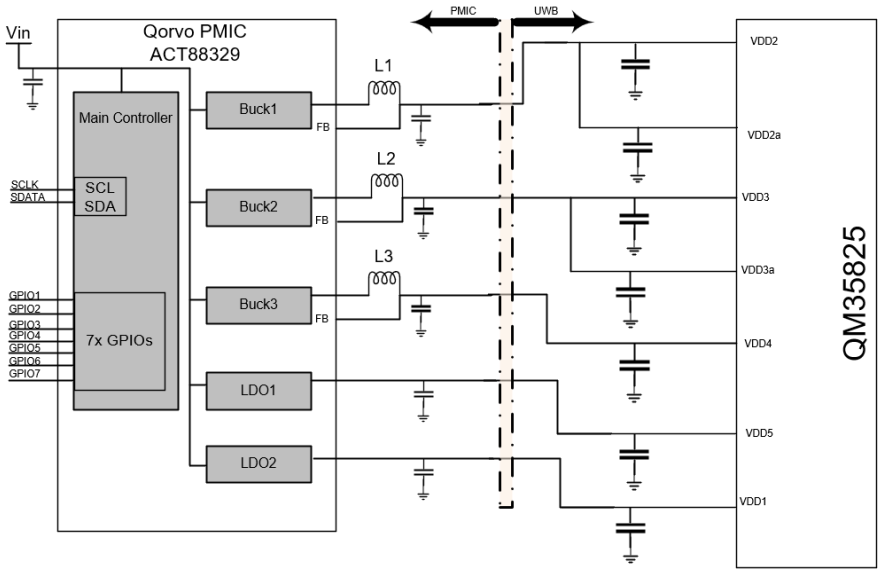


Figure 1. ACT88329 Power Connections to QM35825

Output Voltages and Sequencing

ACT88329VU110 is specifically optimized to power the QM35825. The output voltages are directly compatible with the QM35825 and each can be turned on or off individually by a designated GPIO. This design requires the QM35825 GPIOs to independently drive each ACT88329 GPIO to provide flexible On/Off control for ease of testing, but the timing of the GPIOs can be programmed to meet any desired startup sequencing. The solution is configured for a 5V input voltage. Note that the design provides the QM35825 with two voltage options for VDD5 and RRVDD based on application IO voltage (1.2V and 1.8V), and the two voltages are supported by ACT88329's LDO1 and LDO2 respectively.

The following table shows the configuration of ACT88329VU110 including output voltages, current limit, and switching frequencies to provide for the power rails of the QM35825. This configuration is specific to CMI110. Contact Qorvo if a different configuration is needed.

Table 2. ACT88329VU110 to QM35825 Power Rail Mapping

QM35825 Power Rails	QM35825 Voltage Requirement (V)	ACT88329 Voltage Rail	ACT88329 Output Voltage (V)	ACT88329 Current Limit (A)	Fsw (kHz)	On/Off Control
VDD1	1.62 - 1.98	LDO2	1.8	0.4	-	GPIO1
VDD5	1.2 +/- 5%	LDO1	1.2	0.4	-	GPIO2
VDD5	1.8 +/- 5%	LDO2	1.8	0.4		GPIO1
VDD2	2.40 - 3.60	Buck1	2.5	3.8	2250	GPIO3
VDD2a	2.40 - 3.60					
VDD3	1.50 - 3.60	Buck2	1.6	3.8	2500	GPIO4
VDD3a	1.50 - 3.60					
VDD4	1.80 +/-10%	Buck3	1.8	2	2500	GPIO6

ACT88329VU110 Power Solution Schematic

The following schematic Illustrates the schematic of the power solution for QM35825 using the ACT88329 in a UWB application. Note that all functions are integrated, and that the user only needs to add the power supply's external capacitors and inductors. For detailed schematic please reference Qorvo's QM3582x Hardware Design Guide.

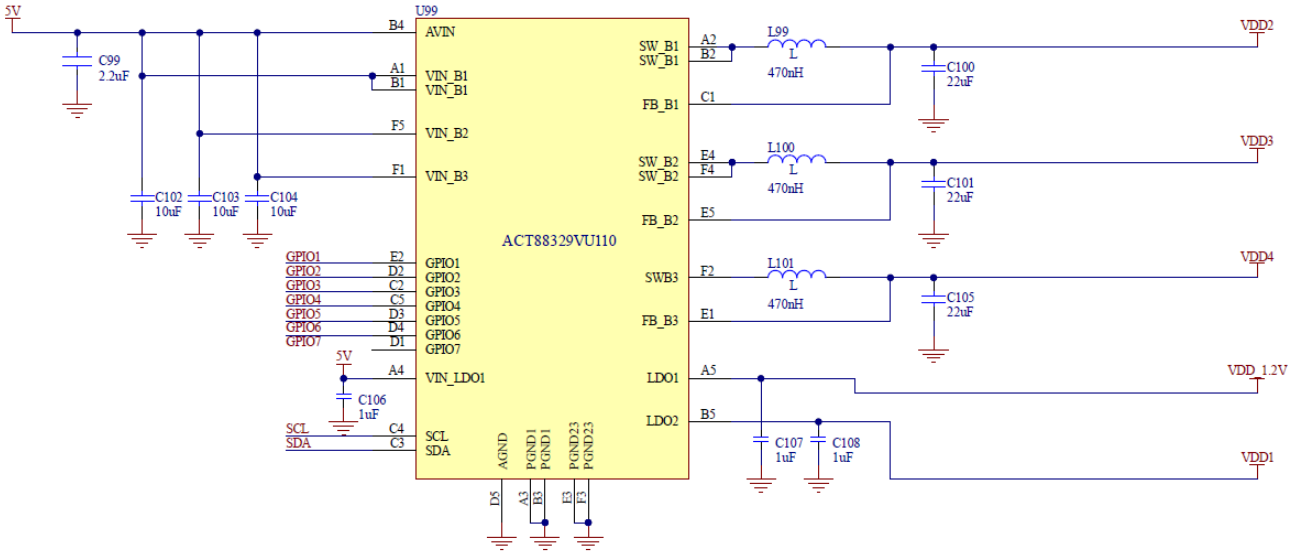
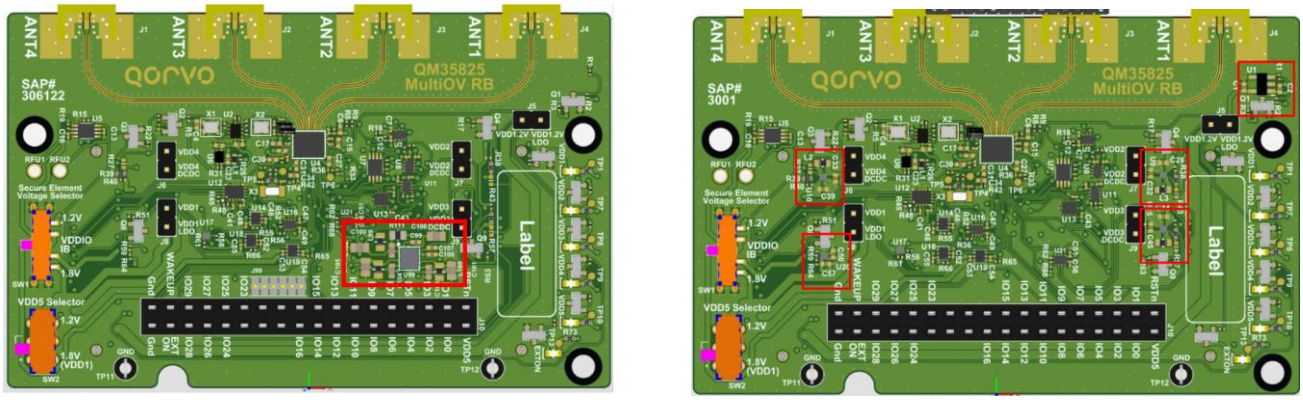


Figure 2. ACT88329VU110 Power Solution Schematic for the UWB QM35825

ACT88329VU110 Power Solution Performance

Solution Size

The ACT88329 PMIC integrates 5 voltage converters in a 2.18 x 2.58 mm 30 ball WLCSP package and hence provides a compact solution size. Figure 3 shows two power solutions for the QM35825 reference design: One using Qorvo's ACT88329 and one using discrete converters. The power solution portion is highlighted in red rectangular boxes. The ACT88329 solution is roughly 70% smaller and uses 4 fewer components.



(a) ACT88329 (b) Discrete Converters

Figure 3. Solution Size using the ACT88329 vs Discrete Converters

QM35825 Reference Design Rx Sensitivity

Figure 4 shows the system sensitivity measurement results over temperature using the ACT88329 power solution. Figure 5 shows a comparison of the results between the ACT88329 and the discrete solution.

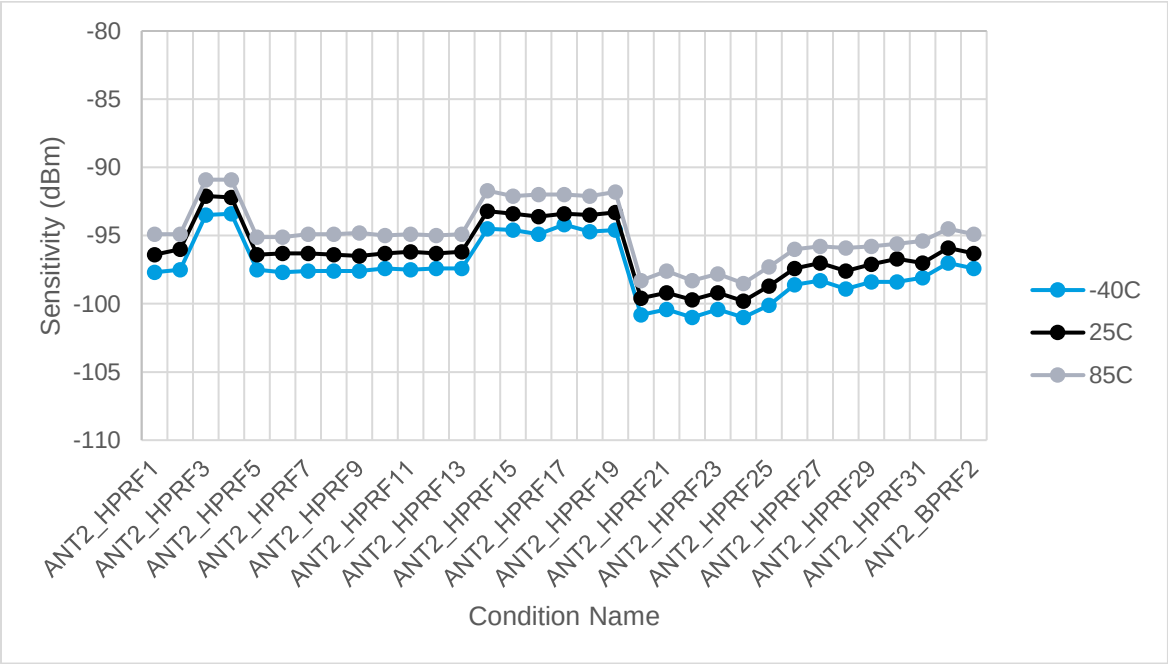


Figure 4. QM35825 System Sensitivity Over Temperature using the ACT88329

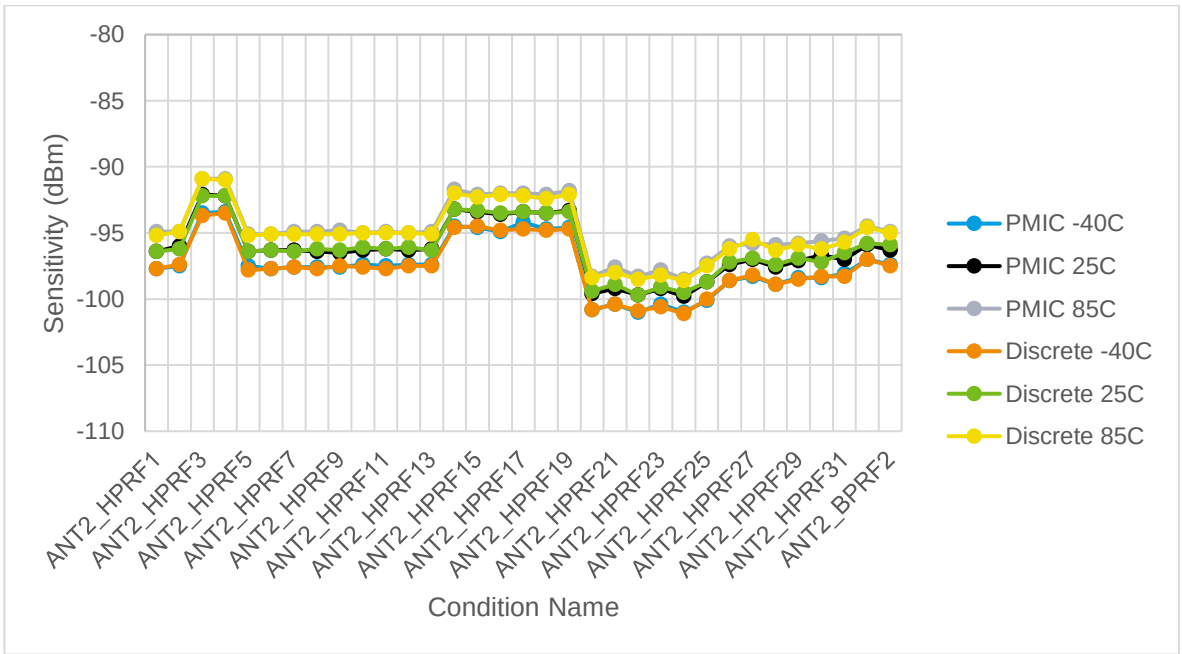


Figure 5. Comparion of System Sensitivity between using ACT88329 and Discrete Power Solution

QM35825 Reference Design Battery Current Consumption

The table below compares the current draw from the battery of the two systems using different power solutions. The ACT88329 provides a 26% reduction in transmit battery current and a 34% reduction in receiving, which translates to significant battery life improvement. Also note the ACT88329's improved sensitivity Packet Error Rate (PER).

Table 3. System Performance Comparison between ACT88329 and Discrete Solution

Power Solution	Max I_battery Rx (mA)	Max I_battery Tx (mA)	Sensitivity (dBm)	PER (%)
ACT88329	117	150	-96.5	0.9
Discrete	177	204	-96.6	1.0

QM35825 Reference Design Transient Packet Error Rate

When load or line transients occur in a UWB system, communication quality or reliability can be affected. The ACT88329 optimizes its buck converters' transient response by configuring the compensation parameters based on the application. Robust transient performance reduces communication errors and improves packet error rate (PER). Figure 6 shows a comparison of the transient packet test between the ACT88329 and discrete power solutions. The ACT88329 doubles the successful packets as the attenuation increases to the edge of the usable range.

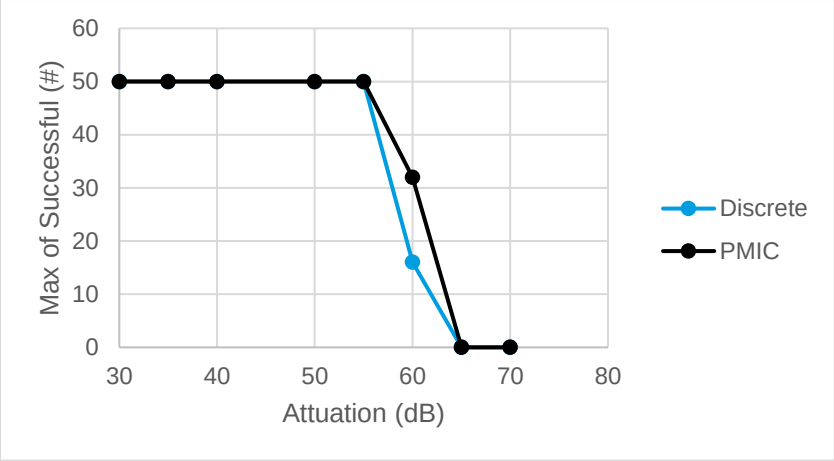


Figure 6. Transient Packet Communication Test Results

ACT88329VU110 Power Solution Layout Guidance

Follow the layout guidelines below when designing the ACT88329 PCB. Refer to both the Qorvo ACT88329 Evaluation Kit and the QM3582x Hardware Design Guide for layout examples.

1. Place the buck input capacitors as close as possible to the IC. Connect the capacitors directly to the corresponding VIN_Bx input pin and PGNDx power ground pin on the same PCB layer as the IC. Avoid using vias.
2. Minimize the switch node trace length between each SW_Bx pin and the inductor. Avoid routing sensitive analog signals near these high frequency, high dV/dt traces.
3. Place the LDO input capacitors close to their input pins. Connect their ground pins into the ground plane that connects the IC's PGNDx pins.

4. The input capacitor and output capacitor grounds should be connected as close together as possible, with short, direct, and wide traces.
5. Connect the PGNDx ground pins and the AGND ground pin directly to the PGND under the IC. The AGND ground plane should be routed separately from the other ground planes and only connect to the main ground plane under the IC at the AGND pin.
6. Connect the VIN input capacitor to the AGND ground pin.
7. Remember that all open drain outputs need pullup resistors.
8. Connect the PGND directly to the top layer ground plane. Connect the top layer ground plane to both internal ground planes and the PCB backside ground plane with thermal vias. Provide ground plane routing on multiple layers that allows the IC's heat to flow into the PCB and then spread radially from the IC. Avoid cutting the ground planes and adding vias that restrict the radial flow of heat of operating conditions and are relatively insensitive to layout considerations

Referenced Documents

The reference documents below take precedence over the contents of this application note and should always be consulted for the latest information.

ACT88329 Data Sheet

ACT88329 EVK

QM35825 Datasheet

Contact Information

For the latest specifications, additional product information, worldwide sales and distribution locations:

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QM35825 reference design