APPLICATION NOTE AN154

ACT88911 Register Definition

Abstract

This application note identifies the ACT88911 internal registers that help make this IC flexible and configurable for many applications. This is the initial released version therefore some registers might be changed in the future.

Introduction

The ACT88911 is a high Integration PMIC for Video/AR/VR Applications. It integrates nine switching regulators, eight LDOs, two load switches, and twelve GPIOs. Each of these regulators can be configured for a wide range of output voltages through the I2C interface.

I2C Serial Interface

To ensure compatibility with a wide range of systems, the ACT88911 uses standard I2C commands. The ACT88911 always operates as a slave device and is addressed using a 7-bit slave address followed by an eighth bit, which indicates whether the transaction is a read-operation or a write-operation. Refer to each specific CMI for the IC's slave address.

The IC contains two sets of configurable I2C addresses. System, GPIOs, Buck 1, Buck 3, Buck-Boost 6, Boost 8, LDO1_LDO2 and LDO5_LSW8 operate from one I2C address and the rest of the regulators have a different I2C address.

The I2C addresses can be set by the external resistor on the ADD pin.

Table 1: ACT88911 I²C Addresses

	7-Bit Slave Address (Set 1: Master, GPIOs, Buck 1, Buck 3, Buck-Boost 6, Boost 8, LDO1_LDO2, LDO5_LSW8**)**		**8-Bit Write Address**	**8-Bit Read Address**
Float	0x67h	110 0111b	0xCEh	0xCFh
200k +/-7.5%	0x6Bh	110 1011b	0xD6h	0xD7h
100k +/-7.5%	0x62h	110 0010b	0xC4h	0xC5h
51k +/-7.5%	0x64h	110 0100b	0xC8h	0xC9h
	7-Bit Slave Address (Set 2: Buck 2, Buck 4, Buck 5, Buck-Boost 7, Boost 9, LDO3_LDO6, LDO4_LSW7**)**		**8-Bit Write Address**	**8-Bit Read Address**
Float	0x68h	110 1000b	0xD0h	0xD1h
200k +/-7.5%	0x6Ch	110 1100b	0xD8h	0xD9h
100k +/-7.5%	0x63h	110 0011b	0xC6h	0xC7h
51k +/-7.5%	0x65h	110 0101b	0xCAh	0xCBh

Register Types

The ACT88911 ICs contain the following register types.

Basic Volatile - Customer R/W (Read and Write) and RO (Read only). The customer can modify these register values to change IC functionality. Any changes to these registers are lost when power is recycled. The default values are fixed and cannot be changed.

Basic Non-Volatile - Customer R/W and RO. The customer can modify these register values to change IC functionality. Any changes to these registers are lost when power is recycled. The default values can be modified at the factory to optimize IC functionality for specific applications. Please consult Sales@Qorvo.com for custom options and minimum order quantities.

The ACT88911 contains 14 major register spaces.

Table 2: ACT88911 Register Addresses for CMI101

Register Space	7-Bit Slave Address	Register Address Range
Master, GPIO, LDO9, LDO10 Register	Set 1	0x00h to 0x07h, 0x09h to 0x14h, 0x27h to 0x2Dh, 0x32h to 0x3Eh
Buck 1 Register	Set 1	0x40h to 0x48h, 0x57
Buck 2 Register	Set 2	0x40h to 0x48h, 0x57
Buck 3 Register	Set 1	0x60h to 0x68h
Buck 4 Register	Set 2	0x60h to 0x68h
Buck 5 Register	Set 2	0x00h to 0x08h, 0x16, 0x17
Buck-Boost 6 Register	Set 1	0xA0h to 0xA7h
Buck-Boost 7 Register	Set 2	0xA0h to 0xA7h
Boost 8 Register	Set 1	0x80h to 0x87h
Boost 9 Register	Set 2	0x80h to 0x87h
LDO1_LDO2	Set 1	0xE0h to 0xEAh
LDO3_LDO6	Set 2	0x20h to 0x2Ah
LDO4_LSW7	Set 2	0xC0h to 0xCAh
LDO5_LSW8	Set 1	0xC0h to 0xCAh

Register Map Overview

The following table shows an overview of the ACT88911 register map.

MASTER, GPIO, LDO9 and LDO10								
ADD (HEX)	7	6	5	4	3	2	1	0
0	RFU	WD_TIMER_ALERT	TWARN	VSYSSTAT	VIN_POK_OV	PBASTAT	VSYSWARN	PBDSTAT
1	RFU	WD_ALERT_MSK	TMSK	VSYSMSK	VIN_POK_OV_MSK	PBAMSK	VSYSWARN_MSK	PBDMSK
2	RFU	OK_START	VSYSWARN_RT	VSYSDAT	DVS_I2C_DB11	DVS_I2C_DB10	DVS_I2C_DB9	PBDAT
3	GPIO8 STAT	GPIO7 STAT	GPIO6 STAT	GPIO5 STAT	GPIO4 STAT	GPIO3 STAT	GPIO2 STAT	GPIO _STAT
4	GPIO8 Toggled	GPIO7 Toggled	GPIO6 Toggled	GPIO5 Toggled	GPIO4 Toggled	GPIO3 Toggled	GPIO2 Toggled	GPIO1 Toggled
5	GPIO8 MASK	GPIO7 MASK	GPIO6 MASK	GPIO5 MASK	GPIO4 MASK	GPIO3 MASK	GPIO2 MASK	GPIO1 MASK
6	INTADR[7:0]							
7	RFU	SLEEP	RFU	DPSLP	RFU	POWER OFF	WDPCEN	WDSREN
2B	GPIO9 STAT	GPIO9 Toggle	GPIO9 MASK	GPIO10 STAT	GPIO10 Toggle	GPIO10 MASK	GPIO11 STAT	GPIO11 Toggle
2C	BK1_DVS_I2C[1:0]		BK2_DVS_I2C[1:0]		BK5_DVS_I2C[1:0]		GPIO11 MASK	LDOUV_FLTMSK
39	ILIM_LDO9	PG_LDO9	ILIM_LDO10	PG_LDO10	LDOILIM_FLTMSK	GPIO12 MASK	GPIO12 STAT	GPIO12 Toggle
9	TRST_DLY[2:0]			PWRCYC_TIME[1:0]		PWROFF_TIME[1:0]		DIS OV UV SD
0A	EN_LDO910_DLY_OFF	EN POWEROFF	RFU	VSYSMON[4:0]				
0B	IO1_DLY[1:0]		IO2_DLY[1:0]		IO3_DLY[1:0]		IO4_DLY[1:0]	
0C	IO5_DLY[1:0]		IO6_DLY[1:0]		IO7_DLY[1:0]		RFU	RETRY TIME
0D	MODE1[3:0]				MUX1[3:0]			
0E	MODE2[3:0]				MUX2[3:0]			
0F	MODE3[3:0]				MUX3[3:0]			
10	MODE4[3:0]				MUX4[3:0]			
11	MODE5[3:0]				MUX5[3:0]			
12	MODE6[3:0]				MUX6[3:0]			
13	MODE7[3:0]				MUX7[3:0]			
14	POK_OV[2:0]			VSYSWARN[4:0]				
27	MODE8[3:0]				MUX8[3:0]			
28	MODE9[3:0]				MUX9[3:0]			
29	MODE10[3:0]				MUX10[3:0]			
2A	MODE11[3:0]				MUX11[3:0]			
32	MODE12[3:0]				MUX12[3:0]			
33	PC[13:6]							
34	nSAVE_IQ_MSTR	EN_PP_IO8	EN_PP_IO7	EN_PP_IO6	EN_PP_IO4	EN_PP_IO3	EN_PP_IO2	EN_PP_IO1
35	EN_PP_IO12	EN_PP_IO11	amode_en	EDGE_IN1[4:0]				
36	EN_LDO10	EN_LDO9	GPIO_ANA_ SLP CTRL EN	EDGE_IN2[4:0]				
37	MSK_FLT_LDO9	RFU	VSET_LDO9[5:0]					
38	MSK_FLT_LDO10	RFU	VSET_LDO10[5:0]					
3B	LED2 DBL BLINK	LED_DELAY2<2:0>			ILED2<3:0>			
3C	LED1 DBL BLINK	LED_DELAY1<2:0>			ILED1<3:0>			

3D	LED_BREATHE 2_EN	PWMFREQ2			PWMDUTY2			
3E	LED_BREATHE 1_EN	PWMFREQ1			PWMDUTY1			
	BUCK 1							
ADD (HEX)	7	6	5	4	3	2	1	0
40	POK	OV	ILIM	IWARN	UVFLTmsk	OVFLTmsk	ILIMFLTmsk	IWARNmsk
41	FREQ_SEL[1:0]		ENPD_LOAD	SST[2:0]			DRV_ADJ[1:0]	
42	EN_LPM	VSET0[6:0]						
43	DIS_PD	VSET1[6:0]						
44	ON	PBINEN	QLTCH	SLEEP_EN	AUXIN_EN	DPSLEEP_EN	ILIM_SET[1:0]	
45	MODE	RST	RFU			RFU		
46	RFU				IPD_LOAD[1:0]		RFU	
47	DVS_SET[1:0]		ON_DLY[2:0]			OFF_DLY[2:0]		
48	VRANGE	BK1_POR_FLT_OPT	FCCM	RFU	RFU	EN_ULPM	EN_LSILIM	EN_ILIM_FB
57	FCCM_DVS	VSET2[6:0]						
	BUCK 2							
ADD (HEX)	7	6	5	4	3	2	1	0
40	POK	OV	ILIM	IWARN	UVFLTmsk	OVFLTmsk	ILIMFLTmsk	IWARNmsk
41	FREQ_SEL[1:0]		ENPD_LOAD	SST[2:0]			DRV_ADJ[1:0]	
42	EN_LPM	VSET0[6:0]						
43	DIS_PD	VSET1[6:0]						
44	ON	PBINEN	QLTCH	SLEEP_EN	AUXIN_EN	DPSLEEP_EN	ILIM_SET<1:0>	
45	MODE	RST	RFU			RFU		
46	RFU				IPD_LOAD[1:0]		RFU	
47	DVS_SET[1:0]		ON_DLY[2:0]			OFF_DLY[2:0]		
48	VRANGE	BK2_POR_FLT_OPT	FCCM	RFU	RFU	EN_ULPM	EN_LSILIM	EN_ILIM_FB
57	FCCM_DVS	VSET2[6:0]						
	BUCK 3							
ADD (HEX)	7	6	5	4	3	2	1	0
60	POK	OV	ILIM	IWARN	UVFLTmsk	OVFLTmsk	ILIMFLTmsk	IWARNmsk
61	FREQ_SEL[1:0]		ENPD_LOAD	SST[2:0]			DRV_ADJ[1:0]	
62	EN_LPM	VSET0[6:0]						
63	DIS_PD	VSET1[6:0]						
64	ON	PBINEN	QLTCH	SLEEP_EN	AUXIN_EN	DPSLEEP_EN	ILIM_SET	FCCM_DVS
65	MODE	RST	RFU			RFU		
66	RFU				IPD_LOAD[1:0]		RFU	
67	DVS_SET[1:0]		ON_DLY[2:0]			OFF_DLY[2:0]		
68	VRANGE	BK3_POR_FLT_OPT	FCCM	RFU	RFU	EN_ULPM	EN_LSILIM	EN_ILIM_FB
	BUCK 4							
ADD (HEX)	7	6	5	4	3	2	1	0
60	POK	OV	ILIM	IWARN	UVFLTmsk	OVFLTmsk	ILIMFLTmsk	IWARNmsk
61	FREQ_SEL[1:0]		ENPD_LOAD	SST[2:0]			DRV_ADJ[1:0]	

62	EN_LPM	VSET0[6:0]						
63	DIS_PD	VSET1[6:0]						
64	ON	PBINEN	QLTCH	SLEEP_EN	AUXIN_EN	DPSLEEP_EN	ILIM_SET	FCCM_DVS
65	MODE	RST	RFU			RFU		
66	RFU				IPD_LOAD[1:0]		RFU	
67	DVS_SET[1:0]		ON_DLY[2:0]			OFF_DLY[2:0]		
68	VRANGE	BK4_POR_FLT_OPT	FCCM	RFU	RFU	EN_ULPM	EN_LSILIM	EN_ILIM_FB
	BUCK 5							
ADD (HEX)	7	6	5	4	3	2	1	0
0	POK	OV	ILIM	IWARN	UVFLTmsk	OVFLTmsk	ILIMFLTmsk	IWARNmsk
1	FREQ_SEL[1:0]		ENPD_LOAD	SST[2:0]			DRV_ADJ[1:0]	
2	EN_LPM	VSET0[6:0]						
3	DIS_PD	VSET1[6:0]						
4	ON	PBINEN	QLTCH	SLEEP_EN	AUXIN_EN	DPSLEEP_EN	ILIM_SET	FCCM_DVS
5	MODE	RST	RFU			RFU		
6	RFU				IPD_LOAD[1:0]		RFU	
7	DVS_SET[1:0]		ON_DLY[2:0]			OFF_DLY[2:0]		
8	VRANGE	BK5_POR_FLT_OPT	FCCM	RFU	RFU	EN_ULPM	EN_LSILIM	EN_ILIM_FB
16	MCLK_ASYNC_BKUP	VSET2[6:0]						
17	RFU	VSET3[6:0]						
	BUCK-BOOST 6							
ADD (HEX)	7	6	5	4	3	2	1	0
A0	POK	OV	ILIM	ILIM_WARN	UV_FLTMSK	OV_FLTMSK	ILIM_FLTMSK	IWARN_FLTMSK
A1	EXT_OFFDL_SEL	EXT_ONDL_SEL	TILE_ON_to_POK	DIS_PULLDOWN	EN_ILIMSD	DIS_ILIM2	DIS_OCP_SD	ALT_FRCBST2BK
A2	VSET[7:0]							
A3	DRV_ADJ_VOUT[1:0]		DTH2L_VOUT	DTL2H_VOUT	DRV_ADJ_VIN[1:0]		DTH2L_VIN	DTL2H_VIN
A4	ON	PBINEN	QLTCH	SLEEP EN	AUXIN EN	DP SLEEP EN	PORFLT_OPT	FCCM
A5	MODE	RST	RFU			RFU		
A6	RFU				SST[1:0]		RFU	AO_CLK
A7	ILIM_SET[1:0]		ON DELAY[2:0]			OFF DELAY[2:0]		
	BUCK-BOOST 7							
ADD (HEX)	7	6	5	4	3	2	1	0
A0	POK	OV	ILIM	ILIM_WARN	UV_FLTMSK	OV_FLTMSK	ILIM_FLTMSK	IWARN_FLTMSK
A1	EXT_OFFDL_SEL	EXT_ONDL_SEL	TILE_ON_to_POK	DIS_PULLDOWN	EN_ILIMSD	DIS_ILIM2	DIS_OCP_SD	ALT_FRCBST2BK
A2	VSET[7:0]							
A3	DRV_ADJ_VOUT[1:0]		DTH2L_VOUT	DTL2H_VOUT	DRV_ADJ_VIN[1:0]		DTH2L_VIN	DTL2H_VIN
A4	ON	PBINEN	QLTCH	SLEEP EN	AUXIN EN	DP SLEEP EN	PORFLT_OPT	FCCM
A5	MODE	RST	RFU			RFU		
A6	RFU				SST[1:0]		RFU	AO_CLK
A7	ILIM_SET[1:0]		ON DELAY[2:0]			OFF DELAY[2:0]		
	BOOST 8							

ADD (HEX)	7	6	5	4	3	2	1	0
80	POK	OV	ILIM	RFU	UV_FLTMSK	OV_MSK	ILIM_MSK	IWARN_MSK
81	RFU	BST_FLT_MSK	BST_POR_FLT_OPT	RFU	FRE_SEL	HS_DRV_ADJ	LS_DRV_ADJ[1:0]	
82	EN_ILIM_SD	VSET[6:0]						
83	CC_ADJ	DEC_MINON	ISET[5:0]					
84	ON	PBINEN	QLTCH	SLEEP_EN	AUXIN_EN	DPSLP_EN	ILIM_SET[1:0]	
85	MODE	RST	RFU			RFU		
86	RFU				OFS_SET_IPK[1:0]		SLP_SET_IPK	INC_OC
87	RFU	RFU	ONDLY[2:0]			OFFDLY[2:0]		

BOOST 9

ADD (HEX)	7	6	5	4	3	2	1	0
80	POK	OV	ILIM	RFU	UV_FLTMSK	OV_MSK	ILIM_MSK	IWARN_MSK
81	RFU	BST_FLT_MSK	BST_POR_FLT_OPT	RFU	FRE_SEL	HS_DRV_ADJ	LS_DRV_ADJ[1:0]	
82	EN_ILIM_SD	VSET[6:0]						
83	CC_ADJ	DEC_MINON	ISET[5:0]					
84	ON	PBINEN	QLTCH	SLEEP_EN	AUXIN_EN	DPSLP_EN	ILIM_SET[1:0]	
85	MODE	RST	RFU			RFU		
86	RFU				OFS_SET_IPK[1:0]		SLP_SET_IPK	INC_OC
87	RFU	RFU	ONDLY[2:0]			OFFDLY[2:0]		

LDO1 and LDO2

ADD (HEX)	7	6	5	4	3	2	1	0
E0	PWR_GOOD_LDO1	OV_LDO1	ILIM_LDO1	RFU	UV_FLTMSK_LDO1	OV_FLTMSK_LDO1	ILIM_FLTMSK_L1	RFU
E1	RFU	RANGE_LDO1	LDO1 VSET[5:0]					
E2	ON LDO1	PBIN EN LDO1	AUXIN EN LDO1	SLEEP EN LDO1	DPSLEEP EN LDO1	RFU		
E3	ON DELAY LDO1[2:0]			OFF DELAY LDO1[2:0]			MODE LDO1	RST LDO1
E4	RFU				RFU			
E5	ILIM_SD_DIS_LDO1	POR_MSK_L2	POR_MSK_L1	DIS_CHARGE_OPT_LDO1	DIS_PD_LDO2	DIS_PD_LDO1	SST_LDO1	QLTCH_LDO1
E6	PWR_GOOD_LDO2	OV_LDO2	ILIM_LDO2	RFU	UV_FLTMSK_LDO2	OV_FLTMSK_LDO2	ILIM_FLTMSK_LDO2	RFU
E7	RFU	RANGE_LDO2	LDO2 VSET[5:0]					
E8	ON LDO2	PBIN EN LDO2	AUXIN EN LDO2	SLEEP EN LDO2	DPSLEEP EN LDO2	RFU		
E9	ON DELAY LDO2[2:0]			OFF DELAY LDO2[2:0]			MODE LDO2	RST LDO2
EA	RFU				RFU			

LDO3 and LDO6

ADD (HEX)	7	6	5	4	3	2	1	0
20	PWR_GOOD_LDO6	OV_LDO6	ILIM_LDO6	RFU	UV_FLTMSK_LDO6	OV_FLTMSK_LDO6	ILIM_FLTMSK_LDO6	RFU
21	RANGE_LDO6	POR_MSK_L6	LDO6 VSET[5:0]					
22	ON LDO6	PBIN EN LDO6	AUXIN EN LDO6	SLEEP EN LDO6	DPSLEEP EN LDO6	RFU		
23	ON DELAY LDO6[2:0]			OFF DELAY LDO6[2:0]			MODE LDO6	RST LDO6
24	RFU				RFU			
25	ILIM SD DIS_LDO6	RFU	OnDLYRangeL6	DIS_PD_LDO6	OffDLYRangeL6	ILIM_SCL_LDO6	SST_LDO6	QLTCH LDO6
26	PWR_GOOD_LDO3	OV_LDO3	ILIM_LDO3	RFU	UV_FLTMSK_LDO3	OV_FLTMSK_LDO3	ILIM_FLTMSK_L3	RFU

27	RANGE_LDO3	POR_MSK_L3	LDO3 VSET[5:0]					
28	ON LDO3	PBIN EN LDO3	AUXIN EN LDO3	SLEEP EN LDO3	DPSLEEP EN LDO3	RFU		
29	ON DELAY LDO3[2:0]			OFF DELAY LDO3[2:0]			MODE LDO3	RST LDO3
2A	RFU				RFU			
	LDO4 and LSW7							
ADD (HEX)	7	6	5	4	3	2	1	0
C0	PWR_GOOD_LSW7	OV_LSW7	ILIM_LSW7	RFU	UV_FLTMSK_LSW7	OV_FLTMSK_LSW7	ILIM_FLTMSK_LSW7	RFU
C1	RFU	BK2_VSET3[6:0]						
C2	ON_LSW7	PBIN_EN_LSW7	AUXIN_EN_LSW7	SLEEP EN LSW7	DPSLEEP EN LSW7	RFU		
C3	ON_DLY_LSW7[2:0]			OFF_DLY_LSW7[2:0]			MODE_LSW7	RST_LSW7
C4	RFU				RFU			
C5	ILIM_SD_DIS_LSW7	POR_MSK_L7	OnDLYRangeL7	DIS_PULLDOWN_LSW7	OffDLYRangeL7	RFU	RFU	QLTCH LSW7
C6	PWR_GOOD_LDO4	OV_LDO4	ILIM_LDO4	RFU	UV_FLTMSK_LDO4	OV_FLTMSK_LDO4	ILIM_FLTMSK_L4	RFU
C7	LDO4_RANGE	POR_MSK_L4	LDO4 VSET[5:0]					
C8	ON LDO4	PBIN EN LDO4	AUXIN EN LDO4	SLEEP EN LDO4	DPSLEEP EN LDO4	RFU		
C9	ON DELAY LDO4[2:0]			OFF DELAY LDO4[2:0]			MODE LDO4	RST LDO4
CA	RFU				RFU			
	LDO5 and LSW8							
ADD (HEX)	7	6	5	4	3	2	1	0
C0	PWR_GOOD_LSW8	OV_LSW8	ILIM_LSW8	RFU	UV_FLTMSK_LSW8	OV_FLTMSK_LSW8	ILIM_FLTMSK_LSW8	RFU
C1	RFU	BK1_VSET3[6:0]						
C2	ON LSW8	PBIN EN LSW8	AUXIN EN LSW8	SLEEP EN LSW8	DPSLEEP EN LSW8	RFU		
C3	ON DELAY LSW8 [2:0]			OFF DELAY LSW8 [2:0]			MODE LSW8	RST LSW8
C4	RFU				RFU			
C5	ILIM SHUTDOWN DIS_L8	POR_MSK_L8	OnDelayRangeL8	DisPULLDOWN_L8	OffDelayRangeL8	RFU	RFU	QLTCH LSW8
C6	PWR_GOOD_LDO5	OV_LDO5	ILIM_LDO5	RFU	UV_FLTMSK_LDO5	OV_FLTMSK_LDO5	ILIM_FLTMSK_L5	RFU
C7	RANGE_LDO5	POR_MSK_L5	LDO5 VSET[5:0]					
C8	ON LDO5	PBIN EN LDO5	AUXIN EN LDO5	SLEEP EN LDO5	DPSLEEP EN LDO5	RFU		
C9	ON DELAY LDO5[2:0]			OFF DELAY LDO5[2:0]			MODE LDO5	RST LDO5
CA	RFU				RFU			

MASTER REGISTERS

MSTR00 - Master Configuration Register

Address = 0x00h	Default = 0x00h	Type = Basic Volatile

BIT	7	6	5	4	3	2	1	0
Name	RFU	WD_TIMER_ALERT	TWARN	VSYSSTAT	VIN_POK_OV	PBASTAT	VSYSWARN	PBDSTAT
Default	0	0	0	0	0	0	0	0
Access	RO	RO	RO	RO	RO	RO	RO	RO

Name	Description	Notes
RFU	Reserved for Future Use	
WDTIMER_ALERT	Watch Dog Timer Alert status: 0 – the timer is not expired 1 – the timer is expired (7.4s)	If watchdog is enabled and watchdog timer times out, this bit goes high and stays latched high until is read.
TWARN	Thermal Interrupt Status: 0: Die temperature is lower than Warning threshold 1: Die temperature is higher than Warning threshold	If die temperature > Thermal Warning Threshold, this bit goes high. It stays latched high until die temperature < Thermal Warning Threshold – Hysteresis and it is read.
VSYSSTAT	VSYSMON status: 0 – VSYS > VSYS Monitor Threshold 1 – VSYS < VSYS Monitor Threshold	VSYSSTAT is latched to 1 at falling edge of VIN and clear to 0 after read back this byte.
VIN_POK_OV	VIN Over Voltage (interrupt) status: 0 – VIN < VIN_POK_OV 1 – VIN> VIN_POK_OV	Input above VIN_POK OV threshold VIN_POK_OV=1: If VIN_POK_nMASK=0 it provides real time status of POK OV If VIN_POK_nMASK=1, POK OV status is latched until POK_OV is read via I2C.
PBASTAT	Push - Button assert Status: 0 – Push-Button is not assert 1 – Push-Button asserting happens	When the Push Button is asserted this bit goes high and stays latched high until is read.
VSYSWARN	VSYSWARN status: 0 – VIN > VSYS_WARN 1 – VIN< VSYS_WARN	SYSWARN is latched to 1 at falling edge of VIN and clear to 0 after read back this byte.
PBDSTAT	Push - Button De-assert Status: 1 – Push-Button de-asserting happen 0 – Push-Button is not de-assert.	When Push Button de-asserting happens, this bit goes high and stays latched high until it is read.

MSTR01 - Master Configuration Register

Address = 0x01h	Default = 0xFFh	Type = Basic Volatile

BIT	7	6	5	4	3	2	1	0
Name	RFU	WD_ALERT_MSK	TMSK	VSYSMSK	VIN_POK_OV_MSK	PBAMSK	VSYSWARN_MSK	PBDMSK
Default	1	1	1	1	1	1	1	1
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Name	Description	Notes
RFU	Reserved for Future Use	
WD_ALERT_MSK	Watch Dog timer Alert Mask: 0: Not mask interrupt 1: Mask interrupt	Mask the interrupt of Watch Dog Timer Expiration.
TMSK	Thermal Interrupt Mask: 0: Not mask interrupt 1: Mask interrupt	Mask the interrupt of Thermal Warning Assert.
VSYSMSK	SYSMON Interrupt Mask: 0: Not mask interrupt 1: Mask interrupt	Mask the interrupt of VSYSMON Assert.
VIN_POK_OV_MSK	VIN POK OV Interrupt Mask: 0: Not mask interrupt 1: Mask interrupt	Mask the interrupt of VIN POK OV Assert.
PBAMSK	Push - Button Assert Interrupt Mask: 0: Not mask interrupt 1: Mask interrupt	Mask the interrupt of Push - Button Assert. Recommend: should readback REG0x00 to clear all PB status before unmask PBA.
VSYSWARN_MSK	SYSWARN Interrupt Mask: 0: Not mask interrupt 1: Mask interrupt	Mask the interrupt of VSYSWARN Assert.
PBDMSK	Push - Button De-Assert Interrupt Mask: 0: Not mask interrupt 1 – Mask interrupt	Mask the interrupt of Push - Button De-Assert. Recommend: should readback REG0x00 to clear all PB stats before unmask PBD

MSTR02 - Master Configuration Register

Address = 0x02h	Default = 0x71h	Type = Basic Volatile

BIT	7	6	5	4	3	2	1	0
Name	RFU	OK_START	VSYSWARN_RT	VSYSDAT	DVS_I2C_DB11	DVS_I2C_DB10	DVS_I2C_DB9	PBDAT
Default								
Access	RO	RW	RO	RO	RW	RW	RW	RO

Name	Description	Notes
RFU	Reserved for Future Use	Do not change this register value. Changing the register value can affect IC functionality.
OK_START	0 – Not allow. 1 – Allow nPB/sleep/dpslp control system.	
VSYSWARN_RAW	VSYSWARN Raw Data: 0 – VIN is lower than VSYSWARN 1 – VIN is higher than VSYSWARN	Real time status of the AVIN voltage being above or below the SYSWARN threshold
VSYSDAT	VSYSMON Raw Data: 0 – VIN is lower than VSYSMON 1 – VIN is higher than VSYSMON	Real time status of the AVIN voltage being above or below the SYSMON threshold
DVS_I2C_DB11	Control BUCK3/4 DVS when I2C_EN_DVS=1	
DVS_I2C_DB10	Control BUCK3/4 DVS when I2C_EN_DVS=1	
DVS_I2C_DB9	Control BUCK3/4 DVS when I2C_EN_DVS=1	
PBDAT	Push-Button mode only. Push - Button Raw Data 0: PB is aserting 1 : PB is not aserting	

MSTR03 - Master Configuration Register

Address = 0x03h	Default = 0x8Ch	Type = Basic Volatile

BIT	7	6	5	4	3	2	1	0
	GPIO8 STAT	GPIO7 STAT	GPIO6 STAT	GPIO5 STAT	GPIO4 STAT	GPIO3 STAT	GPIO2 STAT	GPIO1 STAT
Default	1	0	0	0	1	1	0	0
Access	RO	RO	RO	RO	RO	RO	RO	RO

Name	Description	Notes
GPIO8 STAT	0 – GPIO8 input is logic low 1 – GPIO8 input is logic high	Shows the GPIOx input real-time status when the GPIO is configured as an input.
GPIO7 STAT	0 – GPIO7 input is logic low 1 – GPIO7 input is logic high	
GPIO6 STAT	0 – GPIO6 input is logic low 1 – GPIO6 input is logic high	
GPIO5 STAT	0 – GPIO5 input is logic low 1 – GPIO5 input is logic high	
GPIO4 STAT	0 – GPIO4 input is logic low 1 – GPIO4 input is logic high	
GPIO3 STAT	0 – GPIO3 input is logic low 1 – GPIO3 input is logic high	
GPIO2 STAT	0 – GPIO2 input is logic low 1 – GPIO2 input is logic high	
GPIO1 STAT	0 – GPIO1 input is logic low 1 – GPIO1 input is logic high	

MSTR04 - Master Configuration Register

Address = 0x04h	Default = 0x00h	Type = Basic Volatile

BIT	7	6	5	4	3	2	1	0
	GPIO8 Toggle	GPIO7 Toggle	GPIO6 Toggle	GPIO5 Toggle	GPIO4 Toggle	GPIO3 Toggle	GPIO2 Toggle	GPIO1 Toggle
Default	0	0	0	0	0	0	0	0
Access	RO	RO	RO	RO	RO	RO	RO	RO

Name	Description	Notes
GPIO8 Toggle	0 – GPIO8 input logic level has not changed 1 – GPIO8 input logic level has changed	GPIOx Toggle detect when GPIOx is configured as an input. Set to 1 when GPIOx change status and latched until read back to clear to 0.
GPIO7 Toggle	0 – GPIO7 input logic level has not changed 1 – GPIO7 input logic level has changed	
GPIO6 Toggle	0 – GPIO6 input logic level has not changed 1 – GPIO6 input logic level has changed	
GPIO5 Toggle	0 – GPIO5 input logic level has not changed 1 – GPIO5 input logic level has changed	
GPIO4 Toggle	0 – GPIO4 input logic level has not changed 1 – GPIO4 input logic level has changed	
GPIO3 Toggle	0 – GPIO3 input logic level has not changed 1 – GPIO3 input logic level has changed	
GPIO2 Toggle	0 – GPIO2 input logic level has not changed 1 – GPIO2 input logic level has changed	
GPIO1 Toggle	0 – GPIO1 input logic level has not changed 1 – GPIO1 input logic level has changed	

MSTR05 - Master Configuration Register

Address = 0x05h	Default = 0xFFh	Type = Basic Volatile

BIT	7	6	5	4	3	2	1	0
Name	GPIO8 MASK	GPIO7 MASK	GPIO6 MASK	GPIO5 MASK	GPIO4 MASK	GPIO3 MASK	GPIO2 MASK	GPIO1 MASK
Default	1	1	1	1	1	1	1	1
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Name	Description	Notes
GPIO8 MASK	0: trigger the interrupt when GPIO8 Input change status 1: not trigger the interrupt when GPIO8 Input change status	GPIOx can generate interrupt individual when GPIOx config as input, MASK bit NOT set and Toggle event happens. If not masked, a GPIO input logic level status change triggers an interrupt in register 0x04h..
GPIO7 MASK	0: trigger the interrupt when GPIO7 Input change status 1: not trigger the interrupt when GPIO7 Input change status	
GPIO6 MASK	0: trigger the interrupt when GPIO6 Input change status 1: not trigger the interrupt when GPIO6 Input change status	
GPIO5 MASK	0: trigger the interrupt when GPIO5 Input change status 1: not trigger the interrupt when GPIO5 Input change status	
GPIO4 MASK	0: trigger the interrupt when GPIO4 Input change status 1: not trigger the interrupt when GPIO4 Input change status	
GPIO3 MASK	0: trigger the interrupt when GPIO3 Input change status 1: not trigger the interrupt when GPIO3 Input change status	
GPIO2 MASK	0: trigger the interrupt when GPIO2 Input change status 1: not trigger the interrupt when GPIO2 Input change status	
GPIO1 MASK	0: trigger the interrupt when GPIO1 Input change status 1: not trigger the interrupt when GPIO1 Input change status	

MSTR06 - Master Configuration Register

Address = 0x06h	Default = 0xFFh	Type = Basic Volatile

BIT	7	6	5	4	3	2	1	0
Name	INTADR[7:0]							
Default	1							
Access	RO							

Name	Description	Notes
INTADR[7:0]	Indicates the interrupt tile address: Value: Tile 0x00: MSTR or BK5 0x01: GPIO or LDO9, 10 0x40: BK1 or BK2 0x60: BK3 or BK4 0x80: BST8 or BST9 0xA0: BB6 or BB7 0xE1: LDO1 0xE2: LDO2 0x21: LDO6 0x22: LDO3 0xC1: LSW7 or LSW8 0xC2: LDO4 or LDO5	The value contained in this register identifies the I^2C register block that generated the interrupt. This lets the user know what part of the IC generated an interrupt. Real time value of the interrupt address.

MSTR07 - Master Configuration Register

Address = 0x07h	Default = 0x04h	Type = Basic Volatile

BIT	7	6	5	4	3	2	1	0
Name	RFU	SLEEP	RFU	DPSLP	RFU	POWER OFF	WDPCEN	WDSREN
Default	0	0	0	0	0	1	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Name	Description	Notes
RFU	Reserved for Future Use	Do not change this register value. Changing the register values can affect IC functionality.
SLEEP	0 – Can make IC exit SLEEP state 1 – Can make IC enter SLEEP state	See datasheet for details on how this bit puts IC into SLEEP state
RFU	Reserved for Future Use	Do not change this register value. Changing the register values can affect IC functionality.
DPSLP	0 – Can make IC exit DPSLP state. 1 – Can make IC enter DPSLP state.	See datasheet for details on how this bit puts IC into DPSLP state
RFU	Reserved for Future Use	Do not change this register value. Changing the register values can affect IC functionality.
POWER OFF	0 – IC is operating normally 1 – Clear all VM register, IC move to POWER OFF state.	Write from 1 to 0 to move the IC from POWER OFF to POWER ON
WDPCEN	0 – IC does not power cycle if the watchdog timer times out 1 – IC power cycles if the watchdog timer times out(8s),IC will turn off REGs follow sequence, after 0.5s turn-on again.	Note that this is a higher priority than WDSREN
WDSREN	0 – Disables a soft reset if the watchdog timer times out 1 – Enables a soft reset if the watchdog timer times out	

MSTR2B - Master Configuration Register

Address = 0x2Bh	Default = 0x26h	Type = Basic Volatile

BIT	7	6	5	4	3	2	1	0
Name	GPIO9 STAT	GPIO9 Toggle	GPIO9 MASK	GPIO10 STAT	GPIO10 Toggle	GPIO10 MASK	GPIO11 STAT	GPIO11 Toggle
Default	0	0	1	0	0	1	1	0
Access	RO	RO	R/W	RO	RO	R/W	RO	RO

Name	Description	Notes
GPIO9 STAT	0 – GPIO9 input is logic low 1 – GPIO9 input is logic high	
GPIO9 Toggle	0 – GPIO9 input logic level has not changed 1 – GPIO9 input logic level has changed	
GPIO9 MASK	0: trigger the interrupt when GPIO9 Input change status 1: not trigger the interrupt when GPIO9 Input change status	
GPIO10 STAT	0 – GPIO10 input is logic low 1 – GPIO10 input is logic high	
GPIO10 Toggle	0 – GPIO10 input logic level has not changed 1 – GPIO10 input logic level has changed	
GPIO10 MASK	0: trigger the interrupt when GPIO10 Input change status 1: not trigger the interrupt when GPIO10 Input change status	
GPIO11 STAT	0 – GPIO11 input is logic low 1 – GPIO11 input is logic high	
GPIO11 Toggle	0 – GPIO11 input logic level has not changed 1 – GPIO11 input logic level has changed	

MSTR2C - Master Configuration Register

Address = 0x2Ch	Default = 0x03h	Type = Basic Volatile

BIT	7	6	5	4	3	2	1	0
Name	BK1_DVS_I2C[1:0]		BK2_DVS_I2C[1:0]		BK5_DVS_I2C[1:0]		GPIO11 MASK	LDOUV_FLTMSK
Default	0	0	0	0	0	0	1	1
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Name	Description	Notes
BK1_DVS_I2C[1:0]	With condition BUCK1_I2C_DVS_EN[]=1, select VSET for BUCK1: 00 : select VSET0 01 : select VSET1 10: select VSET2 11: select VSET3	
BK2_DVS_I2C[1:0]	With condition BUCK2_I2C_DVS_EN[]=1, select VSET for BUCK2: 00 : select VSET0 01 : select VSET1 10: select VSET2 11: select VSET3	
BK5_DVS_I2C[1:0]	With condition BUCK5_I2C_DVS_EN[]=1 , select VSET for BUCK5: 00 : select VSET0 01 : select VSET1 10: select VSET2 11: select VSET3	
GPIO11 MASK	0: trigger the interrupt when GPIO11 Input change status 1: not trigger the interrupt when GPIO11 Input change status	
LDOUV_FLTMSK	0: Unmask interrupt cause by nLDO9_POK OR nLDO10_POK. 1: Mask interrupt cause by LDO9_POK OR nLDO10_POK.	

MSTR39 - Master Configuration Register

Address = 0x39h	Default = 0x5Ch	Type = Basic Volatile

BIT	7	6	5	4	3	2	1	0
Name	ILIM_LDO 9	PG_LDO9	ILIM_LDO 10	PG_LDO1 0	LDOILIM_ FLTMSK	GPIO12 MASK	GPIO12 STAT	GPIO12 Toggle
Default	0	1	0	1	1	1	0	0
Access	RO	RO	RO	RO	R/W	R/W	RO	RO

Name	Description	Notes
ILIM_LDO9	Ilim status of LDO9	
PG_LDO9	Power good status of LDO9	
ILIM_LDO10	Ilim status of LDO10	
PG_LDO10	Power good status of LDO10	
LDOILIM_FLTMSK	0: Unmask interrupt cause by LDO9_ILIM OR LDO10_ILIM. 1: Mask interrupt cause by LDO9_ILIM OR LDO10_ILIM.	
GPIO12 MASK	0: trigger the interrupt when GPIO12 Input change status 1: not trigger the interrupt when GPIO12 Input change status	
GPIO12 STAT	0 – GPIO12 input is logic low 1 – GPIO12 input is logic high	
GPIO12 Toggle	0 – GPIO12 input logic level has not changed 1 – GPIO12 input logic level has changed	

MSTR09 - Master Configuration Register

Address = 0x09h	Default = 0x50h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0	
Name	TRST_DLY[2:0]			PWRCYC_TIME[1:0]		PWROFF_TIME[1:0]		DIS OV UV SD	
Default	0	1	1	1	0	0	0	0	0
Access	R/W			R/W		R/W		R/W	

Name	Description	Notes
TRST_DLY[2:0]	Setting delay time for nRESET: 000: 2.5ms 001: 5ms 010: 10ms 011: 20ms 100: 40ms 101: 60ms 110: 80ms 111: 100ms	
PWRCYC_TIME[1:0]	Setting timer for power cycle: 00: 1s<t<4s (trigger at released). 01: 4s<t<8s (trigger at released). 10: 8s, trigger at exact 8s. 11: 12s, trigger at exact 12s.	
PWROFF_TIME[1:0]	Setting timer for power off: 00: 1s<t<4s (trigger at released). 01: 4s<t<8s (trigger at released). 10: 8s, trigger at exact 8s. 11: 12s, trigger at exact 12s.	
DIS OV UV SD	Disable UVOV of REGs: 0 – If an output enters an UV/OV fault condition, the IC enters the OVUV Fault State 1 – If an output enters an UV/OV fault condition, the IC does not enter UVOV Fault State	

MSTR0A - Master Configuration Register

Address = 0x0Ah	Default = 0x80h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	EN_LDO910_DLY_OFF	EN POWEROFF	RFU	VSYSMON[4:0]				
Default	1	0	0	0				
Access	R/W	R/W	R/W	R/W				

Name	Description	Notes
EN_LDO910_DLY_OFF	1: Delay turn-off LDO9/10 variation from 100ms to 200ms 0: There is no delay turn-off	
EN POWEROFF	0 – Disable Power OFF by Push-Button 1 – Enable Power OFF by Push-Button	
RFU	Reserved for Future Use	Do not change this register value. Changing the register values can affect IC functionality.
VSYSMON[4:0]	VSYSMON rising Threshold (hysteresis =100mV) 00000: 2.7V to 10101: 4.8V, Step size = 100mV 10101to 11111: 4.8V	

MSTR0B - Master Configuration Register

Address = 0x0Bh	Default = 0x00h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	IO1_DLY[1:0]		IO2_DLY[1:0]		IO3_DLY[1:0]		IO4_DLY[1:0]	
Default	0		0		0		0	
Access	R/W		R/W		R/W		R/W	

Name	Description	Notes
IOx_DLY[1:0]	Delay setting for both input mode/ output OD mode of GPIOx. 00: 0ms 01: 1ms 10: 2ms 11: 4ms	

MSTR0C - Master Configuration Register

Address = 0x0Ch	Default = 0x00h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	IO5_DLY[1:0]		IO6_DLY[1:0]		IO7_DLY[1:0]		RFU	RETRY TIME
Default	0		0		0		0	0
Access	R/W		R/W		R/W		R/W	R/W

Name	Description	Notes
IOx_DLY[1:0]	Delay setting for both input mode/ output OD mode of GPIOx. 00: 0ms 01: 1ms 10: 2ms 11: 4ms	
RETRY TIME	Retry timer setting 0: 100ms, 1: 250ms	

MSTR0D ~ 13, MSTR27 ~ 32 – GPIOs Mode Configuration

Address = 0x0Dh-0x13h, 0x27-0x32	Default = N/A	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	MODEx[3:0]				MUXx[3:0]			
Default	xxxx				xxxx			
Access	R/W				R/W			

Name	Description	Notes
MODEx[3:0]	Determines startup sequencing from the CMI code	This is a factory expert bit that should not be changed. Modifying this bit may result in unexpected IC behavior.
MUXx[3:0]	Determines startup sequencing from the CMI code	This is a factory expert bit that should not be changed. Modifying this bit may result in unexpected IC behavior.

MSTR14 – Master Configuration Register

Address = 0x14h	Default = 0xCCh	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	POK_OV[2:0]			VSYSWARN[4:0]				
Default	1	1	0	0	1	1	0	0
Access	R/W			R/W				

Name	Description	Notes
POK_OV[2:0]	VIN_POK_OV setting (rising): 000 – 3.50V 100 – 4.70V 001 – 3.80V 101 – 5.00V 010 – 4.10V 110 – 5.30V 011 – 4.40V 111 – 5.60V	
VSYSWARN[4:0]	VSYSWARN Falling Threshold: (hystereris=100mV) 00000: 2.7V to 11000: 3.3V Step size = 25mV 11000 to 11111: 3.3V	

MSTR33 – Master Configuration Register

Address = 0x33h	Default = 0xC4h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	PC[13:6]							
Default	1	1	0	0	0	1	0	0
Access	R/W				R/W			

Name	Description	Notes
PC[13:6]	Product control	

MSTR34 – Master Configuration Register

Address = 0x34h	Default = 0x01h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	nSAVE_IQ_MSTR	EN_PP_IO8	EN_PP_IO7	EN_PP_IO6	EN_PP_IO4	EN_PP_IO3	EN_PP_IO2	EN_PP_IO1
Default	0	0	0	0	0	0	0	1
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Name	Description	Notes
nSAVE_IQ_MSTR	With EN_SAVE_CURRENT_MSTR=1 0 = Shutdown some circuit (VINT REG, OSC…) to save current in POWER OFF state. 1 = Turn-on circuit on MSTR in POWER OFF state, include REF, OSC, VINT REG....	
EN_PP_IOx	0 = GPIOx will be Open drain 1 = Enable push pull option when the GPIOx set as output mode	

MSTR35 – Master Configuration Register

Address = 0x35h	Default = 0xA7h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	EN_PP_IO12	EN_PP_IO11	amode_en	EDGE_IN1[4:0]				
Default	1	0	1	0	0	1	1	1
Access	R/W	R/W	R/W	R/W				

Name	Description	Notes
EN_PP_IOx	0 = GPIOx will be Open drain 1 = Enable push pull option when the GPIOx set as output mode	
amode_en	Enable analog mode for GPIO9,10. Active high.	
EDGE_IN1[4:0]	Select 1st TILE's PG. See table EDGE_IN Select for detail.	

MSTR36 – Master Configuration Register

Address = 0x36h	Default = 0xC1h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	EN_LDO10	EN_LDO9	GPIO_ANA_ SLP CTRL EN	EDGE_IN2[4:0]				
Default	1	1	0	0	0	0	0	1
Access	R/W	R/W	R/W	R/W				

Name	Description	Notes
EN_LDO10	0: Disable LDO10 1: Enable LDO10	
EN_LDO9	0: Disable LDO9 1: Enable LDO9	
GPIO_ANA_ SLP CTRL EN	0 : Disable GPIO Analog Mode in DEEP SLEEP mode. 1: Enable GPIO Analog Mode in DEEP SLEEP mode	
EDGE_IN2[4:0]	Select 2nd TILE's PG. See table EDGE_IN Select for detail.	

MSTR37 - Master Configuration Register

Address = 0x37h	Default = 0x0Ch	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	MSK_FLT_LDO9	RFU	VSET_LDO9[5:0]					
Default	0	0	0	0	1	1	0	0
Access	R/W	R/W	R/W					

Name	Description	Notes
MSK_FLT_LDO9	Mask fault ILIM/UV for LDO9	
RFU	Reserved for Future Use	Do not change this register value. Changing the register values can affect IC functionality.
VSET_LDO9[5:0]	VSET for LDO9	

MSTR38 - Master Configuration Register

Address = 0x38h	Default = 0xAAh	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	MSK_FLT_LDO10	RFU	VSET_LDO10[5:0]					
Default	1	0	1	0	1	0	1	0
Access	R/W	R/W	R/W					

Name	Description	Notes
MSK_FLT_LDO10	Mask fault ILIM/UV for LDO10	
RFU	Reserved for Future Use	Do not change this register value. Changing the register values can affect IC functionality.
VSET_LDO10[5:0]	VSET for LDO10	

MSTR3B - Master Configuration Register

Address = 0x3Bh	Default = 0x00h	Type = Basic Volatile

BIT	7	6	5	4	3	2	1	0
Name	LED2 DBL BLINK	LED_DELAY2<2:0>			ILED2<3:0>			
Default	0	0	0	0	0	0	0	0
Access	R/W	R/W			R/W			

Name	Description	Notes

LED2 DBL BLINK	0 : Single blink mode : one time per each cycle. 1: Double blink mode : two time per each cycle.	
LED_DELAY2<2:0>	LED_DELAY<2:0> : DELAY (%) 000=0 001=12.5 010=25 011=37.5 100=50 101=62.5 110=75 111=87.5	
ILED2<3:0>	ILED<3:0>:LED CURRENT (mA) 0000=0 0001=1 0010=2 0011=3 0100=4 0101=5 0110=6 0111=7 1000=8 1001=9 1010=10 1011=11 1100=12 1101=13 1110=14 1111=15	

MSTR3C - Master Configuration Register

Address = 0x3Ch	Default = 0x00h	Type = Basic Volatile

BIT	7	6	5	4	3	2	1	0
Name	LED1 DBL BLINK	LED_DELAY1<2:0>			ILED1<3:0>			
Default	0	000			0000			
Access	R/W	R/W			R/W			

Name	Description	Notes
LED1 DBL BLINK	0 : Single blink mode : one time per each cycle. 1: Double blink mode : two time per each cycle.	
LED_DELAY1<2:0>	LED_DELAY<2:0> : DELAY (%) 000=0 001=12.5 010=25 011=37.5 100=50 101=62.5 110=75 111=87.5	
ILED1<3:0>	ILED<3:0>:LED CURRENT (mA) 0000=0 0001=1 0010=2 0011=3	

	0100=4 0101=5 0110=6 0111=7 1000=8 1001=9 1010=10 1011=11 1100=12 1101=13 1110=14 1111=15	

MSTR3D - Master Configuration Register

Address = 0x3Dh	Default = 0x00h	Type = Basic Volatile

BIT	7	6	5	4	3	2	1	0
Name	LED_BREATHE2_EN	PWMFREQ2			PWMDUTY2			
Default	0	000			0000			
Access	R/W	R/W			R/W			

Name	Description	Notes
LED_BREATHE2_EN	0 : Disable breathe mode. 1: Enable breathe mode.	
PWMFREQ2	PWMFREQ<2:0> : LED TIME PERIOD (s) 000=0.233 001=0.466 010=0.932 011=1.398 100=1.864 101=2.795 110=3.725 111=5.592	
PWMDUTY2	PWMDUTY<3:0> : LED DUTY CYCLE (%) 0000=6.25 0001=12.5 0010=18.75 0011=25 0100=31.25 0101=37.5 0110=43.75 0111=50 1000=56.25 1001=62.5 1010=68.75 1011=75 1100=81.25 1101=87.5 1110=93.75 1111=100	

MSTR3E - Master Configuration Register

Address = 0x3Eh	Default = 0x00h	Type = Basic Volatile

BIT	7	6	5	4	3	2	1	0
Name	LED_BREATHE1_EN	PWMFREQ1			PWMDUTY1			
Default	0	000			0000			
Access	R/W	R/W			R/W			

Name	Description	Notes
LED_BREATHE1_EN	0 : Disable breathe mode. 1: Enable breathe mode.	
PWMFREQ1	PWMFREQ<2:0> : LED TIME PERIOD (s) 000=0.233 001=0.466 010=0.932 011=1.398 100=1.864 101=2.795 110=3.725 111=5.592	
PWMDUTY1	PWMDUTY<3:0> : LED DUTY CYCLE (%) 0000=6.25 0001=12.5 0010=18.75 0011=25 0100=31.25 0101=37.5 0110=43.75 0111=50 1000=56.25 1001=62.5 1010=68.75 1011=75 1100=81.25 1101=87.5 1110=93.75 1111=100	

BUCK1 REGULATOR REGISTERS

B1_REG00 – Buck1 Configuration Register

Address = 0x40h	Default = 0x8Fh	Type = Basic Volatile

BIT	7	6	5	4	3	2	1	0
Name	POK	OV	ILIM	IWARN	UVFLTmsk	OVFLTmsk	ILIMFLTmsk	IWARNmsk
Default	1	0	0	0	1	1	1	1
Access	RO	RO	RO	RO	R/W	R/W	R/W	R/W

Name	Description	Notes
POK	POK status: 0 – Buck1 voltage is below the power good threshold 1 – Buck1 voltage is above the power good threshold	Provides real-time power good status
OV	OV status: 0 – Buck1 voltage is below the overvoltage threshold 1 – Buck1 voltage is above the overvoltage threshold	When output voltage > OV, this bit goes high. It is latched high until output voltage < OV and this bit is read.
ILIM	ILIM status: 0: Output ILIM is not triggered 1: Output ILIM is triggered	If the peak switch current reaches the ILIMSET threshold for 16 consecutive switching cycles, this bit goes high. It is latched high until peak switch current < ILIMSET and this bit is read.
IWARN	0: IWARN is not triggered 1: IIWARN is triggered	
UVFLTmsk	Mask VOUT UV interrupt: 0: Unmask Vout UV interrupt 1: Default mask Vout UV interrupt	When 1, the Buck1 POK signal is masked and does not go to the master controller. This prevents Buck1 from asserting the nIRQ pin when it is disabled or drops out of regulation. Buck1 POK still provides real-time power good status.
OVFLTmsk	Mask Vout OV interrupt: 0: Unmask Vout OV interrupt 1: Default mask Vout OV interrupt	When 1, the Buck1 OV signal is masked and does not go to the master controller. This prevents Buck1 from asserting the nIRQ pin when it is above regulation limits. Buck1 OV still provides OV status.
ILIMFLTmsk	Mask ILIM interrupt: 0: Unmask ILM interrupt 1: Default mask ILIM interrupt	When 1, the Buck1 ILIM signal is masked and does not go to the master controller. This prevents Buck1 from asserting the nIRQ pin when it is above regulation limits. Buck1 ILIM still provides current limit status.

IWARNmsk	0: Unmask IWARN interrupt, fault 1: Mask IWARN interrupt, fault	

B1_REG01 – Buck1 Configuration Register

Address = 0x41h	Default = 0x56h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	FREQ_SEL[1:0]		ENPD_LOAD	SST[2:0]			DRV_ADJ[1:0]	
Default	0	1	0	1	0	1	1	0
Access	R/W		R/W	R/W			R/W	

Name	Description	Notes
FREQ_SEL[1:0]	Select Frequency setting: 00 – 1.5MHz 01 – 2.0MHz 10 – 2.5MHz 11 – 3.3MHz	
ENPD_LOAD	0 – Disable Buck1 pulldown load current function 1 – Enable Buck1 pulldown load current function	
SST[2:0]	Soft start time setting: 000: 50us 001: 100us 010: 200us 011: 300us 100: 400us 101: 500us 110: 750us 111: 1000us	
DRV_ADJ[1:0]	Adjust Gate Driver (Rising and Falling SW): 00 – Slowest 11 – Fastest	

B1_REG02 – Buck1 Voltage Set0 Register

Address = 0x42h	Default = 0xADh	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	EN_LPM	VSET0[6:0]						
Default	1	0	1	0	1	1	0	1
Access	R/W	R/W						

Name	Description	Notes
EN_LPM	0 – Iqq = 250uA 1 – Iqq = 45uA	This bit is only effective when EN_ULPM[]=0
VSET0[6:0]	Buck1 output voltage setting VSET0: 0.5V to 1.135V in 5mV steps: VRANGE=0 VSET0: 0.5V to 3.675V in 25mV steps: VRANGE=1	

B1_REG03 – Buck1 Voltage Set1 Register

Address = 0x43h	Default = 0x2Dh	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	DIS_PD	VSET1[6:0]						
Default	0	0	1	0	1	1	0	1
Access	R/W	R/W						

Name	Description	Notes
DIS_PD	0 – Discharge VOUT when turn-off BUCK by 10Ohm 1 – Don't discharge VOUT when turn-off BUCK	Option to disable Pull-Down Resistor when BUCK is turned-off.
VSET1[6:0]	Buck1 output voltage setting VSET1: 0.5V to 1.135V in 5mV steps: VRANGE=0 VSET1: 0.5V to 3.675V in 25mV steps: VRANGE=1	

B1_REG04 – Buck1 Configuration Register

Address = 0x44h	Default = 0xD7h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	ON	PBINEN	QLTCH	SLEEP_EN	AUXIN_EN	DPSLEEP_EN	ILIM_SET[1:0]	
Default	1	1	0	1	0	1	1	1
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	

Name	Description	Notes
ON	0 – Not enable Buck 1 – Enable Buck	This functionality is dependent on the overall IC configuration. Consult the factory for details.
PBINEN	0 – Not enable turn on by Push Button 1 – Enable turn on by Push Button	This functionality is dependent on the overall IC configuration. Consult the factory for details.
QLTCH	0 – Buck1 shuts down when its sequenced input shuts down 1 – Buck1 stays on when its sequenced input shuts down	
SLEEP_EN	0 – Buck1 stays on when the IC enters Sleep mode 1 – Buck1 turns off when the IC enters Sleep mode	
AUXIN_EN	0 – Not enable turn on by AUXIN 1 – Enable turn on by AUXIN	This functionality is dependent on the overall IC configuration. Consult the factory for details.
DPSLEEP_EN	0 – Buck1 stays on when the IC enters Deep Sleep mode 1 – Buck1 turns off when the IC enters Deep Sleep mode	
ILIM_SET[1:0]	Setting for current limit: 00: LSILIM/HSILIM = 4.0A 01: LSILIM/HSILIM = 5.5A 10: LSILIM/HSILIM = 7.0A 11: LSILIM/HSILIM = 8.5A	

B1_REG05 – Buck1 Configuration Register

Address = 0x45h	Default = 0xC1h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	MODE	RST	RFU			RFU		
Default	1	1	0	0	0	0	0	1
Access	R/W	R/W	R/W			R/W		

Name	Description	Notes
MODE	Determines startup sequencing from the CMI code	This is a factory expert bit that should not be changed. Modifying this bit may result in unexpected IC behavior.
RST	0 – Buck1 does not affect nRESET output 1 – Buck1 affects nRESET output	
RFU	Reserved for Future Use	Do not change this register value. Changing the register value can affect IC functionality.
RFU	Reserved for Future Use	Do not change this register value. Changing the register value can affect IC functionality.

B1_REG06 – Buck1 Configuration Register

Address = 0x46h	Default = 0x00h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	RFU				IPD_LOAD1:0]		RFU	
Default	0	0	0	0	0	0	0	0
Access	R/W				R/W		R/W	

Name	Description	Notes
RFU	Reserved for Future Use	Do not change this register value. Changing the register value can affect IC functionality.
IPD_LOAD[1:0]	Setting the PD Load: 00: 10mA 01: 24mA 10: 37mA 11: 50mA	
RFU	Reserved for Future Use	Do not change this register value. Changing the register value can affect IC functionality.

B1_REG07 – Buck1 Configuration Register

Address = 0x47h	Default = 0xC4h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	DVS_SET[1:0]		ON_DLY[2:0]			OFF_DLY[2:0]		
Default	1	1	0	0	0	1	0	0
Access	R/W		R/W			R/W		

Name	Description	Notes
DVS_SET[1:0]	Setting DVS Slew Rate: VRANGE=0 "DVS_SET[00]: 11.26mV/us DVS_SET[01]: 5.63mV/us DVS_SET[10]: 2.82mV/us DVS_SET[11]: 1.41mV/us" VRANGE=1 "DVS_SET[00]: 56.31mV/us DVS_SET[01]: 28.15mV/us DVS_SET[10]: 14.08mV/us DVS_SET[11]: 7.04mV/us	
ON_DLY[2:0]	Follow Regulator Startup Delay Table in the Data Sheet	
OFF_DLY[2:0]	Follow Regulator Startup Delay Table in the Data Sheet	

B1_REG08 – Buck1 Configuration Register

Address = 0x48h	Default = 0x5Fh	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	VRANGE	BK1_POR_FLT_OPT	FCCM	RFU	RFU	EN_ULPM	EN_LSILIM	EN_ILIM_FB
Default	0	1	0	1	1	1	1	1
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Name	Description	Notes
VRANGE	Reserved for Future Use	Do not change this register value. Changing the register value can affect IC functionality.
BK1_POR_FLT_OPT	0 – Default loading of the UV_FLTMSK/OV_FLTMSK/ILIM_FLTMSK of BUCK1 "0" 1 – Default loading of the UV_FLTMSK/OV_FLTMSK/ILIM_FLTMSK of BUCK1 "1"	
FCCM	Force Buck work in Continue Control Mode.	
RFU	Reserved for Future Use	Do not change this register value. Changing the register value can affect IC functionality.
RFU	Reserved for Future Use	Do not change this register value. Changing the register value can affect IC functionality.
EN_ULPM	0 – Disable Ultra-LPM 1 – Enable Ultra-LPM, the supply current is 11uA @ No load, no switching	
EN_LSILIM	0 – Disable Low-Side ILIM Protection 1 – Enable Low-Side ILIM Protection. Only allow new High-Side cycle if the inductor current less than LSILIM	
EN_ILIM_FB	0 – Disable ILIM Foldback Function 1 – Enable ILIM Foldback Function	

B1_REG09 – Buck1 Voltage Set2 Register

Address = 0x57h	Default = 0xADh	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	FCCM_DVS	VSET2[6:0]						
Default	1	0	1	0	1	1	0	1
Access	R/W	R/W						

Name	Description	Notes
FCCM_DVS	Option to auto force to work in CCM mode when doing DVS 0: Disable auto force CCM 1: Enable auto force CCM	
VSET2[6:0]	Buck1 output voltage setting VSET0: 0.5V to 1.135V in 5mV steps: VRANGE=0 VSET0: 0.5V to 3.675V in 25mV steps: VRANGE=1	

BUCK2 REGULATOR REGISTERS

B2_REG00 – Buck2 Configuration Register

Address = 0x40h	Default = 0x8Fh	Type = Basic Volatile

BIT	7	6	5	4	3	2	1	0
Name	POK	OV	ILIM	IWARN	UVFLTmsk	OVFLTmsk	ILIMFLTmsk	IWARNmsk
Default	1	0	0	0	1	1	1	1
Access	RO	RO	RO	RO	R/W	R/W	R/W	R/W

Name	Description	Notes
POK	POK status: 0 – Buck2 voltage is below the power good threshold 1 – Buck2 voltage is above the power good threshold	Provides real-time power good status
OV	OV status: 0 – Buck2 voltage is below the overvoltage threshold 1 – Buck2 voltage is above the overvoltage threshold	When output voltage > OV, this bit goes high. It is latched high until output voltage < OV and this bit is read.
ILIM	ILIM status: 0: Output ILIM is not triggered 1: Output ILIM is triggered	If the peak switch current reaches the ILIMSET threshold for 16 consecutive switching cycles, this bit goes high. It is latched high until peak switch current < ILIMSET and this bit is read.
IWARN	0: IWARN is not triggered 1: IIWARN is triggered	
UVFLTmsk	Mask VOUT UV interrupt: 0: Unmask Vout UV interrupt 1: Default mask Vout UV interrupt	When 1, the Buck2 POK signal is masked and does not go to the master controller. This prevents Buck2 from asserting the nIRQ pin when it is disabled or drops out of regulation. Buck2 POK still provides real-time power good status.
OVFLTmsk	Mask Vout OV interrupt: 0: Unmask Vout OV interrupt 1: Default mask Vout OV interrupt	When 1, the Buck2 OV signal is masked and does not go to the master controller. This prevents Buck2 from asserting the nIRQ pin when it is above regulation limits. Buck2 OV still provides OV status.
ILIMFLTmsk	Mask ILIM interrupt: 0: Unmask ILM interrupt 1: Default mask ILIM interrupt	When 1, the Buck2 ILIM signal is masked and does not go to the master controller. This prevents Buck2 from asserting the nIRQ pin when it is above regulation limits. Buck2 ILIM still provides current limit status.
IWARNmsk	0: Unmask IWARN interrupt, fault 1: Mask IWARN interrupt, fault	

B2_REG01 – Buck2 Configuration Register

Address = 0x41h	Default = 0x56h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	FREQ_SEL[1:0]		ENPD_LOAD	SST[2:0]			DRV_ADJ[1:0]	
Default	0	1	0	1	0	1	1	0
Access	R/W		R/W	R/W			R/W	

Name	Description	Notes
FREQ_SEL[1:0]	Select Frequency setting: 00 – 1.5MHz 01 – 2.0MHz 10 – 2.5MHz 11 – 3.3MHz	
ENPD_LOAD	0 – Disable Buck2 pulldown load current function 1 – Enable Buck2 pulldown load current function	
SST[2:0]	Soft start time setting: 000: 50us 001: 100us 010: 200us 011: 300us 100: 400us 101: 500us 110: 750us 111: 1000us	
DRV_ADJ[1:0]	Adjust Gate Driver (Rising and Falling SW): 00 – Slowest 11 – Fastest	

B2_REG02 – Buck2 Voltage Set0 Register

Address = 0x42h	Default = 0xADh	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	EN_LPM	VSET0[6:0]						
Default	1	0	1	0	1	1	0	1
Access	R/W	R/W						

Name	Description	Notes
EN_LPM	0 – Iqq = 250uA 1 – Iqq = 45uA	This bit is only effective when EN_ULPM[]=0
VSET0[6:0]	Buck2 output voltage setting VSET0: 0.5V to 1.135V in 5mV steps: VRANGE=0 VSET0: 0.5V to 3.675V in 25mV steps: VRANGE=1	

B2_REG03 – Buck2 Voltage Set1 Register

Address = 0x43h	Default = 0x2Dh	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	DIS_PD	VSET1[6:0]						
Default	0	0	1	0	1	1	0	1
Access	R/W	R/W						

Name	Description	Notes
DIS_PD	0 – Discharge VOUT when turn-off BUCK by 10Ohm 1 – Don't discharge VOUT when turn-off BUCK	Option to disable Pull-Down Resistor when BUCK is turned-off.
VSET1[6:0]	Buck2 output voltage setting VSET1: 0.5V to 1.135V in 5mV steps: VRANGE=0 VSET1: 0.5V to 3.675V in 25mV steps: VRANGE=1	

B2_REG04 – Buck2 Configuration Register

Address = 0x44h	Default = 0xD7h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	ON	PBINEN	QLTCH	SLEEP_EN	AUXIN_EN	DPSLEEP_EN	ILIM_SET[1:0]	
Default	1	1	0	1	0	1	1	1
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	

Name	Description	Notes
ON	0 – Not enable Buck 1 – Enable Buck	This functionality is dependent on the overall IC configuration. Consult the factory for details.
PBINEN	0 – Not enable turn on by Push Button 1 – Enable turn on by Push Button	This functionality is dependent on the overall IC configuration. Consult the factory for details.
QLTCH	0 – Buck2 shuts down when its sequenced input shuts down 1 – Buck2 stays on when its sequenced input shuts down	
SLEEP_EN	0 – Buck2 stays on when the IC enters Sleep mode 1 – Buck2 turns off when the IC enters Sleep mode	
AUXIN_EN	0 – Not enable turn on by AUXIN 1 – Enable turn on by AUXIN	This functionality is dependent on the overall IC configuration. Consult the factory for details.
DPSLEEP_EN	0 – Buck2 stays on when the IC enters Deep Sleep mode 1 – Buck2 turns off when the IC enters Deep Sleep mode	
ILIM_SET[1:0]	Setting for current limit: 00: LSILIM/HSILIM = 4.0A 01: LSILIM/HSILIM = 5.5A 10: LSILIM/HSILIM = 7.0A 11: LSILIM/HSILIM = 8.5A	

B2_REG05 – Buck2 Configuration Register

Address = 0x45h	Default = 0xC0h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	MODE	RST	RFU			RFU		
Default	1	1	0	0	0	0	0	0
Access	R/W	R/W	R/W			R/W		

Name	Description	Notes
MODE	Determines startup sequencing from the CMI code	This is a factory expert bit that should not be changed. Modifying this bit may result in unexpected IC behavior.
RST	0 – Buck2 does not affect nRESET output 1 – Buck2 affects nRESET output	
RFU	Reserved for Future Use	Do not change this register value. Changing the register value can affect IC functionality.
RFU	Reserved for Future Use	Do not change this register value. Changing the register value can affect IC functionality.

B2_REG06 – Buck2 Configuration Register

Address = 0x46h	Default = 0x00h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	RFU				IPD_LOAD[1:0]		RFU	
Default	0	0	0	0	0	0	0	0
Access	R/W				R/W		R/W	

Name	Description	Notes
RFU	Reserved for Future Use	Do not change this register value. Changing the register value can affect IC functionality.
IPD_LOAD[1:0]	Setting the PD Load: 00: 10mA 01: 24mA 10: 37mA 11: 50mA	
RFU	Reserved for Future Use	Do not change this register value. Changing the register value can affect IC functionality.

B2_REG07 – Buck2 Configuration Register

Address = 0x47h	Default = 0xC4h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	DVS_SET[1:0]		ON_DLY[2:0]			OFF_DLY[2:0]		
Default	1	1	0	0	0	1	0	0
Access	R/W		R/W			R/W		

Name	Description	Notes
DVS_SET[1:0]	Setting DVS Slew Rate: VRANGE=0 "DVS_SET[00]: 11.26mV/us DVS_SET[01]: 5.63mV/us DVS_SET[10]: 2.82mV/us DVS_SET[11]: 1.41mV/us" VRANGE=1 "DVS_SET[00]: 56.31mV/us DVS_SET[01]: 28.15mV/us DVS_SET[10]: 14.08mV/us DVS_SET[11]: 7.04mV/us	
ON_DLY[2:0]	Follow Regulator Startup Delay Table in the Data Sheet	
OFF_DLY[2:0]	Follow Regulator Startup Delay Table in the Data Sheet	

B2_REG08 – Buck2 Configuration Register

Address = 0x48h	Default = 0x5Fh	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	VRANGE	BK2_POR_FLT_OPT	FCCM	RFU	RFU	EN_ULPM	EN_LSILIM	EN_ILIM_FB
Default	0	1	0	1	1	1	1	1
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Name	Description	Notes
VRANGE	Reserved for Future Use	Do not change this register value. Changing the register value can affect IC functionality.
BK2_POR_FLT_OPT	0 – Default loading of the UV_FLTMSK/OV_FLTMSK/ILIM_FLTMSK of BUCK2 "0" 1 – Default loading of the UV_FLTMSK/OV_FLTMSK/ILIM_FLTMSK of BUCK2 "1"	
FCCM	Force Buck work in Continue Control Mode.	
RFU	Reserved for Future Use	Do not change this register value. Changing the register value can affect IC functionality.
RFU	Reserved for Future Use	Do not change this register value. Changing the register value can affect IC functionality.
EN_ULPM	0 – Disable Ultra-LPM 1 – Enable Ultra-LPM, the supply current is 11uA @ No load, no switching	
EN_LSILIM	0 – Disable Low-Side ILIM Protection 1 – Enable Low-Side ILIM Protection. Only allow new High-Side cycle if the inductor current less than LSILIM	
EN_ILIM_FB	0 – Disable ILIM Foldback Function 1 – Enable ILIM Foldback Function	

B2_REG09 – Buck2 Voltage Set2 Register

Address = 0x57h	Default = 0xADh	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	FCCM_DVS	VSET2[6:0]						
Default	1	0	1	0	1	1	0	1
Access	R/W	R/W						

Name	Description	Notes
FCCM_DVS	Option to auto force to work in CCM mode when doing DVS 0: Disable auto force CCM 1: Enable auto force CCM	
VSET2[6:0]	Buck2 output voltage setting VSET0: 0.5V to 1.135V in 5mV steps: VRANGE=0 VSET0: 0.5V to 3.675V in 25mV steps: VRANGE=1	

BUCK3 REGULATOR REGISTERS

B3_REG00 – Buck3 Configuration Register

Address = 0x60h	Default = 0x8Fh	Type = Basic Volatile

BIT	7	6	5	4	3	2	1	0
Name	POK	OV	ILIM	IWARN	UVFLTmsk	OVFLTmsk	ILIMFLTmsk	IWARNmsk
Default	1	0	0	0	1	1	1	1
Access	RO	RO	RO	RO	R/W	R/W	R/W	R/W

Name	Description	Notes
POK	POK status: 0 – Buck3 voltage is below the power good threshold 1 – Buck3 voltage is above the power good threshold	Provides real-time power good status
OV	OV status: 0 – Buck3 voltage is below the overvoltage threshold 1 – Buck3 voltage is above the overvoltage threshold	When output voltage > OV, this bit goes high. It is latched high until output voltage < OV and this bit is read.
ILIM	ILIM status: 0: Output ILIM is not triggered 1: Output ILIM is triggered	If the peak switch current reaches the ILIMSET threshold for 16 consecutive switching cycles, this bit goes high. It is latched high until peak switch current < ILIMSET and this bit is read.
IWARN	0: IWARN is not triggered 1: IIWARN is triggered	
UVFLTmsk	Mask VOUT UV interrupt: 0: Unmask Vout UV interrupt 1: Default mask Vout UV interrupt	When 1, the Buck3 POK signal is masked and does not go to the master controller. This prevents Buck3 from asserting the nIRQ pin when it is disabled or drops out of regulation. Buck3 POK still provides real-time power good status.
OVFLTmsk	Mask Vout OV interrupt: 0: Unmask Vout OV interrupt 1: Default mask Vout OV interrupt	When 1, the Buck3 OV signal is masked and does not go to the master controller. This prevents Buck3 from asserting the nIRQ pin when it is above regulation limits. Buck3 OV still provides OV status.
ILIMFLTmsk	Mask ILIM interrupt: 0: Unmask ILM interrupt 1: Default mask ILIM interrupt	When 1, the Buck3 ILIM signal is masked and does not go to the master controller. This prevents Buck3 from asserting the nIRQ pin when it is above regulation limits. Buck3 ILIM still provides current limit status.
IWARNmsk	0: Unmask IWARN interrupt, fault 1: Mask IWARN interrupt, fault	

B3_REG01 – Buck3 Configuration Register

Address = 0x61h	Default = 0x56h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	FREQ_SEL[1:0]		ENPD_LOAD	SST[2:0]			DRV_ADJ[1:0]	
Default	0	1	0	1	0	1	1	0
Access	R/W		R/W	R/W			R/W	

Name	Description	Notes
FREQ_SEL[1:0]	Select Frequency setting: 00 – 1.5MHz 01 – 2.0MHz 10 – 2.5MHz 11 – 3.3MHz	
ENPD_LOAD	0 – Disable Buck3 pulldown load current function 1 – Enable Buck3 pulldown load current function	
SST[2:0]	Soft start time setting: 000: 50us 001: 100us 010: 200us 011: 300us 100: 400us 101: 500us 110: 750us 111: 1000us	
DRV_ADJ[1:0]	Adjust Gate Driver (Rising and Falling SW): 00 – Slowest 11 – Fastest	

B3_REG02 – Buck3 Voltage Set0 Register

Address = 0x62h	Default = 0xB4h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	EN_LPM	VSET0[6:0]						
Default	1	0	1	1	0	1	0	0
Access	R/W	R/W						

Name	Description	Notes
EN_LPM	0 – Iqq = 250uA 1 – Iqq = 45uA	This bit is only effective when EN_ULPM[]=0
VSET0[6:0]	Buck3 output voltage setting VSET0: 0.5V to 1.135V in 5mV steps: VRANGE=0 VSET0: 0.5V to 3.675V in 25mV steps: VRANGE=1	

B3_REG03 – Buck3 Voltage Set1 Register

Address = 0x63h	Default = 0x34h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	DIS_PD	VSET1[6:0]						
Default	0	0	1	1	0	1	0	0
Access	R/W	R/W						

Name	Description	Notes
DIS_PD	0 – Discharge VOUT when turn-off BUCK by 10Ohm 1 – Don't discharge VOUT when turn-off BUCK	Option to disable Pull-Down Resistor when BUCK is turned-off.
VSET1[6:0]	Buck3 output voltage setting VSET1: 0.5V to 1.135V in 5mV steps: VRANGE=0 VSET1: 0.5V to 3.675V in 25mV steps:VRANGE=1	

B3_REG04 – Buck3 Configuration Register

Address = 0x64h	Default = 0xE7h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	ON	PBINEN	QLTCH	SLEEP_EN	AUXIN_EN	DPSLEEP_EN	ILIM_SET	FCCM_DVS
Default	1	1	1	0	0	1	1	1
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Name	Description	Notes
ON	0 – Not enable Buck 1 – Enable Buck	This functionality is dependent on the overall IC configuration. Consult the factory for details.
PBINEN	0 – Not enable turn on by Push Button 1 – Enable turn on by Push Button	This functionality is dependent on the overall IC configuration. Consult the factory for details.
QLTCH	0 – Buck3 shuts down when its sequenced input shuts down 1 – Buck3 stays on when its sequenced input shuts down	
SLEEP_EN	0 – Buck3 stays on when the IC enters Sleep mode 1 – Buck3 turns off when the IC enters Sleep mode	
AUXIN_EN	0 – Not enable turn on by AUXIN 1 – Enable turn on by AUXIN	This functionality is dependent on the overall IC configuration. Consult the factory for details.
DPSLEEP_EN	0 – Buck3 stays on when the IC enters Deep Sleep mode 1 – Buck3 turns off when the IC enters Deep Sleep mode	
ILIM_SET	Setting for current limit: 0: LSILIM/HSILIM = 2A 1: LSILIM/HSILIM = 3A	
FCCM_DVS	Option to auto force to work in CCM mode when doing DVS 0: Disable auto force CCM 1: Enable auto force CCM	

B3_REG05 – Buck3 Configuration Register

Address = 0x65h	Default = 0xDCh	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	MODE	RST	RFU			RFU		
Default	1	1	0	1	1	1	0	0
Access	R/W	R/W	R/W			R/W		

Name	Description	Notes
MODE	Determines startup sequencing from the CMI code	This is a factory expert bit that should not be changed. Modifying this bit may result in unexpected IC behavior.
RST	0 – Buck3 does not affect nRESET output 1 – Buck3 affects nRESET output	
RFU	Reserved for Future Use	Do not change this register value. Changing the register value can affect IC functionality.
RFU	Reserved for Future Use	Do not change this register value. Changing the register value can affect IC functionality.

B3_REG06 – Buck3 Configuration Register

Address = 0x66h	Default = 0x00h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	RFU				IPD_LOAD[1:0]		RFU	
Default	0	0	0	0	0	0	0	0
Access	R/W				R/W		R/W	

Name	Description	Notes
RFU	Reserved for Future Use	Do not change this register value. Changing the register value can affect IC functionality.
IPD_LOAD[1:0]	Setting the PD Load: 00: 10mA 01: 24mA 10: 37mA 11: 50mA	
RFU	Reserved for Future Use	Do not change this register value. Changing the register value can affect IC functionality.

B3_REG07 – Buck3 Configuration Register

Address = 0x67h	Default = 0xCAh	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	DVS_SET[1:0]		ON_DLY[2:0]			OFF_DLY[2:0]		
Default	1	1	0	0	1	0	1	0
Access	R/W		R/W			R/W		

Name	Description	Notes
DVS_SET[1:0]	Setting DVS Slew Rate: VRANGE=0 "DVS_SET[00]: 11.26mV/us DVS_SET[01]: 5.63mV/us DVS_SET[10]: 2.82mV/us DVS_SET[11]: 1.41mV/us" VRANGE=1 "DVS_SET[00]: 56.31mV/us DVS_SET[01]: 28.15mV/us DVS_SET[10]: 14.08mV/us DVS_SET[11]: 7.04mV/us	
ON_DLY[2:0]	Follow Regulator Startup Delay Table in the Data Sheet	
OFF_DLY[2:0]	Follow Regulator Startup Delay Table in the Data Sheet	

B3_REG08 – Buck3 Configuration Register

Address = 0x68h	Default = 0xDFh	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	VRANGE	BK3_POR_FLT_OPT	FCCM	RFU	RFU	EN_ULPM	EN_LSILIM	EN_ILIM_FB
Default	1	1	0	1	1	1	1	1
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Name	Description	Notes
VRANGE	Reserved for Future Use	Do not change this register value. Changing the register value can affect IC functionality.
BK3_POR_FLT_OPT	0 – Default loading of the UV_FLTMSK/OV_FLTMSK/ILIM_FLTMSK of BUCK3 "0" 1 – Default loading of the UV_FLTMSK/OV_FLTMSK/ILIM_FLTMSK of BUCK3 "1"	
FCCM	Force Buck work in Continue Control Mode.	
RFU	Reserved for Future Use	Do not change this register value. Changing the register value can affect IC functionality.
RFU	Reserved for Future Use	Do not change this register value. Changing the register value can affect IC functionality.
EN_ULPM	0 – Disable Ultra-LPM 1 – Enable Ultra-LPM, the supply current is 11uA @ No load, no switching	
EN_LSILIM	0 – Disable Low-Side ILIM Protection 1 – Enable Low-Side ILIM Protection. Only allow new High-Side cycle if the inductor current less than LSILIM	
EN_ILIM_FB	0 – Disable ILIM Foldback Function 1 – Enable ILIM Foldback Function	

BUCK4 REGULATOR REGISTERS

B4_REG00 – Buck4 Configuration Register

Address = 0x60h	Default = 0x8Fh	Type = Basic Volatile

BIT	7	6	5	4	3	2	1	0
Name	POK	OV	ILIM	IWARN	UVFLTmsk	OVFLTmsk	ILIMFLTmsk	IWARNmsk
Default	1	0	0	0	1	1	1	1
Access	RO	RO	RO	RO	R/W	R/W	R/W	R/W

Name	Description	Notes
POK	POK status: 0 – Buck4 voltage is below the power good threshold 1 – Buck4 voltage is above the power good threshold	Provides real-time power good status
OV	OV status: 0 – Buck4 voltage is below the overvoltage threshold 1 – Buck4 voltage is above the overvoltage threshold	When output voltage > OV, this bit goes high. It is latched high until output voltage < OV and this bit is read.
ILIM	ILIM status: 0: Output ILIM is not triggered 1: Output ILIM is triggered	If the peak switch current reaches the ILIMSET threshold for 16 consecutive switching cycles, this bit goes high. It is latched high until peak switch current < ILIMSET and this bit is read.
IWARN	0: IWARN is not triggered 1: IIWARN is triggered	
UVFLTmsk	Mask VOUT UV interrupt: 0: Unmask Vout UV interrupt 1: Default mask Vout UV interrupt	When 1, the Buck4 POK signal is masked and does not go to the master controller. This prevents Buck4 from asserting the nIRQ pin when it is disabled or drops out of regulation. Buck4 POK still provides real-time power good status.
OVFLTmsk	Mask Vout OV interrupt: 0: Unmask Vout OV interrupt 1: Default mask Vout OV interrupt	When 1, the Buck4 OV signal is masked and does not go to the master controller. This prevents Buck4 from asserting the nIRQ pin when it is above regulation limits. Buck4 OV still provides OV status.
ILIMFLTmsk	Mask ILIM interrupt: 0: Unmask ILM interrupt 1: Default mask ILIM interrupt	When 1, the Buck4 ILIM signal is masked and does not go to the master controller. This prevents Buck4 from asserting the nIRQ pin when it is above regulation limits. Buck4 ILIM still provides current limit status.
IWARNmsk	0: Unmask IWARN interrupt, fault 1: Mask IWARN interrupt, fault	

B4_REG01 – Buck4 Configuration Register

Address = 0x61h	Default = 0x56h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	FREQ_SEL[1:0]		ENPD_LOAD	SST[2:0]			DRV_ADJ[1:0]	
Default	0	1	0	1	0	1	1	0
Access	R/W		R/W	R/W			R/W	

Name	Description	Notes
FREQ_SEL[1:0]	Select Frequency setting: 00 – 1.5MHz 01 – 2.0MHz 10 – 2.5MHz 11 – 3.3MHz	
ENPD_LOAD	0 – Disable Buck4 pulldown load current function 1 – Enable Buck4 pulldown load current function	
SST[2:0]	Soft start time setting: 000: 50us 001: 100us 010: 200us 011: 300us 100: 400us 101: 500us 110: 750us 111: 1000us	
DRV_ADJ[1:0]	Adjust Gate Driver (Rising and Falling SW): 00 – Slowest 11 – Fastest	

B4_REG02 – Buck4 Voltage Set0 Register

Address = 0x62h	Default = 0x9Ch	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	EN_LPM	VSET0[6:0]						
Default	1	0	0	1	1	1	0	0
Access	R/W	R/W						

Name	Description	Notes
EN_LPM	0 – Iqq = 250uA 1 – Iqq = 45uA	This bit is only effective when EN_ULPM[]=0
VSET0[6:0]	Buck4 output voltage setting VSET0: 0.5V to 1.135V in 5mV steps: VRANGE=0 VSET0: 0.5V to 3.675V in 25mV steps: VRANGE=1	

B4_REG03 – Buck4 Voltage Set1 Register

Address = 0x63h	Default = 0x1Ch	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	DIS_PD	VSET1[6:0]						
Default	0	0	0	1	1	1	0	0
Access	R/W	R/W						

Name	Description	Notes
DIS_PD	0 – Discharge VOUT when turn-off BUCK by 10Ohm 1 – Don't discharge VOUT when turn-off BUCK	Option to disable Pull-Down Resistor when BUCK is turned-off.
VSET1[6:0]	Buck4 output voltage setting VSET1: 0.5V to 1.135V in 5mV steps:VRANGE=0 VSET1: 0.5V to 3.675V in 25mV steps:VRANGE=1	

B4_REG04 – Buck4 Configuration Register

Address = 0x64h	Default = 0xD7h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	ON	PBINEN	QLTCH	SLEEP_EN	AUXIN_EN	DPSLEEP_EN	ILIM_SET	FCCM_DVS
Default	1	1	0	1	0	1	1	1
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Name	Description	Notes
ON	0 – Not enable Buck 1 – Enable Buck	This functionality is dependent on the overall IC configuration. Consult the factory for details.
PBINEN	0 – Not enable turn on by Push Button 1 – Enable turn on by Push Button	This functionality is dependent on the overall IC configuration. Consult the factory for details.
QLTCH	0 – Buck4 shuts down when its sequenced input shuts down 1 – Buck4 stays on when its sequenced input shuts down	
SLEEP_EN	0 – Buck4 stays on when the IC enters Sleep mode 1 – Buck4 turns off when the IC enters Sleep mode	
AUXIN_EN	0 – Not enable turn on by AUXIN 1 – Enable turn on by AUXIN	This functionality is dependent on the overall IC configuration. Consult the factory for details.
DPSLEEP_EN	0 – Buck4 stays on when the IC enters Deep Sleep mode 1 – Buck4 turns off when the IC enters Deep Sleep mode	
ILIM_SET	Setting for current limit: 0: LSILIM/HSILIM = 2A 1: LSILIM/HSILIM = 3A	
FCCM_DVS	Option to auto force to work in CCM mode when doing DVS 0: Disable auto force CCM 1: Enable auto force CCM	

B4_REG05 – Buck4 Configuration Register

Address = 0x65h	Default = 0xD3h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	MODE	RST	RFU			RFU		
Default	1	1	0	1	0	0	1	1
Access	R/W	R/W	R/W			R/W		

Name	Description	Notes
MODE	Determines startup sequencing from the CMI code	This is a factory expert bit that should not be changed. Modifying this bit may result in unexpected IC behavior.
RST	0 – Buck4 does not affect nRESET output 1 – Buck4 affects nRESET output	
RFU	Reserved for Future Use	Do not change this register value. Changing the register value can affect IC functionality.
RFU	Reserved for Future Use	Do not change this register value. Changing the register value can affect IC functionality.

B4_REG06 – Buck4 Configuration Register

Address = 0x66h	Default = 0x00h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	RFU				IPDLOAD[1:0]		RFU	
Default	0	0	0	0	0	0	0	0
Access	R/W				R/W		R/W	

Name	Description	Notes
RFU	Reserved for Future Use	Do not change this register value. Changing the register value can affect IC functionality.
IPDLOAD[1:0]	Setting the PD Load: 00: 10mA 01: 24mA 10: 37mA 11: 50mA	
RFU	Reserved for Future Use	Do not change this register value. Changing the register value can affect IC functionality.

B4_REG07 – Buck4 Configuration Register

Address = 0x67h	Default = 0xCBh	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	DVS_SET[1:0]		ON_DLY[2:0]			OFF_DLY[2:0]		
Default	1	1	0	0	1	0	1	1
Access	R/W		R/W			R/W		

Name	Description	Notes
DVS_SET[1:0]	Setting DVS Slew Rate: VRANGE=0 "DVS_SET[00]: 11.26mV/us DVS_SET[01]: 5.63mV/us DVS_SET[10]: 2.82mV/us DVS_SET[11]: 1.41mV/us" VRANGE=1 "DVS_SET[00]: 56.31mV/us DVS_SET[01]: 28.15mV/us DVS_SET[10]: 14.08mV/us DVS_SET[11]: 7.04mV/us	
ON_DLY[2:0]	Follow Regulator Startup Delay Table in the Data Sheet	
OFF_DLY[2:0]	Follow Regulator Startup Delay Table in the Data Sheet	

B4_REG08 – Buck4 Configuration Register

Address = 0x68h	Default = 0xDFh	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	VRANGE	BK4_POR_FLT_OPT	FCCM	RFU	RFU	EN_ULPM	EN_LSILIM	EN_ILIM_FB
Default	1	1	0	1	1	1	1	1
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Name	Description	Notes
VRANGE	Reserved for Future Use	Do not change this register value. Changing the register value can affect IC functionality.
BK4_POR_FLT_OPT	0 – Default loading of the UV_FLTMSK/OV_FLTMSK/ILIM_FLTMSK of BUCK4 "0" 1 – Default loading of the UV_FLTMSK/OV_FLTMSK/ILIM_FLTMSK of BUCK4 "1"	
FCCM	Force Buck work in Continue Control Mode.	
RFU	Reserved for Future Use	Do not change this register value. Changing the register value can affect IC functionality.
RFU	Reserved for Future Use	Do not change this register value. Changing the register value can affect IC functionality.
EN_ULPM	0 – Disable Ultra-LPM 1 – Enable Ultra-LPM, the supply current is 11uA @ No load, no switching	
EN_LSILIM	0 – Disable Low-Side ILIM Protection 1 – Enable Low-Side ILIM Protection. Only allow new High-Side cycle if the inductor current less than LSILIM	
EN_ILIM_FB	0 – Disable ILIM Foldback Function 1 – Enable ILIM Foldback Function	

BUCK5 REGULATOR REGISTERS

B5_REG00 – Buck5 Configuration Register

Address = 0x00h	Default = 0x8Fh	Type = Basic Volatile

BIT	7	6	5	4	3	2	1	0
Name	POK	OV	ILIM	IWARN	UVFLTmsk	OVFLTmsk	ILIMFLTmsk	IWARNmsk
Default	1	0	0	0	1	1	1	1
Access	RO	RO	RO	RO	R/W	R/W	R/W	R/W

Name	Description	Notes
POK	POK status: 0 – Buck5 voltage is below the power good threshold 1 – Buck5 voltage is above the power good threshold	Provides real-time power good status
OV	OV status: 0 – Buck5 voltage is below the overvoltage threshold 1 – Buck5 voltage is above the overvoltage threshold	When output voltage > OV, this bit goes high. It is latched high until output voltage < OV and this bit is read.
ILIM	ILIM status: 0: Output ILIM is not triggered 1: Output ILIM is triggered	If the peak switch current reaches the ILIMSET threshold for 16 consecutive switching cycles, this bit goes high. It is latched high until peak switch current < ILIMSET and this bit is read.
IWARN	0: IWARN is not triggered 1: IIWARN is triggered	
UVFLTmsk	Mask VOUT UV interrupt: 0: Unmask Vout UV interrupt 1: Default mask Vout UV interrupt	When 1, the Buck5 POK signal is masked and does not go to the master controller. This prevents Buck5 from asserting the nIRQ pin when it is disabled or drops out of regulation. Buck5 POK still provides real-time power good status.
OVFLTmsk	Mask Vout OV interrupt: 0: Unmask Vout OV interrupt 1: Default mask Vout OV interrupt	When 1, the Buck5 OV signal is masked and does not go to the master controller. This prevents Buck5 from asserting the nIRQ pin when it is above regulation limits. Buck5 OV still provides OV status.
ILIMFLTmsk	Mask ILIM interrupt: 0: Unmask ILM interrupt 1: Default mask ILIM interrupt	When 1, the Buck5 ILIM signal is masked and does not go to the master controller. This prevents Buck5 from asserting the nIRQ pin when it is above regulation limits. Buck5 ILIM still provides current limit status.
IWARNmsk	0: Unmask IWARN interrupt, fault 1: Mask IWARN interrupt, fault	

B5_REG01 – Buck5 Configuration Register

Address = 0x01h	Default = 0x56h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	FREQ_SEL[1:0]		ENPD_LOAD	SST[2:0]			DRV_ADJ[1:0]	
Default	0	1	0	1	0	1	1	0
Access	R/W		R/W	R/W			R/W	

Name	Description	Notes
FREQ_SEL[1:0]	Select Frequency setting: 00 – 1.5MHz 01 – 2.0MHz 10 – 2.5MHz 11 – 3.3MHz	
ENPD_LOAD	0 – Disable Buck5 pulldown load current function 1 – Enable Buck5 pulldown load current function	
SST[2:0]	Soft start time setting: 000: 50us 001: 100us 010: 200us 011: 300us 100: 400us 101: 500us 110: 750us 111: 1000us	
DRV_ADJ[1:0]	Adjust Gate Driver (Rising and Falling SW): 00 – Slowest 11 – Fastest	

B5_REG02 – Buck5 Voltage Set0 Register

Address = 0x02h	Default = 0xADh	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	EN_LPM	VSET0[6:0]						
Default	1	0	1	0	1	1	0	1
Access	R/W	R/W						

Name	Description	Notes
EN_LPM	0 – Iqq = 250uA 1 – Iqq = 45uA	This bit is only effective when EN_ULPM[]=0
VSET0[6:0]	Buck5 output voltage setting VSET0: 0.5V to 1.135V in 5mV steps: VRANGE=0 VSET0: 0.5V to 3.675V in 25mV steps: VRANGE=1	

B5_REG03 – Buck5 Voltage Set1 Register

Address = 0x03h	Default = 0x2Dh	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	DIS_PD	VSET1[6:0]						
Default	0	0	1	0	1	1	0	1
Access	R/W	R/W						

Name	Description	Notes
DIS_PD	0 – Discharge VOUT when turn-off BUCK by 10Ohm 1 – Don't discharge VOUT when turn-off BUCK	Option to disable Pull-Down Resistor when BUCK is turned-off.
VSET1[6:0]	Buck5 output voltage setting VSET1: 0.5V to 1.135V in 5mV steps: VRANGE=0 VSET1: 0.5V to 3.675V in 25mV steps:VRANGE=1	

B5_REG04 – Buck5 Configuration Register

Address = 0x04h	Default = 0xD7h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	ON	PBINEN	QLTCH	SLEEP_EN	AUXIN_EN	DPSLEEP_EN	ILIM_SET	FCCM_DVS
Default	1	1	0	1	0	1	1	1
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Name	Description	Notes
ON	0 – Not enable Buck 1 – Enable Buck	This functionality is dependent on the overall IC configuration. Consult the factory for details.
PBINEN	0 – Not enable turn on by Push Button 1 – Enable turn on by Push Button	This functionality is dependent on the overall IC configuration. Consult the factory for details.
QLTCH	0 – Buck5 shuts down when its sequenced input shuts down 1 – Buck5 stays on when its sequenced input shuts down	
SLEEP_EN	0 – Buck5 stays on when the IC enters Sleep mode 1 – Buck5 turns off when the IC enters Sleep mode	
AUXIN_EN	0 – Not enable turn on by AUXIN 1 – Enable turn on by AUXIN	This functionality is dependent on the overall IC configuration. Consult the factory for details.
DPSLEEP_EN	0 – Buck5 stays on when the IC enters Deep Sleep mode 1 – Buck5 turns off when the IC enters Deep Sleep mode	
ILIM_SET	Setting for current limit: 0: LSILIM/HSILIM = 2A 1: LSILIM/HSILIM = 3A	
FCCM_DVS	Option to auto force to work in CCM mode when doing DVS 0: Disable auto force CCM 1: Enable auto force CCM	

B5_REG05 – Buck5 Configuration Register

Address = 0x05h	Default = 0xCAh	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	MODE	RST	RFU			RFU		
Default	1	1	0	0	1	0	1	0
Access	R/W	R/W	R/W			R/W		

Name	Description	Notes
MODE	Determines startup sequencing from the CMI code	This is a factory expert bit that should not be changed. Modifying this bit may result in unexpected IC behavior.
RST	0 – Buck5 does not affect nRESET output 1 – Buck5 affects nRESET output	
RFU	Reserved for Future Use	Do not change this register value. Changing the register value can affect IC functionality.
RFU	Reserved for Future Use	Do not change this register value. Changing the register value can affect IC functionality.

B5_REG06 – Buck5 Configuration Register

Address = 0x06h	Default = 0x00h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	RFU				IPDLOAD1:0]		RFU	
Default	0	0	0	0	0	0	0	0
Access	R/W				R/W		R/W	

Name	Description	Notes
RFU	Reserved for Future Use	Do not change this register value. Changing the register value can affect IC functionality.
IPDLOAD[1:0]	Setting the PD Load: 00: 10mA 01: 24mA 10: 37mA 11: 50mA	
RFU	Reserved for Future Use	Do not change this register value. Changing the register value can affect IC functionality.

B5_REG07 – Buck5 Configuration Register

Address = 0x07h	Default = 0xD4h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	DVS_SET[1:0]		ON_DLY[2:0]			OFF_DLY[2:0]		
Default	1	1	0	1	0	1	0	0
Access	R/W		R/W			R/W		

Name	Description	Notes
DVS_SET[1:0]	Setting DVS Slew Rate: VRANGE=0 "DVS_SET[00]: 11.26mV/us DVS_SET[01]: 5.63mV/us DVS_SET[10]: 2.82mV/us DVS_SET[11]: 1.41mV/us" VRANGE=1 "DVS_SET[00]: 56.31mV/us DVS_SET[01]: 28.15mV/us DVS_SET[10]: 14.08mV/us DVS_SET[11]: 7.04mV/us	
ON_DLY[2:0]	Follow Regulator Startup Delay Table in the Data Sheet	
OFF_DLY[2:0]	Follow Regulator Startup Delay Table in the Data Sheet	

B5_REG08 – Buck5 Configuration Register

Address = 0x08h	Default = 0x5Fh	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	VRANGE	BK5_POR_FLT_OPT	FCCM	RFU	RFU	EN_ULPM	EN_LSILIM	EN_ILIM_FB
Default	0	1	0	1	1	1	1	1
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Name	Description	Notes
VRANGE	Reserved for Future Use	Do not change this register value. Changing the register value can affect IC functionality.
BK5_POR_FLT_OPT	0 – Default loading of the UV_FLTMSK/OV_FLTMSK/ILIM_FLTMSK of BUCK5 "0" 1 – Default loading of the UV_FLTMSK/OV_FLTMSK/ILIM_FLTMSK of BUCK5 "1"	
FCCM	Force Buck work in Continue Control Mode.	
RFU	Reserved for Future Use	Do not change this register value. Changing the register value can affect IC functionality.
RFU	Reserved for Future Use	Do not change this register value. Changing the register value can affect IC functionality.
EN_ULPM	0 – Disable Ultra-LPM 1 – Enable Ultra-LPM, the supply current is 11uA @ No load, no switching	
EN_LSILIM	0 – Disable Low-Side ILIM Protection 1 – Enable Low-Side ILIM Protection. Only allow new High-Side cycle if the inductor current less than LSILIM	
EN_ILIM_FB	0 – Disable ILIM Foldback Function 1 – Enable ILIM Foldback Function	

B5_REG09 – Buck5 Voltage Set2 Register

Address = 0x16h	Default = 0x2Dh	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	RFU	VSET2[6:0]						
Default	0	0	1	0	1	1	0	1
Access	R/W	R/W						

Name	Description	Notes
RFU	Option to auto force to work in CCM mode when doing DVS 0: Disable auto force CCM 1: Enable auto force CCM	
VSET2[6:0]	Buck5 output voltage setting VSET0: 0.5V to 1.135V in 5mV steps: VRANGE=0 VSET0: 0.5V to 3.675V in 25mV steps: VRANGE=1	

B5_REG0A – Buck5 Voltage Set3 Register

Address = 0x17h	Default = 0x2Dh	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	RFU	VSET3[6:0]						
Default	0	0	1	0	1	1	0	1
Access	R/W	R/W						

Name	Description	Notes
RFU	Reserved for Future Use	Do not change this register value. Changing the register value can affect IC functionality.
VSET3[6:0]	Buck5 output voltage setting VSET0: 0.5V to 1.135V in 5mV steps: VRANGE=0 VSET0: 0.5V to 3.675V in 25mV steps: VRANGE=1	

BUCK-BOOST6 REGULATOR REGISTERS

BB6_REG00 – Buck-Boost6 Configuration Register

Address = 0xA0h	Default = 0x8Fh	Type = Basic Volatile

BIT	7	6	5	4	3	2	1	0
Name	POK	OV	ILIM	ILIM_WARN	UV_FLTMSK	OV_FLTMSK	ILIM_FLTMSK	IWARN_FLTMSK
Default	1	0	0	0	1	1	1	1
Access	RO	RO	RO	RO	R/W	R/W	R/W	R/W

Name	Description	Notes
POK	POK status: 0 – Buck-Boost6 voltage is below the power good threshold 1 – Buck-Boost6 voltage is above the power good threshold	Provides real-time power good status
OV	OV status: 0 – Buck-Boost6 voltage is below the overvoltage threshold 1 – Buck-Boost6 voltage is above the overvoltage threshold	When output voltage > OV, this bit goes high. It is latched high until output voltage < OV and this bit is read.
ILIM	ILIM status: 0: Output ILIM is not triggered 1: Output ILIM is triggered	If the peak switch current reaches the ILIMSET threshold for 16 consecutive switching cycles, this bit goes high. It is latched high until peak switch current < ILIMSET and this bit is read.
ILIM_WARN	ILIM Warning status. 1: Output ilim warning is trigered 0: Output ilim warning is not trigered	.
UV_FLTMSK	Mask VOUT UV interrupt: 0: Unmask Vout UV interrupt 1: Default mask Vout UV interrupt	When 1, the Buck-Boost6 POK signal is masked and does not go to the master controller. This prevents Buck-Boost6 from asserting the nIRQ pin when it is disabled or drops out of regulation. Buck-Boost6 POK still provides real-time power good status.
OV_FLTMSK	Mask Vout OV interrupt: 0: Unmask Vout OV interrupt 1: Default mask Vout OV interrupt	When 1, the Buck-Boost6 OV signal is masked and does not go to the master controller. This prevents Buck-Boost6 from asserting the nIRQ pin when it is above regulation limits. Buck-Boost6 OV still provides OV status.

ILIM_FLTMSK	Mask ILIM interrupt: 0: Unmask ILM interrupt 1: Default mask ILIM interrupt	pin when it is above regulation limits. Buck-Boost6 ILIM still provides current limit status.
IWARN_FLTMSK	Mask ILIM warning interrupt and fault: 1: Default mask ILIM warning interrupt, fault 0: Unmask ILM warning interrupt, fault	

BB6_REG01 – Buck-Boost6 Configuration Register

Address = 0xA1h	Default = 0x09h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	EXT_OFFDL_SEL	EXT_ONDL_SEL	TILE_ON_to_POK	DIS_PULLDOWN	EN_ILIMSD	DIS_ILIM2	DIS_OCP_SD	ALT_FRCBST2BK
Default	0	0	0	0	1	0	0	1
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Name	Description	Notes
EXT_OFFDL_SEL	Combine with 0xA7[2:0] to setting the turn-off delay	
EXT_ONDL_SEL	Combine with 0xA7[5:3] to setting the turn-on delay	
TILE_ON_to_POK	0: Use actual POK 1: Use TILE ON as POK	
DIS_PULLDOWN	0: Discharge VOUT when turn-off by 5Ohm 1: Don't discharge VOUT when turn-off	
EN_ILIMSD	0 – Disable regulator shut down by ILIM 1 – Enable regulator shut down by ILIM	
DIS_ILIM2	Disable HSILIM2 shutdown 1: Disable 0: Enable	
DIS_OCP_SD	Disable OCP (32 cycles continues got ILIM) shutdown 1: Disable 0: Enable	
ALT_FRCBST2BK	Force BUCK mode as trigger HSILIM in BOOST mode with VO < VIN 0: Disable 1: Enable (Hard force HSILIM2 1 cycle)	

BB6_REG02 – Buck-Boost6 Voltage Set0 Register

Address = 0xA2h	Default = 0x64h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	VSET[7:0]							
Default	0	1	1	0	0	1	0	0
Access	R/W							

Name	Description	Notes
VSET0[6:0]	VOUT = 0.8V + VSET [] * 0.025V Clamp Max 5.0V	

BB6_REG03 – Buck-Boost6 Voltage Set1 Register

Address = 0xA3h	Default = 0x0Fh	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	DRV_ADJ_VOUT[1:0]		DTH2L_VOUT	DTL2H_VOUT	DRV_ADJ_VIN[1:0]		DTH2L_VIN	DTL2H_VIN
Default	0	0	0	0	1	1	1	1
Access	R/W		R/W	R/W	R/W		R/W	R/W

Name	Description	Notes
DRV_ADJ_VOUT[1:0]	Driver Adjust for VOUT Side 00: Slowest 11: Strongest	
DTH2L_VOUT	Adjust deadtime from High-Side OFF to Low-Side ON at VOUT side 1: 0ns 0: 3ns	
DTL2H_VOUT	Adjust deadtime from Low-Side OFF to High-Side ON at VOUT side 1: 0ns 0: 3ns	
DRV_ADJ_VIN[1:0]	Driver Adjust for VIN Side 00: Slowest 11: Strongest	
DTH2L_VIN	"Driver Adjust for VIN Side 00: Slowest 11: Strongest"	
DTL2H_VIN	Adjust deadtime from Low-Side OFF to High-Side ON at VIN side 1: 0ns 0: 3ns	

BB6_REG04 – Buck-Boost6 Configuration Register

Address = 0xA4h	Default = 0x56h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	ON	PBINEN	QLTCH	SLEEP EN	AUXIN EN	DP SLEEP EN	PORFLT_OPT	FCCM
Default	0	1	0	1	0	1	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Name	Description	Notes
ON	0 – Not enable Buck 1 – Enable Buck	This functionality is dependent on the overall IC configuration. Consult the factory for details.
PBINEN	0 – Not enable turn on by Push Button 1 – Enable turn on by Push Button	This functionality is dependent on the overall IC configuration. Consult the factory for details.
QLTCH	0 – Buck-Boost6 shuts down when its sequenced input shuts down 1 – Buck-Boost6 stays on when its sequenced input shuts down	
SLEEP EN	0 – Buck-Boost6 stays on when the IC enters Sleep mode 1 – Buck-Boost6 turns off when the IC enters Sleep mode	
AUXIN EN	0 – Not enable turn on by AUXIN 1 – Enable turn on by AUXIN	This functionality is dependent on the overall IC configuration. Consult the factory for details.
DP SLEEP EN	0 – Buck-Boost6 stays on when the IC enters Deep Sleep mode 1 – Buck-Boost6 turns off when the IC enters Deep Sleep mode	
PORFLT_OPT	0 – Default loading of the UV_FLTMSK/OV_FLTMSK/ILIM_FLTMSK is "0" 1 – Default loading of the UV_FLTMSK/OV_FLTMSK/ILIM_FLTMSK is "1"	
FCCM	Force BB work in PWM mode.	

BB6_REG05 – Buck-Boost6 Configuration Register

Address = 0xA5h	Default = 0x80h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	MODE	RST	RFU			RFU		
Default	1	0	0	0	0	0	0	0
Access	R/W	R/W	R/W			R/W		

Name	Description	Notes
MODE	Determines startup sequencing from the CMI code	This is a factory expert bit that should not be changed. Modifying this bit may result in unexpected IC behavior.
RST	0 – Buck-Boost6 does not affect nRESET output 1 – Buck-Boost6 affects nRESET output	
RFU	Reserved for Future Use	Do not change this register value. Changing the register value can affect IC functionality.
RFU	Reserved for Future Use	Do not change this register value. Changing the register value can affect IC functionality.

BB6_REG06 – Buck-Boost6 Configuration Register

Address = 0xA6h	Default = 0x80h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	RFU				SST[1:0]		RFU	AO_CLK
Default	1	0	0	0	0	0	0	0
Access	R/W				R/W		R/W	R/W

Name	Description	Notes
RFU	Reserved for Future Use	Do not change this register value. Changing the register value can affect IC functionality.
SST[1:0]	Softstart time option 00: 500us 01: 1000us 10: 2000us 11: 3000us	
RFU	Reserved for Future Use	Do not change this register value. Changing the register value can affect IC functionality.
AO_CLK	1: Always call clock when BB is enabled 0: Just call clock when BB needed	

BB6_REG07 – Buck-Boost6 Configuration Register

Address = 0xA7h	Default = 0xA0h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	ILIM_SET[1:0]		ON DELAY[2:0]			OFF DELAY[2:0]		
Default	1	0	1	0	0	0	0	0
Access	R/W		R/W			R/W		

Name	Description	Notes
ILIM_SET[1:0]	Cycle-by-Cycle Current Limit Setting 00: 1.7A 01: 2.1A 10: 2.5A 11: 3.2A	
ON DELAY[2:0]	Follow Regulator Startup Delay Table in the Data Sheet	
OFF DELAY[2:0]	Follow Regulator Startup Delay Table in the Data Sheet	

BUCK-BOOST7 REGULATOR REGISTERS

BB7_REG00 – Buck-Boost7 Configuration Register

Address = 0xA0h	Default = 0x8Fh	Type = Basic Volatile

BIT	7	6	5	4	3	2	1	0
Name	POK	OV	ILIM	ILIM_WARN	UV_FLTMSK	OV_FLTMSK	ILIM_FLTMSK	IWARN_FLTMSK
Default	1	0	0	0	1	1	1	1
Access	RO	RO	RO	RO	R/W	R/W	R/W	R/W

Name	Description	Notes
POK	POK status: 0 – Buck-Boost7 voltage is below the power good threshold 1 – Buck-Boost7 voltage is above the power good threshold	Provides real-time power good status
OV	OV status: 0 – Buck-Boost7 voltage is below the overvoltage threshold 1 – Buck-Boost7 voltage is above the overvoltage threshold	When output voltage > OV, this bit goes high. It is latched high until output voltage < OV and this bit is read.
ILIM	ILIM status: 0: Output ILIM is not triggered 1: Output ILIM is triggered	If the peak switch current reaches the ILIMSET threshold for 16 consecutive switching cycles, this bit goes high. It is latched high until peak switch current < ILIMSET and this bit is read.
ILIM_WARN	ILIM Warning status. 1: Output ilim warning is trigered 0: Output ilim warning is not trigered	.
UV_FLTMSK	Mask VOUT UV interrupt: 0: Unmask Vout UV interrupt 1: Default mask Vout UV interrupt	When 1, the Buck-Boost7 POK signal is masked and does not go to the master controller. This prevents Buck-Boost7 from asserting the nIRQ pin when it is disabled or drops out of regulation. Buck-Boost7 POK still provides real-time power good status.
OV_FLTMSK	Mask Vout OV interrupt: 0: Unmask Vout OV interrupt 1: Default mask Vout OV interrupt	When 1, the Buck-Boost7 OV signal is masked and does not go to the master controller. This prevents Buck-Boost7 from asserting the nIRQ pin when it is above regulation limits. Buck-Boost7 OV still provides OV status.
ILIM_FLTMSK	Mask ILIM interrupt: 0: Unmask ILM interrupt 1: Default mask ILIM interrupt	pin when it is above regulation limits. Buck-Boost6 ILIM still provides current limit status.

IWARN_FLTMSK	Mask ILIM warning interrupt and fault: 1: Default mask ILIM warning interrupt, fault 0: Unmask ILM warning interrupt, fault	

BB7_REG01 – Buck-Boost7 Configuration Register

Address = 0xA1h	Default = 0x09h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	EXT_OFFDL_SEL	EXT_ONDL_SEL	TILE_ON_to_POK	DIS_PULLDOWN	EN_ILIMSD	DIS_ILIM2	DIS_OCP_SD	ALT_FRCBST2BK
Default	0	0	0	0	1	0	0	1
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Name	Description	Notes
EXT_OFFDL_SEL	Combine with 0xA7[2:0] to setting the turn-off delay	
EXT_ONDL_SEL	Combine with 0xA7[5:3] to setting the turn-on delay	
TILE_ON_to_POK	0: Use actual POK 1: Use TILE ON as POK	
DIS_PULLDOWN	0: Discharge VOUT when turn-off by 5Ohm 1: Don't discharge VOUT when turn-off	
EN_ILIMSD	0 – Disable regulator shut down by ILIM 1 – Enable regulator shut down by ILIM	
DIS_ILIM2	Disable HSILIM2 shutdown 1: Disable 0: Enable	
DIS_OCP_SD	Disable OCP (32 cycles continues got ILIM) shutdown 1: Disable 0: Enable	
ALT_FRCBST2BK	Force BUCK mode as trigger HSILIM in BOOST mode with VO < VIN 0: Disable 1: Enable (Hard force HSILIM2 1 cycle)	

BB7_REG02 – Buck-Boost7 Voltage Set0 Register

Address = 0xA2h	Default = 0x64h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	VSET[7:0]							
Default	0	1	1	0	0	1	0	0
Access	R/W							

Name	Description	Notes
VSET0[6:0]	VOUT = 0.8V + VSET [] * 0.025V Clamp Max 5.0V	

BB7_REG03 – Buck-Boost7 Voltage Set1 Register

Address = 0xA3h	Default = 0x0Fh	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	DRV_ADJ_VOUT[1:0]		DTH2L_VOUT	DTL2H_VOUT	DRV_ADJ_VIN[1:0]		DTH2L_VIN	DTL2H_VIN
Default	0	0	0	0	1	1	1	1
Access	R/W		R/W	R/W	R/W		R/W	R/W

Name	Description	Notes
DRV_ADJ_VOUT[1:0]	Driver Adjust for VOUT Side 00: Slowest 11: Strongest	
DTH2L_VOUT	Adjust deadtime from High-Side OFF to Low-Side ON at VOUT side 1: 0ns 0: 3ns	
DTL2H_VOUT	Adjust deadtime from Low-Side OFF to High-Side ON at VOUT side 1: 0ns 0: 3ns	
DRV_ADJ_VIN[1:0]	Driver Adjust for VIN Side 00: Slowest 11: Strongest	
DTH2L_VIN	"Driver Adjust for VIN Side 00: Slowest 11: Strongest"	
DTL2H_VIN	Adjust deadtime from Low-Side OFF to High-Side ON at VIN side 1: 0ns 0: 3ns	

BB7_REG04 – Buck-Boost7 Configuration Register

Address = 0xA4h	Default = 0xD6h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	ON	PBINEN	QLTCH	SLEEP EN	AUXIN EN	DP SLEEP EN	PORFLT_OPT	FCCM
Default	1	1	0	1	0	1	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Name	Description	Notes
ON	0 – Not enable Buck 1 – Enable Buck	This functionality is dependent on the overall IC configuration. Consult the factory for details.
PBINEN	0 – Not enable turn on by Push Button 1 – Enable turn on by Push Button	This functionality is dependent on the overall IC configuration. Consult the factory for details.
QLTCH	0 – Buck-Boost7 shuts down when its sequenced input shuts down 1 – Buck-Boost7 stays on when its sequenced input shuts down	
SLEEP EN	0 – Buck-Boost7 stays on when the IC enters Sleep mode 1 – Buck-Boost7 turns off when the IC enters Sleep mode	
AUXIN EN	0 – Not enable turn on by AUXIN 1 – Enable turn on by AUXIN	This functionality is dependent on the overall IC configuration. Consult the factory for details.
DPSLEEP EN	0 – Buck-Boost7 stays on when the IC enters Deep Sleep mode 1 – Buck-Boost7 turns off when the IC enters Deep Sleep mode	
PORFLT_OPT	0 – Default loading of the UV_FLTMSK/OV_FLTMSK/ILIM_FLTMSK is "0" 1 – Default loading of the UV_FLTMSK/OV_FLTMSK/ILIM_FLTMSK is "1"	
FCCM	Force BB work in PWM mode.	

BB7_REG05 – Buck-Boost7 Configuration Register

Address = 0xA5h	Default = 0xEEh	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	MODE	RST	RFU			RFU		
Default	1	1	1	0	1	1	1	0
Access	R/W	R/W	R/W			R/W		

Name	Description	Notes
MODE	Determines startup sequencing from the CMI code	This is a factory expert bit that should not be changed. Modifying this bit may result in unexpected IC behavior.
RST	0 – Buck-Boost7 does not affect nRESET output 1 – Buck-Boost7 affects nRESET output	
RFU	Reserved for Future Use	Do not change this register value. Changing the register value can affect IC functionality.
RFU	Reserved for Future Use	Do not change this register value. Changing the register value can affect IC functionality.

BB7_REG06 – Buck-Boost7 Configuration Register

Address = 0xA6h	Default = 0x00h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	RFU				SST[1:0]		RFU	AO_CLK
Default	0	0	0	0	0	0	0	0
Access	R/W				R/W		R/W	R/W

Name	Description	Notes
RFU	Reserved for Future Use	Do not change this register value. Changing the register value can affect IC functionality.
SST[1:0]	Softstart time option 00: 500us 01: 1000us 10: 2000us 11: 3000us	
RFU	Reserved for Future Use	Do not change this register value. Changing the register value can affect IC functionality.
AO_CLK	1: Always call clock when BB is enabled 0: Just call clock when BB needed	

BB7_REG07 – Buck-Boost7 Configuration Register

Address = 0xA7h	Default = 0x80h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	ILIM_SET[1:0]		ON DELAY[2:0]			OFF DELAY[2:0]		
Default	1	0	1	0	0	0	0	0
Access	R/W		R/W			R/W		

Name	Description	Notes
ILIM_SET[1:0]	Cycle-by-Cycle Current Limit Setting 00: 1.7A 01: 2.1A 10: 2.5A 11: 3.2A	
ON DELAY[2:0]	Follow Regulator Startup Delay Table in the Data Sheet	
OFF DELAY[2:0]	Follow Regulator Startup Delay Table in the Data Sheet	

BOOST8 REGULATOR REGISTERS

BST8_REG00 – Boost8 Configuration Register

Address = 0x80h	Default = 0x0Fh	Type = Basic Volatile

BIT	7	6	5	4	3	2	1	0
Name	POK	OV	ILIM	RFU	UV_FLTMSK	OV_MSK	ILIM_MSK	IWARN_MSK
Default	0	0	0	0	1	1	1	1
Access	RO	RO	RO	RO	R/W	R/W	R/W	R/W

Name	Description	Notes
POK	POK status: 0 – Boost8 voltage is below the power good threshold 1 – Boost8 voltage is above the power good threshold	Provides real-time power good status
OV	OV status: 0 – Boost8 voltage is below the overvoltage threshold 1 – Boost8 voltage is above the overvoltage threshold	When output voltage > OV, this bit goes high. It is latched high until output voltage < OV and this bit is read.
ILIM	ILIM status: 0: Output ILIM is not triggered 1: Output ILIM is triggered	If the peak switch current reaches the ILIMSET threshold for 16 consecutive switching cycles, this bit goes high. It is latched high until peak switch current < ILIMSET and this bit is read.
RFU	Reserved for Future Use	Do not change this register value. Changing the register value can affect IC functionality.
UV_FLTMSK	Mask VOUT UV interrupt: 0: Unmask Vout UV interrupt 1: Default mask Vout UV interrupt	When 1, the Boost8 POK signal is masked and does not go to the master controller. This prevents Boost8 from asserting the nIRQ pin when it is disabled or drops out of regulation. Boost8 POK still provides real-time power good status.
OV_MSK	Mask Vout OV interrupt: 0: Unmask Vout OV interrupt 1: Default mask Vout OV interrupt	When 1, the Boost8 OV signal is masked and does not go to the master controller. This prevents Boost8 from asserting the nIRQ pin when it is above regulation limits. Boost8 OV still provides OV status.
ILIM_MSK	Mask ILIM interrupt: 0: Unmask ILM interrupt 1: Default mask ILIM interrupt	When 1, the Boost8 ILIM signal is masked and does not go to the master controller. This prevents Boost8 from asserting the nIRQ pin when it is above regulation limits. Boost8 ILIM still provides current limit status.
IWARN_MSK	Mask ILIM warning interrupt and fault: 1: Default mask ILIM warning interrupt, fault 0: Unmask ILM warning interrupt, fault	

BST8_REG01 – Boost8 Configuration Register

Address = 0x81h	Default = 0x20h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	RFU	BST_FLT_MSK	BST_POR_FLT_OPT	RFU	FRE_SEL	HS_DRV_ADJ	LS_DRV_ADJ[1:0]	
Default	0	0	1	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	

Name	Description	Notes
RFU	Reserved for Future Use	Do not change this register value. Changing the register value can affect IC functionality.
BST_FLT_MSK	1: Mask the fault ILIM2/ SSDONE/ SHORT FAULT to shut down the converter. 0: No mask	
BST_POR_FLT_OPT	0 – Default loading of the UV_FLTMSK/OV_FLTMSK/ILIM_FLTMSK is "0" 1 – Default loading of the UV_FLTMSK/OV_FLTMSK/ILIM_FLTMSK is "1"	
RFU	Reserved for Future Use	Do not change this register value. Changing the register value can affect IC functionality.
FRE_SEL	Frequency setting : 1: 1.125M 0: 550K	
HS_DRV_ADJ	Adjust High-Side ON/OFF speed 0: Slowest 1: Fastest	
LS_DRV_ADJ[1:0]	Adjust Gate Driver (Rising and Falling SW): 00 – Slowest 11 – Fastest	

BST8_REG02 – Boost8 Voltage Set0 Register

Address = 0x82h	Default = 0xA8h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	EN_ILIM_SD	VSET[6:0]						
Default	1	0	1	0	1	0	0	0
Access	R/W	R/W						

Name	Description	Notes
EN_ILIM_SD	1: Enable Ilim2 shutdown. 0: Disable.	
VSET[6:0]	5V to 20V in 200mV steps: VOUT = 5 + 0.2*DEC[]	

BST8_REG03 – Boost8 Voltage Set1 Register

Address = 0x83h	Default = 0xB2h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	CC_ADJ	DEC_MINON	ISET[5:0]					
Default	1	0	1	1	0	0	1	0
Access	R/W	R/W	R/W					

Name	Description	Notes
CC_ADJ	Adjust Rcomp for CC loop 0: AND with force IPK function, Rcomp is high - 4LED 1: Rcomp is low for 2LED	
DEC_MINON	0: MinOn = 110ns 1: MinOn = 50ns	
ISET[5:0]	Output current setting from 0 to 30mA in 0.5mA step: IOUT = 0.5*DEC[]	

BST8_REG04 – Boost8 Configuration Register

Address = 0x84h	Default = 0x54h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	ON	PBINEN	QLTCH	SLEEP_EN	AUXIN_EN	DPSLP_EN	ILIM_SET[1:0]	
Default	0	1	0	1	0	1	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	

Name	Description	Notes
ON	0 – Not enable Buck 1 – Enable Buck	This functionality is dependent on the overall IC configuration. Consult the factory for details.
PBINEN	0 – Not enable turn on by Push Button 1 – Enable turn on by Push Button	This functionality is dependent on the overall IC configuration. Consult the factory for details.
QLTCH	0 – Boost8 shuts down when its sequenced input shuts down 1 – Boost8 stays on when its sequenced input shuts down	
SLEEP_EN	0 – Boost8 stays on when the IC enters Sleep mode 1 – Boost8 turns off when the IC enters Sleep mode	
AUXIN_EN	0 – Not enable turn on by AUXIN 1 – Enable turn on by AUXIN	This functionality is dependent on the overall IC configuration. Consult the factory for details.
DPSLP_EN	0 – Boost8 stays on when the IC enters Deep Sleep mode 1 – Boost8 turns off when the IC enters Deep Sleep mode	
ILIM_SET[1:0]	Setting for current limit: 00: 1A 01: 1.25A 10: 1.5A 11: 2A	

BST8_REG05 – Boost8 Configuration Register

Address = 0x85h	Default = 0x80h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	MODE	RST	RFU			RFU		
Default	1	0	0	0	0	0	0	0
Access	R/W	R/W	R/W			R/W		

Name	Description	Notes
MODE	Determines startup sequencing from the CMI code	This is a factory expert bit that should not be changed. Modifying this bit may result in unexpected IC behavior.
RST	0 – Boost8 does not affect nRESET output 1 – Boost8 affects nRESET output	
RFU	Reserved for Future Use	Do not change this register value. Changing the register value can affect IC functionality.
RFU	Reserved for Future Use	Do not change this register value. Changing the register value can affect IC functionality.

BST8_REG06 – Boost8 Configuration Register

Address = 0x86h	Default = 0x00h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	RFU				OFS_SET_IPK[1:0]		SLP_SET_IPK	INC_OC
Default	0	0	0	0	0	0	0	0
Access	R/W				R/W		R/W	R/W

Name	Description	Notes
RFU	Reserved for Future Use	Do not change this register value. Changing the register value can affect IC functionality.
OFS_SET_IPK[1:0]	Adjust the Offset for IPEAK	
SLP_SET_IPK	Adjust the VIN/R ratio for IPEAK	
INC_OC	Increase the OC threshold more 50% for low ISET option.	

BST8_REG07 – Boost8 Configuration Register

Address = 0x87h	Default = 0x98h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	RFU	RFU	ON_DLY[2:0]			OFF_DLY[2:0]		
Default	1	0	0	1	1	0	0	0
Access	R/W	R/W	R/W			R/W		

Name	Description	Notes
RFU	Reserved for Future Use	Do not change this register value. Changing the register value can affect IC functionality.
ON_DLY[2:0]	Follow Regulator Startup Delay Table in the Data Sheet	
OFF_DLY[2:0]	Follow Regulator Startup Delay Table in the Data Sheet	

BOOST9 REGULATOR REGISTERS

BST9_REG00 – Boost9 Configuration Register

Address = 0x80h	Default = 0x0Fh	Type = Basic Volatile

BIT	7	6	5	4	3	2	1	0
Name	POK	OV	ILIM	RFU	UV_FLTMSK	OV_MSK	ILIM_MSK	IWARN_MSK
Default	0	0	0	0	1	1	1	1
Access	RO	RO	RO	RO	R/W	R/W	R/W	R/W

Name	Description	Notes
POK	POK status: 0 – Boost9 voltage is below the power good threshold 1 – Boost9 voltage is above the power good threshold	Provides real-time power good status
OV	OV status: 0 – Boost9 voltage is below the overvoltage threshold 1 – Boost9 voltage is above the overvoltage threshold	When output voltage > OV, this bit goes high. It is latched high until output voltage < OV and this bit is read.
ILIM	ILIM status: 0: Output ILIM is not triggered 1: Output ILIM is triggered	If the peak switch current reaches the ILIMSET threshold for 16 consecutive switching cycles, this bit goes high. It is latched high until peak switch current < ILIMSET and this bit is read.
RFU	Reserved for Future Use	Do not change this register value. Changing the register value can affect IC functionality.
UV_FLTMSK	Mask VOUT UV interrupt: 0: Unmask Vout UV interrupt 1: Default mask Vout UV interrupt	When 1, the Boost9 POK signal is masked and does not go to the master controller. This prevents Boost9 from asserting the nIRQ pin when it is disabled or drops out of regulation. Boost9 POK still provides real-time power good status.
OV_MSK	Mask Vout OV interrupt: 0: Unmask Vout OV interrupt 1: Default mask Vout OV interrupt	When 1, the Boost9 OV signal is masked and does not go to the master controller. This prevents Boost9 from asserting the nIRQ pin when it is above regulation limits. Boost9 OV still provides OV status.
ILIM_MSK	Mask ILIM interrupt: 0: Unmask ILM interrupt 1: Default mask ILIM interrupt	When 1, the Boost9 ILIM signal is masked and does not go to the master controller. This prevents Boost9 from asserting the nIRQ pin when it is above regulation limits. Boost9 ILIM still provides current limit status.

IWARN_MSK	Mask ILIM warning interrupt and fault: 1: Default mask ILIM warning interrupt, fault 0: Unmask ILM warning interrupt, fault	

BST9_REG01 – Boost9 Configuration Register

Address = 0x81h	Default = 0x20h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	RFU	BST_FLT_MSK	BST_POR_FLT_OPT	RFU	FRE_SEL	HS_DRV_ADJ	LS_DRV_ADJ[1:0]	
Default	0	0	1	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	

Name	Description	Notes
RFU	Reserved for Future Use	Do not change this register value. Changing the register value can affect IC functionality.
BST_FLTMSK	1: Mask the fault ILIM2/ SSDONE/ SHORT FAULT to shut down the converter. 0: No mask	
POR_FLT_OPT	0 – Default loading of the UV_FLTMSK/OV_FLTMSK/ILIM_FLTMSK is "0" 1 – Default loading of the UV_FLTMSK/OV_FLTMSK/ILIM_FLTMSK is "1"	
RFU	Reserved for Future Use	Do not change this register value. Changing the register value can affect IC functionality.
FRE_SEL	Frequency setting : 1: 1.125M 0: 550K	
HS_DRV_ADJ	Adjust High-Side ON/OFF speed 0: Slowest 1: Fastest	
LS_DRV_ADJ[1:0]	Adjust Gate Driver (Rising and Falling SW): 00 – Slowest 11 – Fastest	

BST9_REG02 – Boost9 Voltage Set0 Register

Address = 0x82h	Default = 0xC1h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	EN_ILIM_SD	VSET[6:0]						
Default	1	1	0	0	0	0	0	1
Access	R/W	R/W						

Name	Description	Notes
EN_ILIM_SD	1: Enable Ilim2 shutdown. 0: Disable.	
VSET[6:0]	5V to 20V in 200mV steps: VOUT = 5 + 0.2*DEC[]	

BST9_REG03 – Boost9 Voltage Set1 Register

Address = 0x83h	Default = 0xB2h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	CC_ADJ	DEC_MINON	ISET[5:0]					
Default	1	0	1	1	0	0	1	0
Access	R/W	R/W	R/W					

Name	Description	Notes
CC_ADJ	Adjust Rcomp for CC loop 0: AND with force IPK function, Rcomp is high - 4LED 1: Rcomp is low for 2LED	
DEC_MINON	0: MinOn = 110ns 1: MinOn = 50ns	
ISET[5:0]	Output current setting from 0 to 30mA in 0.5mA step: IOUT = 0.5*DEC[]	

BST9_REG04 – Boost9 Configuration Register

Address = 0x84h	Default = 0x54h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	ON	PBINEN	QLTCH	SLEEP_EN	AUXIN_EN	DPSLP_EN	ILIM_SET[1:0]	
Default	0	1	0	1	0	1	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	

Name	Description	Notes
ON	0 – Not enable Buck 1 – Enable Buck	This functionality is dependent on the overall IC configuration. Consult the factory for details.
PBINEN	0 – Not enable turn on by Push Button 1 – Enable turn on by Push Button	This functionality is dependent on the overall IC configuration. Consult the factory for details.
QLTCH	0 – Boost9 shuts down when its sequenced input shuts down 1 – Boost9 stays on when its sequenced input shuts down	
SLEEP_EN	0 – Boost9 stays on when the IC enters Sleep mode 1 – Boost9 turns off when the IC enters Sleep mode	
AUXIN_EN	0 – Not enable turn on by AUXIN 1 – Enable turn on by AUXIN	This functionality is dependent on the overall IC configuration. Consult the factory for details.
DPSLP_EN	0 – Boost9 stays on when the IC enters Deep Sleep mode 1 – Boost9 turns off when the IC enters Deep Sleep mode	
ILIM_SET[1:0]	Setting for current limit: 00: 1A 01: 1.25A 10: 1.5A 11: 2A	

BST9_REG05 – Boost9 Configuration Register

Address = 0x85h	Default = 0x80h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	MODE	RST	RFU			RFU		
Default	1	0	0	0	0	0	0	0
Access	R/W	R/W	R/W			R/W		

Name	Description	Notes
MODE	Determines startup sequencing from the CMI code	This is a factory expert bit that should not be changed. Modifying this bit may result in unexpected IC behavior.
RST	0 – Boost9 does not affect nRESET output 1 – Boost9 affects nRESET output	
RFU	Reserved for Future Use	Do not change this register value. Changing the register value can affect IC functionality.
RFU	Reserved for Future Use	Do not change this register value. Changing the register value can affect IC functionality.

BST9_REG06 – Boost9 Configuration Register

Address = 0x86h	Default = 0x00h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	RFU				OFS_SET_IPK[1:0]		SLP_SET_IPK	INC_OC
Default	0	0	0	0	0	0	0	0
Access	R/W				R/W		R/W	R/W

Name	Description	Notes
RFU	Reserved for Future Use	Do not change this register value. Changing the register value can affect IC functionality.
OFS_SET_IPK[1:0]	Adjust the Offset for IPEAK	
SLP_SET_IPK	Adjust the VIN/R ratio for IPEAK	
INC_OC	Increase the OC threshold more 50% for low ISET option.	

BST9_REG07 – Boost9 Configuration Register

Address = 0x87h	Default = 0x98h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	RFU	RFU	ON_DLY[2:0]			OFF_DLY[2:0]		
Default	1	0	0	1	1	0	0	0
Access	R/W	R/W	R/W			R/W		

Name	Description	Notes
RFU	Reserved for Future Use	Do not change this register value. Changing the register value can affect IC functionality.
ON_DLY[2:0]	Follow Regulator Startup Delay Table in the Data Sheet	
OFF_DLY[2:0]	Follow Regulator Startup Delay Table in the Data Sheet	

LDO1, LDO2 REGISTERS

LDO12_REG00 – LDO1 Configuration Register

Address = 0xE0h	Default = 0x8Eh	Type = Basic Volatile

BIT	7	6	5	4	3	2	1	0
Name	PWR_GOOD_LDO1	OV_LDO1	ILIM_LDO1	RFU	UV_FLTMSK_LDO1	OV_FLTMSK_LDO1	ILIM_FLTMSK_LDO1	RFU
Default	1	0	0	0	1	1	1	0
Access	RO	RO	RO	RO	R/W	R/W	R/W	RO

Name	Description	Notes
PWR_GOOD_LDO1	POK status: 0 – LDO1 voltage is below the power good threshold 1 – LDO1 voltage is above the power good threshold	Provides real-time power good status
OV_LDO1	OV status: 0 – LDO1 voltage is below the overvoltage threshold 1 – LDO1voltage is above the overvoltage threshold	When output voltage > OV, this bit goes high. It is lached high until output voltage < OV and this bit is read.
ILIM_LDO1	ILIM status: 0: Output ILIM is not triggered 1: Output ILIM is triggered	When output current reached ILIM setting, this bit goes high. It is latched high until output current < ILIM and this bit is read.
RFU	Reserved for Future Use	Do not change this register value. Changing the register value can affect IC functionality.
UV_FLTMSK_LDO1	Mask LDO1 VOUT UV interrupt: 0: Unmask Vout UV interrupt 1: Default mask Vout UV interrupt	When 1, the LDO1 PG signal is masked and does not go to the master controller. This prevents LDO1 from asserting the nIRQ pin when it is disabled or drops out of regulation. LDO1 PG still provides real-time status.
OV_FLTMSK_LDO1	Mask LDO1 Vout OV interrupt: 0: Unmask Vout OV interrupt 1: Default mask Vout OV interrupt	When 1, the OV_LDO1 signal is masked and does not go to the master controller. This prevents LDO1 from asserting the nIRQ pin when it is above regulation limits. OV_LDO1 still provides overvoltage status.

ILIM_FLTMSK_LDO1	Mask ILIM interrupt: 0 - Unmasks the LDO1 ILIM interrupt 1 - Masks the LDO1 ILIM interrupt	When 1, the LDO1 ILIM signal is masked and does not go to the master controller. This prevents LDO1 from asserting the nIRQ pin when it is above regulation limits. ILIM still provides current limit status.
RFU	Reserved for Future Use	Do not change this register value. Changing the register value can affect IC functionality.

LDO12_REG01 – LDO1 Voltage Set Register

Address = 0xE1h	Default = 0x4Eh	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	RFU	RANGE_LDO1	LDO1 VSET[5:0]					
Default	0	1	0	0	1	1	1	0
Access	R/W	R/W	R/W					

Name	Description	Notes
RFU	Reserved for Future Use	Do not change this register value. Changing the register value can affect IC functionality.
RANGE_LDO1	1: Vout from 1.2 to 3.6 0: Vout from 0.5 to 1.2875	
LDO1 VSET[5:0]	LDO1 output voltage setting. With RANGE_LDO1=1: 1.2V to 3.6V in 50mV steps With RANGE_LDO1=0: 0.5V to 1.2875V in 12.5mV steps	

LDO12_REG02 – LDO1 Configuration Register

Address = 0xE2h	Default = 0xCEh	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	ON LDO1	PBIN EN LDO1	AUXIN EN LDO1	SLEEP EN LDO1	DPSLEEP EN LDO1	RFU	RFU	RFU
Default	1	1	0	0	1	1	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Name	Description	Notes
ON_ LDO1	0 – Not enable LDO1 1 – Enable LDO1	This functionality is dependent on the overall IC configuration. Consult the factory for details.
PBIN EN LDO1	0 - Not enable turn on by Push Button 1 – Enable turn on by Push Button	This functionality is dependent on the overall IC configuration. Consult the factory for details..
AUXIN EN LDO1	Enable turn on by gb_auxin 1: Enable 0: Disable	
SLEEP EN LDO1	Enable LDO1 SLEEP mode: 0 – LDO1 stays on when the IC enters Sleep mode 1 – LDO1 turns off when the IC enters Sleep mode	
DPSLEEP EN LDO1	Enable LDO1 Deep SLEEP mode: 0 – LDO1 stays on when the IC enters Deep Sleep mode 1 – LDO1 turns off when the IC enters Deep Sleep mode	
RFU	Reserved for Future Use	Do not change this register value. Changing the register value can affect IC functionality.

LDO12_REG03 – LDO1 Configuration Register

Address = 0xE3h	Default = 0x22h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	ON DELAY LDO1[2:0]			OFF DELAY LDO1[2:0]			MODE LDO1	RST LDO1
Default	0	0	1	0	0	0	1	0
Access	R/W			R/W			R/W	R/W

Name	Description	Notes
ON DELAY LDO1[2:0]	Follow Regulator Startup Delay Table in the Data Sheet	
OFF DELAY LDO1[2:0]	Follow Regulator Startup Delay Table in the Data Sheet	
MODE LDO1	Determines startup sequencing from the CMI code	This is a factory expert bit that should not be changed. Modifying this bit may result in unexpected IC behavior.
RST LDO1	0 – LDO1 does not affect nRESET output 1 – LDO1 affects nRESET output	

LDO12_REG04 – LDO1 Configuration Register

Address = 0xE4h	Default = 0x07h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	RFU				RFU			
Default	0	0	0	0	0	1	1	1
Access	R/W				R/W			

Name	Description	Notes
RFU	Reserved for Future Use	Do not change this register value. Changing the register value can affect IC functionality.
RFU	Reserved for Future Use	Do not change this register value. Changing the register value can affect IC functionality.

LDO12_REG05 – LDO1 Configuration Register

Address = 0xE5h	Default = 0XE1h	Type n/a = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	ILIM_SD_DIS_LDO1	POR_MSK_L2	POR_MSK_L1	DIS_CHARGE_OPT_LDO1	DIS_PD_LDO2	DIS_PD_LDO1	SST_LDO1	QLTCH_LDO1
Default	1	1	1	0	0	0	0	1
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Name	Description	Notes
ILIM_SD_DIS_LDO1	Disable the shutdown by current limit of LDO1	
POR_MSK_L2		
POR_MSK_L1		
DIS_CHARGE_OPT_LDO1	Option disable charge Resistor when LDO is turned-off 0: Discharge VOUT when turn-off,Rdis=9.4 Ohm 1: discharge VOUT when turn-off.Rdis=18.8 Ohm	
DIS_PD_LDO2	Option disable pulldown Resistor when LDO2 is turned-off 1: disable pulldown function	
DIS_PD_LDO1	Option disable pulldown Resistor when LDO1 is turned-off 1: disable pulldown function	
SST_ LDO1	Soft start time: 0: 160us 1: 320us.	
QLTCH_ LDO1	Enable for latch of qualify: + 1: The qualify is latched. + 0: The qualify is not latched.	

LDO12_REG06 – LDO2 Configuration Register

Address = 0xE6h	Default = 0x0Eh	Type = Basic Volatile

BIT	7	6	5	4	3	2	1	0
Name	PWR_GOOD_LDO2	OV_LDO2	ILIM_LDO2	RFU	UV_FLTMSK_LDO2	OV_FLTMSK_LDO2	ILIM_FLTMSK_LDO2	RFU
Default	0	0	0	0	1	1	1	0
Access	RO	RO	RO	RO	R/W	R/W	R/W	RO

Name	Description	Notes
PWR_GOOD_LDO2	POK status: 0 – LDO2 voltage is below the power good threshold 1 – LDO2 voltage is above the power good threshold	Provides real-time power good status
OV_LDO2	OV status: 0 – LDO2 voltage is below the overvoltage threshold 1 – LDO2voltage is above the overvoltage threshold	When output voltage > OV, this bit goes high. It is lached high until output voltage < OV and this bit is read.
ILIM_LDO2	ILIM status: 0: Output ILIM is not triggered 1: Output ILIM is triggered	When output current reached ILIM setting, this bit goes high. It is latched high until output current < ILIM and this bit is read.
RFU	Reserved for Future Use	Do not change this register value. Changing the register value can affect IC functionality.
UV_FLTMSK_LDO2	Mask LDO2 VOUT UV interrupt: 0: Unmask Vout UV interrupt 1: Default mask Vout UV interrupt	When 1, the LDO2 PG signal is masked and does not go to the master controller. This prevents LDO2 from asserting the nIRQ pin when it is disabled or drops out of regulation. LDO2 PG still provides real-time status.
OV_FLTMSK_LDO2	Mask LDO2 Vout OV interrupt: 0: Unmask Vout OV interrupt 1: Default mask Vout OV interrupt	When 1, the OV_LDO2 signal is masked and does not go to the master controller. This prevents LDO2 from asserting the nIRQ pin when it is above regulation limits. OV_LDO2 still provides overvoltage status.
ILIM_FLTMSK_LDO2	Mask ILIM interrupt: 0 - Unmasks the LDO2 ILIM interrupt 1 - Masks the LDO2 ILIM interrupt	When 1, the LDO2 ILIM signal is masked and does not go to the master controller. This prevents LDO2 from asserting the nIRQ pin when it is above regulation limits. ILIM still provides current limit status.

RFU	Reserved for Future Use	Do not change this register value. Changing the register value can affect IC functionality.

LDO12_REG07 – LDO2 Voltage Set Register

Address = 0xE7h	Default = 0x4Ch	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	RFU	RANGE_LDO2	LDO2 VSET[5:0]					
Default	0	1	0	0	1	1	0	0
Access	R/W	R/W	R/W					

Name	Description	Notes
RFU	Reserved for Future Use	Do not change this register value. Changing the register value can affect IC functionality.
RANGE_LDO2	1: Vout from 1.2 to 3.6 0: Vout from 0.5 to 1.2875	
LDO2 VSET[5:0]	LDO2 output voltage setting. With RANGE_LDO2=1: 1.2V to 3.6V in 50mV steps With RANGE_LDO2=0: 0.5V to 1.2875V in 12.5mV steps	

LDO12_REG08 – LDO2 Configuration Register

Address = 0xE8h	Default = 0x58h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	ON LDO2	PBIN EN LDO2	AUXIN EN LDO2	SLEEP EN LDO2	DPSLEEP EN LDO2	RFU	RFU	RFU
Default	0	1	0	1	1	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Name	Description	Notes
ON_ LDO2	0 – Not enable LDO2 1 – Enable LDO2	This functionality is dependent on the overall IC configuration. Consult the factory for details.
PBIN_EN_ LDO2	0 - Not enable turn on by Push Button 1 – Enable turn on by Push Button	This functionality is dependent on the overall IC configuration. Consult the factory for details..
AUXIN_EN_LDO2	Enable turn on by gb_auxin 1: Enable 0: Disable	
SLP_EN_LDO2	Enable LDO2 SLEEP mode: 0 – LDO2 stays on when the IC enters Sleep mode 1 – LDO2 turns off when the IC enters Sleep mode	
DPSLP_EN_LDO2	Enable LDO2 Deep SLEEP mode: 0 – LDO2 stays on when the IC enters Deep Sleep mode 1 – LDO2 turns off when the IC enters Deep Sleep mode	
RFU	Reserved for Future Use	Do not change this register value. Changing the register value can affect IC functionality.

LDO12_REG09 – LDO2 Configuration Register

Address = 0xE9h	Default = 0x02h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	ON DELAY LDO2[2:0]			OFF DELAY LDO2[2:0]			MODE LDO2	RST LDO2
Default	0	0	0	0	0	0	1	0
Access	R/W			R/W			R/W	R/W

Name	Description	Notes
ON DELAY LDO2[2:0]	Follow Regulator Startup Delay Table in the Data Sheet	
OFF DELAY LDO2[2:0]	Follow Regulator Startup Delay Table in the Data Sheet	
MODE LDO2	Determines startup sequencing from the CMI code	This is a factory expert bit that should not be changed. Modifying this bit may result in unexpected IC behavior.
RST LDO2	0 – LDO2 does not affect nRESET output 1 – LDO2 affects nRESET output	

LDO12_REG0A – LDO2 Configuration Register

Address = 0xEAh	Default = 0x00h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	RFU				RFU			
Default	0	0	0	0	0	0	0	0
Access	R/W				R/W			

Name	Description	Notes
RFU	Reserved for Future Use	Do not change this register value. Changing the register value can affect IC functionality.
RFU	Reserved for Future Use	Do not change this register value. Changing the register value can affect IC functionality.

LDO3, LDO6 REGISTERS

LDO36_REG00 – LDO6 Configuration Register

Address = 0x20h	Default = 0x0Eh	Type = Basic Volatile

BIT	7	6	5	4	3	2	1	0
Name	PWR_GOOD_LDO6	OV_LDO6	ILIM_LDO6	RFU	UV_FLTMSK_LDO6	OV_FLTMSK_LDO6	ILIM_FLTMSK_LDO6	RFU
Default	0	0	0	0	1	1	1	0
Access	RO	RO	RO	RO	R/W	R/W	R/W	RO

Name	Description	Notes
PWR_GOOD_LDO6	POK status: 0 – LDO6 voltage is below the power good threshold 1 – LDO6 voltage is above the power good threshold	Provides real-time power good status
OV_LDO6	OV status: 0 – LDO6 voltage is below the overvoltage threshold 1 – LDO6voltage is above the overvoltage threshold	When output voltage > OV, this bit goes high. It is lached high until output voltage < OV and this bit is read.
ILIM_LDO6	ILIM status: 0: Output ILIM is not triggered 1: Output ILIM is triggered	When output current reached ILIM setting, this bit goes high. It is latched high until output current < ILIM and this bit is read.
RFU	Reserved for Future Use	Do not change this register value. Changing the register value can affect IC functionality.
UV_FLTMSK_LDO6	Mask LDO6 VOUT UV interrupt: 0: Unmask Vout UV interrupt 1: Default mask Vout UV interrupt	When 1, the LDO6 PG signal is masked and does not go to the master controller. This prevents LDO6 from asserting the nIRQ pin when it is disabled or drops out of regulation. LDO6 PG still provides real-time status.
OV_FLTMSK_LDO6	Mask LDO6 Vout OV interrupt: 0: Unmask Vout OV interrupt 1: Default mask Vout OV interrupt	When 1, the OV_LDO6 signal is masked and does not go to the master controller. This prevents LDO6 from asserting the nIRQ pin when it is above regulation limits. OV_LDO6 still provides overvoltage status.

ILIM_FLTMSK_LDO6	Mask ILIM interrupt: 0 - Unmasks the LDO6 ILIM interrupt 1 - Masks the LDO6 ILIM interrupt	When 1, the LDO6 ILIM signal is masked and does not go to the master controller. This prevents LDO6 from asserting the nIRQ pin when it is above regulation limits. ILIM still provides current limit status.
RFU	Reserved for Future Use	Do not change this register value. Changing the register value can affect IC functionality.

LDO36_REG01 – LDO6 Voltage Set Register

Address = 0x21h	Default = 0x7Fh	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	RANGE_LDO6	POR_MSK_L6	LDO6 VSET[5:0]					
Default	0	1	1	1	1	1	1	1
Access	R/W	R/W	R/W					

Name	Description	Notes
RANGE_LDO6	1: Vout from 1.2 to 3.6 0: Vout from 0.5 to 1.2875	
POR_MSK_L6		
LDO6_VSET[5:0]	LDO6 output voltage setting. With RANGE_LDO6=1: 1.2V to 3.6V in 50mV steps With RANGE_LDO6=0: 0.5V to 1.2875V in 12.5mV steps	

LDO36_REG02 – LDO6 Configuration Register

Address = 0x22h	Default = 0x58h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	ON LDO6	PBIN EN LDO6	AUXIN EN LDO6	SLEEP EN LDO6	DPSLEEP EN LDO6	RFU	RFU	RFU
Default	0	1	0	1	1	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Name	Description	Notes
ON LDO6	0 – Not enable LDO6 1 – Enable LDO6	This functionality is dependent on the overall IC configuration. Consult the factory for details.
PBIN EN LDO6	0 - Not enable turn on by Push Button 1 – Enable turn on by Push Button	This functionality is dependent on the overall IC configuration. Consult the factory for details..
AUXIN EN LDO6	Enable turn on by gb_auxin 1: Enable 0: Disable	
SLEEP EN LDO6	Enable LDO6 SLEEP mode: 0 – LDO6 stays on when the IC enters Sleep mode 1 – LDO6 turns off when the IC enters Sleep mode	
DPSLEEP EN LDO6	Enable LDO6 Deep SLEEP mode: 0 – LDO6 stays on when the IC enters Deep Sleep mode 1 – LDO6 turns off when the IC enters Deep Sleep mode	
RFU	Reserved for Future Use	Do not change this register value. Changing the register value can affect IC functionality.

LDO36_REG03 – LDO6 Configuration Register

Address = 0x23h	Default = 0x00h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	ON DELAY LDO6[2:0]			OFF DELAY LDO6[2:0]			MODE LDO6	RST LDO6
Default	0	0	0	0	0	0	0	0
Access	R/W			R/W				

Name	Description	Notes
ON DELAY LDO6[2:0]	Follow Regulator Startup Delay Table in the Data Sheet	
OFF DELAY LDO6[2:0]	Follow Regulator Startup Delay Table in the Data Sheet	
MODE LDO6	Determines startup sequencing from the CMI code	This is a factory expert bit that should not be changed. Modifying this bit may result in unexpected IC behavior.
RST LDO6	0 – LDO6 does not affect nRESET output 1 – LDO6 affects nRESET output	

LDO36_REG04 – LDO6 Configuration Register

Address = 0x24h	Default = 0x00h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	RFU				RFU			
Default	0	0	0	0	0	0	0	0
Access	R/W				R/W			

Name	Description	Notes
RFU	Reserved for Future Use	Do not change this register value. Changing the register value can affect IC functionality.
RFU	Reserved for Future Use	Do not change this register value. Changing the register value can affect IC functionality.

LDO36_REG05 – LDO6 Configuration Register

Address = 0x25h	Default = 0x80h	Type n/a = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	ILIM SD DIS_LDO6	RFU	OnDLYRangeL6	DIS_PD_LDO6	OffDLYRangeL6	ILIM_SCL_LDO6	SST_LDO6	QLTCH LDO6
Default	1	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Name	Description	Notes
ILIM SD DIS_LDO6	Disable the shutdown by current limit of LDO6	
RFU	Reserved for Future Use	Do not change this register value. Changing the register value can affect IC functionality.
OnDLYRangeL6	Sellect different setting range for turn on delay: 0: use table 1 for delay setting 1: use table 2 for delay setting	
DIS_PD_LDO6	Option disable pulldown Resistor when LDO6 is turned-off 1: disable pulldown function	
OffDLYRangeL6	Sellect different setting range for turn off delay: 0: use table 1 for delay setting 1: use table 2 for delay setting	
ILIM_SCL_LDO6	Current limit setting for LDO/PLSW mode: 0: 350mA 1: 450mA	
SST_ LDO6	Soft start time: 0: 160us 1: 320us.	
QLTCH LDO6	Enable for latch of qualify: + 1: The qualify is latched. + 0: The qualify is not latched.	

LDO36_REG06 – LDO3 Configuration Register

Address = 0x26h	Default = 0x8Eh	Type = Basic Volatile

BIT	7	6	5	4	3	2	1	0
Name	PWR_GOOD_LDO3	OV_LDO3	ILIM_LDO3	RFU	UV_FLTMSK_LDO3	OV_FLTMSK_LDO3	ILIM_FLTMSK_LDO3	RFU
Default	1	0	0	0	1	1	1	0
Access	RO	RO	RO	RO	R/W	R/W	R/W	RO

Name	Description	Notes
PWR_GOOD_LDO3	POK status: 0 – LDO3 voltage is below the power good threshold 1 – LDO3 voltage is above the power good threshold	Provides real-time power good status
OV_LDO3	OV status: 0 – LDO3 voltage is below the overvoltage threshold 1 – LDO3voltage is above the overvoltage threshold	When output voltage > OV, this bit goes high. It is lached high until output voltage < OV and this bit is read.
ILIM_LDO3	ILIM status: 0: Output ILIM is not triggered 1: Output ILIM is triggered	When output current reached ILIM setting, this bit goes high. It is latched high until output current < ILIM and this bit is read.
RFU	Reserved for Future Use	Do not change this register value. Changing the register value can affect IC functionality.
UV_FLTMSK_LDO3	Mask LDO3 VOUT UV interrupt: 0: Unmask Vout UV interrupt 1: Default mask Vout UV interrupt	When 1, the LDO3 PG signal is masked and does not go to the master controller. This prevents LDO3 from asserting the nIRQ pin when it is disabled or drops out of regulation. LDO3 PG still provides real-time status.
OV_FLTMSK_LDO3	Mask LDO3 Vout OV interrupt: 0: Unmask Vout OV interrupt 1: Default mask Vout OV interrupt	When 1, the OV_LDO3 signal is masked and does not go to the master controller. This prevents LDO3 from asserting the nIRQ pin when it is above regulation limits. OV_LDO3 still provides overvoltage status.
ILIM_FLTMSK_LDO3	Mask ILIM interrupt: 0 - Unmasks the LDO3 ILIM interrupt 1 - Masks the LDO3 ILIM interrupt	When 1, the LDO3 ILIM signal is masked and does not go to the master controller. This prevents LDO3 from asserting the nIRQ pin when it is above regulation limits. ILIM still provides current limit status.

RFU	Reserved for Future Use	Do not change this register value. Changing the register value can affect IC functionality.

LDO36_REG07 – LDO3 Voltage Set Register

Address = 0x27h	Default = 0X7Fh	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	RANGE_LDO3	POR_MSK_L3	LDO3_VSET[5:0]					
Default	0	1	1	1	1	1	1	1
Access	R/W	R/W	R/W					

Name	Description	Notes
RANGE_LDO3	1: Vout from 1.2 to 3.6 0: Vout from 0.5 to 1.2875	
POR_MSK_L3	1: Vout from 1.2 to 3.6 0: Vout from 0.5 to 1.2875	
LDO3_VSET[5:0]	LDO3 output voltage setting. With RANGE_LDO3=1: 1.2V to 3.6V in 50mV steps With RANGE_LDO3=0: 0.5V to 1.2875V in 12.5mV steps	

LDO36_REG08 – LDO3 Configuration Register

Address = 0x28h	Default = 0xDBh	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	ON LDO3	PBIN EN LDO3	AUXIN EN LDO3	SLEEP EN LDO3	DPSLEEP EN LDO3	RFU	RFU	RFU
Default	1	1	0	1	1	0	1	1
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Name	Description	Notes
ON LDO3	0 – Not enable LDO3 1 – Enable LDO3	This functionality is dependent on the overall IC configuration. Consult the factory for details.
PBIN EN LDO3	0 - Not enable turn on by Push Button 1 – Enable turn on by Push Button	This functionality is dependent on the overall IC configuration. Consult the factory for details..
AUXIN EN LDO3	Enable turn on by gb_auxin 1: Enable 0: Disable	
SLEEP EN LDO3	Enable LDO3 SLEEP mode: 0 – LDO3 stays on when the IC enters Sleep mode 1 – LDO3 turns off when the IC enters Sleep mode	
DPSLEEP EN LDO3	Enable LDO3 Deep SLEEP mode: 0 – LDO3 stays on when the IC enters Deep Sleep mode 1 – LDO3 turns off when the IC enters Deep Sleep mode	
RFU	Reserved for Future Use	Do not change this register value. Changing the register value can affect IC functionality.

LDO36_REG09 – LDO3 Configuration Register

Address = 0x29h	Default = 0x47h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	ON DELAY LDO3[2:0]			OFF DELAY LDO3[2:0]			MODE LDO3	RST LDO3
Default	0	1	0	0	0	1	1	1
Access	R/W			R/W				

Name	Description	Notes
ON DELAY LDO3[2:0]	Follow Regulator Startup Delay Table in the Data Sheet	
OFF DELAY LDO3[2:0]	Follow Regulator Startup Delay Table in the Data Sheet	
MODE LDO3	Determines startup sequencing from the CMI code	This is a factory expert bit that should not be changed. Modifying this bit may result in unexpected IC behavior.
RST LDO3	0 – LDO3 does not affect nRESET output 1 – LDO3 affects nRESET output	

LDO36_REG0A – LDO3 Configuration Register

Address = 0x2Ah	Default = 0x05h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	RFU				RFU			
Default	0	0	0	0	0	1	0	1
Access	R/W				R/W			

Name	Description	Notes
RFU	Reserved for Future Use	Do not change this register value. Changing the register value can affect IC functionality.
RFU	Reserved for Future Use	Do not change this register value. Changing the register value can affect IC functionality.

LDO4, LSW7 REGISTERS

LDO47_REG00 – LSW7 Configuration Register

Address = 0xC0h	Default = 0x8Eh	Type = Basic Volatile

BIT	7	6	5	4	3	2	1	0
Name	PWR_GOOD_LSW7	OV_LSW7	ILIM_LSW7	RFU	UV_FLTMSK_LSW7	OV_FLTMSK_LSW7	ILIM_FLTMSK_LSW7	RFU
Default	1	0	0	0	1	1	1	0
Access	RO	RO	RO	RO	R/W	R/W	R/W	RO

Name	Description	Notes
PG_LSW7	POK status: 0 – LSW7 voltage is below the power good threshold 1 – LSW7 voltage is above the power good threshold	Provides real-time power good status
OV_LSW7	OV status: 0 – LSW7 voltage is below the overvoltage threshold 1 – LSW7voltage is above the overvoltage threshold	When output voltage > OV, this bit goes high. It is lached high until output voltage < OV and this bit is read.
ILIM_LSW7	ILIM status: 0: Output ILIM is not triggered 1: Output ILIM is triggered	When output current reached ILIM setting, this bit goes high. It is latched high until output current < ILIM and this bit is read.
RFU	Reserved for Future Use	Do not change this register value. Changing the register value can affect IC functionality.
UV_FLTMSK_LSW7	Mask LSW7 VOUT UV interrupt: 0: Unmask Vout UV interrupt 1: Default mask Vout UV interrupt	When 1, the LSW7 PG signal is masked and does not go to the master controller. This prevents LSW7 from asserting the nIRQ pin when it is disabled or drops out of regulation. LSW7 PG still provides real-time status.
OV_FLTMSK_LSW7	Mask LSW7 Vout OV interrupt: 0: Unmask Vout OV interrupt 1: Default mask Vout OV interrupt	When 1, the OV_LSW7 signal is masked and does not go to the master controller. This prevents LSW7 from asserting the nIRQ pin when it is above regulation limits. OV_LSW7 still provides overvoltage status.

ILIM_FLTMSK_LSW7	Mask ILIM interrupt: 0 - Unmasks the LSW7 ILIM interrupt 1 - Masks the LSW7 ILIM interrupt	When 1, the LSW7 ILIM signal is masked and does not go to the master controller. This prevents LSW7 from asserting the nIRQ pin when it is above regulation limits. ILIM still provides current limit status.
RFU	Reserved for Future Use	Do not change this register value. Changing the register value can affect IC functionality.

LDO47_REG01 – LSW7 Voltage Set Register

Address = 0xC1h	Default = 0xADh	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	RFU	Bk2_VSET3[6:0]						
Default	1	0	1	0	1	1	0	1
Access	R/W	R/W						

Name	Description	Notes
RFU	Reserved for Future Use	Do not change this register value. Changing the register value can affect IC functionality.
Bk2_VSET3[6:0]	Buck2 output voltage setting VSET0: 0.5V to 1.135V in 5mV steps: VRANGE=0 VSET0: 0.5V to 3.675V in 25mV steps: VRANGE=1	

LDO47_REG02 – LSW7 Configuration Register

Address = 0xC2h	Default = 0x58h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	ON_ LSW7	PBIN_EN_ LSW7	AUXIN_EN_ LSW7	SLEEP EN LSW7	DPSLEEP EN LSW7	RFU	RFU	RFU
Default	0	1	0	1	1	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Name	Description	Notes
ON_ LSW7	0 – Not enable LSW7 1 – Enable LSW7	This functionality is dependent on the overall IC configuration. Consult the factory for details.
PBIN_EN_ LSW7	0 - Not enable turn on by Push Button 1 – Enable turn on by Push Button	This functionality is dependent on the overall IC configuration. Consult the factory for details..
AUXIN_EN_LSW7	Enable turn on by gb_auxin 1: Enable 0: Disable	
SLEEP EN LSW7	Enable LSW7 SLEEP mode: 0 – LSW7 stays on when the IC enters Sleep mode 1 – LSW7 turns off when the IC enters Sleep mode	
DPSLEEP EN LSW7	Enable LSW7 Deep SLEEP mode: 0 – LSW7 stays on when the IC enters Deep Sleep mode 1 – LSW7 turns off when the IC enters Deep Sleep mode	
RFU	Reserved for Future Use	Do not change this register value. Changing the register value can affect IC functionality.

LDO47_REG03 – LSW7 Configuration Register

Address = 0xC3h	Default = 0x00h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	ON_DLY_ LSW7[2:0]			OFF_DLY_LSW7[2:0]			MODE_ LSW7	RST_LSW7
Default	0	0	0	0	0	0	0	0
Access	R/W			R/W				

Name	Description	Notes
ON_DLY_ LSW7[2:0]	Follow Regulator Startup Delay Table in the Data Sheet	
OFF_DLY_LSW7[2:0]	Follow Regulator Startup Delay Table in the Data Sheet	
MODE_ LSW7	Determines startup sequencing from the CMI code	This is a factory expert bit that should not be changed. Modifying this bit may result in unexpected IC behavior.
RST_ LSW7	0 – LSW7 does not affect nRESET output 1 – LSW7 affects nRESET output	

LDO47_REG04 – LSW7 Configuration Register

Address = 0xC4h	Default = 0x90h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	RFU				RFU			
Default	1	0	0	1	0	0	0	0
Access	R/W				R/W			

Name	Description	Notes
RFU	Reserved for Future Use	Do not change this register value. Changing the register value can affect IC functionality.
RFU	Reserved for Future Use	Do not change this register value. Changing the register value can affect IC functionality.

LDO47_REG05 – LSW7 Configuration Register

Address = 0xC5h	Default = 0XC0h	Type n/a = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	ILIM_SD_ DIS_LSW7	POR_MSK_ L7	OnDelayRa ngeL7	DIS_PULLD OWN_LSW 7	OffDelayRa ngeL7	RFU	RFU	QLTCH LSW7
Default	1	1	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W			R/W

Name	Description	Notes
ILIM_SD_ DIS_LSW7	Disable the shutdown by current limit of LSW7	
POR_MSK_L7	1: Pull the GPIO to VIO by 86kOhm	
OnDelayRangeL7	Sellect different setting range for turn on delay: 0: use table 1 for delay setting 1: use table 2 for delay setting	
DIS_PULLDOWN_LSW7	Option disable pulldown Resistor when LSW7 is turned-off 1: disable pulldown function	
OffDelayRangeL7	Sellect different setting range for turn off delay: 0: use table 1 for delay setting 1: use table 2 for delay setting	
RFU	Reserved for Future Use	Do not change this register value. Changing the register value can affect IC functionality.
RFU	Reserved for Future Use	Do not change this register value. Changing the register value can affect IC functionality.
QLTCH LSW7	Enable for latch of qualify: + 1: The qualify is latched. + 0: The qualify is not latched.	

LDO47_REG06 – LDO4 Configuration Register

Address = 0xC6h	Default = 0x0Eh	Type = Basic Volatile

BIT	7	6	5	4	3	2	1	0
Name	PWR_GOOD_LDO4	OV_LDO4	ILIM_LDO4	RFU	UV_FLTMSK_LDO4	OV_FLTMSK_LDO4	ILIM_FLTMSK_LDO4	RFU
Default	0	0	0	0	1	1	1	0
Access	RO	RO	RO	RO	R/W	R/W	R/W	RO

Name	Description	Notes
PWR_GOOD_LDO4	POK status: 0 – LDO4 voltage is below the power good threshold 1 – LDO4 voltage is above the power good threshold	Provides real-time power good status
OV_LDO4	OV status: 0 – LDO4 voltage is below the overvoltage threshold 1 – LDO4voltage is above the overvoltage threshold	When output voltage > OV, this bit goes high. It is lached high until output voltage < OV and this bit is read.
ILIM_LDO4	ILIM status: 0: Output ILIM is not triggered 1: Output ILIM is triggered	When output current reached ILIM setting, this bit goes high. It is latched high until output current < ILIM and this bit is read.
RFU	Reserved for Future Use	Do not change this register value. Changing the register value can affect IC functionality.
UV_FLTMSK_LDO4	Mask LDO4 VOUT UV interrupt: 0: Unmask Vout UV interrupt 1: Default mask Vout UV interrupt	When 1, the LDO4 PG signal is masked and does not go to the master controller. This prevents LDO4 from asserting the nIRQ pin when it is disabled or drops out of regulation. LDO4 PG still provides real-time status.
OV_FLTMSK_LDO4	Mask LDO4 Vout OV interrupt: 0: Unmask Vout OV interrupt 1: Default mask Vout OV interrupt	When 1, the OV_LDO4 signal is masked and does not go to the master controller. This prevents LDO4 from asserting the nIRQ pin when it is above regulation limits. OV_LDO4 still provides overvoltage status.
ILIM_FLTMSK_LDO4	Mask ILIM interrupt: 0 - Unmasks the LDO4 ILIM interrupt 1 - Masks the LDO4 ILIM interrupt	When 1, the LDO4 ILIM signal is masked and does not go to the master controller. This prevents LDO4 from asserting the nIRQ pin when it is above regulation limits. ILIM still provides current limit status.

RFU	Reserved for Future Use	Do not change this register value. Changing the register value can affect IC functionality.

LDO47_REG07 – LDO4 Voltage Set Register

Address = 0xC7h	Default = 0xCCh	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	RANGE_LDO4	POR_MSK_L4	LDO4 VSET[5:0]					
Default	1	1	0	0	1	1	0	0
Access	R/W	R/W	R/W					

Name	Description	Notes
RANGE_LDO4	1: Vout from 1.2 to 3.6 0: Vout from 0.5 to 1.2875	
POR_MSK_L4	1: Vout from 1.2 to 3.6 0: Vout from 0.5 to 1.2875	
LDO4 VSET[5:0]	LDO4 output voltage setting. With RANGE_LDO4=1: 1.2V to 3.6V in 50mV steps With RANGE_LDO4=0: 0.5V to 1.2875V in 12.5mV steps	

LDO47_REG08 – LDO4 Configuration Register

Address = 0xC8h	Default = 0x58h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	ON LDO4	PBIN EN LDO4	AUXIN EN LDO4	SLEEP EN LDO4	DPSLEEP EN LDO4	RFU	RFU	RFU
Default	0	1	0	1	1	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Name	Description	Notes
ON LDO4	0 – Not enable LDO4 1 – Enable LDO4	This functionality is dependent on the overall IC configuration. Consult the factory for details.
PBIN EN LDO4	0 - Not enable turn on by Push Button 1 – Enable turn on by Push Button	This functionality is dependent on the overall IC configuration. Consult the factory for details..
AUXIN EN LDO4	Enable turn on by gb_auxin 1: Enable 0: Disable	
SLEEP EN LDO4	Enable LDO4 SLEEP mode: 0 – LDO4 stays on when the IC enters Sleep mode 1 – LDO4 turns off when the IC enters Sleep mode	
DPSLEEP EN LDO4	Enable LDO4 Deep SLEEP mode: 0 – LDO4 stays on when the IC enters Deep Sleep mode 1 – LDO4 turns off when the IC enters Deep Sleep mode	
RFU	Reserved for Future Use	Do not change this register value. Changing the register value can affect IC functionality.

LDO47_REG09 – LDO4 Configuration Register

Address = 0xC9h	Default = 0x02h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	ON DELAY LDO4[2:0]			OFF DELAY LDO4[2:0]			MODE LDO4	RST LDO4
Default	0	0	0	0	0	0	1	0
Access	R/W			R/W				

Name	Description	Notes
ON DELAY LDO4[2:0]	Follow Regulator Startup Delay Table in the Data Sheet	
OFF DELAY LDO4[2:0]	Follow Regulator Startup Delay Table in the Data Sheet	
MODE LDO4	Determines startup sequencing from the CMI code	This is a factory expert bit that should not be changed. Modifying this bit may result in unexpected IC behavior.
RST LDO4	0 – LDO4 does not affect nRESET output 1 – LDO4 affects nRESET output	

LDO47_REG0A – LDO4 Configuration Register

Address = 0xCAh	Default = 0x00h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	RFU				RFU			
Default	0	0	0	0	0	0	0	0
Access	R/W				R/W			

Name	Description	Notes
RFU	Reserved for Future Use	Do not change this register value. Changing the register value can affect IC functionality.
RFU	Reserved for Future Use	Do not change this register value. Changing the register value can affect IC functionality.

LDO5, LSW8 REGISTERS

LDO58_REG00 – LSW8 Configuration Register

Address = 0xC0h	Default = 0x0Eh	Type = Basic Volatile

BIT	7	6	5	4	3	2	1	0
Name	PWR_GOOD_LSW8	OV_LSW8	ILIM_LSW8	RFU	UV_FLTMSK_LSW8	OV_FLTMSK_LSW8	ILIM_FLTMSK_LSW8	RFU
Default	0	0	0	0	1	1	1	0
Access	RO	RO	RO	RO	R/W	R/W	R/W	RO

Name	Description	Notes
PWR_GOOD_LSW8	POK status: 0 – LSW8 voltage is below the power good threshold 1 – LSW8 voltage is above the power good threshold	Provides real-time power good status
OV_LSW8	OV status: 0 – LSW8 voltage is below the overvoltage threshold 1 – LSW8 voltage is above the overvoltage threshold	When output voltage > OV, this bit goes high. It is lached high until output voltage < OV and this bit is read.
ILIM_LSW8	ILIM status: 0: Output ILIM is not triggered 1: Output ILIM is triggered	When output current reached ILIM setting, this bit goes high. It is latched high until output current < ILIM and this bit is read.
RFU	Reserved for Future Use	Do not change this register value. Changing the register value can affect IC functionality.
UV_FLTMSK_LSW8	Mask LSW8 VOUT UV interrupt: 0: Unmask Vout UV interrupt 1: Default mask Vout UV interrupt	When 1, the LSW8PG signal is masked and does not go to the master controller. This prevents LSW8 from asserting the nIRQ pin when it is disabled or drops out of regulation. LSW8 PG still provides real-time status.
OV_FLTMSK_LSW8	Mask LSW8 Vout OV interrupt: 0: Unmask Vout OV interrupt 1: Default mask Vout OV interrupt	When 1, the OV_ LSW8 signal is masked and does not go to the master controller. This prevents LSW8 from asserting the nIRQ pin when it is above regulation limits. OV_ LSW8 still provides overvoltage status.

ILIM_FLTMSK_LSW8	Mask ILIM interrupt: 0 - Unmasks the LSW8 ILIM interrupt 1 - Masks the LSW8 ILIM interrupt	When 1, the LSW8 ILIM signal is masked and does not go to the master controller. This prevents LSW8 from asserting the nIRQ pin when it is above regulation limits. ILIM still provides current limit status.
RFU	Reserved for Future Use	Do not change this register value. Changing the register value can affect IC functionality.

LDO58_REG01 – LSW8 Voltage Set Register

Address = 0xC1h	Default = 0xADh	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	RFU	BK1_VSET3[6:0]						
Default	1	0	1	0	1	1	0	1
Access	R/W	R/W						

Name	Description	Notes
RFU	Reserved for Future Use	Do not change this register value. Changing the register value can affect IC functionality.
BK1_VSET3[6:0]	Buck1 output voltage setting VSET0: 0.5V to 1.135V in 5mV steps: VRANGE=0 VSET0: 0.5V to 3.675V in 25mV steps: VRANGE=1	

LDO58_REG02 – LSW8 Configuration Register

Address = 0xC2h	Default = 0x58h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	ON_ LSW8	PBIN_EN_ LSW8	AUXIN_EN_ LSW8	SLEEP EN LSW8	DPSLEEP EN LSW8	RFU	RFU	RFU
Default	0	1	0	1	1	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Name	Description	Notes
ON_ LSW8	0 – Not enable LSW8 1 – Enable LSW8	This functionality is dependent on the overall IC configuration. Consult the factory for details.
PBIN_EN_ LSW8	0 - Not enable turn on by Push Button 1 – Enable turn on by Push Button	This functionality is dependent on the overall IC configuration. Consult the factory for details..
AUXIN_EN_LSW8	Enable turn on by gb_auxin 1: Enable 0: Disable	
SLEEP EN LSW8	Enable LSW8 SLEEP mode: 0 – LSW8 stays on when the IC enters Sleep mode 1 – LSW8 turns off when the IC enters Sleep mode	
DPSLEEP EN LSW8	Enable LSW8 Deep SLEEP mode: 0 – LSW8 stays on when the IC enters Deep Sleep mode 1 – LSW8 turns off when the IC enters Deep Sleep mode	
RFU	Reserved for Future Use	Do not change this register value. Changing the register value can affect IC functionality.

LDO58_REG03 – LSW8 Configuration Register

Address = 0xC3h	Default = 0x00h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	ON_DLY_ LSW8[2:0]			OFF_DLY_LSW8[2:0]			MODE_ LSW8	RST_LSW8
Default	0	0	0	0	0	0	0	0
Access	R/W			R/W				

Name	Description	Notes
ON_DLY_ LSW8[2:0]	Follow Regulator Startup Delay Table in the Data Sheet	
OFF_DLY_LSW8[2:0]	Follow Regulator Startup Delay Table in the Data Sheet	
MODE_ LSW8	Determines startup sequencing from the CMI code	This is a factory expert bit that should not be changed. Modifying this bit may result in unexpected IC behavior.
RST_ LSW8	0 – LSW8 does not affect nRESET output 1 – LSW8 affects nRESET output	

LDO58_REG04 – LSW8 Configuration Register

Address = 0xC4h	Default = 0x00h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	RFU				RFU			
Default	0	0	0	0	0	0	0	0
Access	R/W				R/W			

Name	Description	Notes
RFU	Reserved for Future Use	Do not change this register value. Changing the register value can affect IC functionality.
RFU	Reserved for Future Use	Do not change this register value. Changing the register value can affect IC functionality.

LDO58_REG05 – LSW8 Configuration Register

Address = 0xC5h	Default = 0xC0h	Type n/a = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	ILIM SHUTDOWN DIS_L8	POR_MSK_L8	OnDelayRangeL8	DisPULLDOWN_L8	OffDelayRangeL8	RFU	RFU	QLTCH LSW8
Default	1	1	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Name	Description	Notes
ILIM SHUTDOWN DIS_L8	Disable the shutdown by current limit of LSW8	
POR_MSK_L8	1: Pull the GPIO to VIO by 86kOhm	
OnDelayRangeL8	Sellect different setting range for turn on delay: 0: use table 1 for delay setting 1: use table 2 for delay setting	
DisPULLDOWN_L8	Option disable pulldown Resistor when LSW8 is turned-off 1: disable pulldown function	
OffDelayRangeL8	Sellect different setting range for turn off delay: 0: use table 1 for delay setting 1: use table 2 for delay setting	
RFU	Reserved for Future Use	Do not change this register value. Changing the register value can affect IC functionality.
RFU	Reserved for Future Use	Do not change this register value. Changing the register value can affect IC functionality.
QLTCH LSW8	Enable for latch of qualify: + 1: The qualify is latched. + 0: The qualify is not latched.	

LDO58_REG06 – LDO5 Configuration Register

Address = 0xC6h	Default = 0x0Eh	Type = Basic Volatile

BIT	7	6	5	4	3	2	1	0
Name	PWR_GOOD_LDO5	OV_LDO5	ILIM_LDO5	RFU	UV_FLTMSK_LDO5	OV_FLTMSK_LDO5	ILIM_FLTMSK_LDO5	RFU
Default	0	0	0	0	1	1	1	0
Access	RO	RO	RO	RO	R/W	R/W	R/W	RO

Name	Description	Notes
PWR_GOOD_LDO5	POK status: 0 – LDO5 voltage is below the power good threshold 1 – LDO5 voltage is above the power good threshold	Provides real-time power good status
OV_LDO5	OV status: 0 – LDO5 voltage is below the overvoltage threshold 1 – LDO5voltage is above the overvoltage threshold	When output voltage > OV, this bit goes high. It is lached high until output voltage < OV and this bit is read.
ILIM_LDO5	ILIM status: 0: Output ILIM is not triggered 1: Output ILIM is triggered	When output current reached ILIM setting, this bit goes high. It is latched high until output current < ILIM and this bit is read.
RFU	Reserved for Future Use	Do not change this register value. Changing the register value can affect IC functionality.
UV_FLTMSK_LDO5	Mask LDO5 VOUT UV interrupt: 0: Unmask Vout UV interrupt 1: Default mask Vout UV interrupt	When 1, the LDO5 PG signal is masked and does not go to the master controller. This prevents LDO5 from asserting the nIRQ pin when it is disabled or drops out of regulation. LDO5 PG still provides real-time status.
OV_FLTMSK_LDO5	Mask LDO5 Vout OV interrupt: 0: Unmask Vout OV interrupt 1: Default mask Vout OV interrupt	When 1, the OV_LDO5 signal is masked and does not go to the master controller. This prevents LDO5 from asserting the nIRQ pin when it is above regulation limits. OV_LDO5 still provides overvoltage status.
ILIM_FLTMSK_LDO5	Mask ILIM interrupt: 0 - Unmasks the LDO5 ILIM interrupt 1 - Masks the LDO5 ILIM interrupt	When 1, the LDO5 ILIM signal is masked and does not go to the master controller. This prevents LDO5 from asserting the nIRQ pin when it is above regulation limits. ILIM still provides current limit status.

RFU	Reserved for Future Use	Do not change this register value. Changing the register value can affect IC functionality.

LDO58_REG07 – LDO5 Voltage Set Register

Address = 0xC7h	Default = 0x6Ch	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	RANGE_LDO5	POR_MSK_L5	LDO5 VSET[5:0]					
Default	0	1	1	0	1	1	0	0
Access	R/W	R/W	R/W					

Name	Description	Notes
RANGE_LDO5	1: Vout from 1.2 to 3.6 0: Vout from 0.5 to 1.2875	
POR_MSK_L5	1: Vout from 1.2 to 3.6 0: Vout from 0.5 to 1.2875	
LDO5 VSET[5:0]	LDO5 output voltage setting. With RANGE_LDO5=1: 1.2V to 3.6V in 50mV steps With RANGE_LDO5=0: 0.5V to 1.2875V in 12.5mV steps	

LDO58_REG08 – LDO5 Configuration Register

Address = 0xC8h	Default = 0x58h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	ON LDO5	PBIN EN LDO5	AUXIN EN LDO5	SLEEP EN LDO5	DPSLEEP EN LDO5	RFU	RFU	RFU
Default	0	1	0	1	1	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Name	Description	Notes
ON_ LDO5	0 – Not enable LDO5 1 – Enable LDO5	This functionality is dependent on the overall IC configuration. Consult the factory for details.
PBIN_EN_ LDO5	0 - Not enable turn on by Push Button 1 – Enable turn on by Push Button	This functionality is dependent on the overall IC configuration. Consult the factory for details..
AUXIN_EN_LDO5	Enable turn on by gb_auxin 1: Enable 0: Disable	
SLP_EN_LDO5	Enable LDO5 SLEEP mode: 0 – LDO5 stays on when the IC enters Sleep mode 1 – LDO5 turns off when the IC enters Sleep mode	
DPSLP_EN_LDO5	Enable LDO5 Deep SLEEP mode: 0 – LDO5 stays on when the IC enters Deep Sleep mode 1 – LDO5 turns off when the IC enters Deep Sleep mode	
RFU	Reserved for Future Use	Do not change this register value. Changing the register value can affect IC functionality.

LDO58_REG09 – LDO5 Configuration Register

Address = 0xC9h	Default = 0x02h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	ON DELAY LDO5[2:0]			OFF DELAY LDO5[2:0]			MODE LDO5	RST LDO5
Default	000			000			1	0
Access	R/W			R/W				

Name	Description	Notes
ON_DLY_ LDO5[2:0]	Follow Regulator Startup Delay Table in the Data Sheet	
OFF_DLY_LDO5[2:0]	Follow Regulator Startup Delay Table in the Data Sheet	
MODE_LDO5	Determines startup sequencing from the CMI code	This is a factory expert bit that should not be changed. Modifying this bit may result in unexpected IC behavior.
RST_ LDO5	0 – LDO5 does not affect nRESET output 1 – LDO5 affects nRESET output	

LDO58_REG0A – LDO5 Configuration Register

Address = 0xCAh	Default = 0x00h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	RFU				RFU			
Default	0000				0000			
Access	R/W				R/W			

Name	Description	Notes
RFU	Reserved for Future Use	Do not change this register value. Changing the register value can affect IC functionality.
RFU	Reserved for Future Use	Do not change this register value. Changing the register value can affect IC functionality.

Referenced Documents

The reference documents below take precedence over the contents of this application note and should always be consulted for the latest information.

ACT88911 Data Sheet

Contact Information

For the latest specifications, additional product information, worldwide sales and distribution locations:

Web: www.qorvo.com

Tel: 1-844-890-8163

Email: customer.support@qorvo.com

Important Notice

The information contained in this Data Sheet and any associated documents (“Data Sheet Information”) is believed to be reliable; however, Qorvo makes no warranties regarding the Data Sheet Information and assumes no responsibility or liability whatsoever for the use of said information. All Data Sheet Information is subject to change without notice. Customers should obtain and verify the latest relevant Data Sheet Information before placing orders for Qorvo® products. Data Sheet Information or the use thereof does not grant, explicitly, implicitly or otherwise any rights or licenses to any third party with respect to patents or any other intellectual property whether with regard to such Data Sheet Information itself or anything described by such information.

DATA SHEET INFORMATION DOES NOT CONSTITUTE A WARRANTY WITH RESPECT TO THE PRODUCTS DESCRIBED HEREIN, AND QORVO HEREBY DISCLAIMS ANY AND ALL WARRANTIES WITH RESPECT TO SUCH PRODUCTS WHETHER EXPRESS OR IMPLIED BY LAW, COURSE OF DEALING, COURSE OF PERFORMANCE, USAGE OF TRADE OR OTHERWISE, INCLUDING THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE. Without limiting the generality of the foregoing, Qorvo® products are not warranted or authorized for use as critical components in medical, life-saving, or life-sustaining applications, or other applications where a failure would reasonably be expected to cause severe personal injury or death. Applications described in the Data Sheet Information are for illustrative purposes only. Customers are responsible for validating that a particular product described in the Data Sheet Information is suitable for use in a particular application.