BENEFITS and FEATURES

- JEITA Compliant 1.5 A, 1S, Active Power Path Switching Charger (APSC)
- On-the-Fly Adjustments to Charging Profile to Support Multi-step Battery Charging
- Dual Charging Input Support – USB or Wireless with Independent Input Current Limits
- 23 V Blocking Protection on Charger Inputs
- Max Operating Voltage of 13V on Wireless Charging Input
- Integrated Charger VBAT FET
- Integrated 1.8 V & 3.3 V Low I_Q LDOs Capable of 80 mA Output Currents
- Four 25 mA LED Drivers with 50 mV Drop Out & Programmable Drive Current, Duty Cycle, & PWM Period
- Integrated Volatile Memory for 3 LED Animation Sequences
- Push Button Input with Short, Medium, and Long Press Detection
- Support for Ultra-Low Power Shipping Mode
- 1MHz I2C Compliance with Programmable Address for PMIC Configuration & System Communication
- 2.86 x 2.90 mm 42 Balls 0.4 mm Pitch WLCSP

APPLICATIONS

- Earbud Charging Cases
- IoT Devices
- Portable Single Cell Battery-Powered Electronics

GENERAL DESCRIPTION

The ACT82120 provides a complete one cell charging ecosystem optimized for portable electronic devices in a single highly integrated PMIC. This IC combines a 1.5 A JEITA switching battery charger with integrated VBAT control MOSFET plus two low I_Q LDOs, push-button input, and four 25 mA LED drivers.

Design flexibility is offered through full programmability of the charging profile including pre-charge current, fast charge current, termination current, charge voltage, and battery temperature protection. Additionally, On-the-Fly adjustments to the charging profile allow for fine-tuned, multi-loop charge profiles through communication with an external MCU or processor. Support for both wireless charging and wired charging over USB-C, with smart selection between options, enhances the flexibility of the PMIC to accommodate the needs of many applications.

The ACT82120 provides two auxiliary rails from low I_Q LDOs for powering any peripheral loads in the system. Additionally, the switching charger allows the system voltage to be regulated at the battery voltage for operation even when the battery is completely discharged or removed. When extra power savings are required, the PMIC can be placed into a low I_Q Ship Mode with only two LDOs and basic Push Button and Charge source detection functionality.

A combination of push-button input and quad channel LED drivers allows for basic end user interaction without the need for microcontroller communication. The push-button input can detect short, medium, long, and quick presses with programmable time thresholds for each event. Onboard volatile storage of three flashing sequences for the LED drivers allows for standby, charging, or other status indication.

Communication through the I2C bus allows for configuration of the PMIC during the design process and on-the-fly communication to a microcontroller in end applications. Onboard NVM storage of all programable settings lets the system be fully operational upon start up with minimal external communication. A small form factor WLCSP and few required external components keep the overall solution size compact.

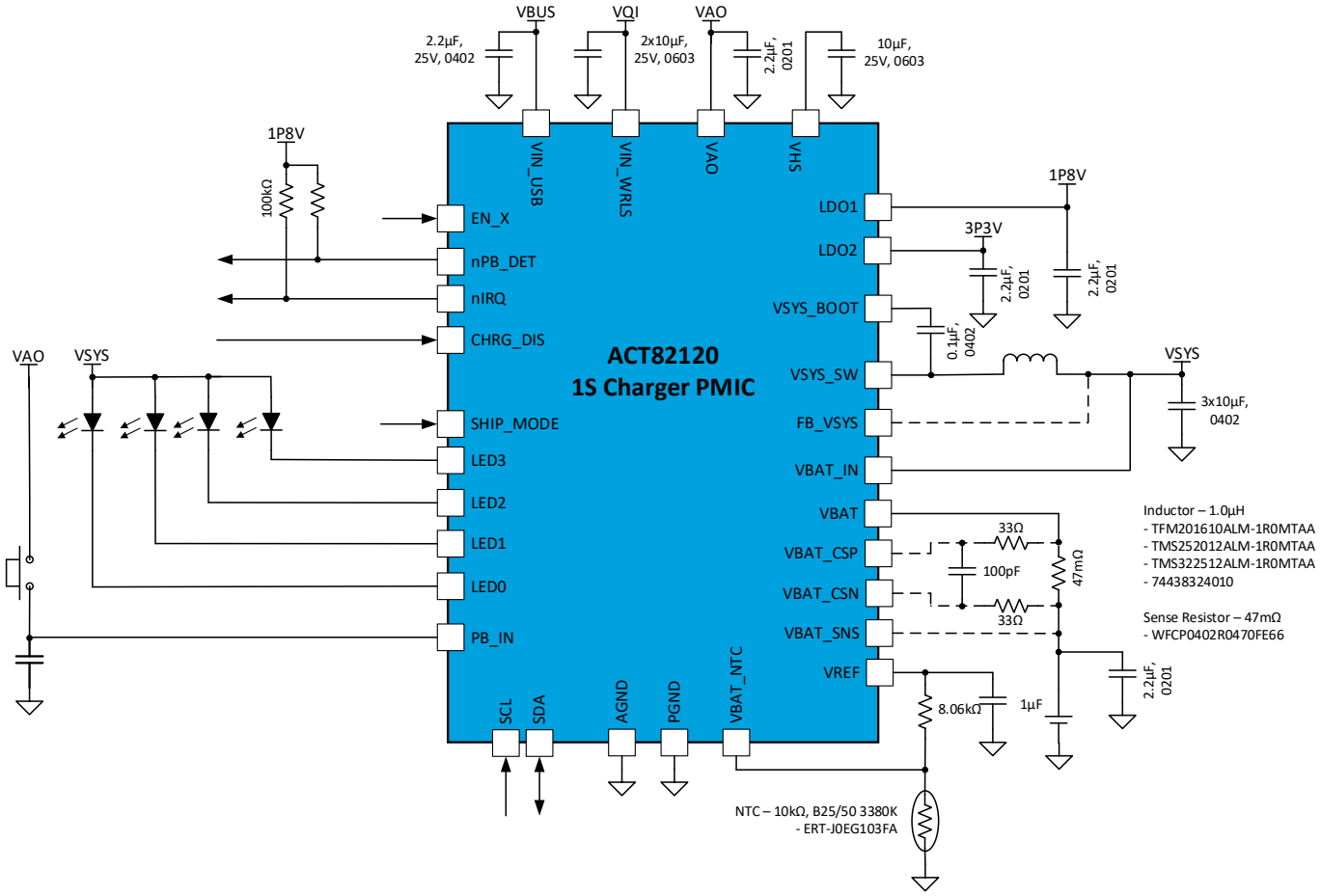


Figure 1: Simplified Applications Schematic

FUNCTIONAL BLOCK DIAGRAM

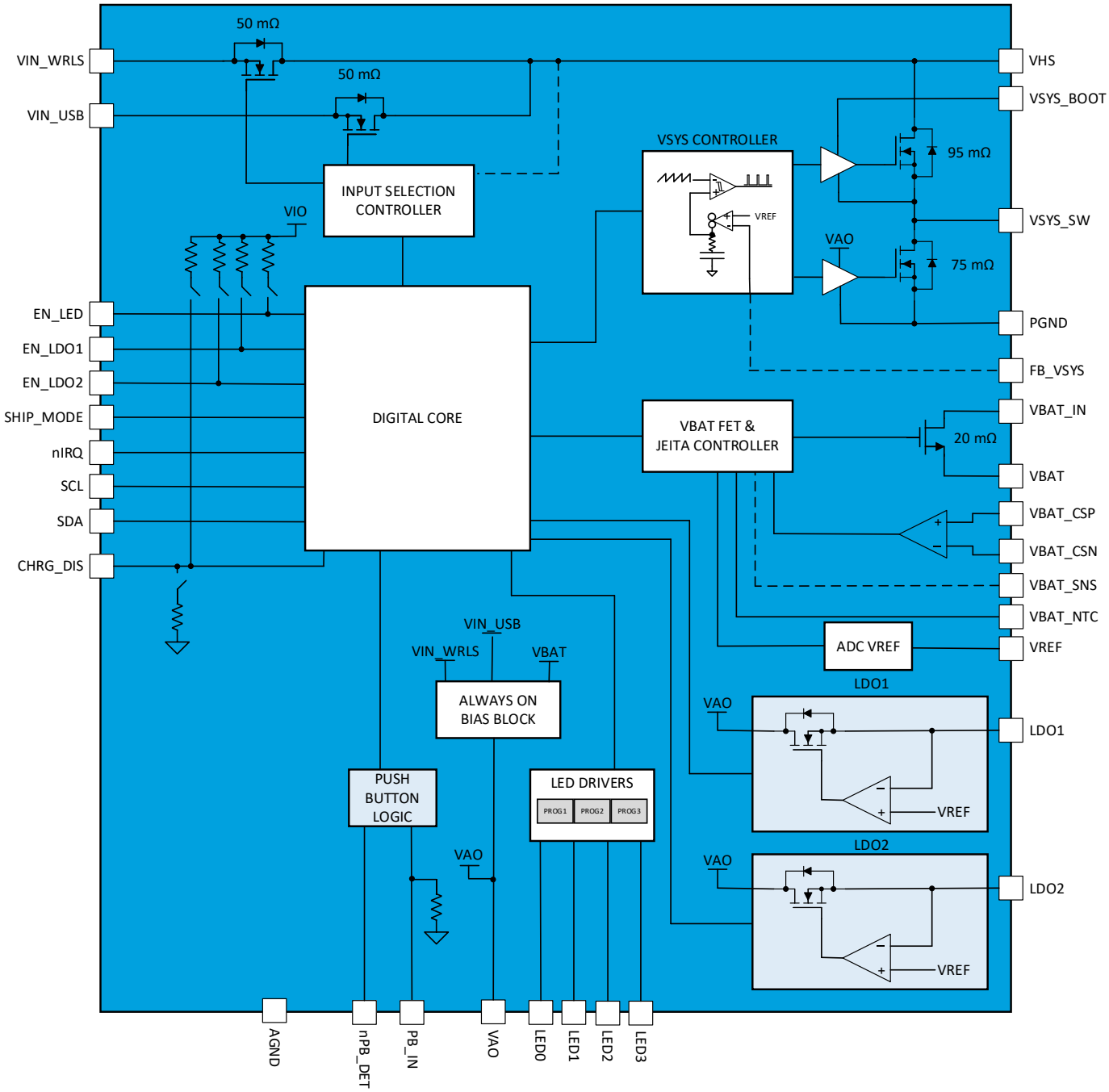
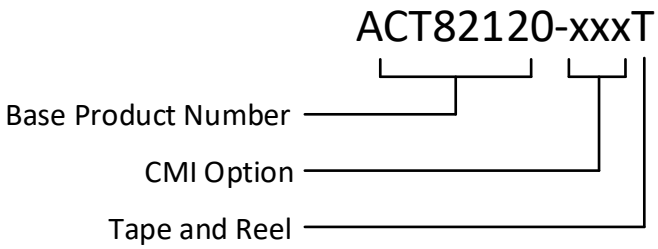


Figure 2: ACT82120 Block Diagram

ORDERING INFORMATION

PART NUMBER	DESCRIPTION
ACT82120-101T	Base PMIC Configuration



Note1: Standard product options are identified in this table. Contact factory for custom options, minimum order quantity required.
Note2: “xxx” represents the CMI (Code Matrix Index) option The CMI identifies the IC’s default register settings.

PIN CONFIGURATION

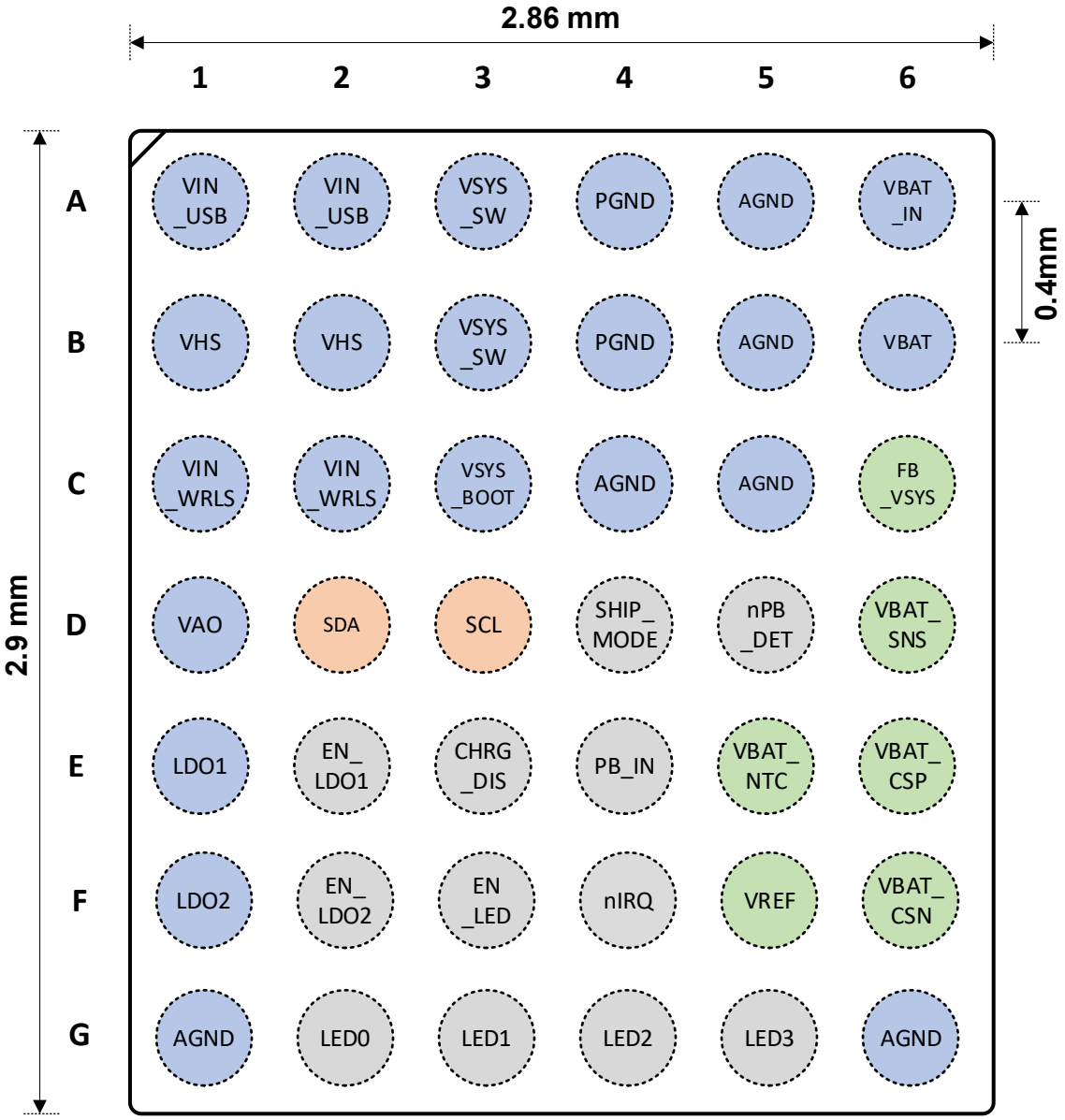


Figure 3: Pinout 42 Ball WLCSP, 0.4mm Pitch – Top View

PIN DESCRIPTIONS

PIN	NAME	DESCRIPTION
A1, A2	VIN_USB	5 V USB Input Supply to the PMIC. Decouple with appropriate capacitor.
A3, B3	VSYS_SW	Switch Node for the VSYS Regulator. Connect to inductor through short, wide copper pour.
A4, B4	PGND	Power Ground – Tie to larger PCB ground planes.
A5, B5, C4, C5, G1, G8	AGND	Analog Ground – Tie to larger PCB ground planes.
A6	VBAT_IN	Battery Charger Input Supply Connection. Connect to VSYS regulator output.

B1, B2	VHS	PMIC Power Supply from either the USB or Wireless Charger Supply Pins. Decouple with appropriate capacitor.
B6	VBAT	Battery Charger Output. Connect to positive terminal of battery current sense resistor.
C1, C2	VIN_WRLS	Wireless Charging Input Supply to the PMIC. Decouple with appropriate capacitor.
C3	VSYS_BOOT	VSYS Upper FET Bootstrap Connection. Connect bootstrap capacitor between BOOT_SYS and SW_SYS pins.
C6	FB_VSYS	VSYS Regulator Sense Line. Kelvin connect to VSYS Output Node.
D1	VAO	Always on regulator powering the internal IC blocks. Do not power external circuitry from this pin. Decouple with at least 1 µF of effective capacitance after DC bias derating is taken into account.
D2	SDA	I2C Data Pin. Connect to appropriate pull-up resistor.
D3	SCL	I2C Clock Pin. Connect to appropriate pull-up resistor.
D4	SHIP_MODE	Active High Input Pin to configure the PMIC into a low power state.
D5	nPB_DET	Active Low Signal generated from 3-tier Push Button Input.
D6	VBAT_SNS	VBAT Sense Pin to monitor battery voltage. Kelvin connect to positive terminal of battery.
E1	LDO1	LDO1 Output Pin. Decouple with appropriate capacitor.
E2	EN_LDO1	LDO1 Enable Pin. If pulled up to an off PMIC supply, ensure voltage is less than VAO for low leakage in Ship Mode & Deep Sleep.
E3	CHRG_DIS	Charge Disable Pin. Tie high to disable battery charging. Internal pulldown allows for either floating or tying pin low to enable charging.
E4	PB_IN	Push Button Input supporting 3 tier control.
E5	VBAT_NTC	Battery Temperature Monitor Pin. Connect to NTC resistor divider from VREF.
E6	VBAT_CSP	Battery Charger Current Sense Amplifier Positive Input Pin. Kelvin connect to positive side of battery current sense resistor.
F1	LDO2	LDO2 Output Pin. Decouple with appropriate capacitor.
F2	EN_LDO2	LDO2 Enable Pin. If pulled up to an off PMIC supply, ensure voltage is less than VAO for low leakage in Ship Mode & Deep Sleep.
F3	EN_LED	LED Driver Enable Pin. If pulled up to an off PMIC supply, ensure voltage is less than VAO for low leakage in Ship Mode & Deep Sleep.
F4	nIRQ	Open-Drain Interrupt Output. nIRQ goes low to indicate a fault condition and remains low until the appropriate Status Register is read to clear the interrupt flag.
F5	VREF	Reference voltage output for ADC temperature measurement circuit. Connect to top of Resistor-NTC voltage divider to VBAT_NTC pin. Do no power external circuitry from this pin. Decouple with appropriate capacitor.
F6	VBAT_CSN	Battery Charger Current Sense Amplifier Negative Input Pin. Kelvin connect to negative side of battery current sense resistor.
G2	LED0	Low-side LED Driver Pin
G3	LED1	Low-side LED Driver Pin
G4	LED2	Low-side LED Driver Pin
G5	LED3	Low-side LED Driver Pin

ABSOLUTE MAXIMUM RATINGS NOTE1

PARAMETER	VALUE	UNIT
VIN_USB, VIN_WRLS, VHS, SW_SYS	-0.3 to 23	V
VSYS_BOOT	-0.3 to 28	V
VSYS_BOOT to VSYS_SW	6	V
EN_X, PG_VIN, nIRQ, nPB_DET, PB_IN, SHIP_MODE, LEDx, CHRG_DIS	-0.3 to VAO + 0.3	V
AGND to PGND	-0.3 to 0.3	V
All Other Pins	-0.3 to 6	V
Junction to Ambient Thermal Resistance (θ_{JA}), Note2	TBD	°C/W
Operating Junction Temperature (T_J)	-40 to 150	°C
Operating Ambient Temperature Range (T_A)	-40 to 85	°C
Store Temperature	-55 to 150	°C
Lead Temperature (Soldering, 10 sec)	300	°C
Electrostatic Discharge (HBM)	2	kV
Electrostatic Discharge (CDM)	500	V

Note1: Do not exceed these limits to prevent damage to the IC. Exposure to absolute maximum rating conditions for long periods may affect IC reliability.
Note2: Measured on Qorvo Evaluation Kit

ELECTRICAL CHARACTERISTICS – SYSTEM CONTROL

(VHS = 5V, VAO = 5V, T_J = -40°C to +125°C, unless otherwise specified)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Operating Voltage Range – VIN_USB	VIN_USB		4.0		5.75	V
Operating Voltage Range – VIN_WRLS	VIN_WRLS		4.0		13.0	V
Operating Supply Current, Charging Input Present, NOTE1		VIN_X present, VSYS regulator & LDOs enabled & unloaded, Battery present, LEDs off, ADC Enabled		2.28	2.50	mA
		VIN_X present, VSYS regulator & LDOs enabled & unloaded, Battery present, LEDs off, ADC Disabled		1.40	1.50	mA
Operating Supply Current, Battery Powered, NOTE1		VIN_X not present, VSYS = VBAT= 3.5 V, LDOs enabled & unloaded, Battery present, LEDs off, ADC Disabled, T_J = -40 °C to 85 °C	0.1	0.19	0.42	mA
Operating Supply Current, SHIP_MODE		VIN_X not present, VSYS = GND, LDOs enabled & unloaded, Battery present, LEDs off, I2C off, ADC Disabled, VBAT = 3.5V, T_J = -40 °C to 85 °C	2	10	40	µA
Operating Supply Current, DEEP_SLEEP_MODE		VIN_X not present, VSYS = GND, LDOs Off, Battery present, LEDs off, I2C off, ADC Disabled, VAO on, VBAT = 3.5V, T_J = -40 °C to 85 °C	2	7.5	20	µA
Thermal Shutdown Temperature, NOTE1	$T_{SD\_SHUTDOWN}$		140	155	170	°C
Thermal Shutdown Hysteresis, NOTE1				15		°C
Thermal Shutdown Deglitch, NOTE1			80	100	120	µs
Thermal Warning Interrupt Threshold, NOTE1	T_{SD_ALERT}	$T_{SD\_SHUTDOWN}$ – 30°C	115	120	125	°C
Thermal Warning Hysteresis, NOTE1				15		°C
Thermal Warning Deglitch, NOTE1			80	100	120	µs
Ship Mode Exit Delay, NOTE1					150	µs
Internal Oscillator Accuracy		4.5MHz Nominal	-5		5	%
VREF Voltage	VREF		1.773	1.8	1.827	V

NOTE 1: Guaranteed by design only. Estimated by simulations over process and voltage corners.

ELECTRICAL CHARACTERISTICS – LOW IQ LDOS

(VHS = 5V, VAO = 5V, T_J = -40°C to +125°C, unless otherwise specified)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
LDO1 Nominal Output Voltage	V_{OUT_LDO1}		1.2		3.3	V
LDO2 Nominal Output Voltage	V_{OUT_LDO2}		0.6		3.3	V
Output Voltage Step Size				50		mV
Output Voltage Accuracy	$V_{OUT\_LDO\_ACC}$	Normal mode	-1.5		1.5	%
		Ship mode	-2		2	
Load Regulation		I_{OUT} = 1mA to 80mA		2		%/A
Line Regulation		I_{OUT} = 1mA, VAO = 2.7 to 5V		0.02		%/V
Active Mode Supply Current	I_{LDO_ACTIVE}	Per LDO in Active Mode		3.2		µA
Ship Mode Supply Current	I_{LDO_SHIP}	Per LDO in Ship Mode		0.5		µA
Output Current	I_{LDO_OUT}				80	mA
Output Current Limit	I_{LDO_MAX}		90		140	mA
Dropout Voltage	V_{DO}	I_{OUT} = 80mA			250	mV
Power Good Threshold	LDO_{PG}	Rising, % of Nominal Voltage, nIRQ goes low	88	92	97	%
Power Good Hysteresis	LDO_{PG_HYS}	Falling		3		%
Overvoltage Fault Threshold	LDO_{OV_LDO1}	Rising % of Nominal Voltage	105	110	117	%
	LDO_{OV_LDO2}	Rising % of Nominal Voltage, if increase threshold is selected	109	112	119	%
Overvoltage Fault Hysteresis	LDO_{OV_HYST}	Falling		3		%
Discharge Resistance	LDO_{RDIS}	Turns on when regulator is disabled, VOUT = 0.1V, Note 1		40		Ω
Startup Slew Rate, NOTE1	LDO_{START_SLEW}	Note 1		4.5		V/ms
Power Supply Rejection Ratio, NOTE1	$PSRR_{LDO}$	f = 1kHz, I_{OUT} = 20mA, Nominal Output Voltage. Note 1		45		dB
Load Transient Regulation, NOTE1		V_{IN}-V_{OUT}>0.4V, V_{OUT} = 1.8V, I_{OUT} = 1mA to 80mA, t_{rise} = t_{fall} = 1µs		100		mV
Line Transient Response, NOTE1		V_{IN} = 2.5V to 5V, V_{OUT} = 1.8V, I_{OUT} = 1mA, Slew Rate = 1V/µs		20		mV
Output Capacitance	C_{OUT_LDO}	Without cap derating	1		22	µF

NOTE 1: Guaranteed by design only. Estimated by simulations over process and voltage corners.

ELECTRICAL CHARACTERISTICS – ACTIVE PATH SWITCHING CHARGER

(VHS = 5V, VAO = 5V, T_J = -40°C to +125°C, unless otherwise specified)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
VSYS Regulator Switching Frequency, NOTE1	V_{SYS_FSW}			2.25		MHz
VBAT_IN to VBAT FET Resistance		T_J = 25°C		12		mΩ
VIN_X to VHS FET Resistance		VIN_USB & VIN_WRLS, T_J = 25°C		50		mΩ
VHS to VSYS_SW FET Resistance		T_J = 25°C		95		mΩ
VSYS_SW to PGND FET Resistance		T_J = 25°C		75		mΩ
VSYS Over Current Limit		Cycle-by-Cycle current limit threshold	2.5			A
Preconditioning Charge Current	I_{PRE}	V_{VBAT} < V_{PRE}, Configurable	10	25	225	mA
Preconditioning Charge Current Step Size		10mA to 50mA step Size		5		mA
		50 to 225mA Step Size		25		mA
Fast Charge Current	I_{CHG}	V_{VPRE} < V_{VBAT} < V_{BAT}, Configurable	0.05	1	1.6	A
Fast Charge Current Step Size				25		mA
Fast Charge Current Accuracy	I_{CHG_ACC}	47mΩ, 1% Sense Resistor, 15°C to 45°C, 50mA to 65mA	-20		20	%
		47mΩ, 1% Sense Resistor, 15°C to 45°C, 75mA to 100mA	-10		10	%
		47mΩ, 1% Sense Resistor, 15°C to 45°C, 100mA to 1.5A	-5		5	%
End-of-Charge Current	I_{TERM}	V_{BAT} = V_{VBAT}, EOC Detection, Configurable	10	100	225	mA
End-of-Charge Current Step Size		10mA to 50mA step Size		5		mA
		50 to 225mA Step Size		25		mA
End-of-Charge Deglitch Time, NOTE1				750		ms
I_{TERM} Accuracy	I_{TERM_ACC}	47mΩ Sense Resistor, 20mA Setting	14.4	20.2	26.5	mA
		47mΩ Sense Resistor, 50mA Setting	45.6	50	55.4	mA
		47mΩ Sense Resistor, 150mA Setting	135	150	160	
Battery Termination Voltage	V_{TERM}	Configurable	3.6	4.25	4.55	V
Battery Termination Voltage Step Size				25		mV
Battery Termination Accuracy	V_{TERM_ACC}			99.5		%
Precondition Threshold	V_{PRE}	V_{VBAT} Rising, Configurable	2.8	3.2	3.55	V
Precondition Step Size				50		mV
Precondition Threshold Hysteresis	V_{PRE_HST}	V_{VBAT} Falling		0.1		V
Precharge Time Out Function, NOTE1		prechg_sel = 0, recalc for low IPRE		1		hr
		prechg_sel = 1, recalc for low IPRE		2		hr
Total Charge Time Out Function,		pchg_sel = 0		6		hr

NOTE1		pchg_sel = 1		9		hr
VSYS Regulator C_{OUT}		Min cap accounting for derating	6		48	µF
VSYS Output Voltage Range	V_{SYSL}	I_{VSYS} = 100mA, V_{VBAT} < V_{PRE}, Configurable	3.0		4.8	V
VSYS Output Voltage Step Size				50		mV
VSYS Regulated Voltage	V_{SYS_REG}	BATFET OFF relative to V_{TERM}, I_{VSYS} = 100mA		V_{TERM} + 300mV		V
VSYS Recharge Voltage	V_{SYS_RECH}	BATFET ON relative to V_{TERM}, I_{VSYS} = 100mA. 4 Options 00b – Recharge Disabled, 01b – 100mV, 10b –150mV, 11b – 200mV		V_{TERM} - 150mV		V
VSYS Maximum Voltage		Relative to VHS			VHS – 200mV	V
VSYS OVLO Threshold		VSYS Rising		5.1		V
VSYS OVLO Hysteresis			100	200	250	mV
Charger Efficiency, NOTE1		I_{CHG} = 0.5A, VHS = 5V, VSYS = 3.8		92		%
		I_{CHG} = 1.0A, VHS = 5V, VSYS = 3.8		88		%
Battery Short Circuit Detection	V_{SHORT}	VBATSHRT[0:1] = 00	1.9	2.0	2.1	V
		VBATSHRT[0:1] = 01	2.1	2.2	2.3	V
		VBATSHRT[0:1] = 10	2.3	2.4	2.5	V
		VBATSHRT[0:1] = 11	2.5	2.6	2.7	V
Battery Short Circuit Detection Hysteresis				100		mV
ISHORT Charge Current	I_{SHORT}			25		mA
NTC Battery Disconnect Threshold, NOTE1		NTC disconnect threshold is relative to VREF or T < -20°C for VREF = 1.8V	125	200	250	mV
NTC Detection Threshold, NOTE1	TZ1	0°C Voltage Threshold, VREF = 1.8V, 8.06kΩ Upper Resistor & 10kΩ, B25/85 = 3435K Thermistor		1.392		V
	TZ1-TZ2	10°C Voltage Threshold		1.245		V
	TZ2-TZ3	20°C Voltage Threshold		1.083		V
	TZ3-TZ4	40°C Voltage Threshold		0.758		V
	TZ4-TZ5	46°C Voltage Threshold		0.670		V
	TZ5	55°C Voltage Threshold		0.552		V
NTC Detection Temperature Hysteresis, NOTE1			2	3	4	°C
Temperature Measurement Accuracy, NOTE1	T_{ACC}	T = 0°C to 60°C	-1.5		1.5	°C
NTC Detection Deglitch Time, NOTE1				100		µs
Battery Detection Current, NOTE1	I_{BDSRC}	Pull Up Current		25		mA
	I_{BDSNK}	Pull Down Current		2.5		mA
VSYS Short Circuit Detection Threshold		VBAT-VSYS		320		mV

Supplement Mode Threshold	$V_{SUP,ENTER}$	VBAT-VSYS, need bit to disable VSYS regulator and force Sup Mode		50		mV
	$I_{SUP,EXIT}$	Battery discharge current threshold to exit Supplement Mode		30		mA
Battery Current Limitation		Only while in supplement mode		2		A
Thermal Regulation Temperature, NOTE1	$TSNS_{REG}$		100	120	140	°C
USB Input Charge Current Limit		Configurable – each option is the MAX value of the setting not TYP	0.5		2	A
USB Input Charge Current Limit Step Size				0.5		A
USB Input Charge Current Limit Accuracy		Setting = 0.5A, T_J = 15°C to 45°C	450		505	mA
Wireless Input Charge Current Limit		Configurable – each option is the MAX value of the setting not TYP	0.1		1	A
Wireless Input Charge Current Limit Step Size				50		mA
Wireless Input Charge Current Limit Accuracy		Setting = 100mA, T_J = 15°C to 45°C	90		100	mA
VIN_USB OVP Threshold, Rising		Falling Threshold is 100mV lower.		6		V
VIN_USB UVP Threshold, Falling		Rising Threshold is 100mV higher.		4.5		V
VIN_WRLS OVP Threshold, Rising		Falling Threshold is 100mV lower.		6		V
VIN_WRLS UVP Threshold, Falling		Rising Threshold is 100mV higher.		4.0		V
VIN_x OV, UV Comparator Rising Edge Deglitch Time, NOTE1		V_{IN_USB} & V_{IN_WRLS}		10		µs
VIN_x OV, UV Comparator Falling Edge Deglitch Time, NOTE1		V_{IN_USB} & V_{IN_WRLS}		1000		µs

NOTE 1: Guaranteed by design only. Estimated by simulations over process and voltage corners.

ELECTRICAL CHARACTERISTICS – LED DRIVER

(VHS = 5, VAO = 5V, T_J = -40°C to +125°C, unless otherwise specified)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
ISINK Range	I_{LED_SINK}	ILEDX [2:0]	0		25.5	mA
ISINK Step Size	I_{LED_STEP}	8-bit control needed		0.1		mA
PWM Duty Cycle Control, NOTE1			0		100	
PWM Duty Cycle Step Size, NOTE1	T_{LED_Step}	8-bit control needed, assuming 255 steps at 250ms period	1			ms
PWM Period Step Size, NOTE1				250		ms
Standby supply current, NOTE1	I_{VDD}	EN = 0 (pin), CHIP_EN = 0 (bit)		0.2	2	µA
		EN = 1 (pin), CHIP_EN = 0 (bit)		2		µA
		EN = 1 (pin), CHIP_EN = 0 (bit)		2.4		µA
Normal Mode Supply Current, NOTE1		LED drivers enabled		0.45		mA
Shipe Mode Supply Current, NOTE1				0.25		µA
Internal Oscillator Frequency Accuracy			-5		5	%
LED0, 1, 2, 3 Leakage Current	$I_{leakage}$	T_A=25ºC		0.1	1	µA
Maximum Source Current		Outputs R, G, B, W		25.5		mA
Output Current Accuracy	I_{OUT}	Output current set to 17.5 mA, VDD = 3.5V	16	17.5	18.5	mA
Matching	I_{match}	Output current set to 17.5 mA, VDD = 3.6 V		99		%
LED PWM Switching Frequency	f_{LED}	PWM_HF = 1		512		Hz
		PWM_HF = 0		256		Hz
Saturation Voltage, NOTE2	V_{SAT}	Output current set to 17.5 mA TA = 25°		70	100	mV

NOTE 1: Guaranteed by design only. Estimated by simulations over process and voltage corners.
NOTE 2: Saturation voltage is defined as the voltage when the LED current has dropped 10% from the set value

ELECTRICAL CHARACTERISTICS – LOGIC PINS

(VHS = 5V, VAO = 5V, T_J = -40°C to +125°C, unless otherwise specified)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Enable, CHRGDIS, & SHIP_MODE Pins						
Input Low Threshold	V_{ILO}	LDO1 = 1.8 V			0.54	V
Input High Threshold	V_{IHI}	LDO1 = 1.8 V	1.26			V
Deglitch Time, NOTE1		Rising & Falling Edges		1	30	µs
Internal Pullup Resistance to VAO, NOTE2		Resistors can be turned on/off. Fail safe and back-to-back switch. EN_X and CHRG_DIS. No pullup on SHIP_MODE		100		kΩ
Internal Pulldown Resistance, NOTE2		Pull down AGND, CHRG_DIS pin only		100		kΩ
Input Leakage Current	I_{GPIO_LEAK}	T_J = 25°C, Pull-up R disabled. Pullup voltage on pins should be less than VAO.	-1		1	µA
nIRQ & nPB_DET Pins						
Output Low Voltage	V_{OL}	Sink Current = 5 mA			0.4	V
High Level Leakage Current	I_{OH}	Output = 5 V, T_A = 25 °C			1	µA
Push Button Input						
Input Low Threshold	$V_{ILO,PB}$	VAO = 5 V			0.54	V
Input High Threshold	$V_{IHI,PB}$	VAO = 5 V	1.26			V
Master Reset Rising Threshold		PB_IN Rising		0.75		V
Internal Pulldown Resistance, NOTE1,2		Pull down to AGND		100		kΩ
De-bounce Time, NOTE1		Presses shorter than this time are ignored		50		ms
Button Hold Detection Time, NOTE1	T1	Hold time after initial button pressed before signaling on nPB_DET.		15		s
Button Hold Low Pulse, NOTE1	T2	nPB_DET Pulse Length After T1, length fine-tuned with external cap		100		µs
Power Cycle Press & Hold Time, NOTE1	T3		30			s
Post Power Cycle Pulse, NOTE1	T4	nPB_DET Pulse Length after Power Cycle		500		ms
Time Measurement Accuracy, NOTE1		T1, T3, & T4	-5		5	%

NOTE 1: Guaranteed by design only. Estimated by simulations over process and voltage corners.
NOTE 2: Pull up and down components are a fixed resistor

ELECTRICAL CHARACTERISTICS – INTERNAL LOW POWER (ALWAYS ON) LDO, VAO

(VHS = 5V, T_J = -40°C to +125°C, unless otherwise specified)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Operating Voltage		VBAT, VIN_USB, or VIN_WRLS supply	2.5		5	V
Output Voltage Range		5Vnom unless running off a supply less than drop out voltage	2.5	5		V
Maximum VAO Output Current	$I_{VAO,MAX}$		180			mA
Output Voltage Accuracy		I_{OUT} = 5mA, VIN > VOUT+ 0.25V	-1.5		1.5	%
Line Regulation		I_{OUT} = 5mA		0.6		%
Load Regulation		I_{OUT} = 0.1 to 20mA		0.6		%
Dropout Voltage		I_{OUT} = 160mA		200		mV
Current Limit, NOTE1		V_{OUT} = 95% of Regulation Voltage		220		mA
Undervoltage	UV_{VAO}	Falling		2.36		V
		Rising		2.51		
Undervoltage Deglitch				10		us
Power-on-Reset, NOTE1	POR_{VAO}	Rising		2.29		V
		Falling		2.2		V

NOTE 1: Guaranteed by design only. Estimated by simulations over process and voltage corners.

ELECTRICAL CHARACTERISTICS - ADC

(VHS = 5V, VAO = 5V, T_J = -40°C to +125°C, unless otherwise specified)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Total Error, NOTE1	$A2D_{ERROR}$	12 Bit Range			2.5	LSB
Total Conversion Time, NOTE1		All 8 Chanels			140	ms
Supply Current	$A2D_{IQ}$	8ms Conversion Time		0.5		mA
Single Channel Conversion Time, NOTE1	$A2D_{tCON}$	Single Channel, Selectable conversion time options of 8/16/32/64 ms		8	15	ms
Input Capacitance, NOTE1	A2DCIN			5		pF
A2D T_{BAT} Range, NOTE1	$A2D_{TBAT}$	Battery Temp Channel 1, reported in °C, Ratio 1:1	-40		150	°C
A2D Battery Charge/Discharge Current, NOTE1	$A2D_{ICHRG}$	Battery Charge/Discharge Current, Channel 3, Ratio 1:1, Muxed signal from bidirectional sense block. No readings in Short or Precharge Mode	0		1.8	V
A2D VIN_USB Range, NOTE1	$A2D_{VUSB}$	USB Input Voltage Reading, Channel 5, Ratio 10:1	0		18	V
A2D VIN_WRLS Range, NOTE1	$A2D_{VWRLS}$	Wireless Input Voltage Reading, Channel 6, Ratio 10:1	0		18	V
A2D VBAT Range, NOTE1	$A2D_{VSYS}$	VBAT Voltage Reading, Channel 7, Ratio 10:1	0		18	V
A2D IIN Range, NOTE1	$A2D_{IIN}$	Input Current Reading, Channel 8, Ratio 1:1, Muxed signal from current charging source (VIN_WRLS or VIN_USB)	0		1.8	V

NOTE 1: Guaranteed by design only. Estimated by simulations over process and voltage corners.

CHANNEL	EQUATION	UNIT
CH1 – Battery Temperature	$T_{BAT} = -1.5543e^{-15} * a^5 + 1.6965e^{-11} * a^4 - 7.3136e^{-8} * a^3 + 1.5691e^{-4} * a^2 - 0.197 * a + 162.18$, Full Temp Range $T_{BAT} = -2.628e^{-9} * a^3 + 1.854e^{-5} * a^2 - 0.06971 * a + 118.6$, 0 to 60°C Temp Range	°C
CH2	Unused	
CH3 – Battery Charge/ Discharge Current	$I_{CHARGE} = 0.4675 * a$	mA
CH4	Unused	
CH5 – VIN_USB Voltage	$VIN_{USB} = 439.45e^{-5} * a$	V
CH6 – VIN_WRLS Voltage	$VIN_{WRLS} = 439.45e^{-5} * a$	V
CH7 – VBAT Voltage	$VBAT = 439.45e^{-5} * a$	V
CH8 – Input Current	$IIN = 0.5859 * a$	mA
$a = hex2dec(ADC_{DOUT}[11:0])$		

ELECTRICAL CHARACTERISTICS - I²C INTERFACE

(VHS = 5V, VAO = 5V, T_J = -40°C to +125°C, unless otherwise specified)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
SCL, SDA Input Low	V_{ILO}	LDO1 = 1.8V			0.54	V
SCL, SDA Input High	V_{IHI}	LDO1 = 1.8V	1.26			V
SDA Leakage Current, NOTE1	I_{OH}	SDA = 5V, T_J = 25°C			1	µA
SDA Output Low, NOTE1	V_{OL}	I_{OL} = 5mA			0.4	V
SCL Clock Frequency, NOTE1, NOTE1	f_{SCL}		0		1000	kHz
SCL Low Period, NOTE1	t_{SCL_LOW}		0.5			us
SCL High Period, NOTE1	t_{SCL_HI}		0.26			us
SDA Data Setup Time, NOTE1	t_{SU}			29.4		ns
SDA Data Hold Time, NOTE1	t_{HD}			25.7		ns
Start Setup Time, NOTE1	t_{ST}			28.0		ns
Stop Setup Time, NOTE1	t_{SP}			18.3		ns
Capacitance on SCL or SDA PIN, NOTE1	C_{IN}				10	pF
Noise suppression on SCL and SDA, NOTE1	$t_{DEGLITCH}$			49.7	67.9	ns
I²C Timeout Function, NOTE1	t_{out}	Total time required for I²C communication to cause I²C state machine to reset		100		ms

NOTE 1: Guaranteed by design only. Estimated by simulations over process and voltage corners.
NOTE 2: Comply with I2C timings for 1MHz operation - “Fast Mode Plus”.
NOTE3: I2C communication state machine will be reset when entering Shipping Mode State.
NOTE4: This is an I2C system specification only. Rise and fall time of SCL & SDA not controlled by the IC.
NOTE5: IC Address is configurable to 46h (Default), 47h, 48h, and 49h.

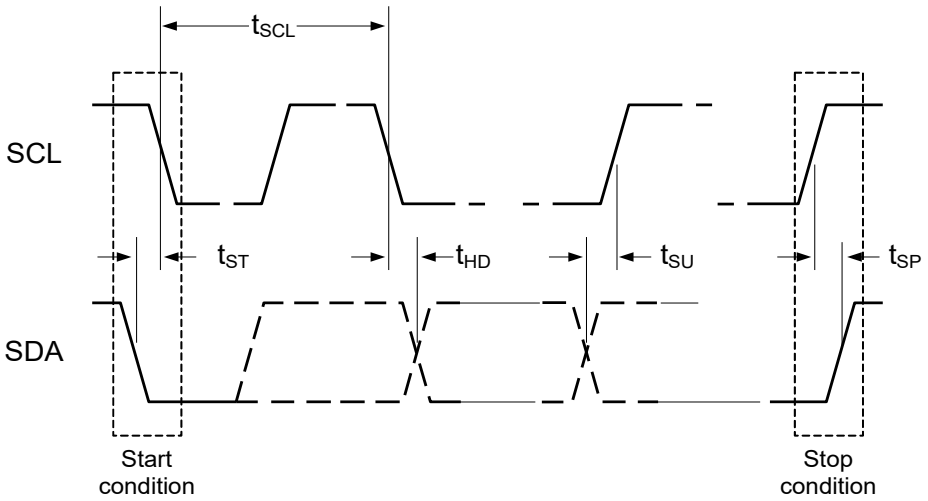
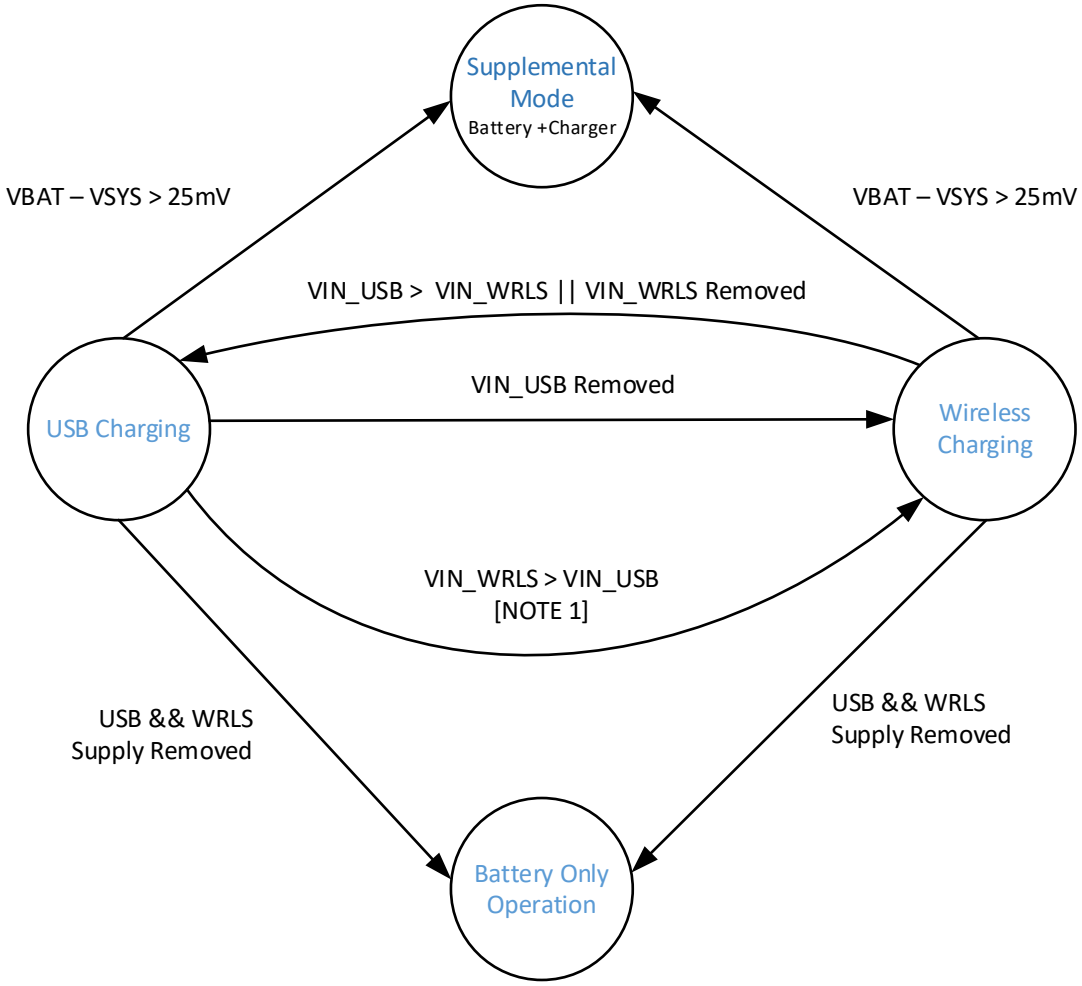


Figure 4: I2C Data Transfer

1 INPUT SELECTION STATE MACHINE



NOTE1: nIRQ Interrupt toggles low to alert MCU or system processor if VIN_WRLS > VINUSB

NOTE2: If VIN_WRLS is present while VIN_USB is charging the battery, there will be a 1ms pause in charging to account for the debounce time on VIN_WRLS under voltage detection circuitry

Figure 5: Input Selection State Machine

2 ACTIVE-PATH SWITCHING CHARGER DESCRIPTION

2.1 General Description

The ACT82120 contains an Active Power-Path Switching Charger (APSC) which is a full-featured active power-path selectable switching charger for Lithium-based cells. It incorporates the Active-Path Switching technology which integrates a switch mode converter, a battery FET, and control circuitry to choose the best available supply (priority on highest voltage input) for hand-held portable equipment.

When either VIN_USB or VIN_WRLS is present, the APSC will regulate the system voltage, monitored on VSYS_SNS, via the high-efficiency switch mode converter. Depending on the state of the connected battery, the JEITA compliant charge controller will adjust the charge current appropriately to safely charge the battery. Once the battery has reached full charge, the BATFET is turned off to disable charging and the charge controller waits for battery voltage to drop below a programmable threshold before recharging. Since the full charging profile is programmable, there is an option available to keep the BATFET on once an end of charge state is reached keeping the battery connected to the system voltage. After a charge cycle is completed, the charge controller can supplement the switching regulator if any time during operation the VSYS load current demands exceed the current limit of the switching regulator.

The APSC inside the ACT82120 monitors seven feedback loops to maintain optimal charging performance over the entire charge cycle.

1. Constant Current (CC)
2. Constant Voltage (CV)
3. Minimum System Voltage
4. Input Current
5. Input Voltage
6. Die Temperature
7. Cycle by Cycle Current Limit

2.2 Control

The ACT82120 input power is supplied to the PMIC from two possible inputs, VIN_USB and VIN_WRLS, either of which can independently power the PMIC. An ideal diode circuit is used to pass the sources to the input of the VSYS switching regulator. The input selection circuitry protects against reverse currents when both sources are present in the system while also providing voltage protection to 23V. Should VIN_USB fall below VIN_WRLS, the nIRQ interrupt is asserted and a status register is updated to notify the host microcontroller so a decision to switch charging inputs can be made. Telemetry of the battery voltage and temperature, sensed via NTC resistor, can be read by the host processor over I2C.

2.3 Charging

The ACT82120 APSC has an internal battery charging circuit which includes a 20mΩ VBATFET and a charging profile configured by internal NVM registers which runs autonomously when enabled. The input voltage to the charger comes from switching regulator output, VSYS. The default charging profile can be fine-tuned to accommodate different battery chemistries and spans five temperature zones, each having separate V_{TERM}, and I_{FAST} settings. Additionally, the thresholds for each temperature zone are adjustable as well through I2C after the system is powered up. Interrupts to the host processor are generated from any of the following changes in charging state:

1. JEITA Temp Threshold Crossed
2. Charging Mode Change – From Short to Pre, Pre to CC, CC to CV, CV to End-of-Charge
3. Battery Voltage Low
4. Battery Removed/Inserted
5. Charge Source Plugged/Unplugged

Conditions 1 and 2 above allow for On-the-Fly adjustments of the charging profile from an external MCU or processor as described in the

On-the-Fly (OTF) Charge Profile Changes Section below. The charger state machine can regulate either a constant battery voltage, constant battery current, constant charger current, or a minimum charger voltage drop.

Example Single Step Charging Profile within a Temperature Zone (**Figure 6**):

1. Short charge current, I_{SHORT}, from 0.0V to Battery Short Voltage, V_{SHORT}.
2. Precondition charge current, I_{PRE}, from Battery Short to Precharge Voltage, V_{PRE}.
3. Regulate in Fast Charge, CC Mode at I_{FAST} Current Level until reaching the End-of-Charge threshold, V_{TERM}.
4. Finish charging cycle maintaining V_{TERM} using the I_{TERM} Termination Charge Current Level.
5. Toggle nIRQ Interrupt to End of Charge to external MCU.

Note that when using the setting VSYS = VTERM + 300mV setting called out in **Figure 6**, a full battery charge to 4.55V is not possible should VIN_USB be at the 4.75V minimum called out in the USB Specifications.

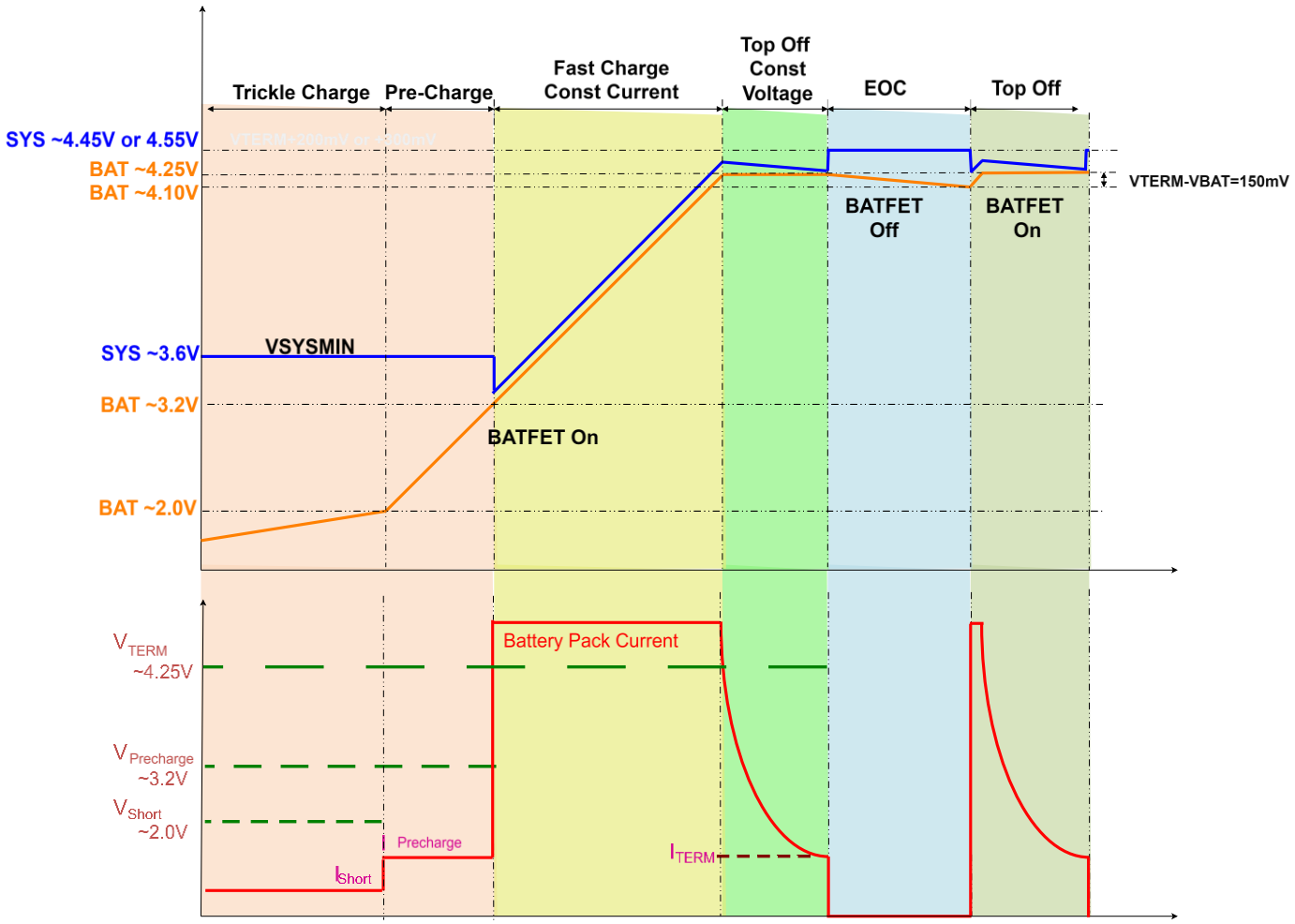


Figure 6: Charging Profile within a Single Temperature Zone

2.4 Thermal Monitoring and Temperature Zones

The voltage on VBAT_NTC pin tracks the battery temperature through an NTC resistor divider from VREF as shown in **Figure 7**. This voltage is then digitized through a 12-bit Delta Sigma ADC and compared against the adjustable temperature zone thresholds stored in NVM. Dedicated comparators monitor the VBAT_NTC voltage to trigger fault protection circuitry if the battery temperature goes below the TZ01 threshold, or above the TZ56 threshold. These

comparators ensure the battery is always protected from extreme temperatures, regardless of if the ADC is active or not.

The monitoring circuit is designed to work with a NTC that has a nominal resistance of 10kΩ at 25°C with a B25/50 of 3380K such as ERT-J0EG103FA from Panasonic. At startup, the ACT82120 checks the voltage on the VBAT_NTC pin to determine the presence of a battery, and which temperature zone is appropriate for charging. Should the voltage on VBAT_NTC be greater than ≈1.6V, a battery connection fault is issued.

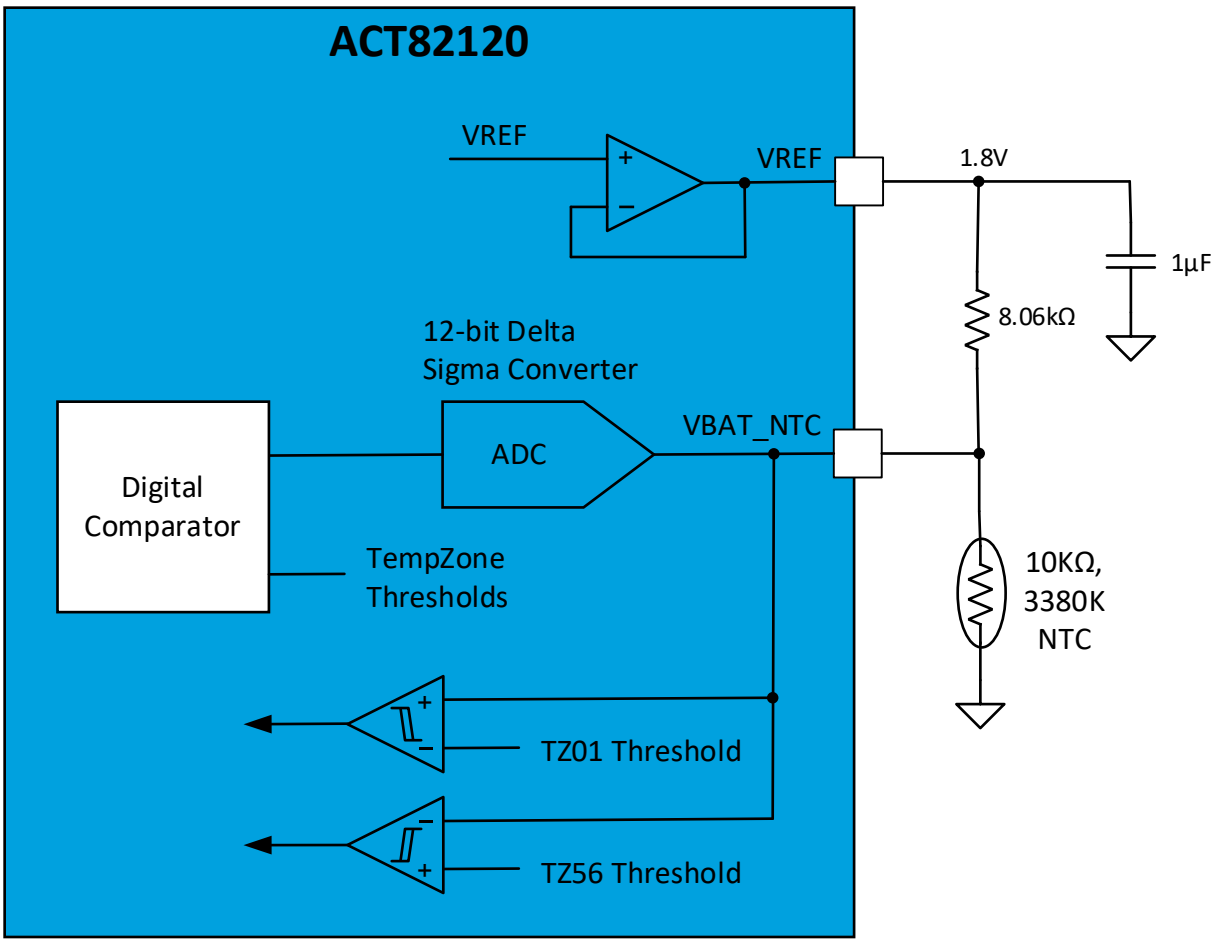


Figure 7: Internal Temperature Monitoring Circuitry

A JEITA Charging Profile example is shown in **Figure 8**. Each of the five temperature zones has a configurable temperature threshold, termination voltage (V_{TERM}), and fast charge current (I_{FAST}) parameters allowing for a custom charge profile to accommodate different battery chemistries. At temperatures below TZ1 and above TZ5 charging is suspended to protect the battery.

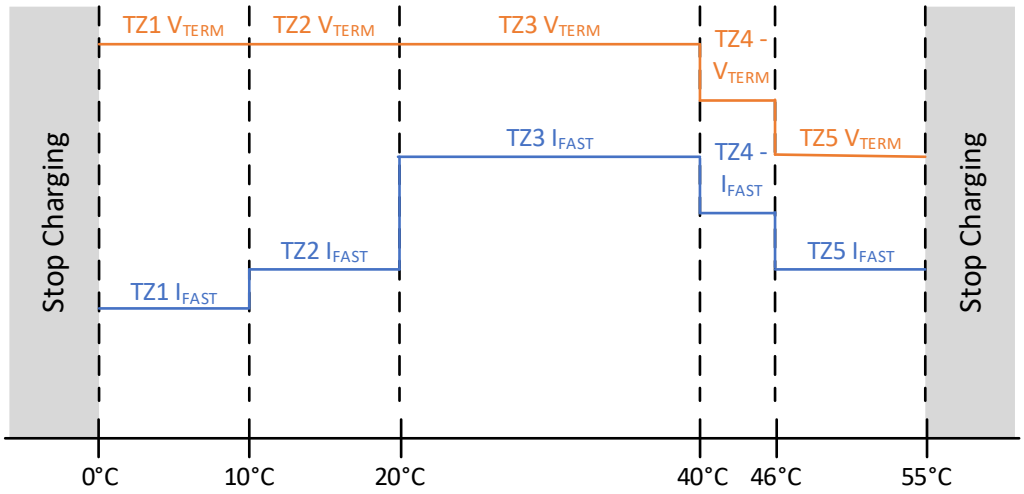


Figure 8: Example JEITA Charging Profile

2.5 On-the-Fly (OTF) Charge Profile Changes

During normal operation the ACT82120 can operate its charging profile independently though the NVM register settings. However, for applications that require multi-step charging, or externally controlled charging algorithms, On-the-Fly changes can be written via I2C to three volatile memory registers controlled V_{TERM}, I_{TERM}, and I_{FAST}. When these registers are written to from an external MCU, the PMIC will update the regulation settings for the charger appropriately and continue charging the battery. As the battery temperature crosses temperature zones, a delay timer, TQUAL, can be set to allow time for the MCU to send OTF changes before the NVM settings for the new temperature zone take effect. If the MCU doesn't write to the OTF registers before TQUAL expires, then the NVM settings for the new temperature zone are used for the charging profile.

Table 1 to **Table 3** below give an overview of the default and On-the-Fly registers available to adjust the charging profile. The Temperature Zone Thresholds and default charging profile per zone are stored in NVM and active once the ACT82120 powers up. Registers associated with On-the-Fly functionality are kept in volatile memory. In the event of TQUAL expiring, or communication loss with the MCU the charging profile stored in NVM for the current temperature zone will be used.

Note that if the base I_{CHARGE} in NVM is set to the minimum fast charge current of 50mA, the PMIC will charge at 50mA in all Temperature Zones without any scaling.

Table 1: On-the-Fly Charge Profile Registers

I_FAST_OTF (VM)							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Reserved		Fast Charge Current – 0.05A to 1.5A in 25mA Steps					
VTERM_OTF (VM)							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Reserved		Termination Voltage – 3.60V to 4.55V in 25mV Steps					
ITERM_OTF (VM)							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Reserved				Termination Current - 10mA to 50mA in 5mA Steps, 50mA to 200mA in 50mA Steps Applies to all Temp Zones			

Table 2: Default NVM Backed Charging Profile Registers

ICHG (NVM)							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Reserved		Fast Charge Current – 0.05A to 1.5A in 25mA Steps					
VTERM (NVM)							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Reserved		Termination Voltage – 3.60V to 4.55V in 25mV Steps					
ITERM (NVM)							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Reserved				Termination Current - 10mA to 50mA in 5mA Steps, 50mA to 200mA in 50mA Steps Applies to all Temp Zones			

Table 3: NVM Backed Temperature Zone Configuration Registers

Temp Zone Config Register 1							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
ICHG_TZ1 00b: 0.125*I_CHG 01b: 0.250 10b: 0.375 11b: 0.500		**ICHG_TZ2** 00b: 0.375*I_CHG 01b: 0.500 10b: 0.625 11b: 0.750		**ICHG_TZ3** 00b: 0.875*I_CHG 01b: 1.000 10b: 1.125 11b: 1.500		**ICHG_TZ4** 00b: 0.500*I_CHG 01b: 0.625 10b: 0.750 11b: 0.875	
Temp Zone Config Register 2							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
ICHG_TZ5 00b: 0.125*I_CHG 01b: 0.250 10b: 0.375 11b: 0.500		**VTERM_TZ1** 00b: VTERM + 0mV 01b: -100mV 10b: -200mV 11b: -300mV		**VTERM_TZ2** 00b: VTERM + 0mV 01b: -100mV 10b: -200mV 11b: -300mV		**VTERM_TZ3** 00b: VTERM + 0mV 01b: -100mV 10b: -200mV 11b: -300mV	
Temp Zone Config Register 3							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
VTERM_TZ4 00b: VTERM + 0mV 01b: -100mV 10b: -200mV 11b: -300mV		**VTERM_TZ5** 00b: VTERM + 0mV 01b: -100mV 10b: -200mV 11b: -300mV		**TempZone01** 00b: -4°C 01b: -2°C 10b: 0°C 11b: 2°C		**TempZone12** 00b: 6°C 01b: 8°C 10b: 10°C 11b: 12°C	
Temp Zone Config Register 4							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
TempZone23 00b: 16°C 01b: 18°C 10b: 20°C 11b: 22°C		**TempZone34** 00b: 36°C 01b: 38°C 10b: 40°C 11b: 42°C		**TempZone45** 00b: 44°C 01b: 46°C 10b: 48°C 11b: 50°C		**TempZone56** 00b: 53°C 01b: 55°C 10b: 57°C 11b: 60°C	

2.6 Charging State Machines

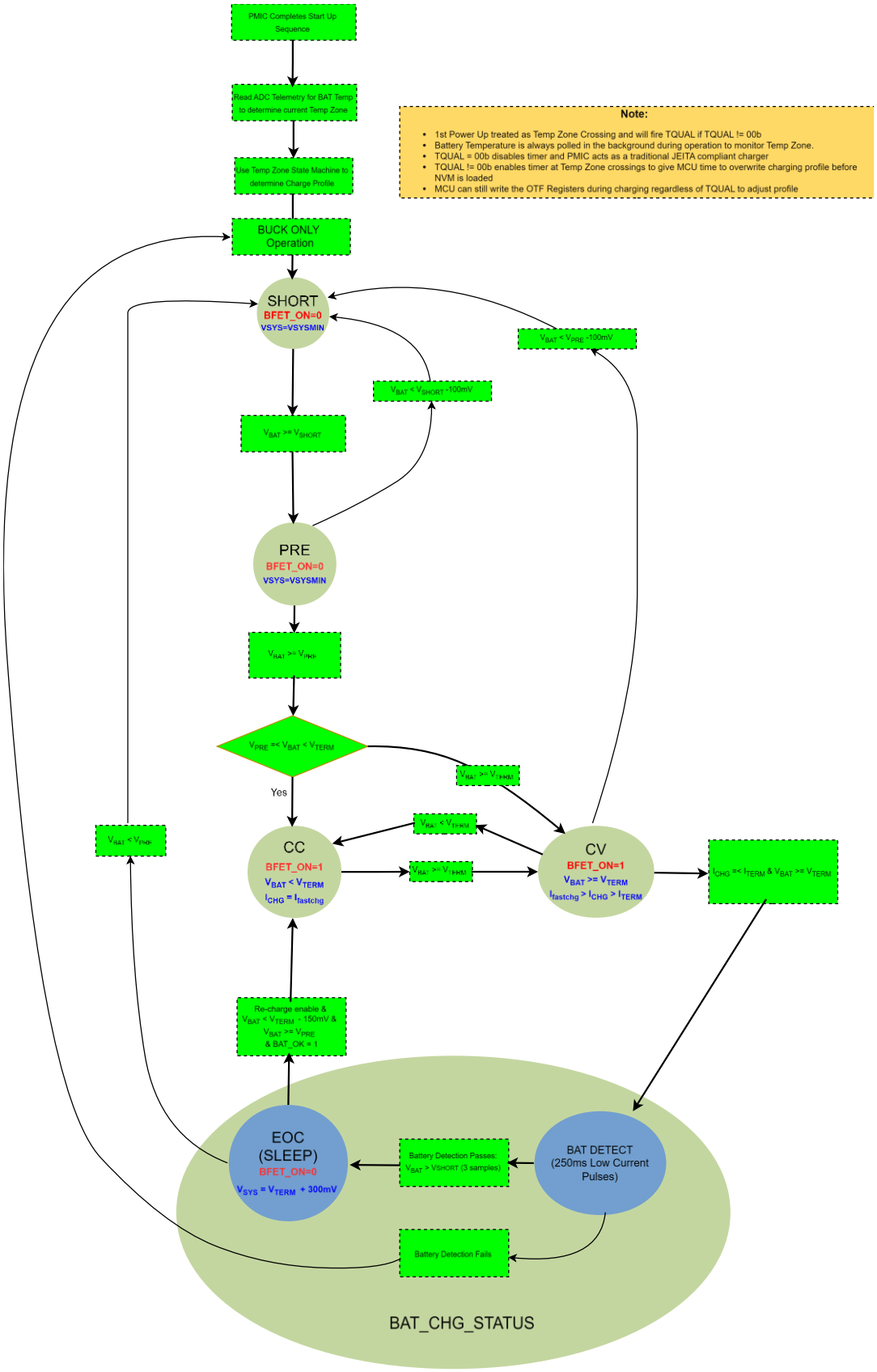


Figure 9: High Level Charging State Machine

Table 4: Battery Charge State & Status Descriptions

State	Entry Conditions
RESET	Battery only operation, APSC buck disabled through I2C, PMIC over temperature, VSYS OCP event, ON_BUCK = 0, or VIN_x fault
VBAT SHORT	Charging battery with the Short Charge Current Level
VBAT PRE	Charging battery with the Precharge Current Level
EOC (Sleep)	End of Charge (Sleep) – Battery is detected and VBAT is greater than the recharge threshold. BATFET is off
EOC (BDSNK or BDSRC)	End of Charge (Source or Sink) – 2.5 mA Source or Sink applied to VBAT for 250 ms to detect if a battery is present. Battery detected after 3 successful samples.
FAULT	Charger fault state entered after a charging timeout, battery temp too hot/cold, or battery OCP event occurs
CC FAST CHARGE	Charging Battery with the Fast Charge Current Level, adjusted for current Temp Zone
CV FAST CHARGE	Charging Battery in the Constant Voltage State
BUCK ONLY	Only the VSYS switcher is active, BATFET is off, and the battery is not charging. In this state briefly during PMIC startup, if CHRG_DISABLE pin is high, or a fault is cleared but charging hasn't resumed

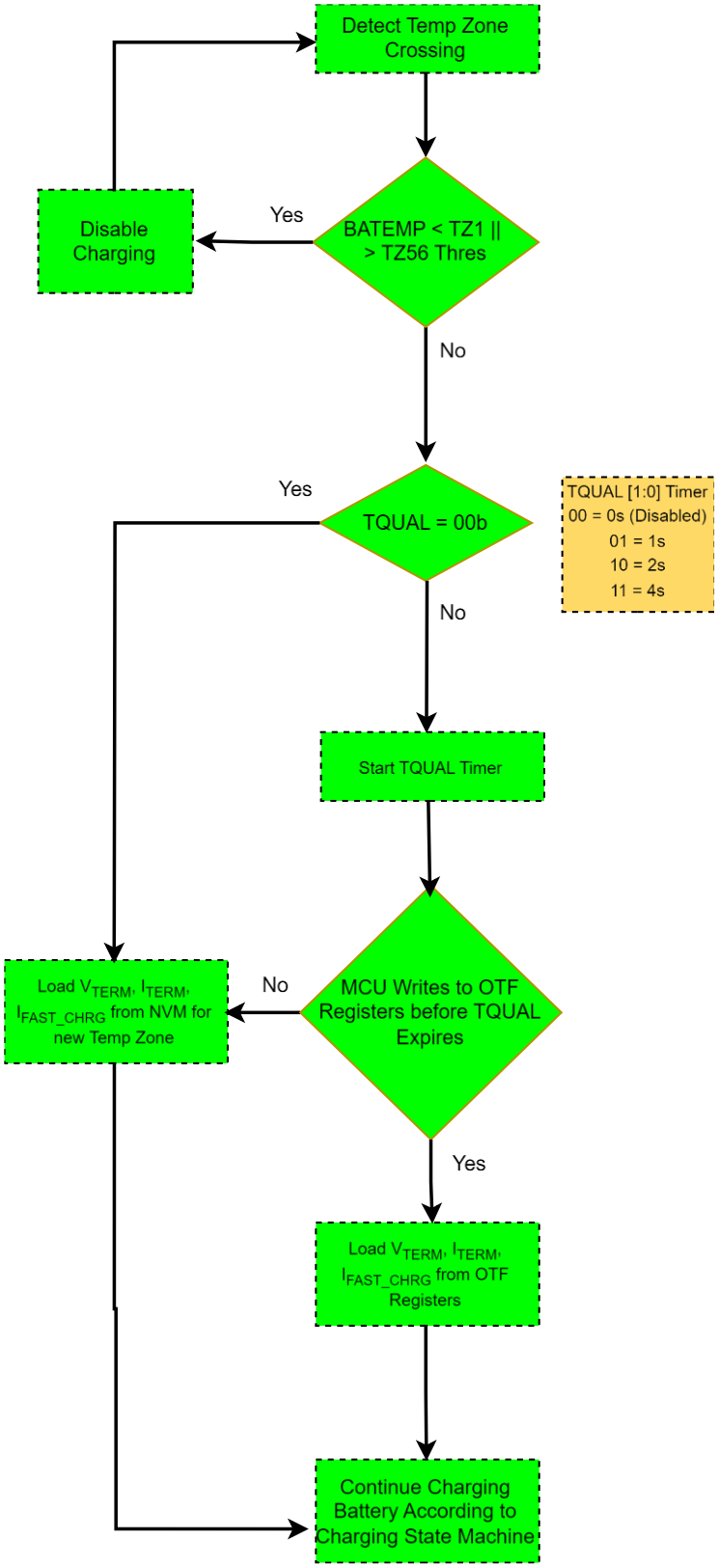


Figure 10: Temp Zone Crossing State Machine

2.7 Safety Timer & Fault Behavior

At the beginning of the charging process, the ACT82120 starts a safety timer which is active during the entire charging process. If charging has not terminated before the safety timer expires, the PMIC disables the charging path. The safety timer is configurable using the I2C interface. If an abnormal condition listed in **Table 5** occurs, the charger and timer take the corresponding action.

Table 5: APSC & Safey Timer Fault Response

Fault	APSC Response	Safety Timer Response
Input OV	Charging Suspended	Reset
Input UV	Charging Suspended	Reset
V_{SYS} < V_{BAT}	Charging Suspended	Paused
Thermal Shutdown	Charging Suspended	Reset
Battery Disconnected	Charging Suspended	Reset
Input Supply Dropout	Charge Current Reduced	Doubles
BAT Temperature Below Temp Zone 1 or Above Temp Zone 5	Charging Suspended	Reset
Thermal Regulation	Charge Current Reduced	Doubles

Should an error occur while the PMIC is charging the battery in either the CV or CC state, the chip will enter the TOFLT state and Bit[1] of Register 46h will get set high. In this state, charging is suspended, the BATFET is disabled, and the PMIC operates the charger in BUCKONLY Mode. To exit this state and resume charging, the system can write this bit back to 0 through I2C after it determines it is safe to do so.

2.7.1 Input Supply Dropout

The ACT82120 features an adaptive input undervoltage regulation level on both VIN_USB and VIN_WRLS. When the input voltage drops below this threshold, the PMIC stops switching the buck charger to throttle the battery charge current and reduce loading on the input source. The battery will continue to charge during this time at a reduced rate. Should the input voltage recover, normal charging at the desired current level will resume. Should the input voltage continue to drop with zero charging current, charging will be suspended when the voltage falls below the undervoltage threshold, triggering a fault condition.

Table 6: Input Supply Dropout Settings

VINLIM[1:0]	Input Undervoltage Threshold		
	VBAT < 3.8V	3.8V < VBAT < 4.05V	4.05V < VBAT
00	Disabled	Disabled	Disabled
01	4.25V	4.50V	4.60V
10	4.50V	4.50V	4.60V
11	4.60V	4.60V	4.60V

2.8 Supplement Mode

While running off a charging input, the ACT82120 can use the battery to provide supplemental current to VSYS during periods of heavy load. Assuming the battery is appropriately charged, when the VSYS voltage dips more than 50mV below the battery voltage the charger will turn on the BATFET and enter Supplement Mode. Once the high current load

is removed and the battery discharge current is below 30mA, the charger will exit Supplement Mode and resume normal operation

To avoid chattering in and out of Supplement Mode accidentally when a charging input is first plugged in, or reenabled after disabling, it's recommended to either set $VSYS_{MIN}$ ≥ VTERM or ensure a load greater than 30mA is present on VSYS.

3 PUSH BUTTON INPUT

The PB_IN pin connects to an external push button that connects the pin to the PMIC VAO supply when the button is depressed, as shown in **Figure 11**. Upon detecting a button press, the ACT82120 notifies the system MCU or processor via the nIRQ interrupt pin and I2C bus. Two possible scenarios for a system reset can occur as shown in **Figure 12** and **Figure 13** depending on the PMIC configuration. Note that these figures only give default values for each of the four timers, see **Electrical Characteristics – Logic Pins** table for more detailed information. To select between each of the reset behaviors, the PB_DISABLE_CONFIG and PB_WAITTIMER_T3 bits in the register map can be adjusted as needed.

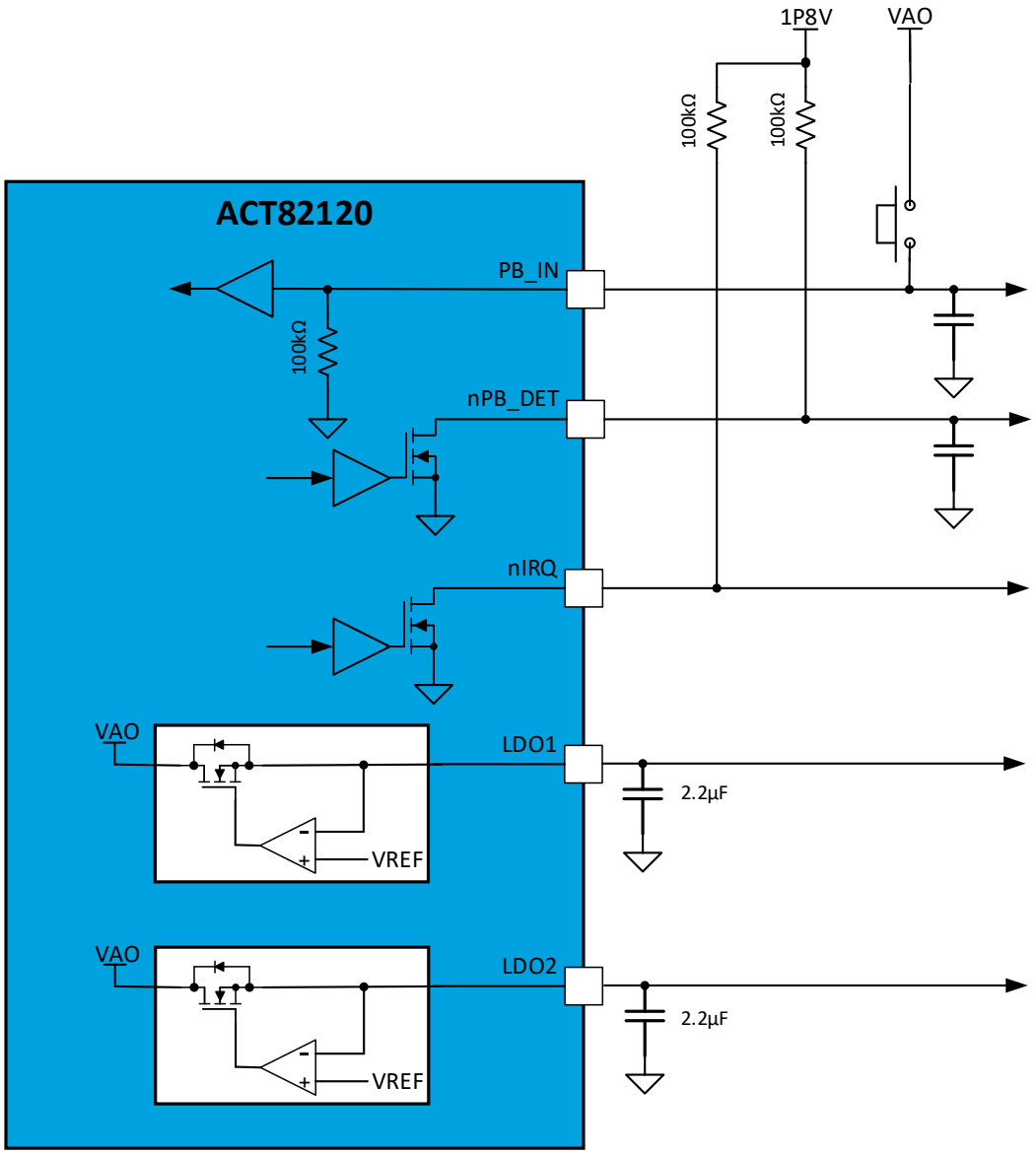


Figure 11: Push Button Detect Connections

The default push button behavior in **Figure 12** initiates a reset pulse to the MCU after timer T1 expires. nPB_DETECT first toggles low and then both LDO outputs are disabled and pulled down by their internal 40Ω discharge resistors.

nPB_DETECT and the LDOs will remain low until the push button is released while timer T2 sets the minimum reset time for the system. After the push button is released, both LDOs softstart and nPB_DETECT tracks the 1.8V LDO output. Note that if nPB_DETECT is holding the system MCU in a reset state, it cannot send the I2C commands needed to control the LED drivers and their program engines.

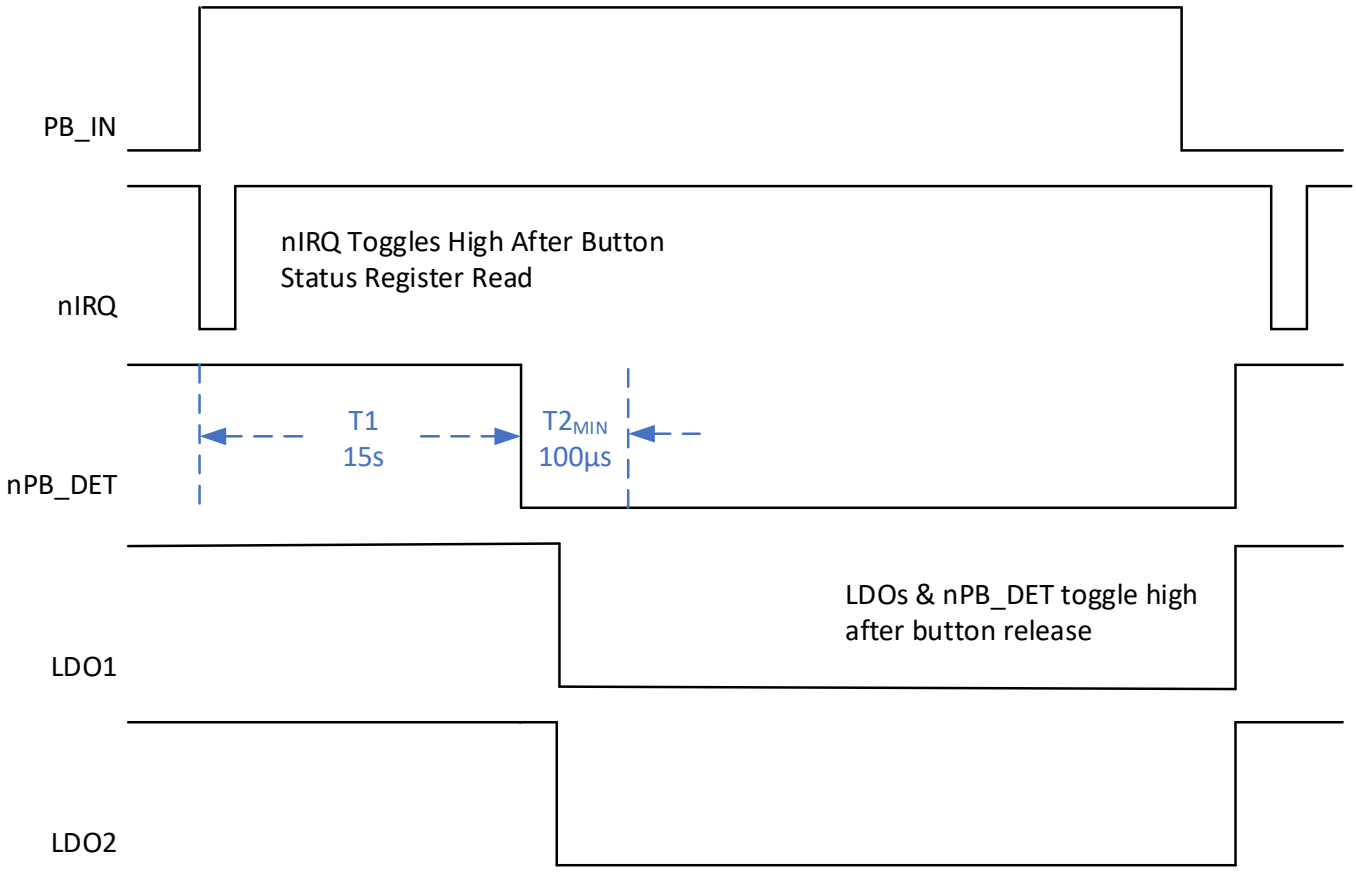


Figure 12: Default Push Button Detect Behavior

The second option for push button behavior in **Figure 13** enables timers T3 and T4 and generates a short pulse, the length of T2, on nPB_DETECT after T1 expires. Both LDOs are again shut down after the push button is held down for the length of T3. Timer T4 sets the duration of the LDO shutdown.

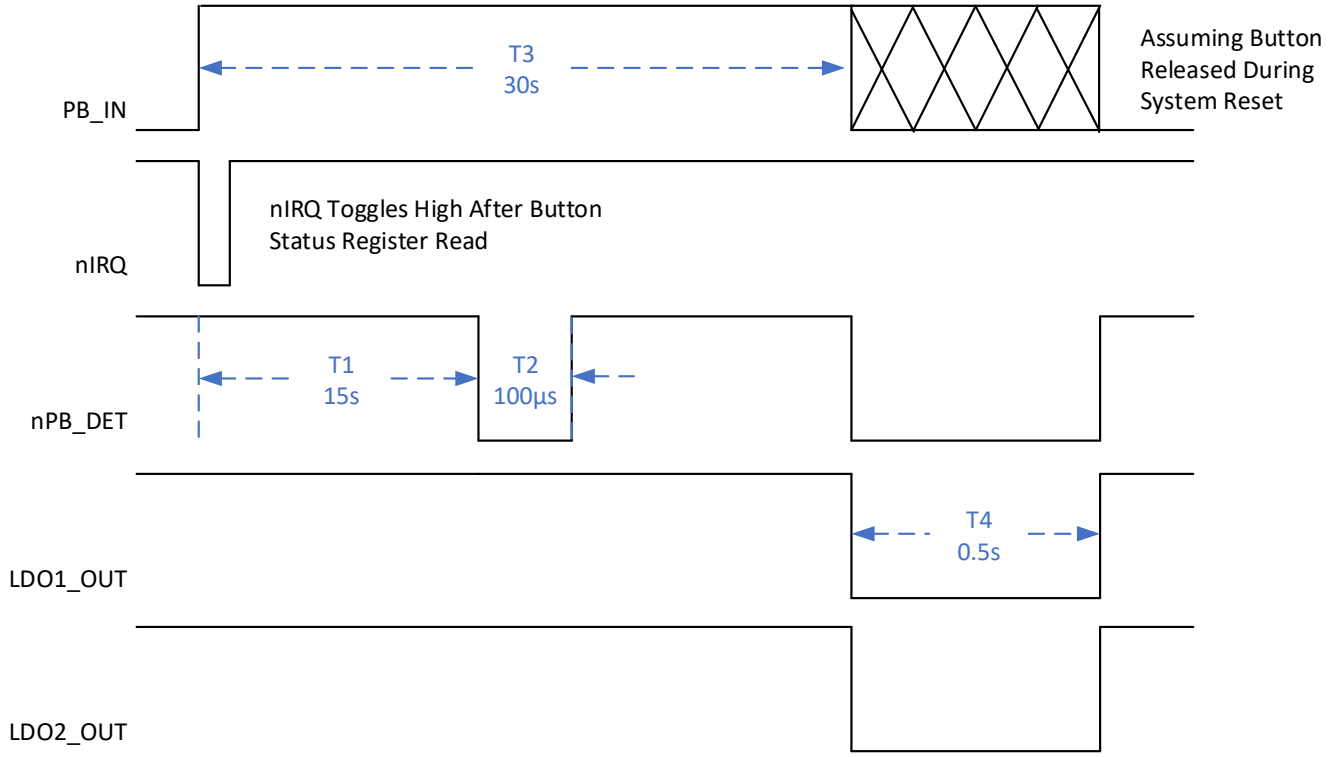


Figure 13: Push Button Detect Behavior with T3 Enabled

Should the LDOs need to be kept active during a push button reset, there is a configuration bit in the register map that can be set to only hold nPB_DET low instead. A continuous reset loop is avoided by monitoring the state of the button through the PB_IN pin. If the PMIC detects the button is still pressed after a reset occurs it won't initiate another reset until the button is released.

4 INTERRUPT EVENTS & FAULT RESPONSE

During operation, the ACT82120 will toggle the nIRQ interrupt pin and update the appropriate status registers for the following events shown in **Table 7.** The nIRQ pin will remain low until the appropriate status registers are read by the external MCU to clear the interrupt flag.

Note that in Ship Mode and Deep Sleep Mode, all interrupts are masked and nIRQ does not toggle low as internal oscillators are disabled to reduce current consumption.

Table 7: nIRQ Interrupt Events

Event	**Notes**
LDO1 – Over Voltage/Under Voltage/Over Current	Fault Condition
LDO2 – Over Voltage/Under Voltage/Over Current	Fault Condition
Push Button Press	Starts Timer for Push Button Functionality as shown in **Figure 13**
Push Button Release	
Charge Source Present/Removed	
Charge Source Over Voltage	Fault Condition
VIN_WRLS > VIN_USB	Switch to VIN_WRLS and signal to MCU so system level measures can be taken

Battery Removed/Inserted	
Battery Voltage Low	
End of Charge Reached	
Battery Temperature Zone Crossed	Battery temperature below TZ01 threshold or above TZ56 threshold is a fault condition.
60°C Battery Over Temperature	Warns MCU of excessive battery temperature
Battery Over Current	Fault Condition
V_{SYS} Over Voltage/Under Voltage/ Over Current	Fault Condition
PMIC Die Temperature Exceeds 125°C	Warns MCU of excessive PMIC temperature
PMIC Over Temperature	Fault Condition

For the fault conditions listed in **Table 7** the PMIC response for each is listed below in **Table 8**. During a fault event, the nIRQ pin toggles low and remains low until the fault conditions are cleared and the appropriate status register is read to clear the interrupt flag as shown in **Figure 14**.

Table 8: PMIC Fault Response & Recovery

Fault Event	**PMIC Response**	**Recovery**
LDO OVP/UVP/OCP	LDO output shuts off and output voltage pulls down according to load and output capacitance.	Hiccup Mode, see Section **6.1** for more details.
Battery OCP – Battery Operation	Shutdown BATFET and VSYS.	BATFET and VSYS restart once fault is removed.
Battery OCP – Supplement Mode	Exit Supplement Mode.	Supplement Mode restarts once fault is removed if necessary.
Battery OTP – Charging Input Present	Charging disabled.	PMIC restarts charging as necessary once temperature enters safe range.
Battery OTP – Battery Operation	Interrupt to MCU only. BATFET and VSYS remain active	MCU reads fault to clear interrupt bit.
VSYS OCP	Disable battery charging, Tristate VSYS output	VSYS restarts once fault is removed.
VSYS OVP/UVP – Charging Input Present	Tristate VSYS output	VSYS restarts once fault is removed.
Charge Source OVP/UVP	Switch to battery operation	Reenable charge source once fault clears.
PMIC Over Temperature (155°C typ)	Disable VSYS, LDOs, LED drivers, and battery charging to protect the PMIC	Restart operation after PMIC temperature drops below shutdown hysteresis. Restarted treated as a POR event, Volatile Memory is not cleared.

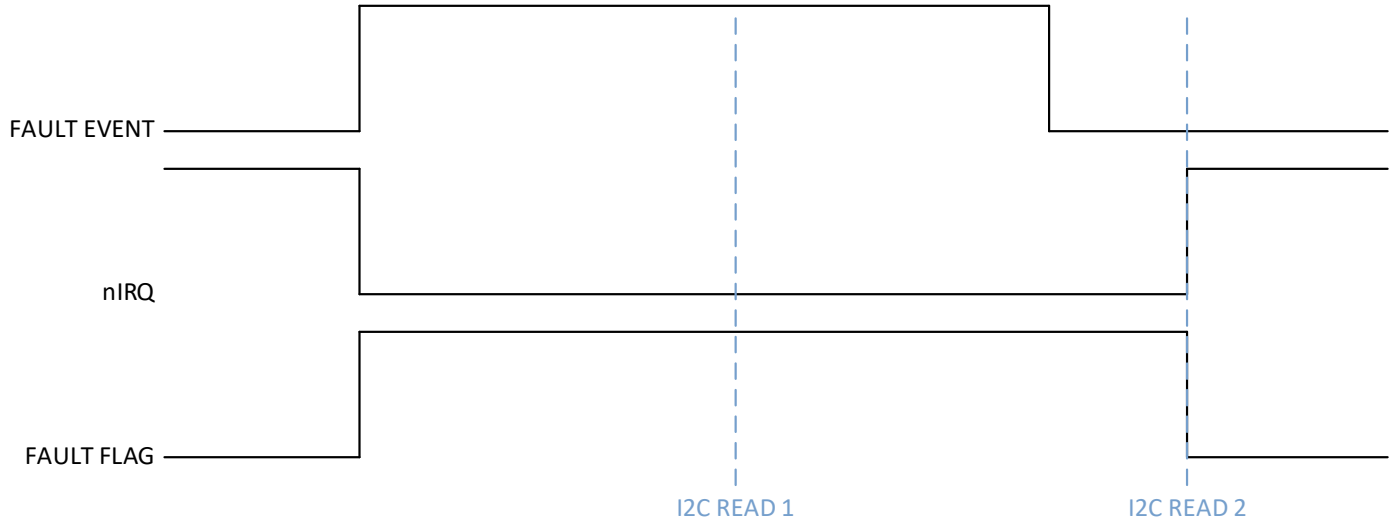
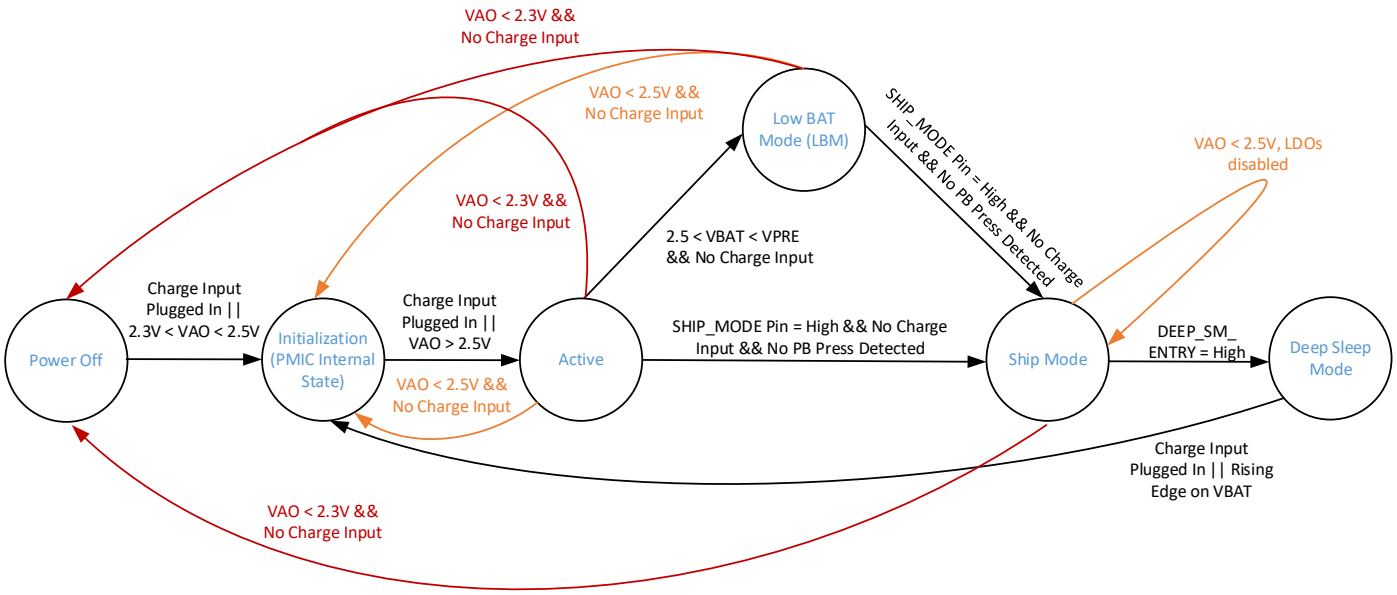


Figure 14: nIRQ Behavior During Fault Events

5 PMIC POWER STATES & DIAGRAM



Note:
- Setting Ship_Mode Pin = Low reverts back to Active/LBM States per operating conditions
- PMIC will wake from Ship Mode if a PB Press is detected or if a Charge Source is supplied. PMIC will reenter Ship Mode when button press ends or source is removed and SHIP_MODE is still high.
- Deep Sleep Mode Entry I2C Command is ignored if received outside of Ship Mode. Entry command hard coded in digital to be detected when main I2C block is off
- Deep Sleep Mode exit only occurs when an Input Charging Source is plugged in, or a rising edge on VBAT is detected
- Deep Sleep Mode exit detection circuitry on VIN_USB, VIN_WRLS, and VBAT is 3.2V ±0.8V in order to keep power draw minimal

Figure 15: ACT82120 Power State Diagram

Table 9: ACT82120 Power State Descriptions

Power Mode	Notes	VM Reset	PMIC Circuit Blocks										Typ Iq
			VAO	ADC	LDO1	LDO2	VSYS	I2C	LEDs	Push Button	BATFET	Charger	
Active	Normal Operating Mode	No	On	On (Controlled by I2C EN Bit)	On (Controlled by EN_LDO1	On (Controlled by EN_LDO2	On (Controlled by I2C EN Bit)	On	On (Controlled by EN_LED)	On	On	On (Controlled by CHRG_DIS)	2.28mA
Low Bat Mode	2.5V < VBAT < VPRE and no Charging Input	No	On	On (Controlled by I2C EN Bit)	On (Controlled by EN_LDO1)	On (Controlled by EN_LDO2)	Off	On	Off	On	Off	Off	0.19mA
Ship Mode	Low Power Ship Mode Controlled by Ship_Mode	No	On	Off	On (Controlled by EN_LDO1)	On (Controlled by EN_LDO2)	Off	Off	Off	Off	Off	Off	7µA
Deep Sleep Mode	Accessible only through Ship_Mode and I2C command. VAO POR Disabled. VAO comes up first after exiting state.	No	On	Off	Off	Off	Off	Off	Off	Off	Off	Off	3.4µA
Initialization (PMIC Internal State)	2.3V < VAO < 2.5V	No	On	Off	Off	Off	Off	On	Off	Off	Off	Off	0.15mA
Power Off	No Charging Input and VAO = VBAT < 2.3V. VAO POR Circuit Active. VAO comes up first after exiting state.	Yes	Off	Off	Off	Off	Off	Off	Off	Off	Off	Off	1µA

5.1 Low I_Q Ship Mode

The ACT82120 can be placed into a low I_Q Ship Mode with a typical current draw of 7µA that shuts down all unnecessary circuitry as described in **Table 9**. By default, the PMIC keeps both LDO outputs active to power external MCUs, sensors, or other circuits needed in the system. Each LDO can be disabled externally through its enable pin in Ship Mode if not needed.

Entry into Ship Mode is controlled through the SHIP_MODE pin provided no charging input is present or push button press is detected as shown in **Figure 16**. If SHIP_MODE is high while a charging input is present or the button is depressed, the PMIC will enter Ship Mode once the conditions are removed. Setting SHIP_MODE low at any time will bring the PMIC out of Ship Mode.

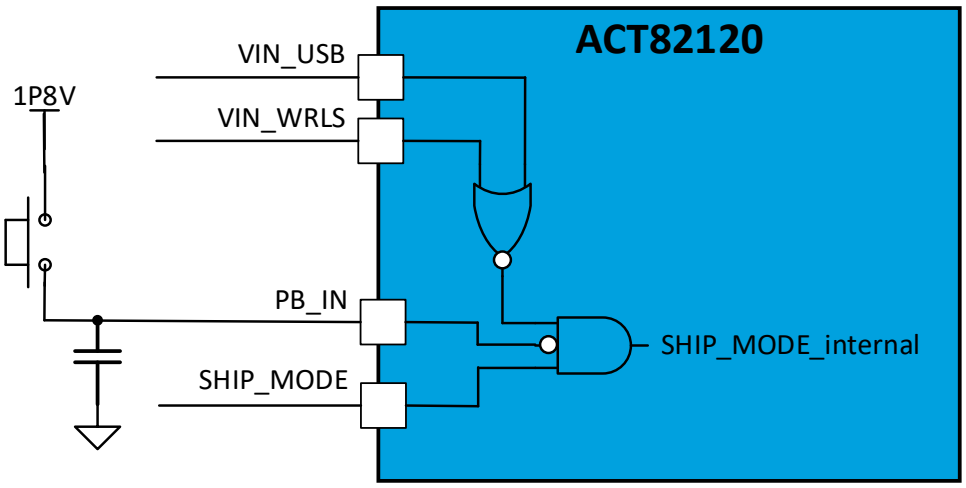


Figure 16: High Level Ship Mode Entry Logic

As the PMIC transitions into Ship Mode, all interrupts to the system are masked. While in Ship Mode no interrupts are sent from the PMIC as internal oscillators are disabled to reduce current consumption. However, in the event of a button press or detecting a charging input, the PMIC will wake from Ship Mode to send the appropriate interrupt to the MCU. If the SHIP_MODE pin remains high while the interrupts are sent, the charger will enter back into Ship Mode automatically once the appropriate conditions are met.

5.2 Low I_Q Deep Sleep Mode

To reduce current consumption even further than Ship Mode, the ACT82120 can also be placed into a Deep Sleep Mode where the I_Q of the PMIC is essentially only leakage currents. A hard coded I2C command sent to the PMIC enables Deep Sleep Mode, however, entry can only happen if the part is already in Ship Mode. The PMIC will ignore the Sleep Mode Entry command if it is received in any other power state.

While in Deep Sleep, all internal circuitry is disabled save for simple edge detection circuitry that monitors VIN_WRLS, VIN_USB, and VBAT. Exiting Deep Sleep Mode occurs when either a charging input is connected to the device, or a rising edge on VBAT is detected. Upon exit, the volatile memory is cleared and the PMIC reboots as if from a first power up as the internal VAO supply must restart.

6 LDO OUTPUTS

6.1 LDO Fault Response

In the event of an overvoltage, overcurrent, or undervoltage fault the LDO output shuts off and pulls down through its 40Ω discharge resistance as well as residual load current. The LDO then enters a hiccup mode reset state and attempts to restart its output. The hiccup period can be configured from 250ms to 2000ms over I2C in Register 22h, bits 7 and 6.

Note, in Shipe Mode, the LDO protection circuitry is disabled because the deglitch timer on the fault detection circuitry is inactive as all internal oscillators are turned off to save power.

6.2 Internal VIO Logic Level Supply from LDO1

The various I/O signals to and from the PMIC are nominally designed around 1.8V logic levels and their circuitry is powered from an internal voltage supply, VIO. Before LDO1 is enabled, VIO is connected to VAO internally. However, after LDO1 completes a successful startup, VIO is connected to LDO1 to switch to zero-bias current circuit blocks on the IO buffers. If a pin has an internal pullup resistor connected to it, that resistor is also connected to VIO.

When VIO is connected to LDO1, VIL = 0.3*LDO1 and VIH = 0.7*LDO1. The default NVM configuration for LDO1 is a 1.8V output, giving the logic levels called out in **Electrical Characteristics – Logic Pins**.

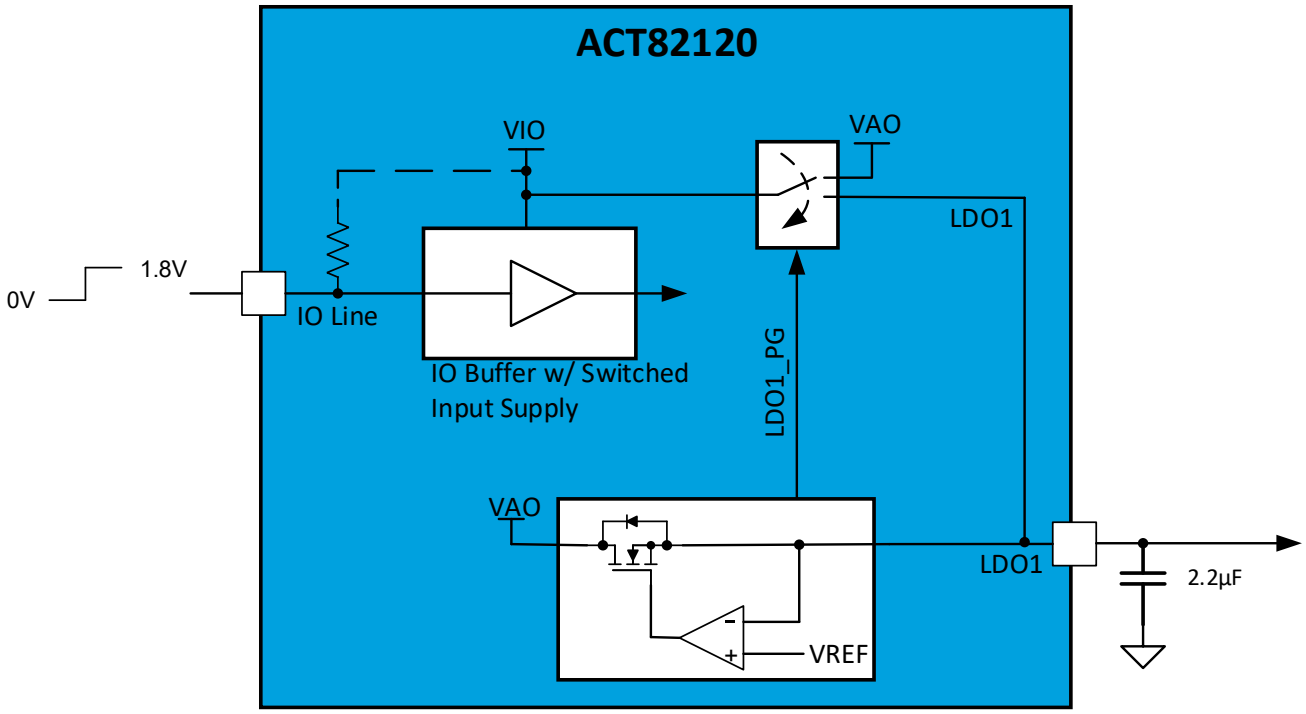


Figure 17: Internal VIO Supply Connections

6.3 LDO Drop Out Behavior

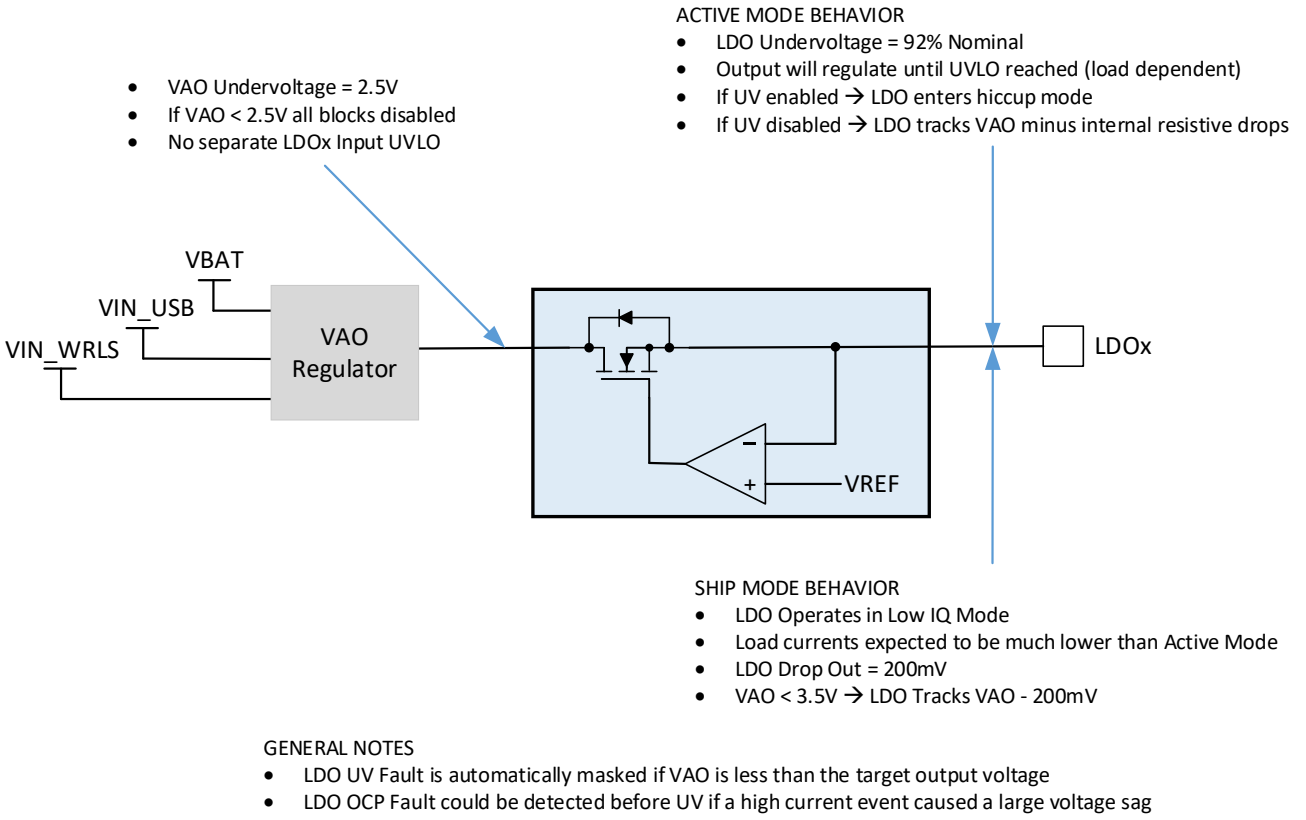


Figure 18: LDO Drop Out Behavior

7 LED DRIVERS

The ACT82120 provides a four LED Driver to power RGBW LEDs. This driver block has an internal volatile program memory for creating and storing a variety of lighting sequences. When the program memory has been loaded via I2C, the LED Drivers can operate independently without external processor control.

Each of the four PWM output drivers are constant current sinks with 8-bit control. The current sink can be controlled over I2C via the execution engines or direct PWM register control from 0mA to 25mA in 100µA increments. The execution engines have six different functions used for building flashing sequences: Ramp, Set PWM, Go to Start, Branch, End, or Trigger.

Brightness adjustment is either linear or logarithmic as shown **Figure 19**, set with a LOG_EN bit.

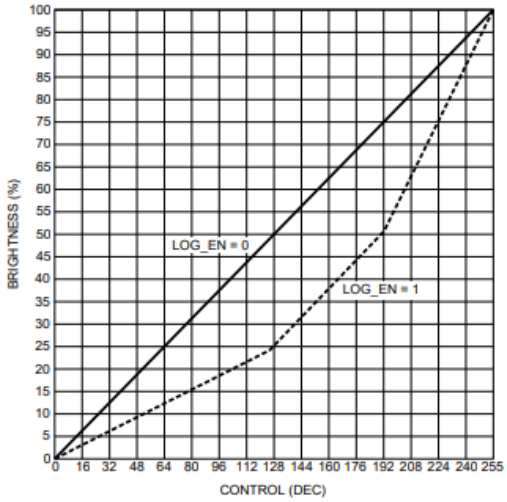


Figure 19: LED Brightness Graph, Log & Linear Plots

7.1 LED Functional Mode

At a high level, the LED Driver circuitry is separated into 4 parts, the I²C Slave Block, Control Unit, Pattern Generator, Clock Divider and Design for Test (DFT) shown in **Figure 20**. The operation of Master Control Unit (mstr_ctrl_u) state machine is described in detail in **Figure 21**.

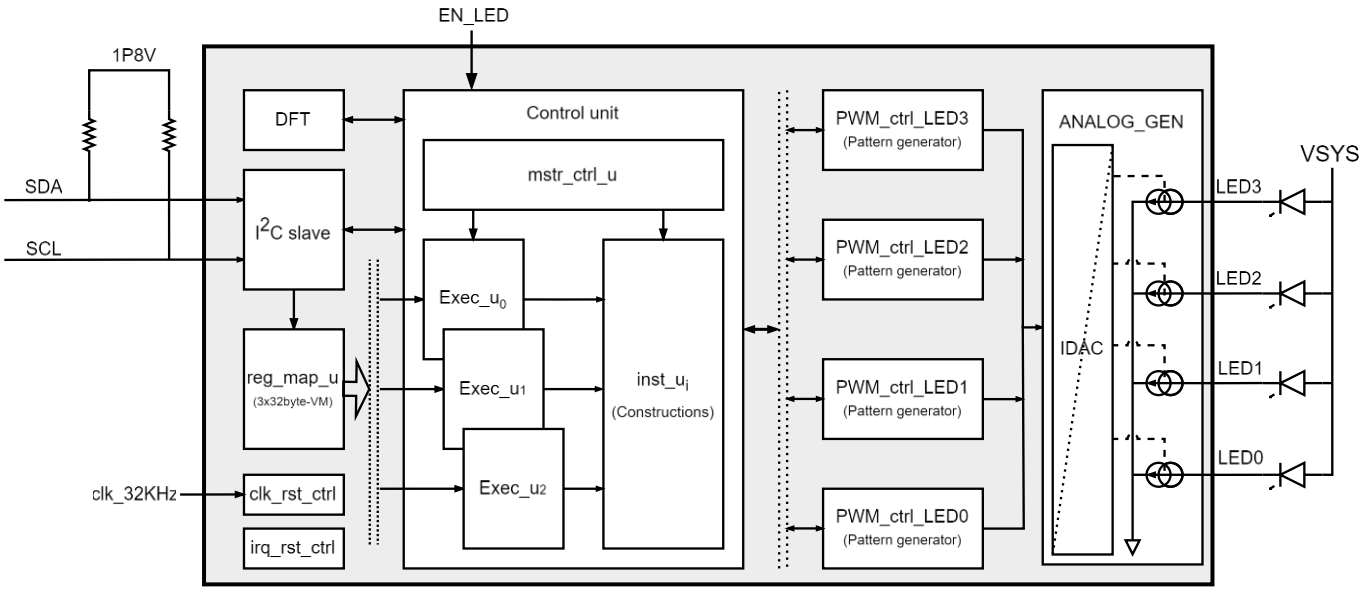


Figure 20: LED Driver Block Diagram

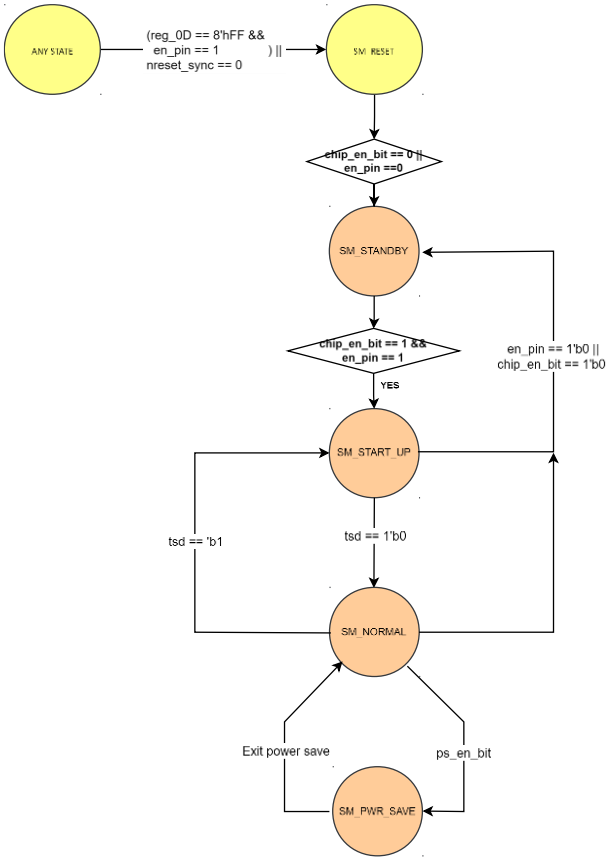


Figure 21: LED Driver Master Control Unit State Machine

SM_RESET: All the internal registers are reset to default values. A reset can be performed if FFh is written to the Reset register or internal Power on Reset (POR) is active. Once VAO rises above its POR threshold 1.9V (typical), the chip will move to Standby Mode. The CHIP_EN control bit is low after POR by default.

SM_STANDBY: This mode is entered if the EN_LED pin is low, and Reset is not active. SM_STANDBY is a low power consumption mode with all of LED driver circuit functionality disabled. Registers can be written in this mode if EN_LED is high.

SM_START_UP: When CHIP_EN and EN_LED are high, the internal start up sequence powers up all the required blocks, such as: bias, clock from system analog. Typically, the time from enabling the LED Driver to when the block is fully operational is 1ms.

SM_NORMAL: The LED Driver is being controlled externally via the I2C bus writing to the various control registers. If EN_LED is set low, the CHIP_EN bit is reset to 0.

SM_PWR_SAVE: If the PMIC is put into Ship Mode via the SHIP_MODE pin all analog blocks, of the LED Driver circuitry are disabled to minimize power consumption. In each instruction cycle all engine commands are analyzed, if there is sufficient time left with no PWM activity, LED driver will enter power save mode.

7.2 LED PWM Driver Output Control

The LED PWM driver outputs can be controlled via either program execution engines or manually through I2C registers. The control method is selected by the user and can be updated during operation through I^{2}C signal. The selection path is described in detail in **Figure 22**.

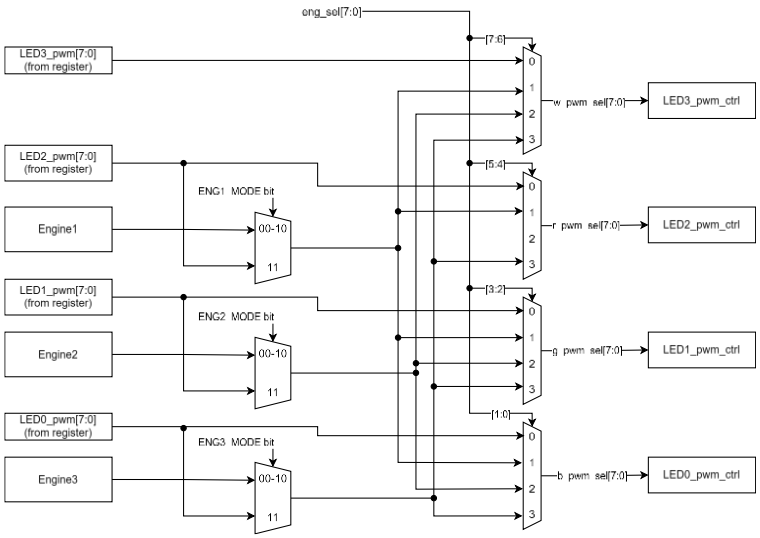


Figure 22: LED Driver Selection Circuitry

7.2.1 Direct I²C Register Control of PWM Outputs

In direct mode, the engine PWM output is controlled by LED0, LED1, LED2, and LED3 PWM I2C registers.

7.2.2 Program Execution Engines

The ACT82120 LED Driver has three program execution engines outlined in **Figure 23**. These engines create PWM controlled lighting patterns to the mapped LED outputs according to program codes developed by the user.

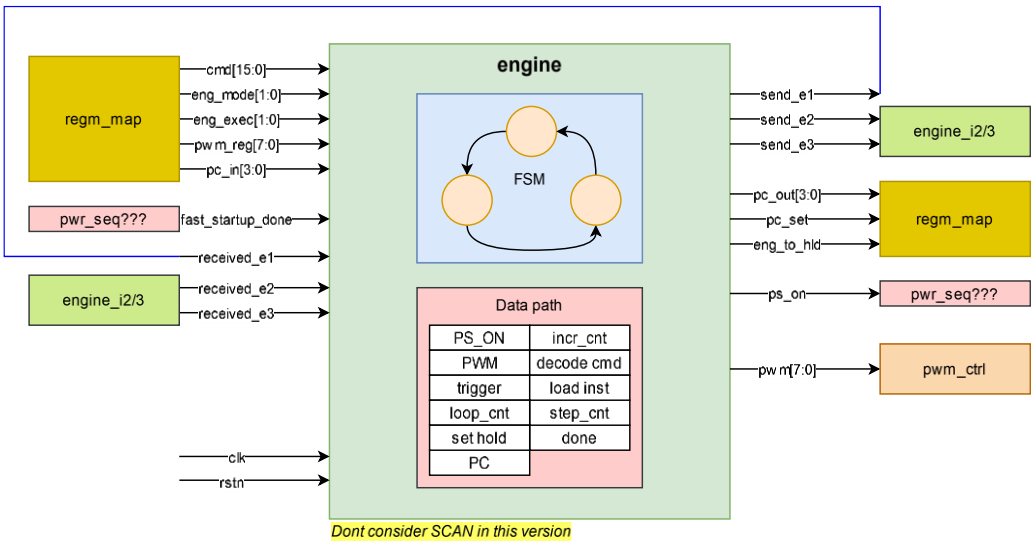


Figure 23: Block Diagram of an LED Driver Program Engine

Program codes are loaded into volatile memory registers using the commands outlined in **Section 7.2.3**. Engine control bits are then used to run these programs autonomously. A state machine for the Program Execution Engine is shown in **Figure 24** and described below.

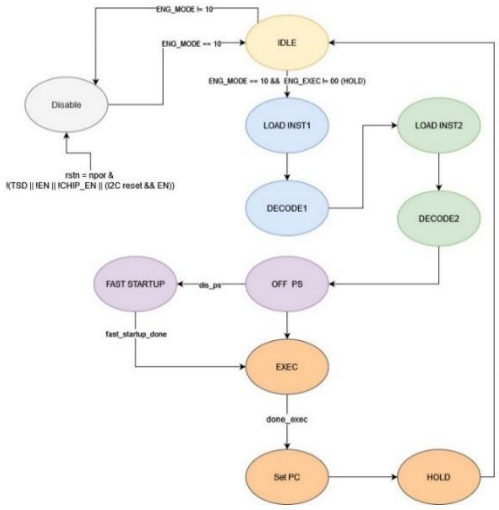


Figure 24: Program Execution State Machine

Each of the four channels can be configured to Disable Mode where the mapped LED output brightness will be 0mA. This mode also resets the respective engines program counter (PC).

Each engine in the LED Driver can store a maximum of 16 commands (2 bytes/command). Writing to the SRAM registers is allowed only during the Channel Load program mode (LOAD $INST_{1,2}$). All engines are in hold while one or several engines are in load program mode, and PWM values are frozen for the engines which are not in load program mode. Program execution continues when all engines are out of load program mode. Load program mode resets the respective engine's PC.

Execution register bits in ENABLE register define how the program is executed. The program start position can be programmed to Program Counter register. By manually selecting the PC start value, the user can write different lighting sequences to the VM memory and select appropriate sequence with the PC register. If PC runs to end (15), the next command will be executed from program location 0. If internal clock is used in the run program mode, operation mode needs to be written disabled (00b) before disabling the chip (with CHIP_EN bit or EN pin) to ensure that the sequence starts from the correct program counter (PC) value when restarting the sequence. PC registers and Execution registers are synchronized to 32 kHz clock. – Note that entering LOAD program or Direct Control Mode from RUN

PROGRAM mode is not allowed. Engine execution mode should be set to Hold, and Operation Mode to disabled, when changing operation mode from RUN mode.

Program execution engine program counter (set PC) tells the current program code command, which engine is executing. By setting the program counter value before starting the engine execution, the user can set starting point of the program.

7.2.3 Engine Programming Commands

Command	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RampWait	0	Pre-scale	Step time						Sign	Increment (number of step)						
Set PWM	0	1	0						PWM Value							
Go to Start	0	0	0						0	0	0	0	0	0	0	0
Branch	1	0	1	Loop count						x	Step/command number					
End	1	1	0	Int	reset	x										
Trigger	1	1	1	x	x	x	Wait for trigger on $engine_{1,2,3}$			x	x	x	Send trigger to $engine_{1,2,3}$			x

7.2.4 LED Engine Programming Registers

Table 10: Control Register Names and Default Values

ADDR (HEX)	REGISTER	D7	D6	D5	D4	D3	D2	D1	D0	DEFAULT
80	ENABLE	LOG_EN	CHIP_EN	ENG1_EXEC[1:0]		ENG2_EXEC[1:0]		ENG3_EXEC[1:0]		0000_0000
81	OP MODE			ENG1_MODE[1:0]		ENG2_MODE[1:0]		ENG3_MODE[1:0]		0000_0000
82	B PWM	LED0_PWM[7:0]								0000_0000
83	G PWM	LED1_PWM[7:0]								0000_0000
84	R PWM	LED2_PWM[7:0]								0000_0000
85	B CURRENT	LED0_CURRENT[7:0]								1010_1111
86	G CURRENT	LED1_CURRENT[7:0]								1010_1111
87	R CURRENT	LED2_CURRENT[7:0]								1010_1111
88	CONFIG		PWM_HF	PS_EN						0000_0000
89	ENG1 PC					ENG1_PC[3:0]				0000_0000
8A	ENG2 PC					ENG2_PC[3:0]				0000_0000
8B	ENG3 PC					ENG3_PC[3:0]				0000_0000
8C	INTERRUPT						ENG1_INT	ENG2_INT	ENG2_INT	0000_0000
8D	RESET	RESET[7:0]								0000_0000
8E	W PWM	LED3_PWM[7:0]								0000_0000
8F	W CURRENT	LED3_CURRENT[7:0]								1010_1111
90	PROG MEM ENG1	CMD_1_ENG1[15:8]								0000_0000
91	PROG MEM ENG1	CMD_1_ENG1[7:0]								0000_0000
…										
AE	PROG MEM ENG1	CMD_16_ENG1[15:8]								0000_0000
AF	PROG MEM ENG1	CMD_16_ENG1[7:0]								0000_0000
B0	PROG MEM ENG2	CMD_1_ENG1[15:8]								0000_0000
B1	PROG MEM ENG2	CMD_1_ENG1[7:0]								0000_0000
…										
CE	PROG MEM ENG2	CMD_16_ENG1[15:8]								0000_0000
CF	PROG MEM ENG2	CMD_16_ENG1[7:0]								0000_0000
D0	PROG MEM ENG3	CMD_1_ENG1[15:8]								0000_0000
D1	PROG MEM ENG3	CMD_1_ENG1[7:0]								0000_0000
…										
EE	PROG MEM ENG3	CMD_16_ENG1[15:8]								0000_0000
EF	PROG MEM ENG3	CMD_16_ENG1[7:0]								0000_0000
F0	LED MAP	LED3_ENG_SEL								LED2_ENG_SEL

7.2.4.1 Enable Register (Enable) (Address = 80h)

D7	D6	D5	D4	D3	D2	D1	D0
LOG_EN	CHIP_EN	ENG1_EXEC[1:0]		ENG2_EXEC[1:0]		ENG3_EXEC[1:0]	
R/W	R/W	R/W		R/W		R/W	

Bit	Field	Type	Reset	Description
7	LOG_EN	R/W		Logarithmic PWM adjustment generation enable
6	CHIP_EN	R/W		Master chip enable. Enables device internal startup sequence. Setting EN pin low resets the CHIP_EN state to 0. Allow 500 µs delay after setting chip_en bit to '1'
5:4	ENG1_EXEC	R/W		Engine 1 program execution. **00b** = Hold: Wait until current command is finished then stop while EXEC mode is hold. PC can be read or written only in this mode. **01b** = Step: Execute instruction defined by current engine 1 PC value, increment PC and change ENG1_EXEC to 00b (Hold) **10b** = Run: Start at program counter value defined by current engine 1 PC value **11b** = Execute instruction defined by current engine 1 PC value and change ENG1_EXEC to 00b (Hold)
3:2	ENG2_EXEC	R/W		Engine 2 program execution. **00b** = Hold: Wait until current command is finished then stop while EXEC mode is hold. PC can be read or written only in this mode.

				01b = Step: Execute instruction defined by current engine 2 PC value, increment PC and change ENG2_EXEC to 00b (Hold) **10b** = Run: Start at program counter value defined by current engine 2 PC value **11b** = Execute instruction defined by current engine 2 PC value and change ENG2_EXEC to 00b (Hold)
1:0	ENG3_EXEC	R/W		Engine 3 program execution. **00b** = Hold: Wait until current command is finished then stop while EXEC mode is hold. PC can be read or written only in this mode. **01b** = Step: Execute instruction defined by current engine 3 PC value, increment PC and change ENG3_EXEC to 00b (Hold) **10b** = Run: Start at program counter value defined by current engine 3 PC value **11b** = Execute instruction defined by current engine 3 PC value and change ENG3_EXEC to 00b (Hold)

7.2.4.2 Operation Mode Register (OP Mode) (address = 81h)

D7	D6	D5	D4	D3	D2	D1	D0
		ENG1_MODE[1:0]		ENG2_MODE[1:0]		ENG3_MODE[1:0]	
		R/W		R/W		R/W	

Bit	Field	Type	Reset	Description
5:4	ENG1_MODE	R/W		Engine 1 operation mode 00b = Disabled 01b = Load program to VM register, reset engine 1 PC 10b = Run program defined by ENG1_EXEC 11b = Direct control
3:2	ENG2_MODE	R/W		Engine 2 operation mode 00b = Disabled 01b = Load program to VM register, reset engine 2 PC 10b = Run program defined by ENG2_EXEC 11b = Direct control
1:0	ENG3_MODE	R/W		Engine 3 operation mode 00b = Disabled 01b = Load program to VM register, reset engine 3 PC 10b = Run program defined by ENG3_EXEC 11b = Direct control

7.2.4.3 LED0 Output PWM Control Register (LED0_PWM) (address = 82h)

D7	D6	D5	D4	D3	D2	D1	D0
LED0_PWM[7:0]							
R/W							

Bit	Field	Type	Reset	Description
7:0	LED0_PWM	R/W		LED0 output PWM value during direct control operation mode

7.2.4.4 LED1 Output PWM Control Register (LED1_PWM) (address = 83h)

D7	D6	D5	D4	D3	D2	D1	D0
LED1_PWM[7:0]							
R/W							

Bit	Field	Type	Reset	Description
7:0	LED1_PWM	R/W		LED1 output PWM value during direct control operation mode

7.2.4.5 LED2 Output PWM Control Register (LED2_PWM) (address = 84h)

D7	D6	D5	D4	D3	D2	D1	D0
LED2_PWM[7:0]							
R/W							

Bit	Field	Type	Reset	Description
7:0	LED2_PWM	R/W		LED2 output PWM value during direct control operation mode

7.2.4.6 LED0 Output Current Control Register (LED0_CURRENT) (address = 85h)

D7	D6	D5	D4	D3	D2	D1	D0
LED0_CURRENT[7:0]							
R/W							

Bit	Field	Type	Reset	Description
7:0	LED0_CURRENT	R/W		Current setting 0000 0000b = 0.0 mA 0000 0001b = 0.1 mA 0000 0010b = 0.2 mA 0000 0011b = 0.3 mA 0000 0100b = 0.4 mA 0000 0101b = 0.5 mA 0000 0110b = 0.6 mA ... 1010 1111b = 17.5 mA (default) ... 1111 1011b = 25.1 mA 1111 1100b = 25.2 mA 1111 1101b = 25.3 mA 1111 1110b = 25.4 mA 1111 1111b = 25.5 mA

7.2.4.7 LED1 Output Current Control Register (LED1_CURRENT) (address = 86h)

D7	D6	D5	D4	D3	D2	D1	D0
LED1_CURRENT[7:0]							
R/W							

Bit	Field	Type	Reset	Description
7:0	LED1_CURRENT	R/W		Current setting 0000 0000b = 0.0 mA 0000 0001b = 0.1 mA 0000 0010b = 0.2 mA 0000 0011b = 0.3 mA 0000 0100b = 0.4 mA 0000 0101b = 0.5 mA 0000 0110b = 0.6 mA ... 1010 1111b = 17.5 mA (default) ... 1111 1011b = 25.1 mA 1111 1100b = 25.2 mA 1111 1101b = 25.3 mA 1111 1110b = 25.4 mA 1111 1111b = 25.5 mA

7.2.4.8 LED2 Output Current Control Register (LED2_CURRENT)(address = 87h)

D7	D6	D5	D4	D3	D2	D1		D0
	LED2_CURRENT[7:0]							
	R/W							

Bit	Field	Type	Reset	Description
	LED2_CURRENT	R/W		Current setting 0000 0000b = 0.0 mA 0000 0001b = 0.1 mA 0000 0010b = 0.2 mA 0000 0011b = 0.3 mA 0000 0100b = 0.4 mA 0000 0101b = 0.5 mA 0000 0110b = 0.6 mA ... 1010 1111b = 17.5 mA (default) ... 1111 1011b = 25.1 mA 1111 1100b = 25.2 mA 1111 1101b = 25.3 mA 1111 1110b = 25.4 mA

				1111 1111b = 25.5 mA

7.2.4.9 Configuration Control Register (CONFIG) (address = 88h)

D7	D6	D5	D4	D3	D2	D1	D0
	PWM_HF	PS_EN					
	R/W	R/W					

Bit	Field	Type	Reset	Description
6	PWM_HF	R/W		PWM clock 0 = 256-Hz PWM clock used 1 = 512-Hz PWM clock used
5	PS_EN	R/W		Power save mode enable

7.2.4.10 Engine 1 Program Counter Value Register (Engine 1 PC) (address = 89h)

PC register can be read or written only when EXEC mode is hold

D7	D6	D5	D4	D3	D2	D1	D0
				ENG1_PC[3:0]			
				R/W			

Bit	Field	Type	Reset	Description
3:0	ENG1_PC	R/W		Engine 1 program counter value

7.2.4.11 Engine 2 Program Counter Value Register (Engine 2 PC) (address = 8Ah)

PC register can be read or written only when EXEC mode is hold

D7	D6	D5	D4	D3	D2	D1	D0
				ENG2_PC[3:0]			
				R/W			

Bit	Field	Type	Reset	Description
3:0	ENG2_PC	R/W		Engine 2 program counter value

7.2.4.12 Engine 3 Program Counter Value Register (Engine 3 PC) (address = 8Bh)

PC register can be read or written only when EXEC mode is hold

D7	D6	D5	D4	D3	D2	D1	D0
				ENG3_PC[3:0]			
				R/W			

Bit	Field	Type	Reset	Description
3:0	ENG3_PC	R/W		Engine 3 program counter value

7.2.4.13 INTERRUPT Register (address = 8Ch)

D7	D6	D5	D4	D3	D2	D1	D0
					ENG1_INT	ENG2_INT	ENG3_INT
					R	R	R

Bit	Field	Type	Reset	Description
2	ENG1_INT	R		Interrupt from engine 1
1	ENG2_INT	R		Interrupt from engine 2
0	ENG3_INT	R		Interrupt from engine 3

7.2.4.14 RESET Register (address = 8Dh)

D7	D6	D5	D4	D3	D2	D1	D0
RESET[7:0]							
R/W							

Bit	Field	Type	Reset	Description
7:0	RESET	R/W		Reset all register values when FFh is written

7.2.4.15 LED3 Output PWM Control Register (LED3_PWM) (address = 8Eh)

D7	D6	D5	D4	D3	D2	D1	D0
W_PWM[7:0]							
R/W							

Bit	Field	Type	Reset	Description
7:0	LED3_PWM	R/W		LED3 output PWM value during direct control operation mode

7.2.4.16 LED3 Output Current Control Register (LED3_CURRENT) (address = 8Fh)

D7	D6	D5	D4	D3	D2	D1	D0
LED3_CURRENT[7:0]							
R/W							

Bit	Field	Type	Reset	Description
7:0	LED3_CURRENT	R/W		Current setting 0000 0000b = 0.0 mA 0000 0001b = 0.1 mA 0000 0010b = 0.2 mA 0000 0011b = 0.3 mA 0000 0100b = 0.4 mA 0000 0101b = 0.5 mA 0000 0110b = 0.6 mA ... 1010 1111b = 17.5 mA (default) ... 1111 1011b = 25.1 mA 1111 1100b = 25.2 mA 1111 1101b = 25.3 mA 1111 1110b = 25.4 mA 1111 1111b = 25.5 mA

7.2.4.17 LED Mapping Register (LED Map) (address = F0h)

D7	D6	D5	D4	D3	D2	D1	D0
W_ENG_SEL[1:0]		R_ENG_SEL[1:0]		G_ENG_SEL[1:0]		B_ENG_SEL[1:0]	
R/W		R/W		R/W		R/W	

Bit	Field	Type	Reset	Description
7:6	LED3_ENG_SEL	R/W		Selection from where LED3 output PWM is controlled, 00 = I 2C register 0Eh, 01 = Engine 1, 10 = Engine 2, 11 = Engine 3
5:4	LED2_ENG_SEL	R/W		Selection from where LED2 output PWM is controlled 00 = I 2C register 04h, 01 = Engine 1, 10 = Engine 2, 11 = Engine 3
3:2	LED1_ENG_SEL	R/W		Selection from where LED1 output PWM is controlled 00 = I 2C register 03h, 01 = Engine 1, 10 = Engine 2, 11 = Engine 3
1:0	LED0_ENG_SEL	R/W		Selection from where LED0 output PWM is controlled 00 = I 2C register 02h, 01 = Engine 1, 10 = Engine 2, 11 = Engine 3

7.3 LED Programming Examples

7.3.1 Three Blink Pattern

This program ramps the PWM duty cycle from 0% to 100%, and back to 0% three times with a pause between blinks as shown below in **Figure 25**.

RAMP 64, 128
RAMP 64, 128
RAMP 64, -128
RAMP 64, -128
WAIT 25
WAIT 25
BRANCH 5, 0 // From first command
WAIT 32
BRANCH 31, 7 // From WAIT command
END

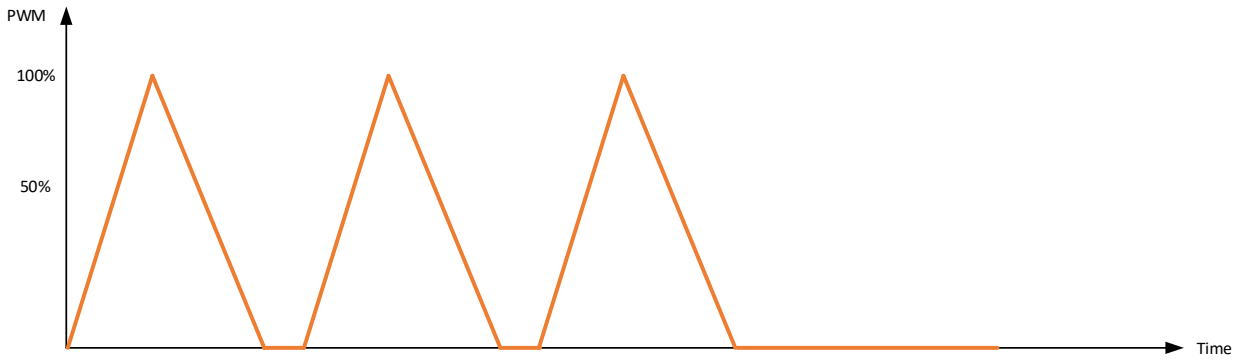


Figure 25: LED Programming Example Waveform #1

7.3.2 Three Quick Blink Pattern with Indefinite Dim Blinks

This program ramps the PWM duty cycle from 0% to 100%, and back to 0% three times. After the three fully duty cycle blinks, a 0% - 25% - 0% blink is repeated indefinitely.

RAMP 64, 127
RAMP 64, 127
RAMP 64, -127
RAMP 64, -127
RAMP 512, 127
RAMP 512, 127
RAMP 512, -127
RAMP 512, -127
LOOP 4,4 // Loop 4 times from Command 4
RAMP 1024, 63
RAMP 1024, -63
LOOP 0,9 //Indefinite Loop from Command 9

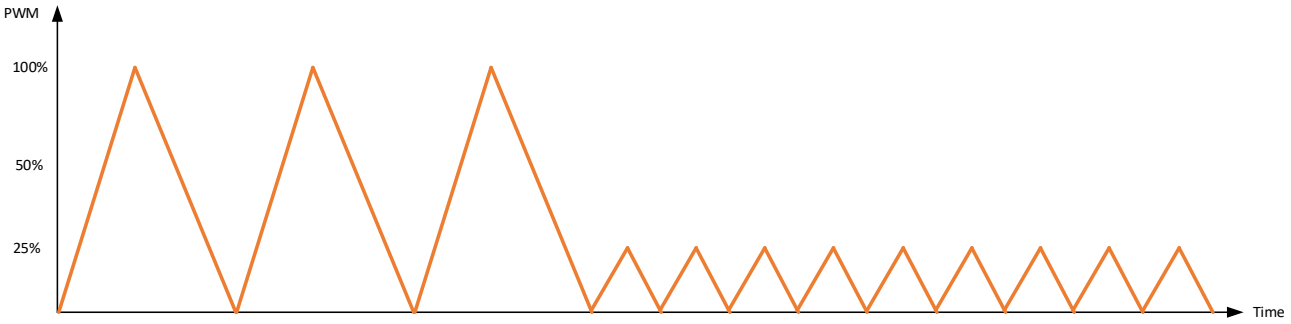
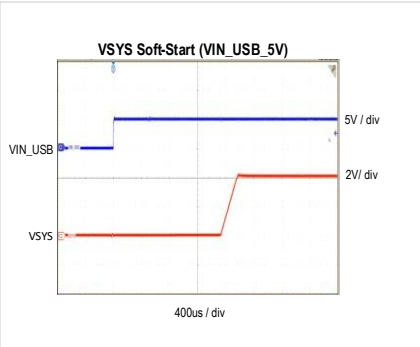
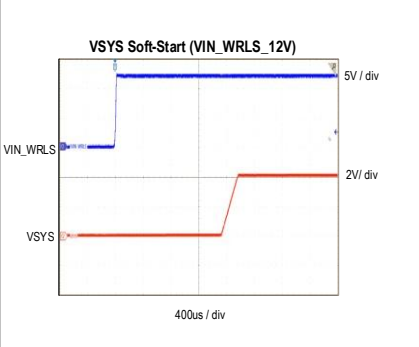


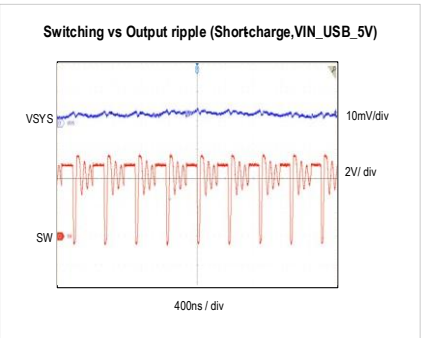
Figure 26: LED Programming Example Waveform #2

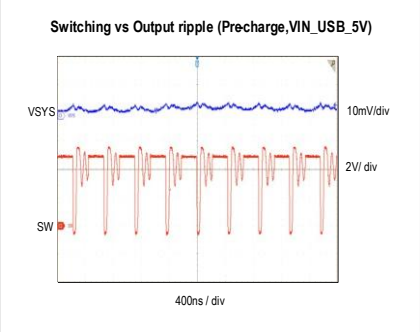
TYPICAL OPERATING CHARACTERISTICS

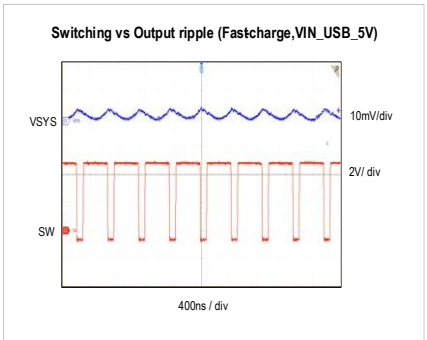
(CMI101)

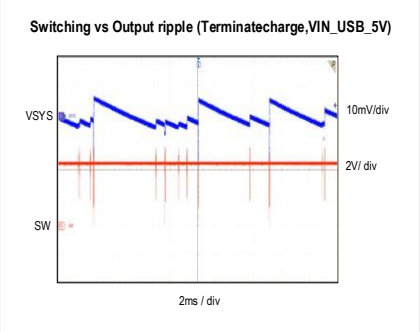


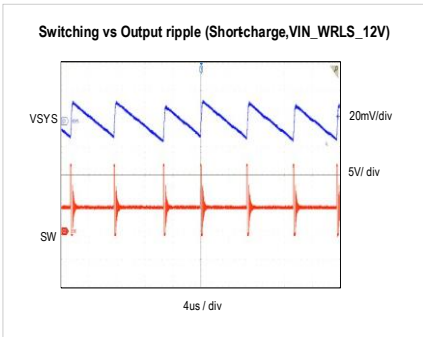


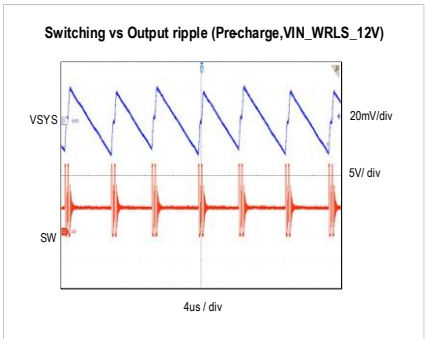


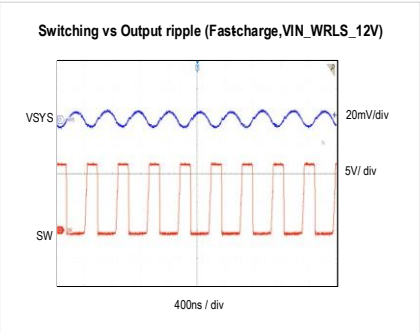


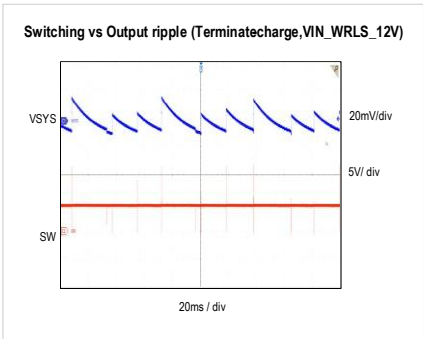


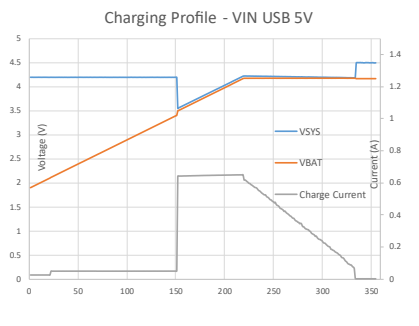


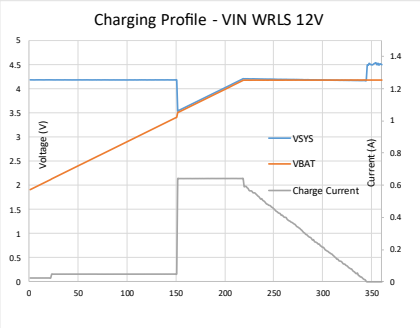


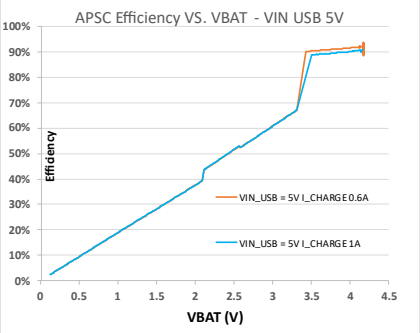


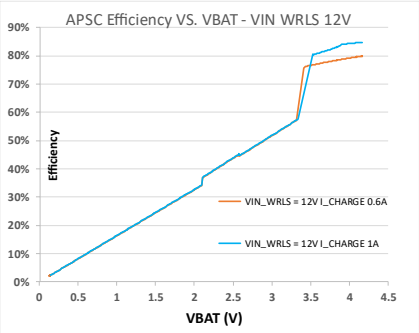












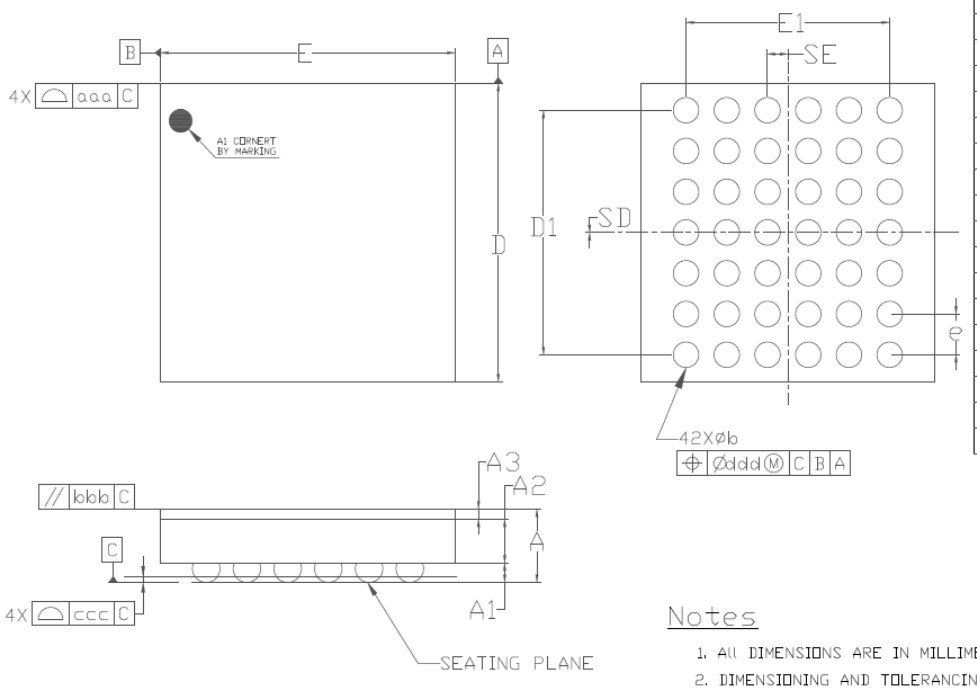
CMI OPTIONS

This section provides the basic default configuration settings for each available ACT82120 CMI option. IC functionality in this section supersedes functionality in the main datasheet. Generating the desired functionality for a custom CMI sometimes requires reassigning internal resources, resulting in removal of base IC functionality. The following sections attempt to describe any removed functionality from the base IC functionality. The user is required to fully test all required functionality to ensure the CMI fully meets their requirements.

CMI 101: ACT82120-101T

CMI 101 is made for mass market. Contact Qorvo for more details about this IC.

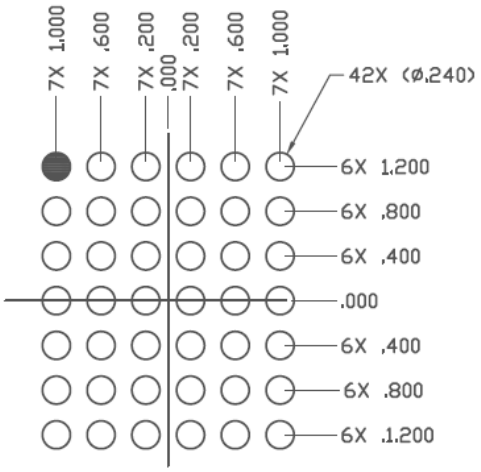
PACKAGE OUTLINE AND DIMENSIONS



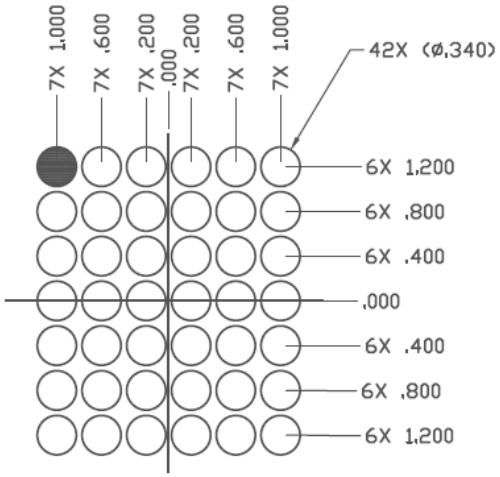
Dimensional Ref.			
REF.	Min.	Nom.	Max.
A	0.515	0.540	0.565
A1	0.140	0.165	0.190
A2	0.335	0.350	0.365
A3	0.022	0.025	0.028
E	2.845	2.860	2.875
D	2.885	2.900	2.915
E1	1.950	2.000	2.050
D1	2.350	2.400	2.450
b	0.216	0.240	0.264
e	0.400 BSC		
SD	0.000 BSC		
SE	0.200 BSC		
Tol. of Form&Position			
aaa	0.10		
bbb	0.10		
ccc	0.05		
ddd	0.05		

Notes

1. ALL DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
2. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M-1994.



RECOMMENDED PCB METAL TOP VIEW



RECOMMENDED SOLDERMASK TOP VIEW

NOTES:
1. SHADED AREA REPRESENTS PIN 1 LOCATION.

Product Compliance

This part complies with RoHS directive 2011/65/EU as amended by (EU) 2015/863.

This part also has the following attributes:

- Lead Free
- Halogen Free (Chlorine, Bromine)
- Antimony Free
- TBBP-A ($C_{15}H_{12}Br_4O_2$) Free
- PFOS Free
- SVHC Free

Contact Information

For the latest specifications, additional product information, worldwide sales and distribution locations:

Web: www.qorvo.com **Tel: 1-844-890-8163**

Email: customer.support@qorvo.com

For technical questions and application information:

Email: appsupport@qorvo.com

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