ACT43750 Datasheet Brief

Please refer to the ACT43750 Product Page for more information. Click here for a link to request the full datasheet.

BENEFITS and FEATURES

- **Wide Operating Range**
  - Vin = 10V to 55V
  - Vgate = -6V to 0V
- **RF PA Biasing Solution**
  - Turn on and off sequencing
  - Negative gate voltage supply
  - Supports GaN and Silicon FETs
  - High-speed drain switching
  - Autonomous Bias Point Calibration
- **Autonomous $I_{DQ(DRAIN)}$ calibration**
  - Resistor Setpoint Range: 10mA to 2A
  - Digitally adjustable ±31% of setpoint in 1% steps
- **Space and Cost savings**
  - Fully integrated gate drive voltage
  - High switching frequency: 2.05 MHz
  - Integrated FETs and small chip inductor
  - 37-pin, 5 mm x 5 mm, 0.4-mm pitch QFN package
- **High-Performance Negative Gate Drive Supply**
  - REGG input voltage: +12V (TYP)
  - REGG output voltage: -6V to -1.5V by 732µV step
  - REGG output source current: 300mA
  - REGG output sink current: -100mA
  - REGG output noise: <200µVRMS
- **Protection**
  - UVLO, OVLO, OVP, UVP, OCP, TSD

APPLICATIONS

- Military Radar System
- Civilian Radar System
- RF GaN / GaAs PA Power Supply

GENERAL DESCRIPTION

The ACT43750, part of Qorvo's RF POL regulator family, is the last stage of a three-chip radar power supply solution. This three-stage solution, developed with the ACT43950, ACT43850, and ACT43750, forms a compact, complete power supply system for radio frequency (RF) power amplifiers (PAs) that demand fast transient, high current pulse loads. The first stage, ACT43950 converts a high voltage dc input voltage into a regulated dc constant-current (CC) to charge bulk capacitor. The second stage, ACT43850, regulates the capacitor voltage into a tightly regulated DC voltage to power the drain for GaN RF power amplifiers.

The third stage, ACT43750, provides several functions specifically designed to optimize RF GaN power amplifier performance. It operates either standalone or as the third stage in a multiple stage power solution. It provides the RF PA negative gate voltage using an ultra-low noise inverting buck dc-to-dc regulator with integrated FETs and programmable voltage reference. It provides the required GaN power up and power down sequencing between the drain and gate voltages. All GaN RF PAs require calibrating the gate voltage to set the desired operating point. The ACT43750 automatically calibrates and stores the optimal gate voltage. This fully automated procedure eliminates the system-level design's need for discrete calibration circuitry. The autocalibration routine can be run at any time to compensate for changes in RF PA performance due to aging, temperature, or voltage changes. The ACT43750 also enables drain switching in pulsed radar applications. The ICs contain an I^2C slave bus that allows the user to dynamically change the IC's settings. It also contains an I^2C master, which controls companion devices ACT43850 and external I^2C memory, on the sub-I^2C bus. The IC also contains protection circuitry to prevent RF PA damage in the event of temperature, RF power, bias power, and current faults.

The ACT43750 is available in a 37-pin, 5 mm x 5 mm, 0.4 mm pitch QFN package.

SYSTEM BLOCK DIAGRAM

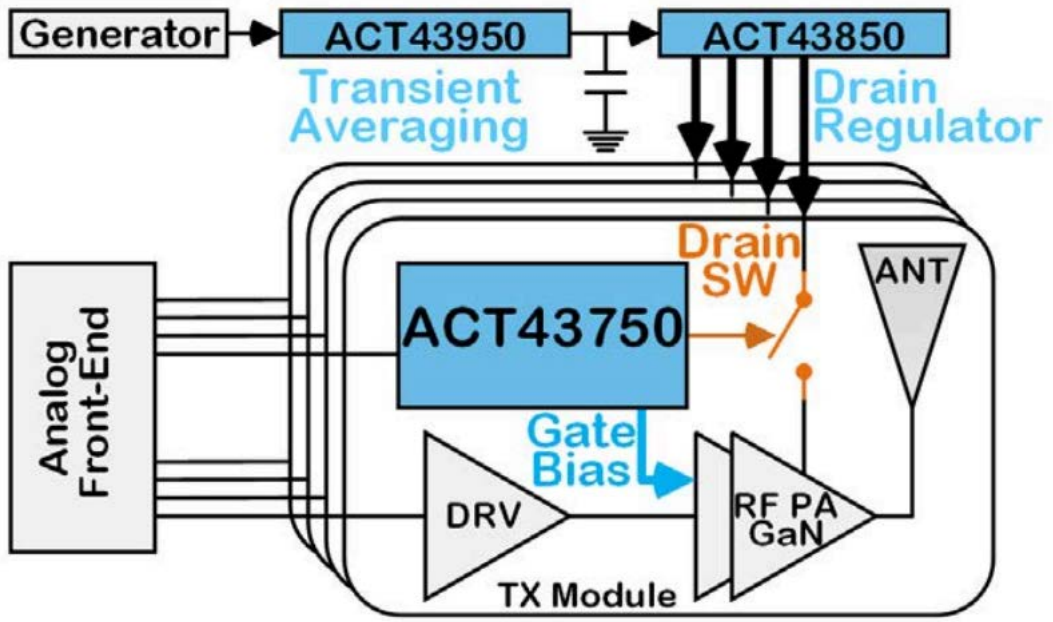
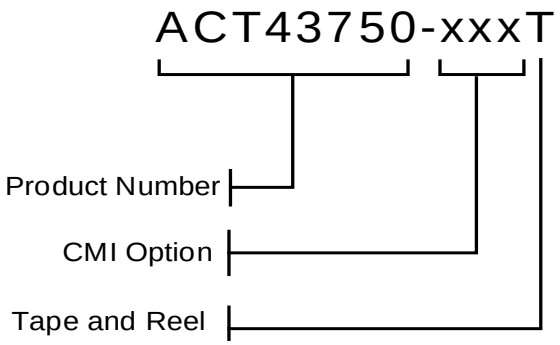


Figure 1. 3 Chip System Block Diagram

ORDERING INFORMATION

PART NUMBER	Min RF PA Gate Voltage	Max RF PA Gate Voltage	Power FET Type	Power FET Gate Voltage (LSR regulator)	Targeted Qorvo RFPA
ACT43750-101T	-4.5V	-1.5V	GaN	5V	Generic Use
ACT43750-102T (proposed functions)	-4.5V	-1.5V	Si	10V	Generic Use



Note 1: Standard product options are identified in this table. Contact the factory for custom options, a minimum order quantity is required.

Note 2: “xxx” represents the CMI (Code Matrix Index) option The CMI identifies the IC’s default register settings.

PIN CONFIGURATION

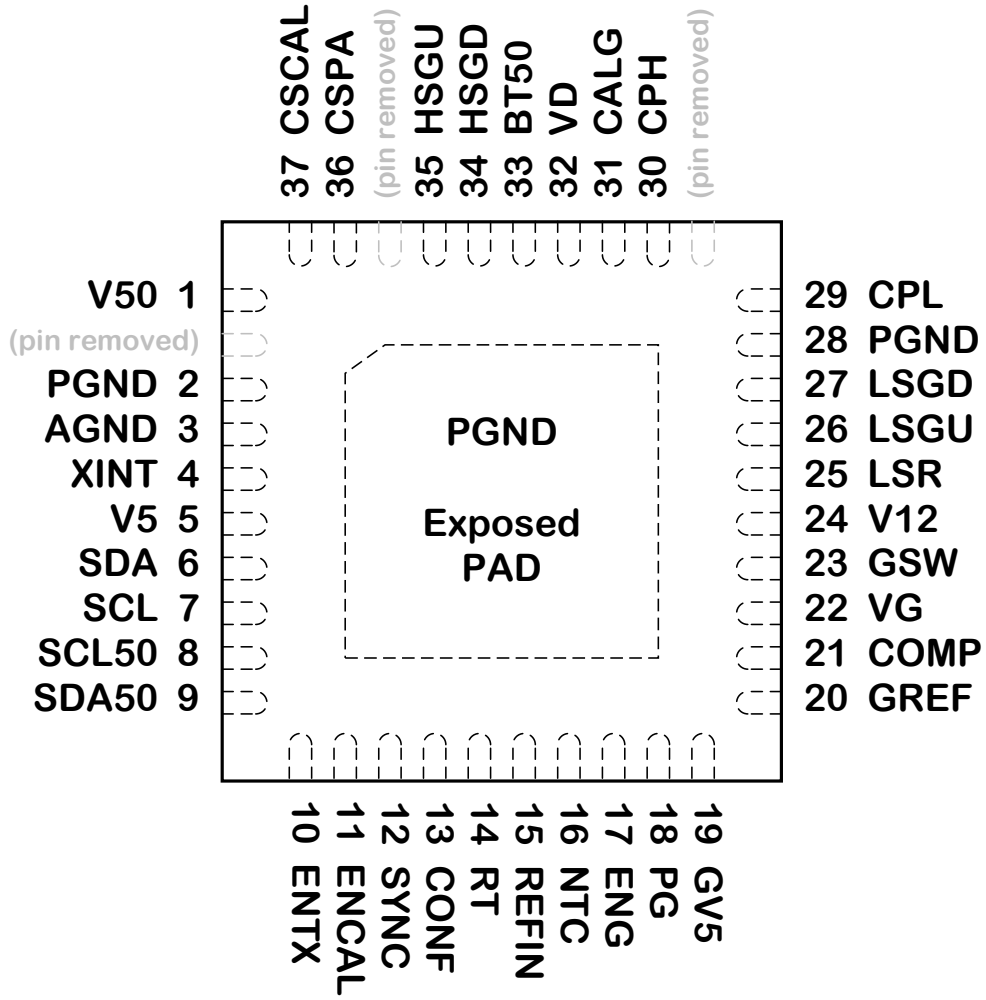
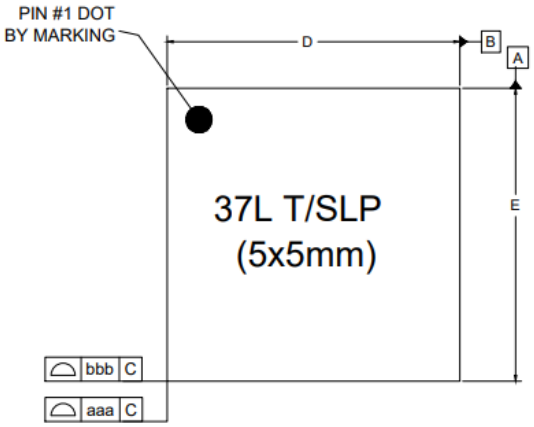


Figure 2: Pin Configuration – Top View – 37 pin QFN, 5 mm x 5mm, 0.4 mm pitch

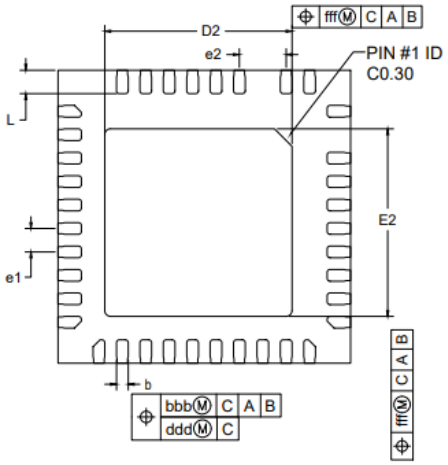
PIN DESCRIPTIONS

Pin	NAME	DESCRIPTION
1	V50	Input power to the DSW50 control section of the IC.
2, 28	PGND	Dedicated power ground for the DSW50 gate drive. Connect to AGND with a Kelvin connection.
3	AGND	Ground pin for the analog blocks. Connect to PGND with a Kelvin connection.
4	XINT	Interrupt output. Open drain. Connect it through a pull-up resistor to V5.
5	V5	5V Bias regulator output. Requires a 2.2uF capacitor to AGND
6	SDA	I^2C Data Pin for Slave mode
7	SCL	I^2C Clock Pin for Slave mode
8	SCL50	I^2C Data Pin for Master mode
9	SDA50	I^2C Clock Pin for Master mode
10	ENTX	Enable input for the DSW50 block. Don't float this pin. Connect it through a 100kΩ resistor to the ground. ENTX pin needs to be logic low when startup.
11	ENCAL	Enable input to start an autocalibration routine. Don't float this pin. Connect it through a 100kΩ resistor to the ground.
12	SYNC	External clock synchronization input
13	CONF	External configuration resistor input. Connect a resistor between CONF and V5 and between CONF and AGND to configure IC settings.
14	RT	Sets the negative gate voltage switching frequency. Connect a resistor between RT and AGND.
15	REFIN	External voltage reference input. Leave open if not used.
16	NTC	Negative temperature coefficient resistor input.
17	ENG	Enable input for the REGG block (negative voltage regulator). Don't float this pin. Connect it through a 100kΩ resistor to the ground.
18	PG	Power good output. Open drain. Connect it through a pull-up resistor to V5.
19	GV5	Floating negative gate voltage output. Connect a 2.2uF capacitor between GV5 and VG.
20	GREF	The local voltage reference for the REGG output. Connect a 100nF capacitor between GREF and VG.
21	COMP	Compensation input. Connect a 470pF capacitor between COMP and VG.
22	VG	Feedback input for the REGG output. Connect a 10nF capacitor between VG and V12.
23	GSW	REGG switching node.
24	V12	External 12V bias input pin. Connect a 10uF capacitor between V12 and PGND. Connect a 10nF capacitor between V12 and VG.
25	LSR	Low-side gate drive regulator for the DSW50 block. Connect a 2.2uF capacitor between LSR and PGND.
26	LSGU	Pullup output for the low-side FET gate.
27	LSGD	Pulldown output for the low-side FET gate.
29	CPL	High-side gate drive regulator flying capacitor terminal. Connect a 47nF capacitor and a 47Ω resistor in series between CPL and CPH.
30	CPH	High-side gate drive regulator flying capacitor terminal. Connect a 47nF capacitor and a 47Ω resistor in series between CPH and CPL.
31	CALG	Calibration FET gate output.
32	VD	DSW50 output voltage for the high side FET. Connect a 2.2uF capacitor between VD and BT50.
33	BT50	High-side gate drive regulator bootstrap output. Connect a 2.2uF capacitor between BT50 and VD.
34	HSGD	Pulldown output for the high-side FET gate.
35	HSGU	Pullup output for the high-side FET gate.
36	CSPA	Overcurrent sense resistor input for the drain FET
37	CSCAL	Calibration current sense resistor input for the calibration FET.
-	Exposed PAD	Exposed thermal pad. Connect directly to PGND.

PACKAGE OUTLINE AND DIMENSIONS

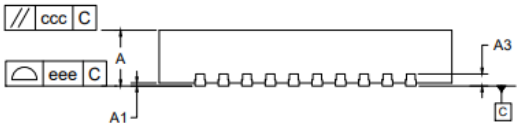


TOP VIEW



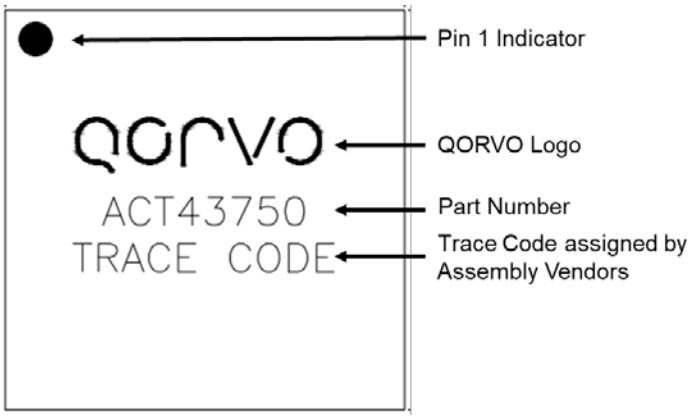
BOTTOM VIEW

Dimensional Ref.			
REF.	Min.	Nom.	Max.
A	0.700	0.750	0.800
A1	---	---	0.050
A3	0.203 Ref.		
D	4.950	5.000	5.050
E	4.950	5.000	5.050
D2	3.150	3.200	3.250
E2	3.150	3.200	3.250
b	0.150	0.200	0.250
e1	0.400 BSC		
e2	0.800 BSC		
L	0.350	0.400	0.450
Tol. of Form&Position			
aaa	0.10		
bbb	0.10		
ccc	0.10		
ddd	0.05		
eee	0.08		
fff	0.10		



SIDE VIEW

PART MARKING



Product Compliance

This part complies with RoHS directive 2011/65/EU as amended by (EU) 2015/863.

This part also has the following attributes:

- Lead Free
- Halogen Free (Chlorine, Bromine)
- SVHC Free
- PFOS Free
- Antimony Free
- TBBP-A (C15H12Br402) Free

Contact Information

For the latest specifications, additional product information, worldwide sales and distribution locations:

Web: www.qorvo.com **Tel: 1-844-890-8163**

Email: customer.support@qorvo.com

For technical questions and application information:

Email: appsupport@qorvo.com

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